A High Value, Linear and Tunable CMOS Pseudo Resistor for Bio-medical Applications

R. Nagulapalli, K. Hayatleh, S. Barker, P. Georgiou* &F. J. Lidgey
Oxford Brookes University, Oxford, UK
*Imperial College, London, UK
khayatleh@brookes.ac.uk

Abstract—A sub-threshold MOS based pseudo resistor featuring a very high value and ultra-low distortion is proposed. A band-pass neural amplifier with a very low high-pass cutoff frequency is designed, to demonstrate the linearity of the proposed resistor. A BJT less CTAT current generator has been introduced to minimize the temperature drift of the resistor and make tuning easier. The stand-alone resistor has achieved 0.5% better linearity and a 12% improved temperature coefficient over the existing architectures. A neural amplifier has been designed with the proposed resistor as a feedback element. It demonstrated 31dB mid-band gain and a low-pass cutoff frequency of 0.85Hz. The circuit operates from a 1V supply and draws 950nA current at room temperature.

Keywords—Neural amplifier, biomedical, pseudo resistor, OTA, linearity, feedback, CTAT.

I. INTRODUCTION

To evaluate various neurological disorders such as Alzheimer's, epilepsy and cerebrovascular diseases, the neuro-electrical activity in the brain requires monitoring. Neural signals are very weak and low frequency. Typical neural signals are in the range of 5uV to 5mV with the frequencies in the range 0.05Hz to 10KHz [1]. A few examples of biological signals amplitudes and frequencies are listed in table-I. Another issue is that as well as being very weak in nature, they are susceptible to random noise from the electrodes, with a typical 1MΩ electrode adding ~10uV RMS of noise. A neural amplifier will be used to amplify the signal to improve SNR. The input DC voltage of a neural amplifier can be as high as 1V due to galvanic voltages generated at the tissue/electrode interface, hence AC coupling or DC cancellation circuitry is required.

Table-I
BIOLOGICAL SIGNAL DETAILS

Signal name	Frequency Range (Hz)	Signal Amplitude (mV)
ECG	0.05-150	0.1-5
EMG	25-5000	0.1-100
EEG	0.1-100	0.025-0.1
EOG	0.1-10	0.01-0.1
Action Potential of Neurons	0-10000	50-100

Fig:1 shows a very commonly used single ended neural amplifier. The closed-loop gain is set by the ratio of the input capacitor (C_{in}) to the feedback capacitor (C_f).

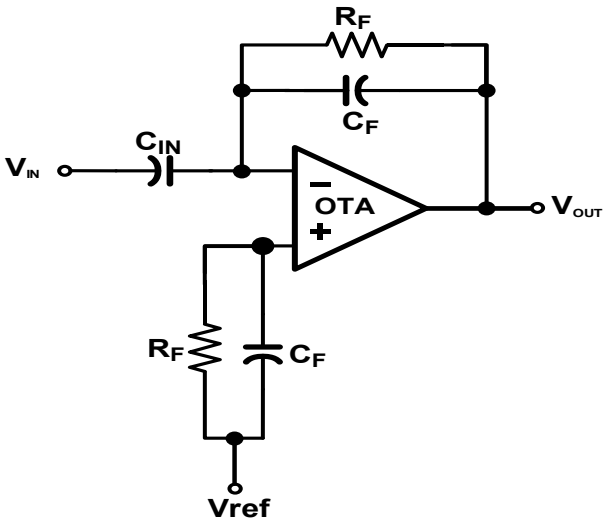

Fig. 1. Single Ended AC Coupled Neural Amplifier

The lower cutoff frequency of the amplifier is set by the feedback time constant (R_fC_f). To make this cutoff frequency to very low, R_fC_f must be very high. Due to the area restrictions of the chip, C_f can't be more than 10pF, hence R_f needs to be very high, that is, in the range of 500MΩ and above. In a typical CMOS process, the maximum poly-sheet resistance is ~ 2KΩ, hence to realize such a large resistance (500MΩ), a 50mm long and 0.2um wide ploy material is required, which is larger than a typical IC size. This demonstrates that a passive implementation is impossible, and for this reason a better approach would be to employ pseudo-resistors. There have been several ways proposed to synthesize very high resistances, for instance, Jiang [2] used a switched resistor with a clock, but this requires an extra clock generator which is power hungry. Several people attempted to solve the problem with the sub-threshold region based MOS resister [3], [6], and they achieved very a high resistance without consuming much power but poor linearity, therefore this is the approach considered here to synthesize a high value resistor whilst proposing a novel biasing technique to improve the linearity. The rest of the paper has been organized as follows, section-II describes previous implementations, section-III explains the proposed technique, and finally section-IV depicts the prototype of the proposed technique.

II. PSEUDO RESISTORS

A MOS transistor biased in subthreshold region (week inversion), acts as a very high value resistor, which is frequently referred to as a pseudo-resistor. From the EKV model [5] the small signal resistance (at very low V_{ds}) can be derived as follows.

$$R_{Pse@vds=0} = \frac{dV_{ds}}{dI_d} = \frac{U_T}{I_{d0}}$$

Where U_T is thermodynamic voltage and I_{d0} is the residual channel current given by

$$I_{D0} = 2n\mu_n C_{ox} \frac{W}{L} U_T^2 e^{-\frac{V_{T0}}{nU_T}} \quad (1)$$

Where n is sub-threshold slope and Cox is oxide unit cap. From (1), the pseudo resistance has strong function Process, Voltage, and temperature (PVT) corners.

Harrison [3] proposed the use of a MOS-Bipolar pseudo resistor in conventional CMOS technology. This approach results in very high value while occupying a very small area, but it has a limited operating voltage range. When the voltage across the pseudo-resistance is changed due to PVT variation, its resistance value drops to very low values, hence the cut-off frequency will be increased and in-band signal will experience attenuation. The main problem with this implementation is that the V_{GS} of the transistor is varying with the signal, hence the resistance is varying, and more importantly, the distortion increases because system gain changes with input amplitude. Fig:2 shows the concept of the implementation. It shows that the V_{GS} of transistors M_1, M_2 is varying with the input signal. To quantify the effect of this V_{GS} variation, we implemented these two circuits.

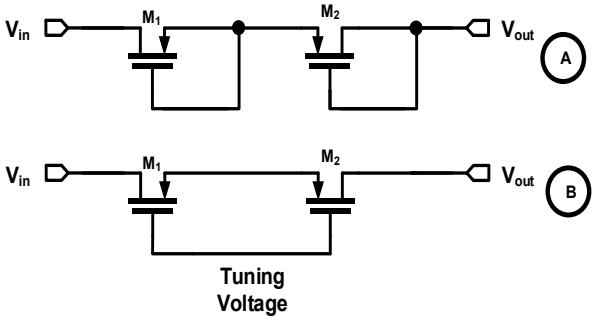

Fig. 2. Variable V_{gs} implementations.

Fig:3 shows the simulated resistance as a function of the voltage swing across the resistor. Due to the V_{GS} variation, the resistance varies from 500MΩ to 750MΩ, while its voltage swing varies by 0.7V. Both architectures shown in Fig:2 have resistance variation problems. Fig:3 shows linearity degradation from 2% to 4.2% for architecture A, and 5% to 7.1% for the new architecture while varying the voltage swing.

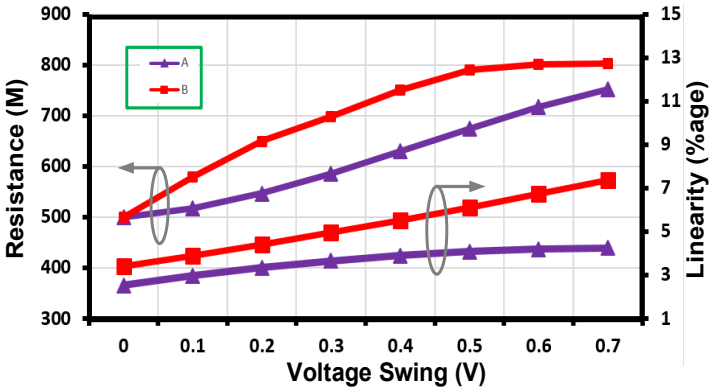

Fig. 3. Resistance versus voltage swing.

To solve varying V_{GS} problem, Tajalli [6] proposed a way to keep V_{GS} constant as shown in Fig:4. Two PMOS devices M_1, M_2 are connected in series to realize a large resistance with reduced sensitivity to the voltage swing. A source follower (M_3) is used to generate a voltage V_{th} less than the input voltage, while tracking the input variations (assuming the source follower has enough bandwidth). The output of the source follower will drive the gate of the pseudo resistor. Under balanced conditions this scheme looks good, but when the threshold voltage (V_{th}) of both the NMOS and PMOS deviates from the nominal value, this could result in a very low resistance, because PMOS will move out of the weak-inversion region. Fig:5, shows the simulated linearity of this circuit, and confirms that there is less variation with signal voltage swing compared to the variable V_{GS} technique [3]. Apart from the V_{GS} effect, higher a V_{DS} also could contribute some nonlinearity. To mitigate this problem, an improved circuit has been proposed [7], which uses a combination of NMOS and PMOS pseudo resistors with two different source followers driving these transistors, as shown in Fig:6.

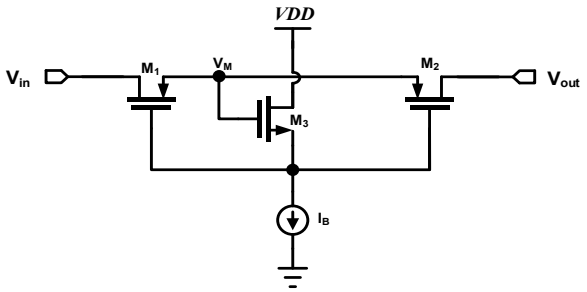

Fig. 4. Pseudo resistor Proposed by Tajalli [3]

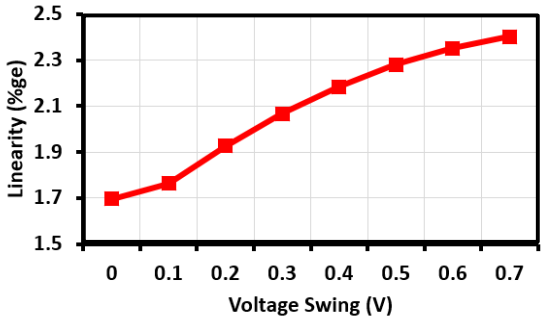

Fig. 5. Linearity of Tajalli [3] resistor.

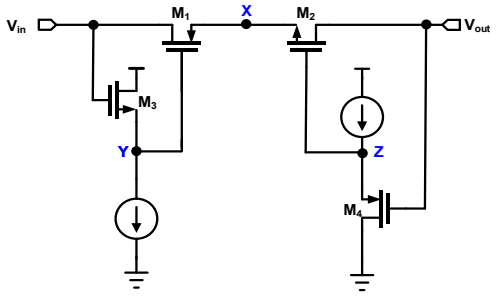

Fig. 6. Pseudo resistor Proposed in [7]

This technique achieved the best linearity, and more importantly, consistent variation across the signal voltage swing. The downside however of this approach is as follows. When psuedo resistors are connected in the feedback path of an OTA, one terminal is at virtual ground and another terminal swings by a large amount, as shown in Fig:1. V_{in} stays at a DC potential and Vout potential swings around the common mode of the Opamp. During the positive half cycle of the signal at V_{out}, node x is the source of M_2 and the potential of node Z is V_{th} less than Vout, hence the V_{GS} of M_2 is constant. However, during the negative half cycle of V_{out}, node x is the drain of M_2, so V_{GS} is no longer constant, hence the linearity is compromised.

III. Proposed Technique.

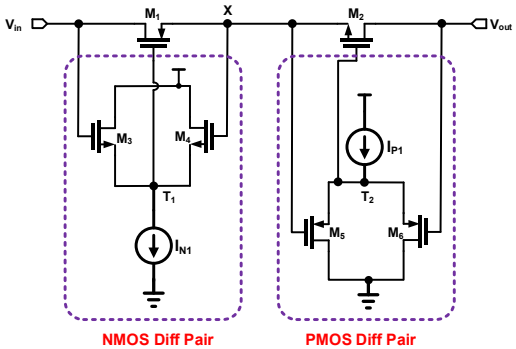

Fig. 7. Proposed Pseudo resistance.

To solve the problems in the previous techniques, we extended the implementation in [7]. The present technique uses the tail node of a differential pair instead of a source follower as shown in Fig:7. The differential pair tail node (T_1) potential will be at the average of V_{in},V_x. Assuming Vin is at the virtual node of the Opamp, node x will have an approximate swing of Vout/2. The V_{GS} of M_1 is Vout/4 and V_{GD} is -Vout/4. The gate source voltage of the transistor is not held constant in this approach. Whilst the variation is Vout/2, it is also independent of the positive and negative half of the signal. In the previous approach, V_{GS} is held constant only for either the positive or negative half, and for the other half the V_{GS} has a swing of Vout/2. To simulate the resistance, V_{in} terminal voltage is fixed at a DC potential of 0.3V and V_{out} terminal voltage varied up to its max swing voltage. For the proposed circuit the resistance varied by 9% across the full DC sweep range.

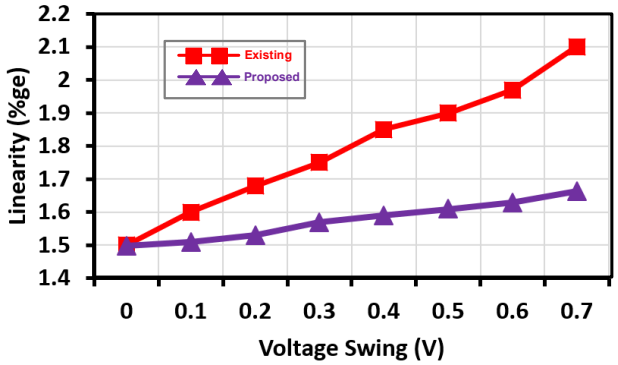

Fig. 8. Proposed Pseudo resistance.

Resistor linearity has been simulated and compared with the implementation in [7]. Looking at Fig:8 (the linearity results), it is clear from the gragh that the proposed pseudo-resistance shows an 11% linearity variation across the swing range, whereas Kassiri [7] has 19% variation. This improvement is the result of the differential-pair bias, which works for the +ve and -ve half of the cycle, whereas the prior approach works for +ve or -ve half-cycle.

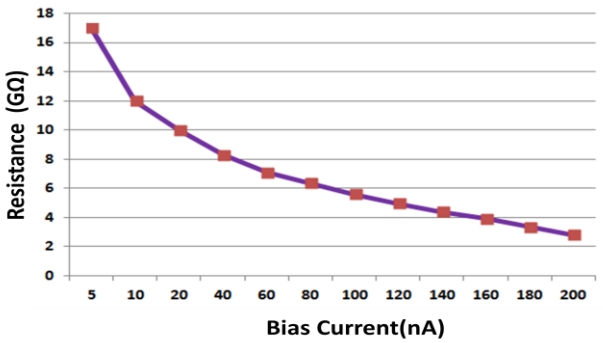

Fig. 9. Resistance vs bias current plot

Apart from resistance value and linearity, tunability is also one of the main requirements of a pseudo resistance, since an analog frontend needs to support several types biological signals. The proposed pseudo-resistance can be tuned by changing the differential pair currents (I_{n1}, I_{p1}). By

increasing I_{p1} current, the V_{GS} of M_5 and M_6 will increase and the node T_2 voltage will also increase, which in turn will increases the V_{GS} for M_2, hence the resistance will decrease. Fig:9 shows how the resistance can be tuned by a varying current. Apart from linearity, a temperature stable resistance is also an essential feature for any biomedical application. In the circuit shown in Fig:7, I_{p1} and I_{n1} current sources play a major role in determining the temperature stability of the resistance. From the simulations we observed, using CTAT (complementary to absolute temperature) bias current, the resistance had better temperature stability compared with the constant bias current. Because with a constant bias current V_{GS} will increase with temperature due to the carier mobility degradation with temperature, where as with CTAT bias, V_{GS} will be relatively constant (first order approximation), hence the resistance will have less temperature sensetivity.

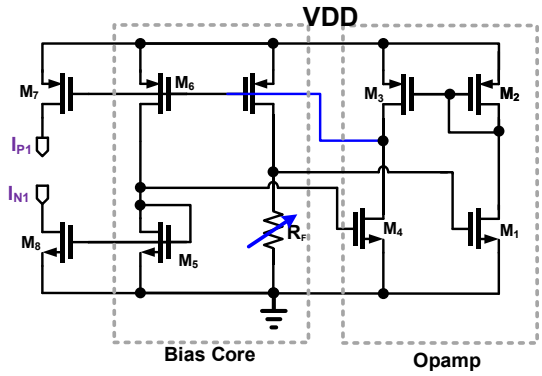

Fig. 10. Pure CMOS based CTAT generator.

Fig:10 shows a CTAT bias generator, which consists of a bias core and an opamp. The bias core generates a current proportional to the V_{th} of M_5 (M_5 is large enough to neglect overdrive voltage), by equating the voltage drop across R_f and V_{GS} of M_5. The opamp compares these two voltages and adjusts the gate voltage of M_6 with -ve feedback. Since the input common mode voltage of the opamp is very close to V_{GS5}, there is no need to have a tail current source for the opamp. Though this is not as good as a BJT based CTAT, for this application it is good enough and makes the circuit CMOS compatible. Fig:11 shows the resistance versus temperature with the CTAT current and with constant current. The results show a 12% improvement with CTAT and 26% improvement with the constant bias.

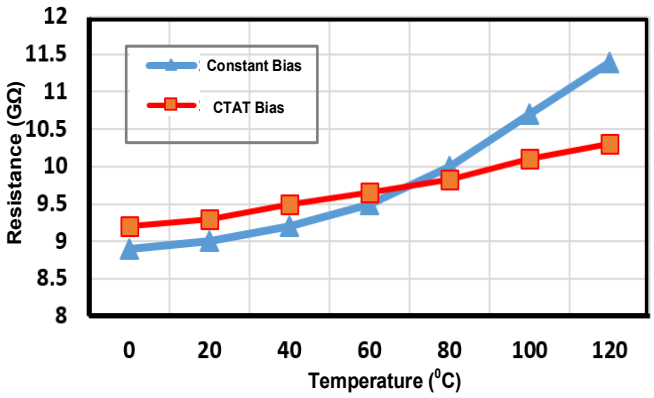

Fig. 11. Temp coefficient of resistance with constant bias and CTAT bias

IV. Prototype and Simulation Results.

The neural amplifier depicted in Fig:1 has been designed, in standard 65nm CMOS technology, to demonstrate the proposed pseudo resistance. A two stage cascode opamp architecture is very similar to Aziz's [8] and has been implimented to function as an OTA. The first stage is an pmos input cascode stage and the second stage is an nmos based common source amplifier. The only difference between [8] and the present implimenation is a self cascode differential pair to minimize the offset voltage. The OTA achives 68dB loop gain in the worst PVT corner. The cascode amplifier differential pair device size was adjusted to make an g_m/i_d ratio of ~16, and the power noise tradeoff has been optimised to get an acceptable noise level of $1.8uV_{rms}$ while consuming only 0.58uA (only OTA) from the 1V power supply. Fig. 12 shows the OTA schematic diagram (biasing was not shown).

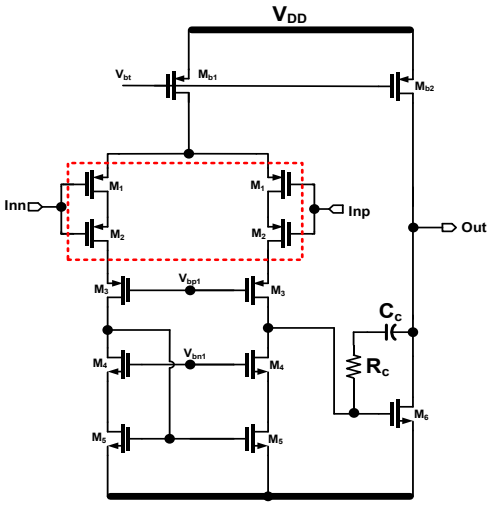

Fig. 12. Two stage opamp schematic

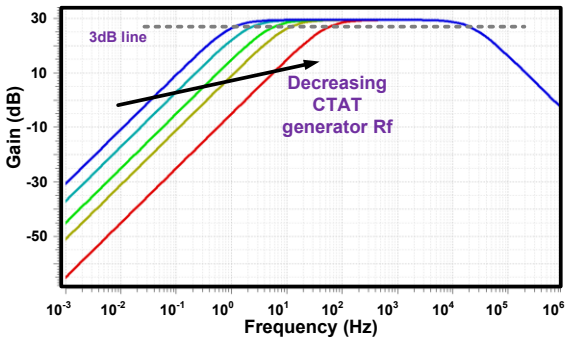

Fig. 13. Closed loop response of the Neural amplifier (High pass pole tuning).

The feedback capacitor's ratio has been adjusted to get a closed loop gain to 30dB. To demonstrate the tunability of the high pass corner frequency, by varying the CTAT generator Rf manually, the neural amplifier frequency response is plotted and shown in Fig:13. Th feedback capacitor C_f is ~2.5pF and the high pass cut-off frequency starts from 0.85Hz, and the upper cutoff frequency (depending on the OTA design) is around 20KHz. Fig:14 depicts the layout of the proposal, which occupies 0.05mm^2. The majority of the silicon area is occupied by the input and feedback capacitors distributed around the circuit. The differential pair and current mirror devices were laid out with enough dummies on both sides of the actives and matching patterns.

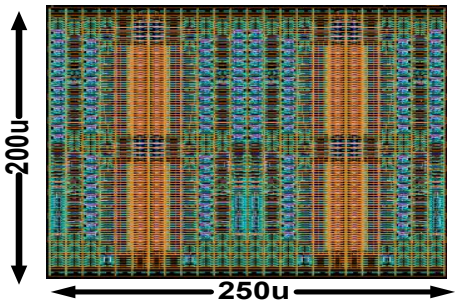

Fig. 14. Layout of the Total Implementation

V. Conclusion

In this paper, we demonstrated a tunable, highly linear pseudo resistor with a reduced temperature dependency. The proposed circuit is an improved version of Kassiri's circuit [7] and consumes very similar power. We have added a CTAT generator which only consumes 150nA DC current. The total Circuit draws 0.95uA from a 1V supply.

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