A 15uW, 12 ppm/°C Curvature Compensated Bandgap in 0.85V Supply

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***Abstract*—In this paper, a curvature-compensated bandgap reference circuit is presented which generates 0.538V from 0.85V supply voltage. The PTAT voltage generated in the bandgap core is added to the partial CTAT voltage to generate the sub-bandgap reference, reducing the CTAT current mirror mismatch. Furthermore, this architecture eases the opamp's requirements on offset and flicker noise significantly and doesn't require sophisticated techniques, such as chopping. A novel curvature compensation scheme is proposed and validated across PVT simulations and achieves 12 ppm/°C with a single point trim. The proposed bandgap consumes a power of 15 μW and occupies an area of 7315 μm^2 in TSMC 28nm.**

Keywords: Bandgap, Curvature-Compensation, Sub-1V, offset, noise.

I. INTRODUCTION

Almost every SOC requires a voltage reference circuit. Reference voltages are essential for many blocks, such as data converters, oscillators, PLL, and power management circuits. Low voltage and low power are essential and required in battery-operated circuits to increase their efficiency and product longevity. Brokaw [1] proposed a bandgap reference based on the exponential properties of the BJT devices with a moderate temperature coefficient (temp-co) of 65ppm/°C, which became the golden reference circuit designed on the modern CMOS technologies. The main principle of this circuit is to generate a Proportional to Absolute Temperature (PTAT) voltage, a Complimentary to Absolute Temperature (CTAT) voltage, and then to scale and sum them to obtain a temperature-independent reference voltage. With technology scaling, power supplies have been scaled to sub-1V to meet transistor reliability and to ensure lower power consumption in digital circuits. consequently, there is a need for generating reference voltages with nominal values less than 1V. There has been extensive research on designing a bandgap voltage reference with sub 1V operation. Banba et al [2] proposed the concept of a sub-bandgap reference which enables low voltage realization by operating in current mode. The idea is to generate a PTAT and CTAT current and add them in the current domain to get a constant current. This current is mirrored and used to generate a constant reference voltage across a resistor. The current that can be mirrored from this architecture is a constant current rather than PTAT. This is a major disadvantage for circuits like temperature sensors and oscillators etc.

Typically bandgap reference is designed with PNP bipolar transistors, which results in the amplification of amplifier offset and flicker noise. Recently, the use of NPN bipolar in Bandgap reference [3]–[7] has gained traction due availability of triple well CMOS process. The inherent gain of the NPN transistors eases the specification of the amplifier. However, the bipolar beta variation leads to larger error in these NPN based bandgap reference. The base-emitter voltage of the bipolar typically varies from 800mV to about 400mV across the temperature range of -40 C to 125 C. Operating the bandgap to sub 1V [8] is difficult owing to the headroom requirements on the current sources. Lower headroom also results in larger errors in these current sources. This work relaxes the headroom on current sources leading to higher accuracy allows the use of supply voltages as low as 0.85V without compromising accuracy. Vbe of the transistor is having 2nd order terms (i.e., curvature), which will results in significant temp-co. Several techniques have been proposed to tackle this problem, the Curvature compensation is proposed by [4] lowers the virtual node impedance of opamp, resulting in higher flicker noise and offset amplification. This work exploit's the base resistance of the BJT for the curvature compensation [3]. The mechanism of the curvature compensation is explained analytically and is shown that single point trim brings the worst-case accuracy to 12 ppm/°C with typical being 4ppm/°C.

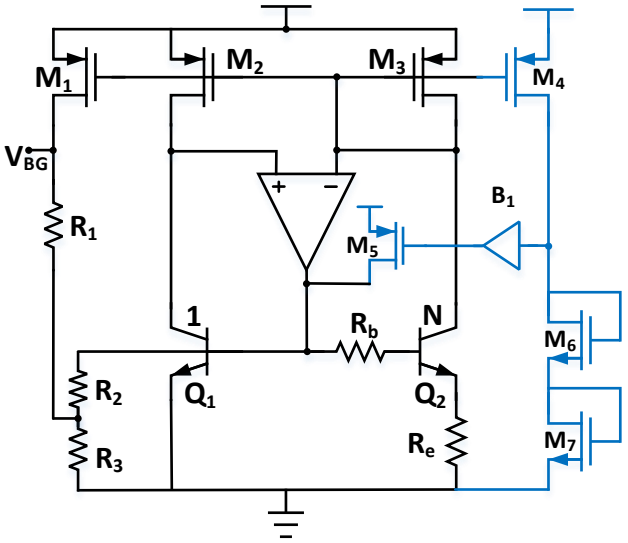

Fig. 1. Schematic of proposed sub bandgap voltage reference

The paper is organized as follows. Section-II discusses the proposed bandgap with curvature compensation. Error sources and start-up circuits are discussed in section-III and IV. Simulation results are discussed in section V which is then followed by the conclusion.

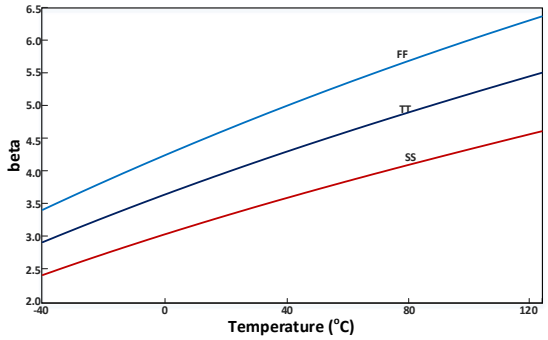

Fig. 2. Variation of β across temperature over BJT corners

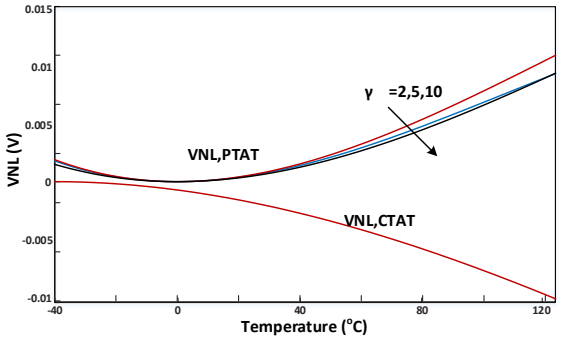

Fig. 3. PTAT and CTAT non-linear terms across temperature

II. PROPOSED SUB-BANDGAP VOLTAGE REFERENCE

Fig 1 shows the proposed sub 1V bandgap reference circuit which uses the vertical parasitic npn transistors Q_1 and Q_2. The ratio of the npn is chosen to be 24 in this design. The current mirror M2 and M3 maintain the same current in the BJTs. The operational amplifier reduces the drain-source mismatch of the transistors. It is to be noted that the BJTs will be in active region even if the collector voltage is lower than base voltage by a diode voltage. This results in a sufficient headroom for the current sources M_{1-3} even at 0.85V supply. The cascodes on these current mirrors are not shown for simplicity. The voltage source V_T is used to check the start up as discussed in section IV.

The resistor R_b is used for curvature compensation and is explained in section III. The opamp output is the base-emitter voltage of the bipolar which is CTAT in nature. Unlike other sub 1V bandgap references, this circuit equalizes the collector currents of BJTs. The PTAT current (I_c) generated by the difference in the base-emitter voltages of the BJT is given by EQ 1.

$$I_C = \frac{\beta}{\left(1+\frac{R_b}{R_e}\right)+\beta}\frac{V_T ln(N)}{R_e} \tag{1}$$

This current is mirrored, converted to voltage using resistors R_{1-3} and then added to the scaled version of the CTAT voltage, resulting in a constant reference voltage. The resistors R_2 and R_3 placed at the output of the opamp scales the CTAT voltage. Resistor R_1 converts the mirrored PTAT current by M_1 into voltage, which is added to the scaled CTAT voltage. The sub 1V bandgap voltage is given by EQ 2. Fig 4 shows the schematic of the pmos input-stage opamp. A level-shifter M_{15} is used to provide headroom to differential pair. The final stage M_{10} drives the resistance $R_{2,3}$ in 1. The loop is compensated with zero created by RC.

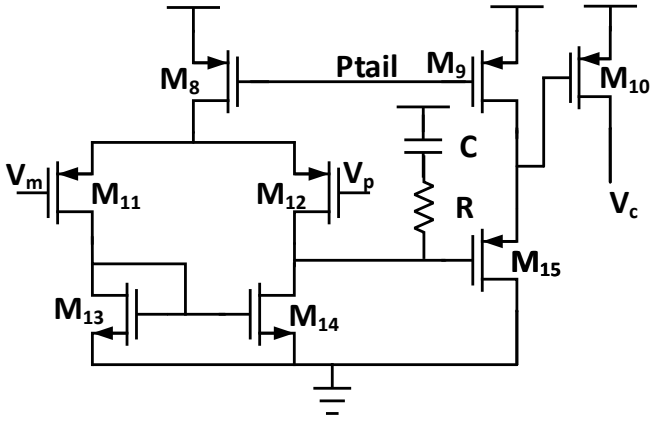

Fig. 4. Schematic of operational amplifier

$$V_{BG} = \left(R_1 + \frac{R_2 R_3}{R_2+R_3}\right)\frac{\beta}{\left(1+\frac{R_b}{R_e}\right)+\beta}\frac{V_T ln(N)}{R_e} + V_{BE1}\frac{R_3}{R_2+R_3} \tag{2}$$

where V_{BE1} is given by [4].

$$V_{BE1}(T) = V_{BG} - (V_{BG} - V_{BE10})\frac{T}{T_0} - (\eta-\alpha)V_T ln\frac{T}{T_0} \tag{3}$$

where η depends on the bipolar structure and is around 4, and α is equal to 1 or 0 depending on PTAT or ZTAT current.

$$V_{NL,ctat} = -(\eta-\alpha)V_T ln\frac{T}{T_0} \tag{4}$$

Expanding the log term of EQ 4 in taylor series and retaining only two terms, we get

$$V_{NL,ctat} = (\eta-\alpha)\frac{k}{q}\left(\frac{T^3}{2{T_o}^2} - \frac{2T^2}{T_o} + \frac{3T}{2}\right) \tag{5}$$

It is to be noted that the coefficient of quadratic term of temperature in EQ 5 is always negative leading to inverting parabola in the curvature of V_{BE1}.

The transistor forward gain β increases with temperature [9] as shown in Fig 2 β can be represented using a polynomial equation as shown in EQ6.

$$\beta = \beta_0 + \beta_1 T + \beta_2 T^2 \tag{6}$$

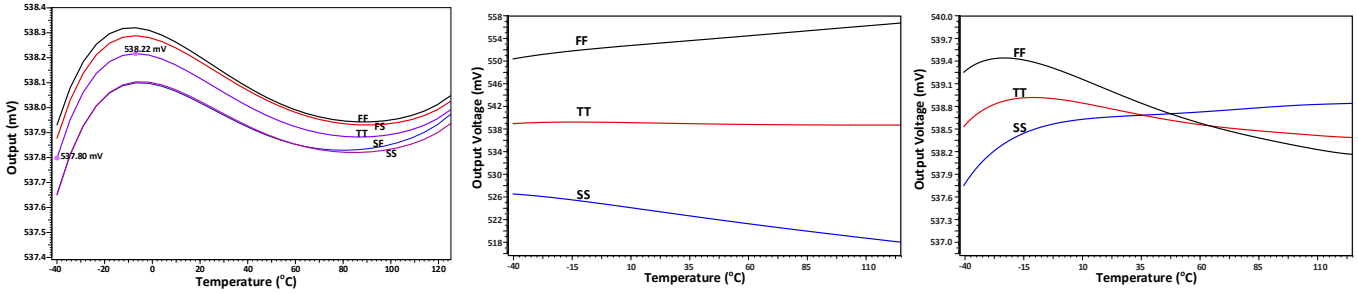

Fig. 5. a)Bandgap voltage with temperature across MOS corners. b)Bandgap voltage with temperature across BJT corners. c)Bandgap voltage with temperature across BJT corners with single point trim

It is to be noted that β_1 is always positive. The quadratic coefficient in the PTAT voltage is approximated in EQ 7. β is ignored in the denominator as it is smaller than γ. This is especially true in vertical BJTs in CMOS process. However, quadratic coefficient in PTAT voltage can be adjusted with base and emitter resistances in EQ 7.

$$V_{NL,ptat} = \left(R_1 + \frac{R_2R_3}{R_2+R_3}\right)\frac{\beta_1}{\gamma}\frac{kln(N)}{qR_e} \tag{7}$$

where γ is $1+R_b/R_e$. The quadratic terms in both PTAT and CTAT voltages has opposite polarity as shown in Fig 3 and they are added in EQ 2 to obtain constant reference voltage.

III. Error Sources

The finite output impedance and offset of the current mirrors, operational amplifier offset, the transistor beta mismatch and resistor mismatch are the error sources in the bandgap. The base resistor R_b will be trimmed at room temperature and all other resistors appear as the ratio in EQ 2. This architecture is insensitive to β variations between transistors as the collector current being matched and the opamp is delivering the base current. The opamp is assumed to have an input-referred offset of V_{off}, whose standard deviation is given by σ_{voff}. This creates a difference in the current between BJTs to be V_{off}/ro, where ro is the impedance at the positive terminal of the opamp. This introduces an error in the bandgap voltage, given by EQ 8. The architecture is insensitive to the amplifier offset as it appears in the logarithmic function.

$$\sigma_{e,off} = \left(\frac{\left(R_1 + \frac{R_2R_3}{R_2+R_3}\right)\beta}{(R_e+R_b)+R_e\beta}\frac{V_T}{I_c ro}\right)^2 \sigma^2_{voff} \tag{8}$$

The current mirror mismatch M_{2-3} causes a current gmv_{cmr} to flow into Q1, where gm is the transconductance of current source and v_{cmr} is the offset between current sources with a standard deviation of σ_{cmr}. This creates a similar error to the opamp offset and is given in EQ 9. Let the current mismatch between $M_{1,3}$ caused by both offset and vds mismatch be represented as I_m with standard deviation of σ_m. This results in an error as given by EQ 10.

$$\sigma^2_{e,cmr} = \left(\frac{\left(R_1 + \frac{R_2R_3}{R_2+R_3}\right)\beta}{(R_e+R_b)+R_e\beta}\frac{V_T g_m}{I_c}\right)^2 \sigma^2_{cmr} \tag{9}$$

$$\sigma^2_{e,m} = \sigma^2_m\left(R_1 + \frac{R_2R_3}{R_2+R_3}\right)^2 \tag{10}$$

Since all are uncorrelated random variables, the total error is obtained as

$$\sigma^2_e = \sigma^2_{e,off} + \sigma^2_{e,cmr} + \sigma^2_{e,m} \tag{11}$$

It is observed from EQ 11, that all error sources except $\sigma_{e,m}$ are suppressed by the npn gain. Hence in this design the current sources are cascoded and heavily degenerated. However, they are not shown here for simplicity. It is to be noted that the current sources have sufficient headroom as the collector voltage can go below the base by one diode voltage for bipolar.

IV. Simulation Results

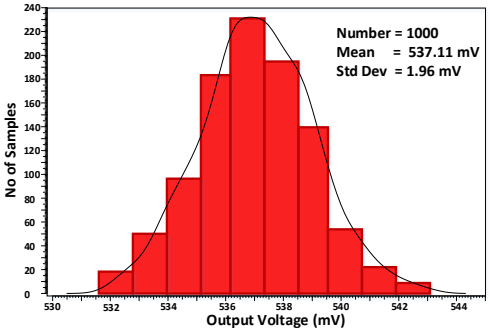

Fig. 6. Monte-Carlo simulation on proposed bandgap

The proposed bandgap reference as shown in Fig 8 was designed and simulated in TSMC 28nm CMOS process and occupies an area of $77um$ X $95um$. The layout includes all decaps and compensation capacitors used in the design. The bandgap core has the ratio of 24 for noise optimization. This bandgap was simulated across all MOS corners and the reference voltage is plotted with temperature in Fig 5a.

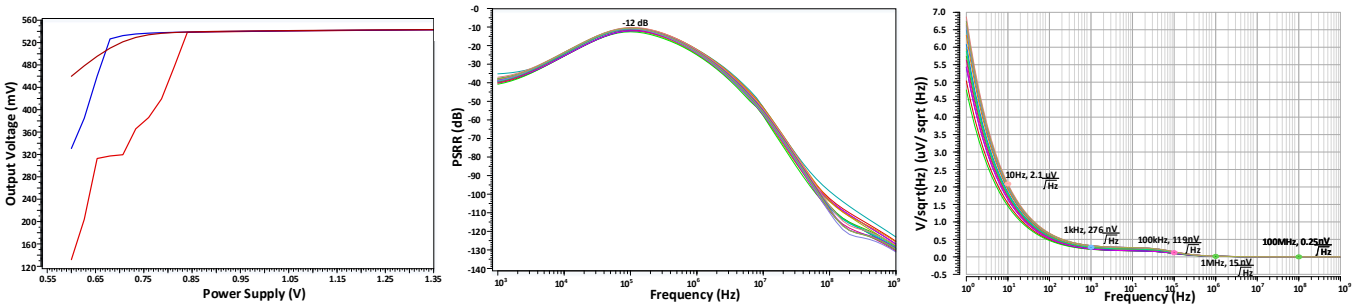

Fig. 7. a)Bandgap voltage with power supply. b)Power Supply Rejection Ratio at bandgap output across corners. c)Noise power spectral density at bandgap output across corners

The bandgap has about 4.7 ppm/°C across temperature in a typical corner. The variation of the reference voltage across corners is about 0.2mV. The bandgap is simulated across all BJT corners in Fig 5b. The variation of the reference voltage in about 5%. We cross verified this variation against a standard Brokaw [1] architecture. A single point trim at R_b reduces the worst case accuracy from 139ppm/°C to 12ppm/°C as shown in Fig 5c. This is attributed to change in the PTAT current and the BJT corner which changes its base emitter voltage. The circuit is simulated across a power supply to see its line regulation as shown in Fig 7a and line sensitivity obtained is 0.5 % when the supply changes from 850mV to 1.35V.

Monte-Carlo simulations were run across 1000 samples to see the effect of mismatches as shown in Fig 6. As explained in section III, only PTAT current mirror $M_{1,3}$ contributes to a significant part of the mismatch. The mean across 1000 runs is about 537.1mV with a standard deviation of 1.96mV which is 0.36%. The Power Supply Rejection Ratio (PSRR)

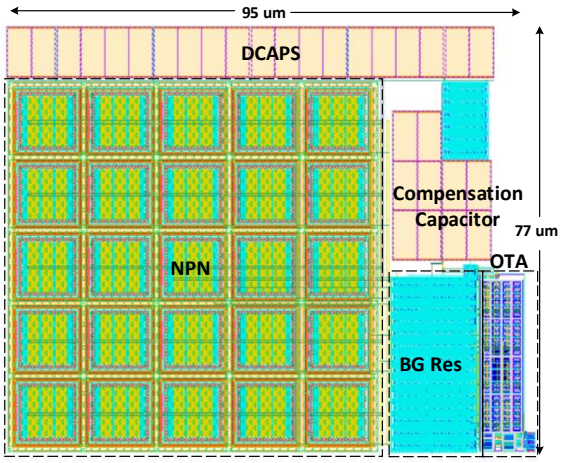

Fig. 8. Layout of the bandgap circuit

was simulated across all corners by injecting a 1V AC signal at the power supply and the gain at the output reference node was plotted against input frequency. Fig 7b shows that the DC PSRR is -40dB. A filter with the resistance of 100kΩ and capacitor of 7.5pF is placed at the bandgap output to limit the maximum PSR to -12dB. The noise spectral density at the output is plotted in Fig 7c across all corners and is $276nV/\sqrt{(Hz)}$ at 1KHz.

V. Conclusion

A voltage mode sub-1V bandgap reference voltage has been designed in TSMC 28nm CMOS technology with a 0.85V power supply. This architecture relaxes the opamp offset and flicker noise specifications and doesn't necessitates the use of techniques,such as chopping. Curvature compensation is achieved with the help of the base resistor. The mechanism of curvature-compensation is derived analytically and verified across simulations. Single point trim places the worst case accuracy at 12ppm/°C. This circuit also inherently provides PTAT current along with a constant voltage to be used for applications like temperature sensors and oscillators.

References

[1] A. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 388–393, Dec. 1974.

[2] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 670–674, May 1999.

[3] G. Zhu, Y. Yang, and Q. Zhang, "A 4.6-ppm/c High-Order Curvature Compensated Bandgap Reference for BMIC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, pp. 1492–1496, Sep. 2019.

[4] P. Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, "Curvature-compensated BiCMOS bandgap with 1-V supply voltage," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1076–1081, Jul. 2001.

[5] J. Yin, J. Yi, M. K. Law, Y. Ling, M. C. Lee, K. P. Ng, B. Gao, H. C. Luong, A. Bermak, M. Chan, W.-H. Ki, C.-Y. Tsui, and M. Yuen, "A System-on-Chip EPC Gen-2 Passive UHF RFID Tag With Embedded Temperature Sensor," *IEEE Journal of Solid-State Circuits*, pp. 2404–2420, Nov. 2010.

[6] Sanborn, Keith, D. Ma, and V. Ivanov, "A sub-1-v low-noise bandgap voltage reference," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2466–2081, Nov. 2007.

[7] Q. Duan and J. Roh, "A 1.2-V 4.2 ppm/c High-Order Curvature-Compensated CMOS Bandgap Reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, Mar. 2015.

[8] R. Nagulapalli, R. K. Palani, and S. Bhagavatula, "A 24.4 ppm/oc voltage mode bandgap reference with a 1.05v supply," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2020.

[9] S. Hussain, R. C. Jaeger, J. C. Suhling, B. M. Wilamowski, M. C. Hamilton, and P. Gnanachchelvi, "Understanding the impact of temperature variations on measurement of stress dependent parameters of bipolar junction transistors," in *Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, May 2014, pp. 1244–1250.