An investigation on the discrete-time nature of excess phase and jitter

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Abstract—**Excess phase in oscillators or phase locked loops is a very important design specification typically modelled as a continuous time signal. In this paper we explain why, when the quantity of interest is jitter, excess phase should be treated as a discrete quantity. This treatment helps explaining noise folding in frequency dividers and analyse its consequences in Phase Locked Loops.**

I. INTRODUCTION

When referring to jitter of a clock signal we are interested in how the crossings of the signal though a certain threshold (A_0) change, due to noise or interferences, when compared to an ideal "clean" reference. In the time domain this quantity is often represented by the excess phase component represented by $\varphi(t)$ in equation 1 where $f(t)$ is periodic in 2π and $V_{CLK}(t)$ periodic in T, with T given by $2\pi/\omega_0$ [1].

$$V_{CLK}(t) = A(t) \cdot f[\omega_0 t + \varphi(t)] \qquad [1]$$

Assuming that $A(t)$ is constant and that the crossings of $A(t) \cdot f(\omega_0 t)$ through A_0 occur at $t = nT$ it becomes apparent that when considering the real case of a clock signal, where A_0 could represent the switching point in a mixer, the instant when an ADC samples the incoming signal or the moment when a flip-flop captures its input, the continuous nature of $\varphi(t)$ is of little importance. In spite of having an impact in the overall wave shape of $V_{CLK}(t)$ the excess phase signal $\varphi(t)$ only affects the threshold crossings at time instants when $\omega_0 t$ reaches multiples of 2π meaning nT.

Therefore it is possible to treat excess phase as the discrete quantity $\varphi(nT)$ or $\varphi[n]$ for simplicity where $\varphi[n]$ represents the value of the excess phase signal at the threshold crossing number n.

Fig.1 illustrates how the discrete excess phase $\varphi[n]$ of the Jittery Clock signal $V_{CLK}(t)$ in (a) may be computed by comparing each rising edge with an Ideal Reference in Fig.1 (b). It should be understood that there is a degree of error associated with taking nT as the time reference for plotting $\varphi[n]$ because, as expected, the instant when the Jittery Clock $V_{CLK}(t)$ crosses the threshold A_0 is not an exact multiple of nT. This limitation is however of no consequence in the majority of practical cases where jitter often represents only a small percentage of the overall period.

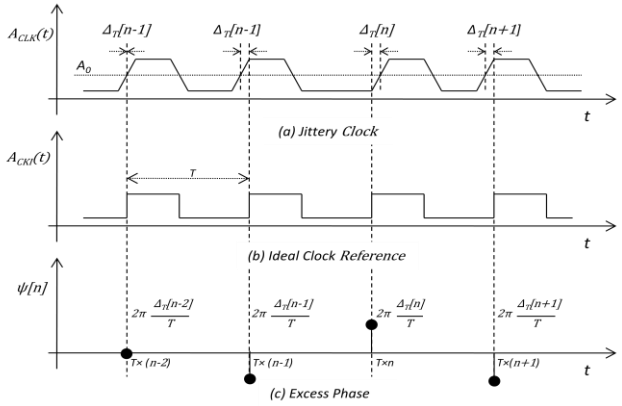

Figure 1. Excess Phase of a Jittery Clock Signal

This approach should also be used carefully in the context of free running oscillators where, due to phenomenon of phase diffusion [2] the variance of $\varphi(t)$ monotonically increases with the time difference between clock edges implying that a free running oscillator completely loses its initial phase information after a sufficiently long amount of time. Therefore oscillator edges eventually wander and drift, loosing synchronicity with a fixed timing reference. With locked oscillators however, such Voltage Controlled Oscillators (VCOs) at the core of Phase Locked Loops (PLLs), the phase drifts are bounded by the feedback path [4] making it possible to use the nT in Fig. 1 as the base to represent $\varphi[n]$.

In this paper we will show how treating excess phase as a discrete quantity provides a powerful insight towards understanding noise folding in frequency dividers and PLLs.

Section II explains why frequency division may be treated as down-sampling and how that explains noise folding. Section III analyzes the consequences of that in the context of PLLs.

II. Frequency Division

A. *Frequecncy Division as edge down sampling.*

In conventional frequency dividers the edges of the output low frequency clock are synchronous with the edges of the input clock signal. There may exist some amount of delay between input and output caused by finite propagation times of digital gates, or due to the number of stages in a cascade of dividers, but the fact is that an edge at the output of the divider only occurs when triggered by an edge at the input. This is the case as well for high frequency pre-scalars that in an LC PLL form the interface between the VCO and the Feedback Divider. However, and as expected, not all input edges cause transitions at the output of the frequency divider. This is illustrated in Fig. 2 where (a) and (c) are the input and output signals of a divider by 4 respectively.

As expected, being a divider by 4 only 1 in 4 input edges is propagated to the output and the location of intermediate edges is unimportant, as long as they occur. Of course in a real implementation the corresponding frequency of the narrow intermediate pulses may cause a failure in the internal digital state machine, but for the purpose of this explanation we assume that that is not the case.

Fig. 2(b) represents the excess phase $\varphi_{IN}[n]$ of the input clock $clk_{VCO}(t)$ and due to the synchronous nature of the divider, the output clock, $clk_{fbk}(t)$, is jittery with only 1 in 4 samples of the excess phase signal arriving at the output.

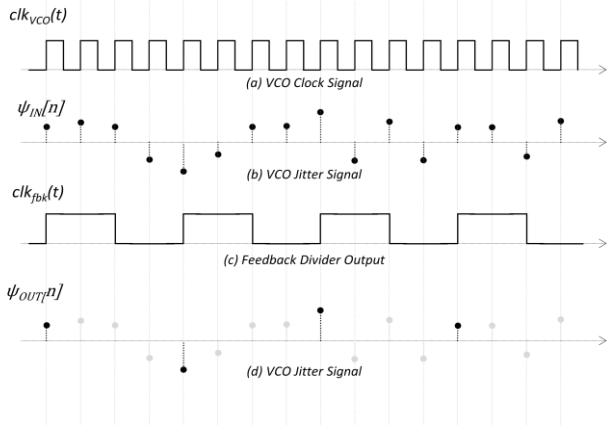

Figure 2. Clock Division as Down Sampling

Therefore one may represent $\varphi_{OUT}[n]$ as $\varphi_{IN}[n \cdot 4]$ meaning the first is a down sampled version of the later, with 4 being used as an example that could be generalized for any N integer.

It is also interesting to observe that if the input excess phase signal $\varphi_{IN}[n]$ had a repetitive pattern of 4 $clk_{VCO}(t)$ periods then the excess phase $\varphi_{OUT}[n]$ at the output would simply have a DC component, representing a phase shift which would be inconsequent as jitter.

As an example Fig. 2 uses rising edges as reference but, as stated earlier on, the conclusions may be generalised to any effective edge used by the circuit that follows the divider, such as a Phase Frequency Detector that following the feedback divider in a PLL or the edge that triggers a particular event in a digital state machine.

B. *Frequecncy Division in the frequency domain.*

The effect of down-sampling may be better understood by looking its effect in the frequency domain. If we consider $X(e^{j\omega})$ to be the discrete-time Fourier transform of the input excess phase $\varphi_{IN}[n]$ of Fig. 2 than we may express the discrete-time Fourier transform of $\varphi_{OUT}[n]$ as [5] :

$$X_d(e^{j\omega}) = \frac{1}{N}\sum_{i=0}^{N-1} X\left(e^{j(\frac{\omega}{N}-\frac{2\pi i}{N})}\right) \quad (2)$$

In equation (2) it should be noted that both spectrum are periodic in the relative frequency 2π however due to the different sampling ratios of $\varphi_{IN}[n]$ and $\varphi_{OUT}[n]$ when expressing the discrete-time Fourier transforms in absolute frequency 2π represents $f_0$and f_0/N respectively with f_0 being the frequency of $clk_{VCO}(t)$.

Fig. 3 has a frequency domain illustration, using absolute frequency, of how the excess phase discrete-time Fourier transform for the original and down sampled spectrums of an arbitrary division ratio of N.

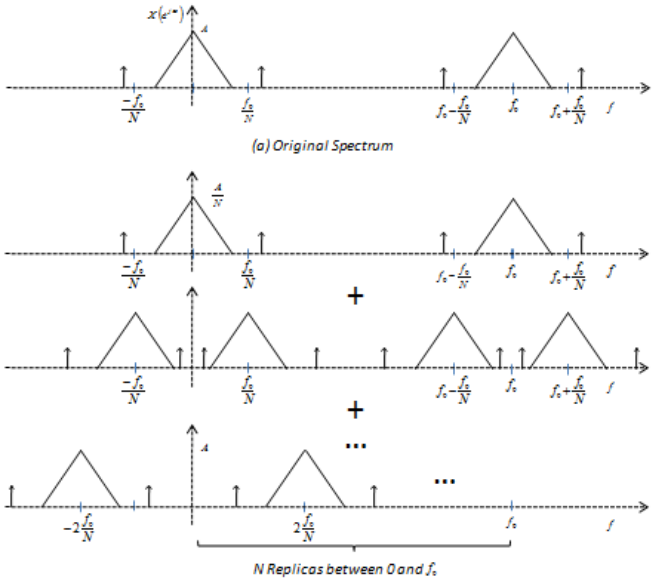

Figure 3. Down-Sampled Spectrum

It may be observed that the replicas of the periodic spectrum centred at multiples of the absolute frequency f_0 are re-centred around multiples of f_0/N, which, due to the absence of filtering create an aliasing effect if $\varphi_{IN}[n]$ contain frequency components bigger than $(f_0/N)/2$. This mechanism is responsible for noise folding in frequency division.

By inspecting equation 2 and ignoring all the terms in the sum with the exception of the first $(i = 0)$ we get the

conventional assumption for the mathematical modelling of frequency division in PLL theory [3], a gain scaling by a factor $1/N$ with N representing the division ratio.

C. *Example Results with a frequency divider.*

As an illustrative example in Fig. 4(a) we represent the first harmonic of a 1MHz square wave clock signal modulated by a 0.1rad peak 40KHz excess phase pattern. This signal was submitted through a behavioral time domain model of a divider by 4. The rich spectrum of the output square wave is represented in Fig.4(b) up to the 5^{th} harmonic and in Fig.4(c) and (d) we can a see plot of the excess phase signals at the input and output of the divider against time respectively. It may be observed by comparing Fig. 4(c) with (d) the phase scaling following the frequency division. It can also be observed that the frequency of the excess phase signal at the output of the divider is was not altered but however the output excess phase has less samples per period due to the reduction in sampling rate following the division.

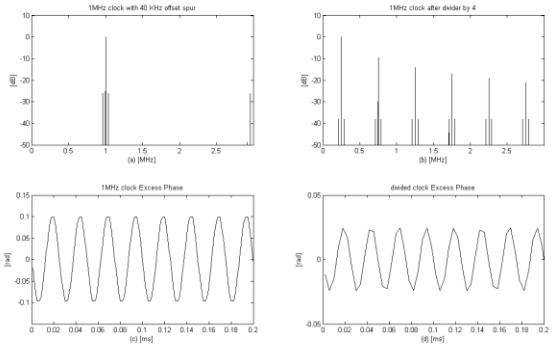

Figure 4. 1MHz clock signal with 40KHz spur

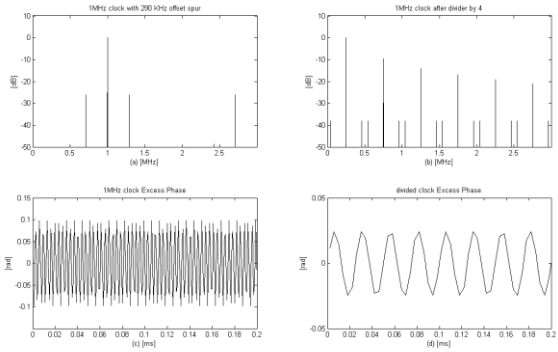

Figure 5. 1MHz clock signal with 290KHz spur

In Fig. 5(a) we illustrate the spectrum of the same 1MHz clock signal as before. It is also modulated by an excess phase pattern with 0.1rad peak amplitude but with a frequency of 290KHz. It is interesting to note that 290KHz is higher than $(f_0/4)/2$, with f_0 now being 1MHz. This means that we expect to observe aliasing when referring the 290KHz spur to the re-sampling frequency of 250KHz with a frequency component appearing at 40KHz, (290KHz - 250KHz). This is observable by inspecting the resulting excess phase signal after the division in Fig. 5(d).

The occurrence of aliasing after the re-sampling is clear by comparing Fig. 5(c) with (d) where we clearly see the 290KHz disappearing to give place to a 40KHz component. Another interesting phenomenon is the observation that even though having spectrums with spurs at different locations the outputs of the dividers with the spectrum, plotted in Fig. 4(b) and Fig. 5(b) have excess phase signals, plotted in Fig. 4(d) and Fig. 5(d), with the same amplitude and frequency. This apparent inconsistency regarding the phase noise and jitter will be the subject of future work by the authors.

III. DIVIDER NOISE FOLDING IN PHASE LOCK LOOPS

A. *Phase Locked Loop description.*

On an integer N PLL such as the one represented in Fig.6 the VCO runs at a frequency N times bigger than the comparison frequency at the inputs of the Phase Frequency Detector (PFD). So for each N VCO edges at the output of the PLL only 1 edge is passed on to the PFD for comparison with the input reference clock. This may be analysed from the point of view of the down sampling of edges as explained in the previous section. And for the purpose of analysing this phenomenon an accurate time domain model for the block diagram of Fig. 6 was built in *Simulink*, with the characteristics described in Table 1.

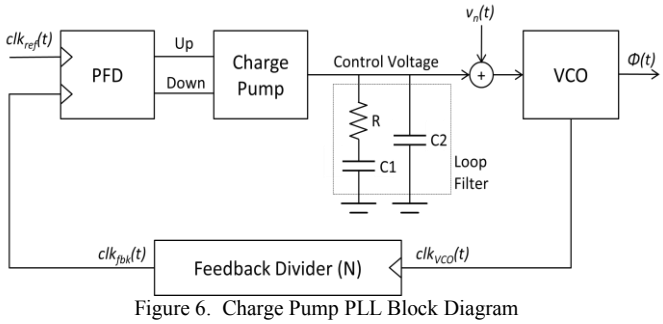

Figure 6. Charge Pump PLL Block Diagram

The additional input Vn(t) shown in Fig. 6 allows for disturbances to be introduced in the control voltage in order to analyze the excess phase response at the output of the VCO. Measuring the excess phase fluctuations, can be done via phase noise measurement. This method uses an inverted low noise op-amp as voltage adder to be used as the disturbance injection mechanism of the control voltage. This op-amp will be connected at the additional input Vn(t) as shown in Fig. 6.

TABLE I. PLL CHARACTERISTICS

Parameter	Table Column Head		
	Descripton	***Value***	***Unit***
f_0	VCO Center Frequency	100	MHz
K_{VCO}	VCO Gain	500	MHz/V
R_2	Zero Resistor	10	kΩ
C_2	Anti-Riple Capacitor	5	pF
C_2	Integration Capacitor	100	pF
I_{CP}	Charge Pump Current	10	μA

Parameter	Table Column Head		
	Descripton	***Value***	***Unit***
N_{DIV}	Feedback Division Ratio	10	-
BW	PLL Bandwidth	1.1	MHz

B. Noise Folding Results.

The circuit was simulated with a range of test signals with varying amplitudes and frequencies. Fig. 7(b) shows the time domain excess phase response to a 10.1MHz disturbance injected in the Control Voltage. The amplitude of the noise signal is 10mVpk and because the PLL bandwidth is 1.1MHz the feedback loop is insensitive to the 10.1MHz frequency, meaning that the output peak excess phase is simply given by VCO transfer characteristic [3] $V_{npk} \times K_{VCO}/10.1MHZ$: 0.5rad. In Fig. 7(b) it is clear the effect 10.1MHz component in the excess phase at the output of the VCO. However, besides this high frequency component it is also visible a low frequency with the same peak magnitude.

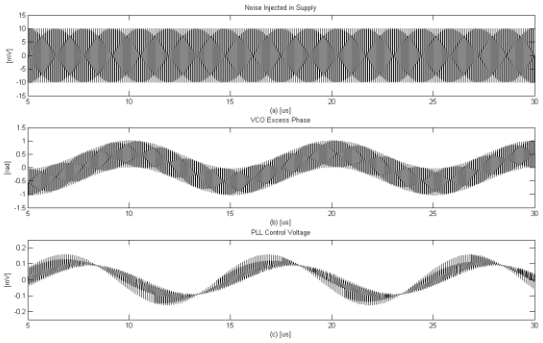

Figure 7 Response to 10.1MHz Vn(t) disturbance

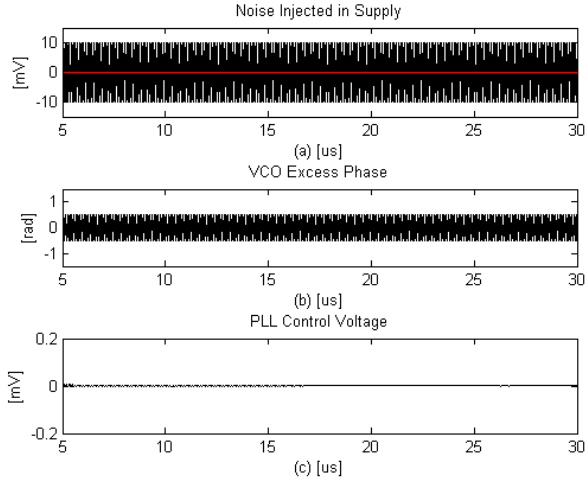

Figure 8 Response to 10.0MHz Vn(t) disturbance

The low frequency components visible in Fig. 7(b) at the output of the VCO is created by the feedback divider when it down-samples by a factor of 10 the 10.1MHz spur injected in the loop. The 10.1MHz signal at the input of the divider is aliases and appears at the output with a frequency of 0.1MHz. But because the bandwidth of the PLL is 1.1MHz, this 0.1MHz components is not filtered is goes straight to the VCO output, with the same amplitude as the original 10.1MHz disturbance. Fig. 7(c) shows the Control Voltage tracking the aliased low frequency spur.

Also interesting is to observe is the response of the loop to a 10MHz disturbance injected in the control voltage in Fig. 8(a). In (b) the excess phase at the output of the VCO is visible, however in these conditions the PLL Control Voltage remains almost static, the reason being that the 10MHz spur, sampled at 100MHz by the VCO, is aliased to DC when down-sampled by a factor of 10. Therefore the PLL control loop is completely insensitive to it.

C. Overal Transfer Characteristic.

By exercising the previous model it is possible to plot, the overall transfer characteristic from noise injected in the control voltage to excess phase at the output of the VCO, shown in Fig. 9. The waveform identified as 1st and 2nd are the PLL forward transfer characteristic, re-centered at multiples of the reference frequency and shaped by the VCO forward transfer characteristic.

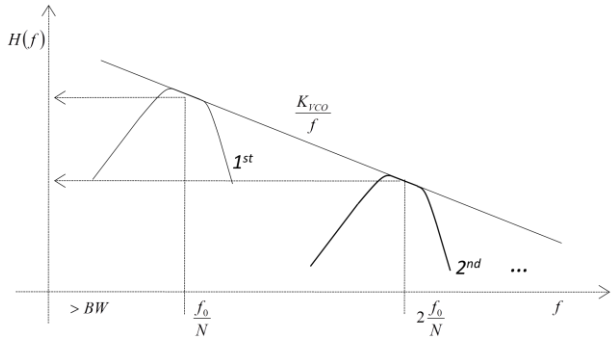

Figure 9. Control Voltage to Excess Phase Transfer Characteristic

Noise injected in Vn(t) at small offsets of multiples of the reference frequency, follows two paths to the output of the VCO. The first, direct sees a scaling by the VCO transfer characteristic K_{VCO}/f. The second is folded to DC and further shaped by the PLL closed loop forward (input to out) transfer characteristic as illustrated in Fig. 9.

IV. CONCLUSION

We presented excess phase as a discrete-time quantity, and frequency division as down-sampling of clock edges. This treatment allows us to explain noise folding as observed in frequency dividers. We then extend this analysis to phase locked loops and present the overall transfer characteristic for control voltage disturbances with the replicas created by down-sampling. All simulation results presented in this paper were performed using Cadence Virtuoso suite 6.1.3 with real, silicon proven spice models.

References

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