Development of a Temperature Insensitive Current Controlled Current Source for LNA Bias Circuit Applications

By

Matthew Richard Green

School of Technology
Oxford Brookes University

A thesis submitted in partial fulfilment of the requirements of Oxford Brookes University for the degree of

Doctor of Philosophy

October 2006

THE FOLLOWING HAVE NOT BEEN COPIED ON INSTRUCTION FROM THE UNIVERSITY

Page 2-5 figure 2.3 and 2.4

Page 2-6 figure 2.5

Page 2-7 figure 2.6

Page 2-24 figure 2.18

Page 2-29 figure 2.25

Page 5-4 figure 5.2 and 5.3

Appendix B

DEDICATION

This thesis is dedicated to Yunyee and Lydia.

ACKNOWLEDGEMENTS

I would like to gratefully acknowledge the help and support received from friends and colleagues without whom this thesis would have been a significantly weaker offering. In particular, I am especially thankful to Bryan Hart for his helpful comments and discussions throughout the duration of my studies. In addition, I would like to thank Dr. Khaled Hayatleh and Prof. John Lidgey for being my Director of Studies and PhD supervisor, respectively. Your help and guidance has been invaluable.

Finally, I would like to thank my family for all their support and encouragement over the years, my partner Yunyee for her understanding and devotion throughout the months taken to prepare this thesis and our baby daughter Lydia who joined us near the end and filled our lives with happiness.

ABSTRACT

The research described in this thesis is concerned with the analysis, design and development of a novel temperature insensitive Current Controlled Current Source (CCCS), in bipolar technology, in order to provide accurate amplification of a Proportional To Absolute Temperature (PTAT) reference current. The output current of the CCCS is intended for application as the bias current for a bipolar Low Noise Amplifier (LNA) in order to minimise gain variations with temperature across the industrial temperature range (-40°C to 85°C).

The thesis begins with an explanation of key parameters concerned with LNA design and a target specification is defined. In Chapter 2, a conventional LNA, with constant with temperature bias current, is developed following a methodical approach based on conventional techniques. This meets the previously defined specification at room temperature but exhibits large gain variations with changes in temperature. The analysis and simulation results of this conventional LNA serve as a benchmark for comparison with later designs.

In order to minimise any gain variations with temperature of a bipolar amplifier it is well known that the applied bias current should be PTAT. Thus, a thorough analysis and comparative review of traditional and novel PTAT reference current generator circuits is conducted in Chapters 3 and 4. Based on these findings the PTAT generator exhibiting best performance in terms of output current accuracy and insensitivity to power supply variations is presented. However, this circuit cannot accurately produce large *mA* level currents necessary for LNA bias applications so that sufficient linearity of the LNA is maintained. Thus, a need for some form of accurate CCCS or Voltage Controlled Current Source (VCCS), which should be temperature insensitive in order to preserve the desired temperature coefficient of the reference current/voltage, is highlighted.

Traditional VCCS/CCCS designs are investigated in Chapter 5. Limitations of these approaches leads to the design and development of a novel CCCS with built in PTAT reference. The presented CCCS utilises a new, previously unseen, architecture and has led to a patent application [1]. The author has reported the majority of this work in technical literature [2-4].

In Chapter 6, the output of the novel CCCS is adapted to include the conventional LNA circuit designed previously in Chapter 2. The results of the combined LNA and CCCS are compared with the conventional LNA. The combined LNA and CCCS offers a dramatic reduction in gain variation with temperature.

LIST OF AUTHOR'S PUBLICATIONS

[1] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'Direct Current Converter Circuit', *UK Patent Application GB051623.8*, 2005.

[2] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'Temperature-Independent Direct Current Converter Technique', *IEE Electronic Letters*, Nov. 2005, Vol. 41, No. 23, pp. 1258-1259.

[3] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'PTAT Direct Current Converter for Bias Circuit Applications', *IEE Electronic Letters*, Apr. 2006, Vol. 42, No. 9, pp. 530-531.

[4] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'A Novel *mA* Level PTAT Current Generator Technique', *Proceedings of North East Workshop on Circuits And Systems (NEWCAS)*, Gatineau, Canada, June 2006, pp. 221-224.

LIST OF SYMBOLS AND ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
A_I	Current Gain
A_V	Voltage Gain
BJT	Bipolar Junction Transistor
BWCS+VFCM	Buffered Widlar Current Source with Voltage Following Current Mirror
C	Coulombs
CC	Current Conveyor
CCCS	Current Controlled Current Source
CMOS	Complementary Metal Oxide Semiconductor
CP_{-1dB}	1dB Compression Point
DC	Direct Current
DSP	Digital Signal Processor
DR	Dynamic Range
g_m	Transconductance
HG	High Gain
I_C	Collector Current
I_{COPT}	Optimum Collector Current
ICP_{-1dB}	Input-referred 1dB Compression Point
I_{in}	Input Current
IP_3	Third Order Intermodulation Intercept Point
IIP_3	Input-referred Third Order Intermodulation Intercept Point
I_{out}	Output Current
I_S	Saturation Current
ITR	Industrial Temperature Range
k	Boltzmann's Constant
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law

LG	Low Gain
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
NF	Noise Figure
OA	Operational Amplifier
OCP_{-1dB}	Output-referred 1dB Compression Point
OIP_3	Output-referred Third Order Intermodulation Intercept Point
ppm/°C	Parts per Million per Degree Celcius
ppm/V	Parts per Million per Volt
PTAT	Proportional To Absolute Temperature
q	Amount of Charge on a Single Electron
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RRV	Reduced Resistor Version (of the advanced circuit)
S	Sensitivity to Changes in V_{CC}
SFDR	Spurious Free Dynamic Range
SoC	System on Chip
T	Temperature in Degrees Kelvin
TC	Temperature Coefficient
TC_{gm}	Transconductance Temperature Coefficient
TC_{IC}	Collector Current Temperature Coefficient
TC_{Iout}	Output Current Temperature Coefficient
TC_{VT}	Thermal Voltage Temperature Coefficient
UMTS	Universal Mobile Telecommunications System
V_{AQ}	Early Voltage (subscript Q (N or P) indicates the device type (NPN or PNP))
V_{BE}	Collector-Emitter Voltage
VBS	Voltage Balancing Stage
V_{CB}	Collector-Base Voltage
V_{CC}	Power Supply Voltage (Common Collector Voltage)
VCCS	Voltage Controlled Current Source
V_{CE}	Collector-Emitter Voltage
VSWR	Voltage Standing Wave Ratio

V_T	Thermal Voltage
WCS+BCM	Wilson Current Source with Buffered Current Mirror
WCS+CCM	Wilson Current Source with Cascode Current Mirror
WCS+SCM	Wilson Current Source with Simple Current Mirror
WCS+VFCM	Wilson Current Source with Voltage Following Current Mirror
WCS+WCM	Wilson Current Source with Wilson Current Mirror
X_{IN}	Input Reactance
X_{OPT}	Optimum noise reactance
Z_{IN}	Input Impedance
Z_{OPT}	Optimum noise impedance
Z_L	Load Impedance
β	Current Gain of a Single Transistor
°C	Degrees Celsius
°K	Degrees Kelvin
2G	2nd Generation
3G	3rd Generation

CONTENTS

CHAPTER 1

Thesis Introduction and Definition of Important Low Noise Amplifier Design Parameters

The wireless communications marketplace has experienced tremendous growth in the last two decades. This is largely due to the successful global deployment of second-generation (2G) and third generation (3G) digital cellular systems. A 2G technology known as Global Systems for Mobile Communications (GSM) has become the world's fastest growing communications technology of all time and is currently the leading global mobile standard. GSM was first implemented in 1991, and now operates in approximately 210 countries across the world serving an estimated 1.7 billion users [1].

In more recent years an increasing number of other wireless communication products have begun to appear. In May 2003 a 3G cellular system, namely, the Universal Mobile Telephone Service (UMTS) [2], was launched in the UK. In addition, many wireless interconnectivity systems have become commonplace. These include Wi-Fi [3] (based on the IEEE 802.11 family of standards [4]), Bluetooth [5] (based on the IEEE 802.15.1 standard [4]), Zigbee [6] (based on the IEEE 802.15.4 standard [4]) and Ultra Wide-Band (UWB) [7] (based on the IEEE 802.15.3a standard [4]).

The development of yet more communication standards and products looks set to continue unabated. This will result in many innovative circuits and systems but will also lead to numerous complex design challenges that are not encountered in conventional low frequency systems.

1.1 System on Chip – The Need for Integration

The introduction of 3G cellular telecommunication systems, such as UMTS, has hugely increased the complexity of wireless handsets. This added complexity coupled with the need for lower cost, more power efficient and smaller sized wireless products has resulted in increasing the levels of system integration being sought by the research community.

Figure 1.1 shows a block diagram of a generic receiver circuit. This features a front-end sub-circuit comprising of an antenna, Low Noise Amplifier (LNA), mixer, Local Oscillator (LO) and Low Pass Filter (LPF). In addition, the receiver also consists of a back-end sub-circuit comprising of an Analogue to Digital Converter (ADC) and Digital Signal Processing blocks.

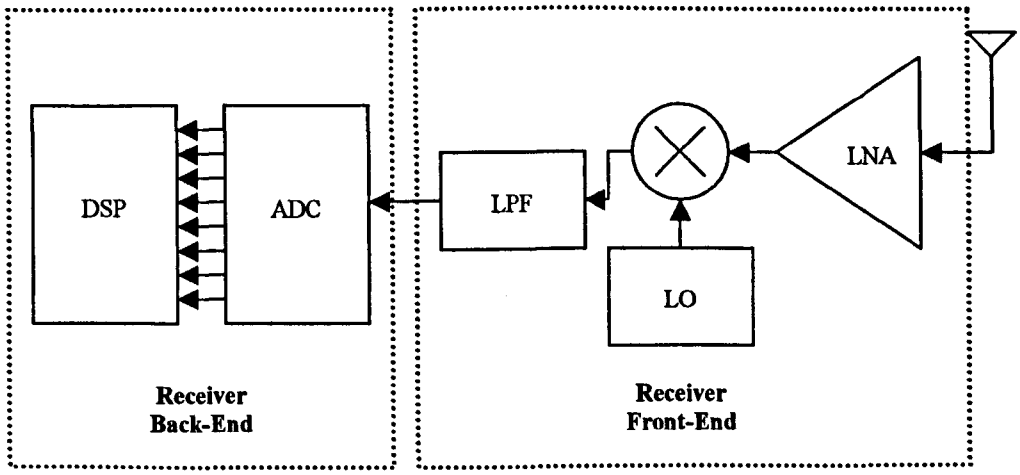

Figure 1.1 – Block Diagram of a Generic Receiver Circuit

In most commercial Radio Frequency Integrated Circuits (RFICs), the mainly digital circuitry contained within the receiver back-end is formed in CMOS technology. In order to achieve a high degree of integration, it is desirable to integrate the receiver front-end and back-end sub-circuits into the same 'chip' or RFIC. Thus, creating a complete radio receiver System on Chip (SoC) design. However, in order for this work to be applicable to SoC design, the front-end must be constructed in a technology that is currently compatible with CMOS technology. Therefore, it is fair to say that, the front-end must use either CMOS or BiCMOS (a combination of bipolar and CMOS) technologies.

Traditionally, RFIC circuits were often constructed in bipolar processes because they exhibit high gain, high linearity and low noise performance at Radio Frequencies (RF). However, in recent years CMOS device geometries have significantly decreased. Commercial CMOS processed now offer device geometries down to $0.13\mu m$ while $90nm$, and smaller, device geometries are currently under development.

This reduction in device size, together with the advent of improved integrated passive components, has led to CMOS technology becoming a viable alternative for RF applications. Such technology is often referred to as RFCMOS. Unfortunately CMOS or RFCMOS wafers, which use very small geometry devices, are still significantly more expensive to fabricate than BiCMOS wafers that use more mature CMOS processes with slightly larger device geometries. Table 1.1 illustrates the cost of fabrication for various RFCMOS and BiCMOS processes available through the Europractice IC Service [8].

Vendor	Process Type	CMOS Device Geometry	Process	Cost (Euro)
UMC	RFCMOS	0.18μm	L180 Mixed-Mode/RFCMOS	16000 (1)
UMC	RFCMOS	0.13μm	L130E Mixed-Mode/RFCMOS	35600 (1)
UMC	RFCMOS	90nm	L90N Logic/Mixed-Mode/RFCMOS	55200 (2)
AMS	BiCMOS	0.35μm	S35 SiGe 4M/4P	1000 (3)
IHP	BiCMOS	0.25μm	SGC25B	3500 (4)

(1) price per 5x5mm block needed
(2) price per 4x4mm block needed
(3) price = area (mm^2) x quantity (min cost equivalent to $7mm^2$)
(4) price = area (mm^2) x quantity (min cost equivalent to $5mm^2$)

Table 1.1 – Comparison of Fabrication Cost for Various RFCMOS and BiCMOS Processes Available Through the Europractice IC Service [8]

Table 1.1 clearly demonstrates that BiCMOS currently offers significant savings in terms of fabrication cost. For this reason, the work discussed in subsequent sections of this thesis will utilise bipolar devices intended for use in a BiCMOS process.

1.2 The Role of a Low Noise Amplifier

A low noise amplifier (LNA) is a fundamental part of any RF receiver system. In real-world situations, such as cellular-phone systems, the received signal is generally extremely small in amplitude. Therefore, the main role of an LNA is to amplify the

initial carrier signal to a sufficient level before the information it contains can be properly demodulated by subsequent sections of the receiver. However, all amplifiers add noise to the signals they boost. Thus, when amplifying a very low-level signal, the amplifier's own noise can swamp the signal. Therefore, the LNA must amplify the carrier signal without adding significant noise, thus, preserving the required Signal to Noise Ratio (*SNR*) at very low power levels.

Additionally, for large signal levels, the LNA should amplify the received signal without introducing significant distortion in order to minimise channel interference. Therefore, the LNA should be highly linear. Typical measures of linearity are the 1dB compression point and 3rd order intermodulation intercept point. These, and other key LNA parameters, are discussed in the following sub-sections.

1.2.1 Noise Factor and Noise Figure

As the name suggests, the noise performance of an LNA is its most important attribute. A useful measure of the noise performance of any system or circuit is the Noise Factor (*F*). This is a measure of how much additional noise a system will contribute to the output signal on top of that already present due to the source. *F* is defined as either:

$$F = \frac{input\ SNR}{output\ SNR} \tag{1.1}$$

or

$$F = \frac{total\ equivalent\ input\ noise\ power}{input\ noise\ power\ due\ to\ source\ only} \tag{1.2}$$

A receiver system, regardless of the particular topology, consists of a cascade of different circuit blocks. Therefore, in order to calculate the *F* of an entire receiver system, it is necessary to calculate the *F* of multiple cascaded systems. This is easily achieved using Friis' formula [9]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots\ldots \frac{F_n - 1}{G_1 G_2 \ldots\ldots G_{(n-1)}} \tag{1.3}$$

where F_1 and G_1 represent the noise factor and gain of the 1st stage of the receiver. F_2 and G_2 represent the noise factor and gain of the 2nd stage of the receiver etc. Often it is useful to express F in a decibel form. The Noise Figure (NF) is a decibel representation of F. Thus:

$$NF = 10 \log_{10} (F) \tag{1.4}$$

The NF of an LNA is particularly critical in determining the overall NF of the whole receiver system, since it is generally the 1st stage of the receiver. From (1.3) it is clearly seen that provided the LNA has sufficient gain; the LNA is the majority contributor to the overall receiver NF.

1.2.2 Linearity

The linearity of an LNA is an indication of the maximum input signal power that can be handled, without introducing significant distortion to its output signal. Ideally the output signal $y(t)$ of an amplifier is linearly related to the input signal $x(t)$. However, the gain of a bipolar transistor, in a memoryless system, is weakly non-linear and can be described by the Taylor expansion series [10]:

$$y(t) = K_1 . x(t) + K_2 . (x(t))^2 + K_3 . (x(t))^3 + \ldots\ldots \tag{1.5}$$

For simplicity, the following analysis neglects non-linear terms above the 3rd order. Thus, when the input-output relationship is given by the analytic relationship:

$$y(t) = f(x(t)) \tag{1.6}$$

The coefficients K_1, K_2 and K_3 are given as:

$$K_1 = \frac{\partial f}{\partial x} \tag{1.7}$$

$$K_2 = \frac{\partial^2 f}{2\partial x^2} \tag{1.8}$$

$$K_3 = \frac{\partial^3 f}{6\partial x^3} \tag{1.9}$$

The coefficient K_1 describes the linear 1st order behaviour of the device. Similarly, the coefficients K_2 and K_3 describe the 2nd order and 3rd order non-linear behaviour of the device. Now, in this case, the input signal is a single tone that takes the form:

$$x(t) = A_1 \cos(\omega_1 t) \tag{1.10}$$

By substitution of (1.10) into (1.5), an expression for the output signal is obtained.

$$\begin{aligned} y(t) = {} & A_1 K_1 \cos(\omega_1 t) + A_1^2 K_2 \left(\frac{1}{2} + \frac{1}{2}\cos(2\omega_1 t) \right) \\ & + A_1^3 K_3 \left(\frac{3}{4}\cos(\omega_1 t) + \frac{1}{4}\cos(3\omega_1 t) \right) \end{aligned} \tag{1.11}$$

This result can be rewritten as:

$$\begin{aligned} y(t) = {} & \frac{A_1^2 K_2}{2} + \left(A_1 K_1 + \frac{3A_1^3 K_3}{4} \right) \cos(\omega_1 t) + \frac{A_1^2 K_2}{2} \cos(2\omega_1 t) \\ & + \frac{A_1^3 K_3}{4} \cos(3\omega_1 t) \end{aligned} \tag{1.12}$$

Thus, a single tone input signal at the fundamental frequency results an output signal, at the same frequency, with the addition of a DC term, a 2nd harmonic term and a 3rd harmonic term. However, the fundamental frequency term is of most interest. See overleaf (1.13).

$$\left(A_1K_1+\frac{3A_1^3K_3}{4}\right)\cos(\omega_1 t) \tag{1.13}$$

From (1.13) it is clear that the fundamental frequency is amplified by the sum of a linear gain term A_1K_1 and a third order term $\frac{3A_1^3K_3}{4}$. At low input signal levels the linear term is dominant. However, as the input signal level increases; the 3rd order term becomes more significant. If the sign of the 3rd order term is positive then this results in gain expansion. Conversely, if the sign of the 3rd order term is negative then this results in gain compression. However amplifiers, in the usual case, exhibit gain compression. Therefore, a useful figure of merit for linearity is the 1dB Compression Point (CP_{-1dB}). This is defined as the signal level at which the gain has dropped by 1dB from its small-signal value. This is shown in Figure 1.1 and can be input referred (ICP_{-1dB}) or output referred (OCP_{-1dB}).

Using the same method as presented in the above analysis, it is now assumed that the input signal consists of two tones at the fundamental frequencies ω_1 and ω_2. Thus:

$$x(t)=A_1\cos(\omega_1 t)+A_2\cos(\omega_2 t) \tag{1.14}$$

Again, by substitution of (1.14) into (1.5), an expression for the output signal is obtained.

$$\begin{aligned}
y(t)=&\frac{\left(A_1^2+A_2^2\right)K_2}{2}+\left(A_1K_1+\frac{3K_3}{4}\left(A_1^3+2A_1A_2^2\right)\right)\cos(\omega_1 t)\\
&+\left(A_2K_1+\frac{3K_3}{4}\left(A_2^3+2A_1^2A_2\right)\right)\cos(\omega_2 t)+\frac{A_1^2K_2}{2}\cos(2\omega_1 t)\\
&+\frac{A_2^2K_2}{2}\cos(2\omega_2 t)+\frac{A_1^3K_3}{4}\cos(3\omega_1 t)+\frac{A_2^3K_3}{4}\cos(3\omega_2 t)\\
&+K_2A_1A_2\cos(\omega_1\pm\omega_2)t+\frac{3K_3A_1^2A_2}{4}\cos(2\omega_1\pm\omega_2)t\\
&+\frac{3K_3A_1A_2^2}{4}\cos(2\omega_2\pm\omega_1)t
\end{aligned} \tag{1.15}$$

In this case, an input signal consisting of two tones, at the fundamental frequencies ω_1 and ω_2, results in an output signal containing the same fundamental frequencies, again, with the addition of a DC term, a 2nd harmonic term, a 3rd harmonic term and further intermodulation terms. However, the fundamental frequency and intermodulation terms are of most interest. See expressions (1.16) to (1.20).

$$\left(A_1K_1+\frac{3K_3}{4}\left(A_1^3+2A_1A_2^2\right)\right)\cos(\omega_1 t) \tag{1.16}$$

$$\left(A_2K_1+\frac{3K_3}{4}\left(A_2^3+2A_1^2A_2\right)\right)\cos(\omega_2 t) \tag{1.17}$$

From (1.16) and (1.17) it is easily seen that the fundamental frequencies are amplified by a linear term A_1K_1 or A_2K_1, as in the case of a single tone input signal, and a cross modulation term $\frac{3K_3}{4}\left(A_1^3+2A_1A_2^2\right)$ or $\frac{3K_3}{4}\left(A_2^3+2A_1^2A_2\right)$. The presence of cross modulation terms means that the amplitude of the fundamental ω_1 is dependent on the amplitude of the signal ω_2 and vice versa. As discussed previously, the cross modulation terms result in gain compression. This can result in a particular problem known as desensitisation. Suppose ω_1 represents a desired signal and ω_2 is an unwanted signal with an amplitude much greater than that of ω_1. Large amplitude unwanted signals are often called blockers. Now, assuming the cross modulation term has a negative sign, the blocker will cause the gain to compress prematurely. Thus, reducing the sensitivity of the receiver. For this reason, care must be taken when measuring the compression point. It is therefore common to specify CP_{1dB} both with and without blocker signals present. The intermodulation terms are given via expressions (1.18) to (1.20).

$$\frac{3K_3A_1^2A_2}{4}\cos(2\omega_1\pm\omega_2)t \tag{1.18}$$

$$\frac{3K_3A_1A_2^2}{4}\cos(2\omega_2\pm\omega_1)t \tag{1.19}$$

The above intermodulation terms result in additional signals at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. If ω_1 and ω_2 are close together, these intermodulation terms can fall within the bandwidth of the circuit where they cannot be filtered out, thus, creating distortion in the output signal. A common measure of the intermodulation distortion is the 3rd order intercept point (IP_3). This is a fictional value that is defined by the point at which the extrapolated values the fundamental and intermodulation signals intercept each other. This is also shown in Figure 1.1. With a two-tone input signal, there are two possible IP_3 results (i.e. using either $2\omega_1 - \omega_2$ or $2\omega_2 - \omega_1$). Generally, both results are identical. However, differences may arise if both tones are not well within the circuit bandwidth so that the small-signal frequency response differs at each intermodulation frequency. Also, differences will arise if ω_1 and ω_2 have differing amplitudes. In either case, the lowest IP_3 value is taken. IP_3 can be input referred (IIP_3) or output referred (OIP_3).

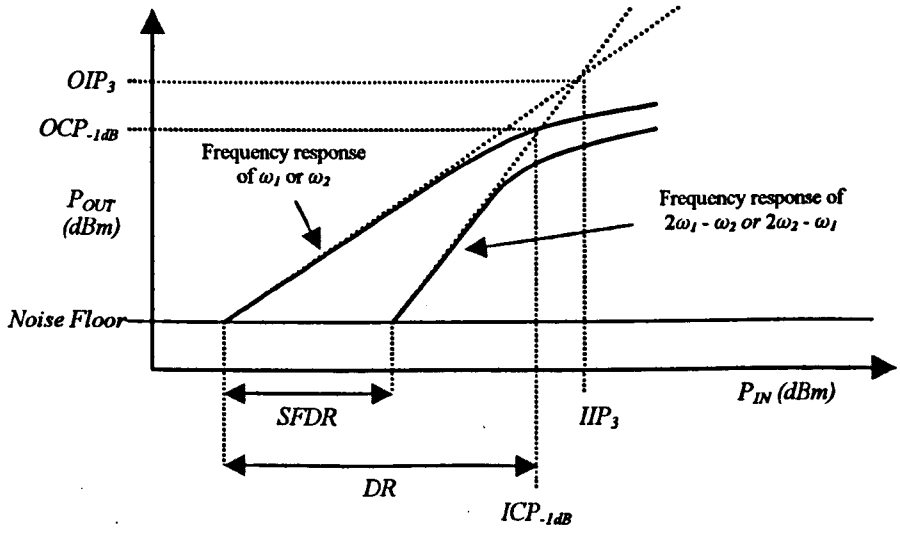

Figure 1.1 - A Graphical Illustration of how the 1dB Compression Point, 3rd Order Intermodulation Intercept Point, Dynamic Range and Spurious Free Dynamic Range are Derived

$$K_2 A_1 A_2 \cos(\omega_1 \pm \omega_2)t \qquad (1.20)$$

The expression (1.20) illustrates another intermodulation product that is present at $\omega_1 \pm \omega_2$. Initially this may seem of little concern, as it is highly likely to fall outside the circuit bandwidth. However, due to weak internal feedback in an amplifier, this

term may re-mix with other terms resulting in additional intermodulation terms at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. Thus, it is often useful to filter out the $\omega_1 \pm \omega_2$ term at the input in order to enhance IP_3 [11].

Figure 1.1 also illustrates two other useful parameters. These are the Dynamic Range (DR) and Spurious Free Dynamic Range (SFDR). DR is defined as the range of input signal amplitude over which the circuit can be used without introducing significant signal degradation at the output. The lower limit is determined by the input referred noise, or noise floor, whilst the upper limit defined by ICP_{-1dB}. SFDR is the range of input signal amplitude that can be handled by the circuit before the intermodulation products become stronger than the noise floor. Thus, the noise floor defines the lower limit and the point at which the amplitude of the 3rd order intermodulation product (i.e. $2\omega_1 - \omega_2$ or $2\omega_2 - \omega_1$) intercepts the noise floor defines the upper limit.

1.2.3 Stability

A fundamental requirement of all RF amplifiers is unconditional stability across the entire frequency range of interest. That is the frequency range at which the amplifier exhibits greater than unity gain. Unconditional stability requires that the amplifier will not oscillate under any source or load impedance termination conditions provided that the real part of the source or load impedance is positive.

In 1962 Rollet first proposed a simple stability criterion [12]. This is known as the Rollet Factor or *K*-Factor (*K*). In scattering parameter [13] form, *K* is defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{1.21}$$

where:

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{1.22}$$

However, in order to achieve unconditional stability at a particular frequency, the conditions $K>1$ and $|\Delta|<1$ must be met. Unfortunately, K is unable to quantify stability, thus, it merely serves as an indicator if a point of stability has been reached. Therefore, if K is found to be less than unity, the degree of instability cannot be directly inferred. Instead a graphical method (i.e. plotting stability circles on a smith chart) must be employed [14]. In addition, simultaneously satisfying two stability conditions is not as convenient as a single one. Therefore, Lombardi and Neri proposed a new stability criterion [15] in 1992. This is defined as:

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-S_{11}^{*}\Delta|+|S_{21}S_{12}|} \tag{1.23}$$

In this case, unconditional stability at a particular frequency is achieved provided the single condition $\mu>1$ is met. By contrast to K, μ is defined as the minimum distance between the origin of a smith chart and any unstable region. Thus, it is not only more convenient than K to use but provides insightful meaning in order to assess the degree of instability.

1.3 Motivation for Thesis

LNA design is a very active area of interest within academic and industrial research groups. This is because an LNA plays such a key role in all forms of receiver design; as explained in the previous section. Many papers detailing a wide variety of LNA research can be seen in technical literature. However, little of this is devoted to LNA bias circuits. Bias circuits are necessary in order to provide the necessary DC bias conditions for an LNA to function as desired. However, most bias circuits seen in the technical literature rely on the use of practically identical current mirror schemes.

The major motivation behind this thesis is to improve on traditional bias circuit design for LNA applications. Particularly, with regards to, providing temperature-independent DC current amplification of a much smaller temperature-dependent

reference current (i.e. bandgap or proportional to absolute temperature current). The amplified output current can then be used to ensure that the LNA will maintain either constant voltage gain or DC power consumption across a wide temperature range.

1.4 LNA Specification

UMTS is the intended application for all LNA designs in this thesis. However, in order to develop a specification for a particular LNA design, it is first necessary to know the overall receiver system requirements along with the proposed receiver topology. From the overall receiver requirements, it is necessary to determine the individual requirements of the analog front-end and digital back-end.

Several examples for determining analog receiver requirements have been reported in the technical literature [16-18]. However, in order for these methods to be accurate, a detailed knowledge of the digital back-end performance is required. Once this is known, the required analog front-end performance can be specified. Only then can the individual requirements for each receiver front-end block be determined. However, complete receiver planning is beyond the scope of this thesis. Therefore, the final LNA design in this thesis is targeted to meet a typical specification adapted from [19] and [20]. This is shown in Table 1.2.

Parameter (Frequency = 2140 *MHz*)	Targeted Performance
Gain (S_{21})	15-20 *dB* (*HG Mode*) 3-8 *dB* (*LG Mode*)
Noise Figure	<2*dB* (*HG Mode*)
$ICP_{.1dB}$	>-15 *dBm*
IIP_3	>-5 *dBm*
Input Return Loss (S_{11})	>12 *dB*
Output Return Loss (S_{22})	>12 *dB*
Reverse Isolation -(S_{12})	>60 *dB*

Table 1.2 – Proposed LNA Specification

In addition to the parameters in Table 1.2, the final LNA is required to provide constant gain between -40°C and 85°C across the whole UMTS frequency range (2110-2170 *MHz*). The LNA should have two gain modes. Namely, a High Gain (HG) mode for weak signals and a Low Gain (LG) mode for large signals. The LG mode is necessary to relax the linearity requirements of following segments of the receiver chain. In both modes the input and output should be matched to 50Ω and the total power consumption should be minimised.

1.5 Summary

In recent years the introduction of numerous telecommunication products and systems has created enormous growth in the telecommunications industry. Increased complexity of these products has led the need for increased circuit and component integration. Therefore, Section 1.1 discussed the need for SoC design. In the scope of this thesis, this is where a complete radio receiver system is integrated within a single RFIC.

Section 1.2 discussed the role of an LNA. This being to amplify small signal carrier signals to a sufficient level, without adding significant noise, before the information it contains can be properly demodulated by subsequent sections of the receiver. Additionally, for large signal levels, the LNA should amplify the received signal without introducing significant distortion. Thus, the LNA is a fundamental part within the analog front-end of any receiver system.

However, the mainly digital receiver back-end is usually implemented in a CMOS technology. Thus, in order to be compatible with SoC design, the receiver front-end, and hence the LNA, should be implemented in a technology that is compatible with CMOS. One such technology is RFCMOS. This uses small geometry CMOS devices that are suitable for LNA design. Alternatively, BiCMOS offers compatibility through a hybrid of bipolar devices and a mature CMOS process (i.e. one that uses slightly larger geometry CMOS devices). From Table 1.1, it was found that BiCMOS currently offers considerable savings in implementation costs. Therefore, it was

decided that all LNA designs in this thesis would be constructed from bipolar devices intended for implementation in a BiCMOS process.

Subsections 1.2.1, 1.2.2 and 1.2.3 discussed the definition of key LNA parameters. Namely, noise factor, noise figure, 1dB compression point, third order intermodulation intercept point, dynamic range, spurious free dynamic range and unconditional stability. It was demonstrated that the LNA is responsible for the majority of noise present at the output of a receiver system.

A major objective of this thesis is to develop a LNA that can meet a typical UMTS specification. However, as discussed in Section 1.4, it is beyond the scope of this thesis to undertake receiver planning in order to eventually derive the necessary LNA parameter targets. Therefore, a typical specification was formed using existing values in the technical literature [19-20].

In the author's view, the incidences of novel bias circuit design techniques in the technical literature, which are suitable for use in LNA design, are few and far between. Most bias circuits seen in the technical literature rely on the use of practically identical current mirror schemes. Therefore, the major motivation behind and main focus of this thesis, as discussed in Section 1.3, is to improve on traditional bias circuit design for LNA applications. Particularly, with regards to, providing temperature-independent DC current amplification of a much smaller temperature-dependent reference current (i.e. a Bandgap or PTAT current). The amplified output current can then be used to ensure that the LNA will maintain either constant voltage gain or DC power consumption across a wide temperature range.

1.6 References

[1] GSM Association Website. http://www.gsmworld.com

[2] UMTS Forum Website. http://www.umts-forum.org

[3] Wi-Fi Alliance Website. http://www.wifialliance.com

[4] IEEE Standards Website. http://standards.ieee.org

[5] Official Bluetooth Website. http://www.bluetooth.com

[6] Zigbee Alliance Website. http://www.zigbee.org

[7] UWB Forum Website. http://www.uwbforum.org

[8] Europractice Website. http://www.europractice.com

[9] H. Friis, 'Noise Figures of Radio Receivers,' *Proceedings of the Institute of Radio Engineers*, July 1944, pp. 419-422.

[10] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*, Kluwer Academic Publishers, Boston, 2001, Chapter 2, pp. 7-25.

[11] K. L. Fong and R. G. Meyer, 'High-Frequency Nonlinearity Analysis of Common-Emitter and Differential-Pair Transconductance Stages,' *IEEE Journal of Solid State Circuits*, Vol. 33, No. 1, January 1998, pp.2-17.

[12] J. M. Rollet, 'Stability and Power-Gain Invariants of Linear Twoports', *Institute of Radio Engineers Transactions on Circuit Theory*, March 1962.

[13] R. Ludwig and P. Bretchko, '*RF Circuit Design: Theory and Applications*,' Prentice Hall, Upper Saddle River, 2000, pp. 473-476.

[14] R. Ludwig and P. Bretchko, '*RF Circuit Design: Theory and Applications*,' Prentice Hall, Upper Saddle River, 2000, pp. 470-483.

[15] G. Lombardi and B. Neri, 'Criteria for the Evaluation of Unconditional Stability of Microwave Linear Two-Ports: A Critical Review and New Proof,' *IEEE Transactions on Microwave Theory and Techniques*, June 1999.

[16] B. Razavi, 'A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's,' *IEEE Journal of Solid-State Circuits*, Vol. 34, October 1999, pp. 1382-1385.

[17] A. Springer, L. Maurer, R. Weigel, 'RF System Concepts for Highly Integrated RFICs for W-CDMA Mobile Radio Terminals,' *IEEE Transactions on Microwave Theory and Techniques*, Vol. 50, January 2001, pp. 254-267.

[18] P. Orsatti, F. Piazza, Q. Huang, 'A 20mA-Receive, 55mA-Transmit, Single-Chip GSM Transceiver in 0.25μm CMOS,' *IEEE Journal of Solid State Circuits*, Vol. 34, December 1999, pp. 1869-1880.

[19] S. K. Reynolds, B. A. Floyd, T. J. Beukema, T Zwick, U. R. Pfeiffer and H. A. Ainspan, 'A Direct Conversion Receiver Integrated Circuit for WCDMA Mobile Systems,' *IBM Journal of Research and Development*, Vol. 47, No. 2/3, March/May 2003, pp. 337-353.

[20] J. Rogin, I. Kouchev, G. Brenna, D. Tschopp and Q. Huang, 'A 1.5V 45mW Direct Conversion WCDMA Receiver IC in 0.13μm CMOS,' *IEEE Journal of Solid State Circuits*, Vol. 38, No. 12, December 2003, pp. 2239-2248.

Note: All website links last checked on 31/8/06.

CHAPTER 2

Review of LNA Design

This chapter begins with a discussion of various LNA input stages, in order to determine an input stage that will result in best noise performance. Two circuit techniques, namely neutralisation and unilateralisation, are investigated. A LNA design procedure is then defined and followed in order to provide a circuit that meets the LNA specification defined in Chapter 1 at room temperature.

2.1 LNA Topologies

In analog design there are three basic bipolar circuit building blocks available to the designer. These are the common emitter, common base and common collector transistor configurations as shown in Figure 2.1.

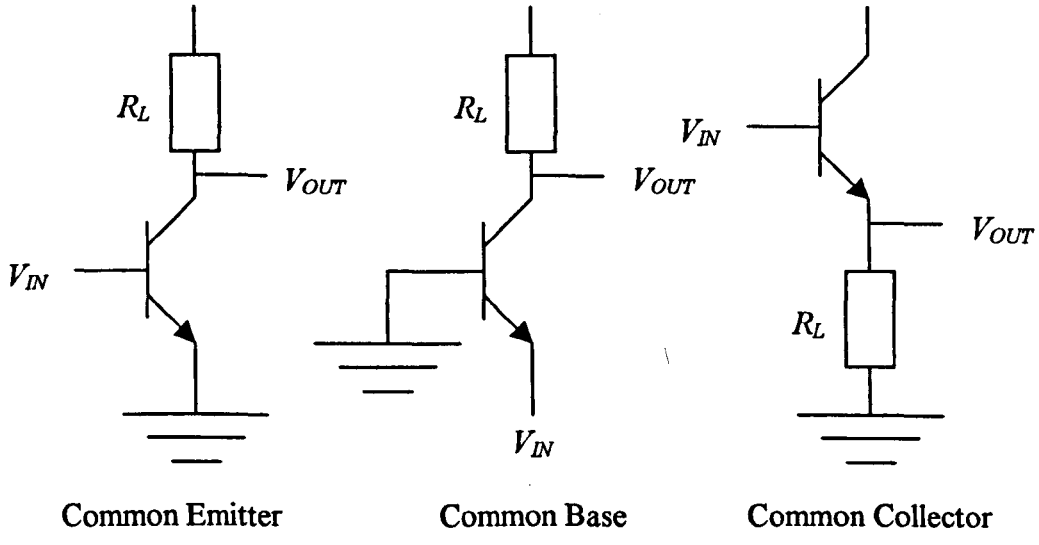

Figure 2.1 – Fundamental Bipolar Transistor Configurations

In order to design an LNA, it is necessary to know which configuration will offer the best noise performance. Extensive theoretical noise analysis of these configurations is covered in [1]. From this previous work it is found that the noise performances of common emitter, common base and common collector stages are nominally identical.

However, in practice, common base stages are generally impractical as low noise input stages because their current gain is equal to unity. Thus, any noise current

present at the output of the common base stage will be directly inferred back to the input without any reduction. Similarly, common collector stages exhibit unity voltage gain. Thus, in this case, the equivalent input noise voltage of the following stage will be transformed directly back to the common collector input.

In contrast, a common emitter stage offers both current gain and voltage gain that is significantly greater than unity. Therefore, both the equivalent input noise voltage and equivalent input noise current of the following stage will be attenuated by the voltage gain and current gain, respectively, when referred back to the common emitter input. Thus the common emitter will exhibit a lower NF when compared to that of the previously mentioned common base and common collector configurations.

Figure 2.2 illustrates a simplified model of a bipolar transistor in common emitter configuration.

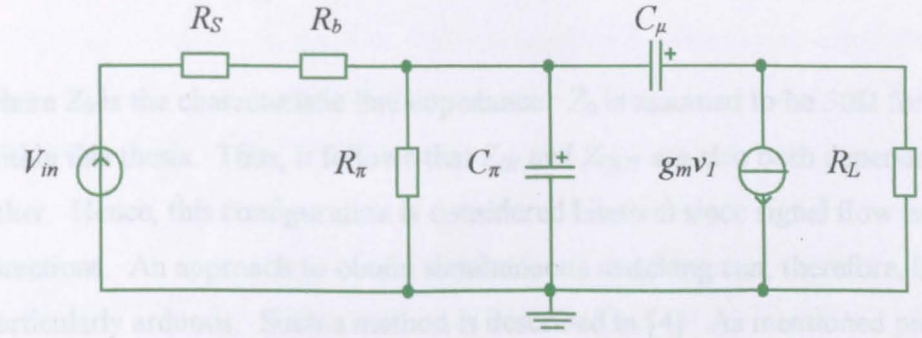

Figure 2.2 – Simplified model of a Common Emitter Configuration

Unfortunately, the presence of C_μ results in coupling between the input and output ports of the transistor. This can create problems that may render the common emitter configuration unsuitable in its present form. Firstly, C_μ causes the input capacitance to increase due to the Miller Effect [2], thus, reducing the circuit bandwidth. Secondly, the coupling also results in a non-zero reverse transmission coefficient (S_{12}). This can create difficulties in providing simultaneous input and output impedance matching and often leads to instability. In order to design impedance matching networks, the input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) for a two-port device (e.g. a common emitter amplifier) must be known. These are given by the well-known equations overleaf [3].

$$S_{11} = \Gamma_S^* + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.1}$$

$$S_{22} = \Gamma_L^* + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.2}$$

where S_{21} is the forward transmission coefficient, Γ_S is the source reflection coefficient and Γ_L is the load reflection coefficient. It is clear from (2.1) and (2.2) that S_{11} and S_{22} are both dependent on each other. Now, the input and output impedances (Z_{IN} and Z_{OUT}, respectively) can be expressed as:

$$Z_{IN} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{2.3}$$

$$Z_{OUT} = Z_0 \frac{1 + S_{22}}{1 - S_{22}} \tag{2.4}$$

where Z_0 is the characteristic line impedance. Z_0 is assumed to be 50Ω for all designs within this thesis. Thus, it follows that Z_{IN} and Z_{OUT} are also both dependent on each other. Hence, this configuration is considered bilateral since signal flow exists in both directions. An approach to obtain simultaneous matching can, therefore, be particularly arduous. Such a method is described in [4]. As mentioned previously, a non-zero S_{12} value may also give rise to instability. Referring to the stability factor equation defined by Lombard and Neri (1.23), it is easily seen that a non-zero S_{12} value may lead to the denominator of (1.23) becoming greater than the numerator. This will result in the condition $\mu<1$, thus, indicating an unstable design. Methods to overcome these potential problems can be grouped into two types of technique.

2.1.1 Neutralisation

The first technique is to cancel or 'neutralise' the coupling from the output port to input port. This is achieved by creating an additional coupling path with equal magnitude and opposite phase. Therefore, the overall or 'net' coupling between the

ports becomes equal to zero. The classic form of neutralised amplifier [5] is shown in Figure 2.3.

Figure 2.3 – The Classic Neutralised Amplifier [5]

In this case, a tapped inductor or autotransformer (L_1) in conjunction with C_1 forms a tuned load. By symmetry, the signal voltages at the top and bottom of L_1 have a phase difference of 180°. Therefore, the signal voltages at the top of C_N and the base of Q_1 will also have a phase difference of 180°. Assuming, from Figure 2.2, that the undesired coupling is solely due to C_μ then, it follows that, there will be zero net feedback from collector to base provided that the condition $C_N = C_\mu$ is met.

An alternative neutralisation technique, proposed by Cassan and Long [6], utilises transformer feedback and is shown in Figure 2.4. Here magnetic coupling between the collector and emitter of Q_1 is used to cancel the effective feedback through C_μ. However, at present integrated transformer models are frequently not available from foundries for initial analysis

Figure 2.4 – Alternative Neutralisation Technique Using Magnetic Coupling [6]

purposes and, in any case, actual implemented examples [6,7] exhibit non-ideal coupling behaviour, although, the technique shown in Figure 2.4 actually requires a non-ideal coupling coefficient value. For these reasons, designs relying on integrated transformers have found little or no widespread use.

However, it is observed that the circuit of Figure 2.3 only requires a transformer to achieve signal inversion. This is easily achieved in many other ways. A more practical topology for RFIC applications uses a differential amplifier to achieve signal inversion [8], thus, avoiding the need for an integrated transformer. This is shown in Figure 2.5.

Figure 2.5 – Neutralised Amplifier Using a Differential Pair to Obtain Signal Inversion [8]

A further alternative neutralisation technique [6] uses an inductor to resonate with C_μ at the desired centre frequency. See Figure 2.6. However, this technique is usually impractical for RFIC implementation due to the large value of L_1 needed. For example, a typical value of C_μ is approximately $65fF$, thus, the required value of L_1 is $85nH$ at $2.14GHz$. Clearly, this is too large to integrate! Furthermore, the DC blocking capacitance (C_{BLK}) severely loads the base and collector causing a reduction

of forward gain through the transistor transconductance. This, in conjunction with a low inductor Q factor, may lead to an increase in NF.

Figure 2.6 - Neutralised Amplifier Using an Inductor to Resonate with C_μ [6]

Unfortunately, in order to achieve precise neutralisation, the value of C_μ must be known. However, C_μ is somewhat voltage dependent. This makes precise cancellation difficult particularly when dealing with additional variability in process parameters. For this reason, neutralisation has been largely neglected in recent times.

2.1.2 Unilateralisation

The second method to overcome the problems associated with C_μ is called unilateralisation [6]. Unilateralisation decreases reverse signal flow and, thus, coupling between the output and input ports of an amplifier. This is commonly achieved by means of a cascode amplifier or emitter coupled amplifier (a combination of a common collector stage with a common base stage) as shown in Figure 2.7(a) and (b), respectively.

Both the cascode and emitter coupled amplifiers reduce the voltage swing across C_μ by concentrating the amplifiers voltage gain across a common base stage. In the case of the cascode topology, the miller multiplication of C_μ, which is seen at the input of the common emitter stage, is greatly reduced. Therefore, the cascode exhibits a much greater bandwidth than that of the simple common-emitter amplifier. In the case of

the emitter-coupled amplifier, the miller effect is eliminated as the collector is effectively grounded to all AC signals.

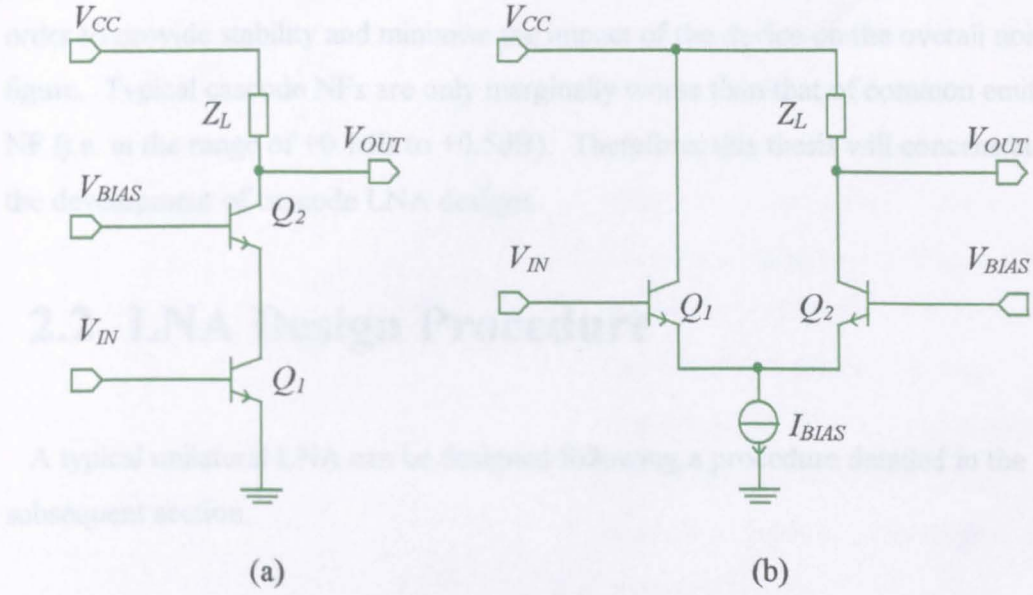

Figure 2.7 – Two common Unilateralisation Techniques Consisting of (a) a Cascode Amplifier and (b) an Emitter-Coupled Amplifier

In both cases, the common base stage isolates the output from the input. Therefore these topologies can be considered unilateral, since, signal flow only exists from input to output. In addition, the increased reverse isolation increases stability and allows for much simpler impedance matching network design. Unilateralisation is much less prone to process parameter variation and is therefore generally considered to be the preferred technique for LNA design.

Both designs offer adequate noise performance as each offers both significant voltage and current gain. Therefore, voltage and current noise present at the amplifier output is significantly attenuated by the amplifier voltage and current gain when referred back to the input. However, both configurations will exhibit a higher noise figure than that of the simple common emitter configuration. This is because, in both cases, voltage noise present at the input of the common base stage will be directly referred back to the amplifier input due to the fact that the initial input stage of both circuits has a unity voltage gain. This is more of a problem with the coupled emitter topology as additional voltage noise will be present due to the bias current source. Therefore,

in terms of noise performance, the cascode amplifier is most suitable for use as a LNA as it will exhibit a lower NF than that of the emitter-coupled topology. However, it is noted that the base of the common base transistor must be at small-signal ground in order to provide stability and minimise the impact of the device on the overall noise figure. Typical cascode NFs are only marginally worse than that of common emitter NF (i.e. in the range of +0.1dB to +0.5dB). Therefore, this thesis will concentrate on the development of cascode LNA designs.

2.2 LNA Design Procedure

A typical unilateral LNA can be designed following a procedure detailed in the subsequent section.

2.2.1 Optimum Collector Current for Minimum NF

The first task of a LNA designer is to choose a suitable device with a transition frequency (f_T) that is significantly larger than that of the intended operating frequency (f_0). The device is then biased in cascode configuration, since this is the chosen amplifier topology but also to isolate the input and output ports, at varying collector current values. In this case, a simple current mirror with beta helper [9] is used to provide the bias current as it

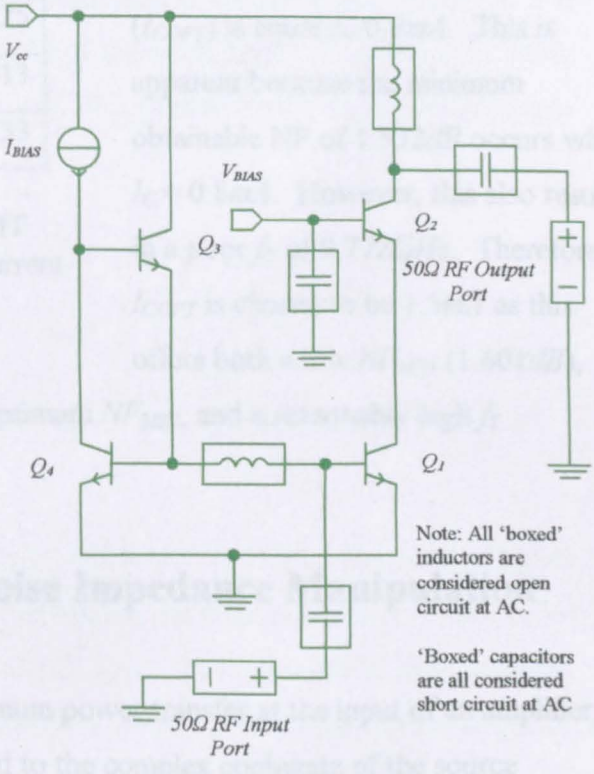

Figure 2.8 – Schematic of Test Circuit for Determination of the Optimum Collector Current

I_C (mA)	NF_{MIN} (dB) (2.14GHz)	f_T (GHz)
0.5	1.560	7.313
0.6	1.542	8.205
0.7	1.533	9.024
0.8	1.532	9.772
0.9	1.535	10.539
1	1.541	11.152
1.1	1.550	11.777
1.2	1.561	12.419
1.3	1.574	12.988
1.4	1.587	13.373
1.5	1.601	13.717
1.6	1.616	14.102
1.7	1.632	14.396
1.8	1.648	14.725
1.9	1.664	15.013
2	1.680	15.233

Table 2.1 – Minimum NF and fT Obtained at Various Collector Current Values

allows acceptable current transfer ratio accuracy whilst providing freedom of the cascode transistor base voltage selection. The minimum NF and f_T of the input transistor Q_1 are then measured at each corresponding collector current value. Here V_{CC} and V_{BIAS} are chosen to be 5V and 2.5V, respectively. Figure 2.8 illustrates the test circuit schematic. During simulation, all circuit components, apart from Q_1, were considered noiseless. Table 2.1 demonstrates the observed results.

The 'true' optimum collector current (I_{COPT}) is equal to $0.8mA$. This is apparent because the minimum obtainable NF of $1.532dB$ occurs when $I_C = 0.8mA$. However, this also results in a poor f_T of $9.772GHz$. Therefore, I_{COPT} is chosen to be $1.5mA$ as this offers both a low NF_{MIN} ($1.601dB$), only $0.069dB$ greater than the true optimum NF_{MIN}, and a reasonably high f_T ($13.717GHz$).

2.2.2 Optimum Noise Impedance Manipulation

In order to provide maximum power transfer at the input of an amplifier, the input impedance must be matched to the complex conjugate of the source impedance. In this thesis, the source impedance is always equal to 50+j0Ω. Therefore, the input impedance should be 50-j0Ω (i.e. identical to the source

impedance). In addition, the measured *NF* of an amplifier is dependent on its input impedance at the desired operating frequency. Thus, an optimum input impedance value exists, often referred to as the optimum noise impedance, which will yield the lowest *NF* (i.e. $NF = NF_{MIN}$). It is therefore necessary to provide a simultaneous matching for optimum noise performance and maximum power transfer. This is only possible if the optimum noise impedance also equals 50±j0Ω.

According to [10], NF_{MIN} is obtained at an optimum value of input admittance (Y_{OPT}). This is given by:

$$Y_{OPT} = \frac{f}{f_T R_n}\left[\sqrt{\frac{I_C}{2V_T}(r_E + r_B)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2 f_T^2}{4\beta_0 f^2}} - j\frac{n}{2}\right] \tag{2.5}$$

where R_n is the equivalent noise resistance, r_E is the emitter resistance, r_B is the base resistance, f is the signal frequency, V_T is the thermal voltage, β_0 is the DC current gain and n is the forward emission coefficient (approximately equal to unity). It is straightforward to obtain the optimum input impedance since $Z_{OPT} = Y_{OPT}^{-1}$. Thus, it can be shown that the resistive real part of the optimum input impedance (R_{OPT}) is given by:

$$R_{OPT} = \frac{R_n f_T}{f}\left[\frac{\sqrt{\frac{I_C}{2V_T}(r_E + r_B)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2 f_T^2}{4\beta_0 f^2}}}{\frac{I_C}{2V_T}(r_E + r_B)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2}{4}\left(1+\frac{f_T^2}{\beta_0 f^2}\right)}\right] \tag{2.6}$$

According to [10], R_{OPT} is inversely proportional to the emitter length of a Bipolar Junction Transistor (BJT). However, as long as the emitter length-to-width ratio (l_E / w_E) remains in excess of ten, NF_{MIN} remains invariant to changes in emitter length. Therefore, R_{OPT} can be manipulated to equal 50Ω by altering the emitter length of the input common-emitter transistor.

However, in many cases it is not possible to alter individual transistor parameters. Instead a designer has to develop designs from a set of existing transistor models supplied for a particular process. In this case a slightly different approach is adopted.

Referring to Figure 2.8, using N parallel BJTs to form composite devices Q_1 and Q_2, can also alter R_{OPT}. In this case, each BJT is biased so that its collector current is set equal to I_{COPT}. As shown in [11], R_{OPT} decreases as N is increased. Thus, an optimum value of N exists when $R_{OPT} \approx 50\Omega$. Using an identical test circuit as shown previously in Figure 2.8, R_{OPT} was measured for different values of N. Each time $I_{IN} = I_{COPT} = 1.5mA$, $V_{CC} = 5V$ and $V_{BIAS} = 2.5V$. The tabulated results are shown in Table 2.2 and plotted in Figure 2.9.

N	R_{OPT} (Ω)
1	185.243
2	92.624
3	61.751
4	46.314
5	37.052
6	30.877
7	26.466
8	23.158
9	20.586

Table 2.2 – The Effect of N on R_{OPT}

Figure 2.9 – Plot Showing the Effect of N on R_{OPT}

From Table 2.2 and Figure 2.9, it is clear that $R_{OPT} = 50\Omega$ when N is between 3 and 4. However, as it is only possible to have an integer number of BJTs in parallel, the optimal value is taken to be $N = 4$ because R_{OPT} is closest to 50Ω ($R_{OPT} = 46.314\Omega$) under this condition. Though not shown above, the use of parallel N devices has a negligible effect on the overall f_T of the composite device Q_1.

One drawback of this technique is that the required total LNA collector current, given by:

$$I_{CTOT} = N.I_{COPT} \tag{2.7}$$

may be unnecessarily large. This is because I_{CTOT} is defined by matching and noise conditions rather than gain, linearity and power consumption requirements as would be desirable. In order to overcome these shortcomings, an improved method [11] to manipulate R_{OPT} is highlighted below.

The alternative method involves the connection of a capacitor C_{BE} between the base and emitter of the common-emitter device Q_1. See Figure 2.10. As C_{BE} is increased R_{OPT} decreases in similar fashion to that shown in Figure 2.9. Thus, for an arbitrary number of N devices, each biased at I_{COPT}, there exists an optimum value of C_{BE} when $R_{OPT} = 50\Omega$. Using the test set-up in shown in Figure 2.10, R_{OPT} was measured for different values of C_{BE} when $N = 1$, $N = 2$ and $N = 3$. Each time $I_{IN} = I_{COPT} = 1.5mA$, $V_{CC} = 5V$ and $V_{BIAS} = 2.5V$. The results are plotted in Figure 2.11.

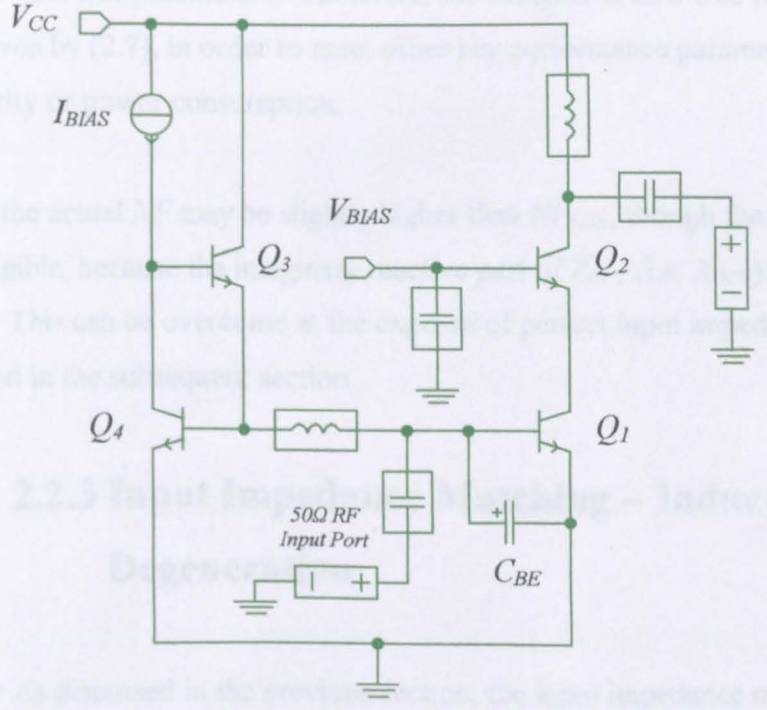

Figure 2.10 - Schematic of Test Circuit for Determination of the Optimum C_{BE} Value

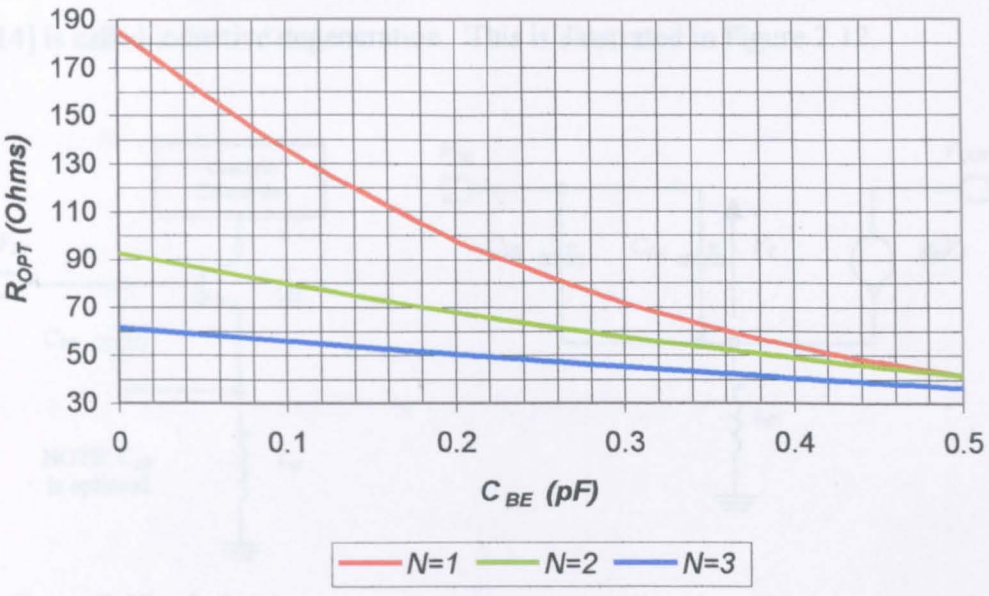

Figure 2.11 – Plot Showing the Effect of C_{BE} on R_{OPT} when N=1, N=2 and N=3

From Figure 2.11, the optimum values of C_{BE}, to ensure $R_{OPT} = 50\Omega$, are $0.43pF$, $0.39pF$ and $0.21pF$ when $N = 1$, $N = 2$ and $N = 3$, respectively. Thus, the use of C_{BE} ensures a close to minimum NF at any current level. The emitter area and overall bias current are now free parameters. Therefore, the designer is now free to set the bias current, given by (2.7), in order to meet other key performance parameters such as gain, linearity or power consumption.

However, the actual NF may be slightly higher than NF_{MIN}, though the difference is often negligible, because the imaginary reactive part of Z_{OPT} (i.e. X_{OPT}) is unlikely to equal 0Ω. This can be overcome at the expense of perfect input impedance matching as discussed in the subsequent section.

2.2.3 Input Impedance Matching – Inductive Degeneration

As discussed in the previous section, the input impedance must be matched to equal 50+j0Ωn order to provide maximum input power transfer from the signal

source. The 'state of the art' solution most commonly seen in the technical literature [12-14] is called inductive degeneration. This is illustrated in Figure 2.12.

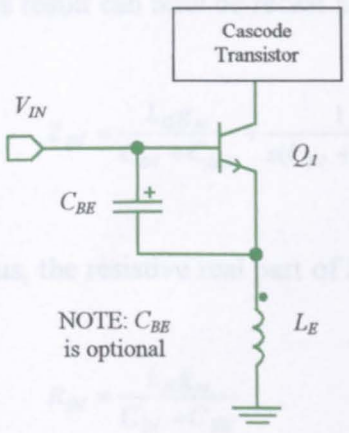

Figure 2.12 – Inductive Degeneration

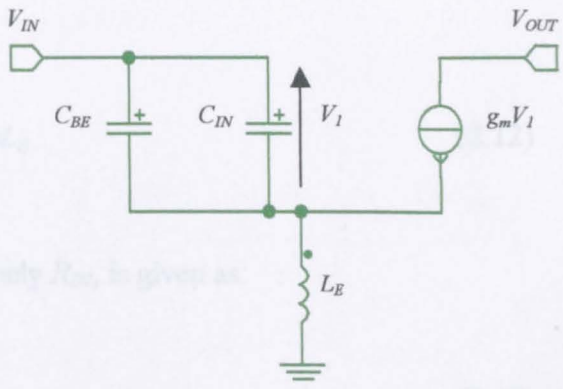

Figure 2.13 – Simplified Model of Q_1 with Inductive Degeneration

Q_1 can now be modelled as shown in Figure 2.13. Using this model, the input impedance (Z_{IN}) is analysed below.

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{v_1 + i_{LE} sL_E}{v_1 s(C_{IN} + C_{BE})} \tag{2.8}$$

The current through the inductor L_E can be given by:

$$i_{LE} = v_1 [s(C_{IN} + C_{BE}) + g_m] \tag{2.9}$$

The equation (2.9) is then substituted into (2.8) to give:

$$Z_{IN} = \frac{v_1 + v_1 [s(C_{IN} + C_{BE}) + g_m] sL_E}{v_1 s(C_{IN} + C_{BE})} \tag{2.10}$$

The square bracketed term, present in the numerator of (2.10), is then multiplied out while cancelling the v_1 terms. This results in:

$$Z_{IN} = \frac{1 + s^2 (C_{IN} + C_{BE}) L_E + s L_E g_m}{s(C_{IN} + C_{BE})} \tag{2.11}$$

This result can now be recast as:

$$Z_{IN} = \frac{L_E g_m}{C_{IN} + C_{BE}} + \frac{1}{s(C_{IN} + C_{BE})} + s L_E \tag{2.12}$$

Thus, the resistive real part of Z_{IN}, namely R_{IN}, is given as:

$$R_{IN} = \frac{L_E g_m}{C_{IN} + C_{BE}} \tag{2.13}$$

Since the angular transition frequency (ω_T) is given by $\omega_T = \frac{g_m}{C_{IN}} = \frac{g_m}{C_\pi + C_\mu}$, (2.13) is often recast as [10]:

$$R_{IN} = \left(\frac{C_{IN}}{C_{IN} + C_{BE}} \right) \omega_T L_E \tag{2.14}$$

Thus, in order that $R_{IN} = 50\Omega$, the required value of L_E is given by:

$$L_E = \frac{50}{\omega_T} \left(1 + \frac{C_{BE}}{C_{IN}} \right) \tag{2.15}$$

If the additional base-emitter capacitance is not required, (2.15) simply reverts to:

$$L_E = \frac{50}{\omega_T} \tag{2.16}$$

From (2.12), the reactive imaginary part of Z_{IN}, namely X_{IN}, is given as:

$$X_{IN} = \frac{1}{s(C_{IN} + C_{BE})} + s L_E \tag{2.17}$$

From (2.17), it appears that X_{IN} is determined via a series LC circuit. In reality X_{IN} is often capacitive at the operating frequency f_0. Therefore, it is common practice to add a further inductor in series with the base of Q_1 in order to provide series resonance (i.e. $X_{IN} = 0\Omega$) at f_0. This is shown in Figure 2.14.

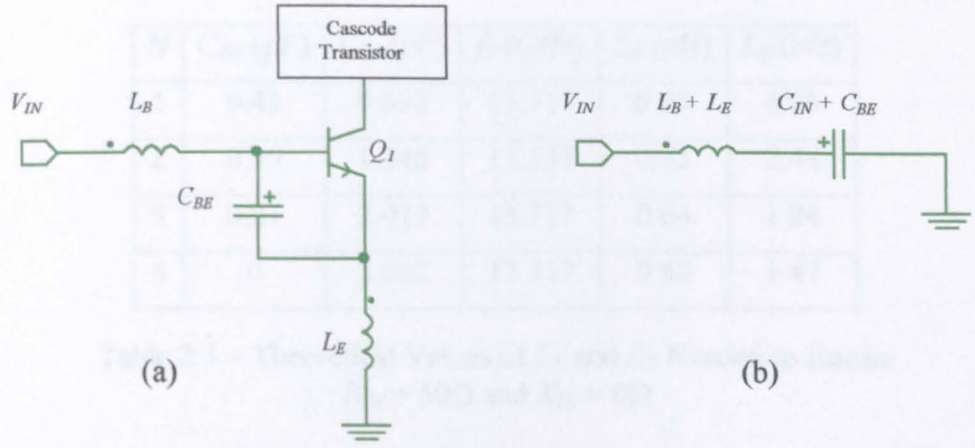

Figure 2.14 – (a) Inductive Degeneration with Additional Base Inductance
(b) X_{IN} Equivalent Circuit

The resonant angular frequency of a series LC circuit is given by the well-known equation:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.18}$$

In this case, (2.18) is equivalent to:

$$\omega_0 = \frac{1}{\sqrt{(L_B + L_E)(C_{IN} + C_{BE})}} \tag{2.19}$$

Therefore, the required value of L_B needed to ensure $X_{IN} = 0\Omega$ is given by:

$$L_B = \frac{1}{\omega_0^2 (C_{IN} + C_{BE})} - L_E \tag{2.20}$$

The theoretical values of L_E and L_B needed to ensure $R_{IN} = 50\Omega$ and $X_{IN} = 0\Omega$ are calculated, using (2.15) and (2.20), for the conditions $N = 1$ and $C_{BE} = 0.43pF$, $N = 2$ and $C_{BE} = 0.39pF$ and $N = 3$ and $C_{BE} = 0.21pF$. These theoretical values are presented in Table 2.3.

N	C_{BE} (pF)	C_{IN} (pF)	f_T (GHz)	L_E (nH)	L_B (nH)
1	0.43	0.673	13.717	0.95	4.06
2	0.39	1.346	13.717	0.75	2.44
3	0.21	2.019	13.717	0.64	1.84
4	0	2.692	13.717	0.58	1.47

Table 2.3 – Theoretical Values of L_E and L_B Needed to Ensure $R_{IN} = 50\Omega$ and $X_{IN} = 0\Omega$

Using the circuit schematic shown in Figure 2.15, the actual values of L_E and L_B needed to ensure $R_{IN} = 50\Omega$ and $X_{IN} = 0\Omega$, for each previously mentioned condition, were obtained via iterative simulations. These actual values are presented in Table 2.4 along with the corresponding measured values of Z_{IN}, Z_{OPT}, NF_{MIN} and NF.

N	C_{BE} (pF)	L_E (nH)	L_B (nH)	Z_{IN} (Ω)	Z_{OPT} (Ω)	NF (dB)	NF_{MIN} (dB)
1	0.43	0.92	4.8	50.185+j0.027	50.082+j22.316	1.704	1.592
2	0.39	0.76	3.07	49.972-j0.058	50.409+j9.408	1.604	1.584
3	0.21	0.67	2.45	50.067+j0.045	50.768-j1.449	1.578	1.577
4	0	0.62	2.09	49.993-j0.061	47.319-j9.569	1.595	1.571

Table 2.4 – Actual Values of L_E and L_B Needed to Ensure $R_{IN} = 50\Omega$ and $X_{IN} = 0\Omega$ with Corresponding Values of Z_{IN}, Z_{OPT}, NF_{MIN} and NF

If Tables 2.3 and 2.4 are compared, it is seen that the theoretical values of L_E cohere reasonably closely (i.e. within $0.04nH$) with the actual required values found via simulation. However, the theoretical values of L_B are consistently greater those obtained via simulation. Thus, the expression (2.20) used to calculate L_B seems to

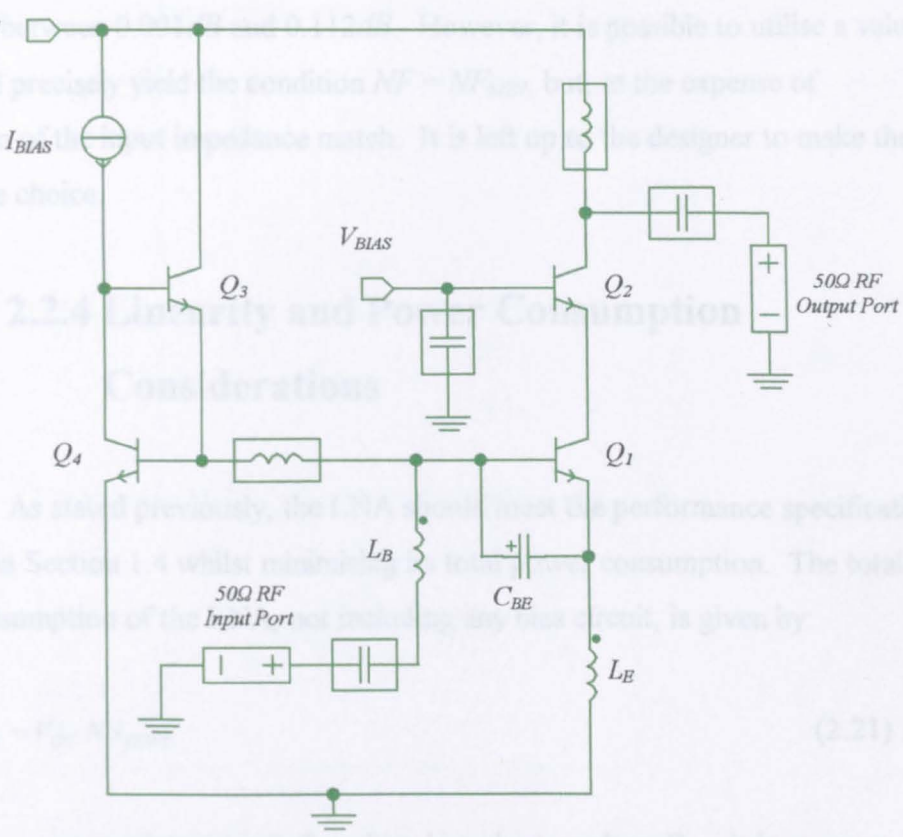

Figure 2.15 – Schematic of Test Circuit Used to Determine L_B and L_E

underestimate the actual required value. This is due to the simple model used in Figure 2.13, which neglects the effects of additional parameters such as the base resistance. Inclusion of these additional parameters would yield closer coherence with the observed values of L_B. However, this results in increased analysis complexity and a cumbersome design equation. Nevertheless, (2.20) serves as a good 'rule of thumb' in order to provide a starting value that can be easily optimised via circuit simulation.

From Table 2.4, it is interesting to note that although the real part of Z_{IN} is approximately equal to the real part of Z_{OPT} (i.e. 50Ω), the same cannot be said for the corresponding imaginary parts. It is stated in the technical literature [10] that L_B is used to simultaneously transform both the input reactance X_{IN} and the optimum noise reactance X_{OPT} to 0Ω. Clearly, this is misleading. A non-zero X_{OPT} value results in a NF that is greater than NF_{MIN}.

In this case, the differences in the actual NF and NF_{MIN} are considered negligible as they range between $0.001dB$ and $0.112dB$. However, it is possible to utilise a value of L_B that will precisely yield the condition $NF = NF_{MIN}$, but, at the expense of degradation of the input impedance match. It is left up to the designer to make the appropriate choice.

2.2.4 Linearity and Power Consumption Considerations

As stated previously, the LNA should meet the performance specification described in Section 1.4 whilst minimising its total power consumption. The total power consumption of the LNA, not including any bias circuit, is given by:

$$P_{TOT} = V_{CC} . N I_{COPT} \tag{2.21}$$

V_{CC} and I_{COPT} are predetermined, therefore, in order to reduce P_{TOT} it is necessary to reduce N to a minimum allowable value. N is thus determined via the large signal performance of the LNA. This is because linearity increases as the total collector current increases. Since $I_{CTOT} = N I_{COPT}$ (2.7), it follows that the linearity also increases as N is increased. Thus, a minimum value of N exists that will allow ICP_{-1dB} to exceed $-15dBm$, as defined in Section 1.4, whilst providing minimum power consumption.

In order to determine ICP_{-1dB}, the cascode LNA circuit of Figure 2.16 was simulated using each of the corresponding N, C_{BE}, L_B and L_E values, determined previously in Section 2.2.3, with a common load impedance. Each time $V_{CC} = 5V$. However, ICP_{-1dB} cannot be directly compared for each configuration since the small signal power gain (A_P) will vary with transconductance. Therefore, it is necessary to first determine each OCP_{-1dB} value. Now, ICP_{-1dB} is defined as:

$$ICP_{-1dB} = OCP_{-1dB} - A_P \tag{2.22}$$

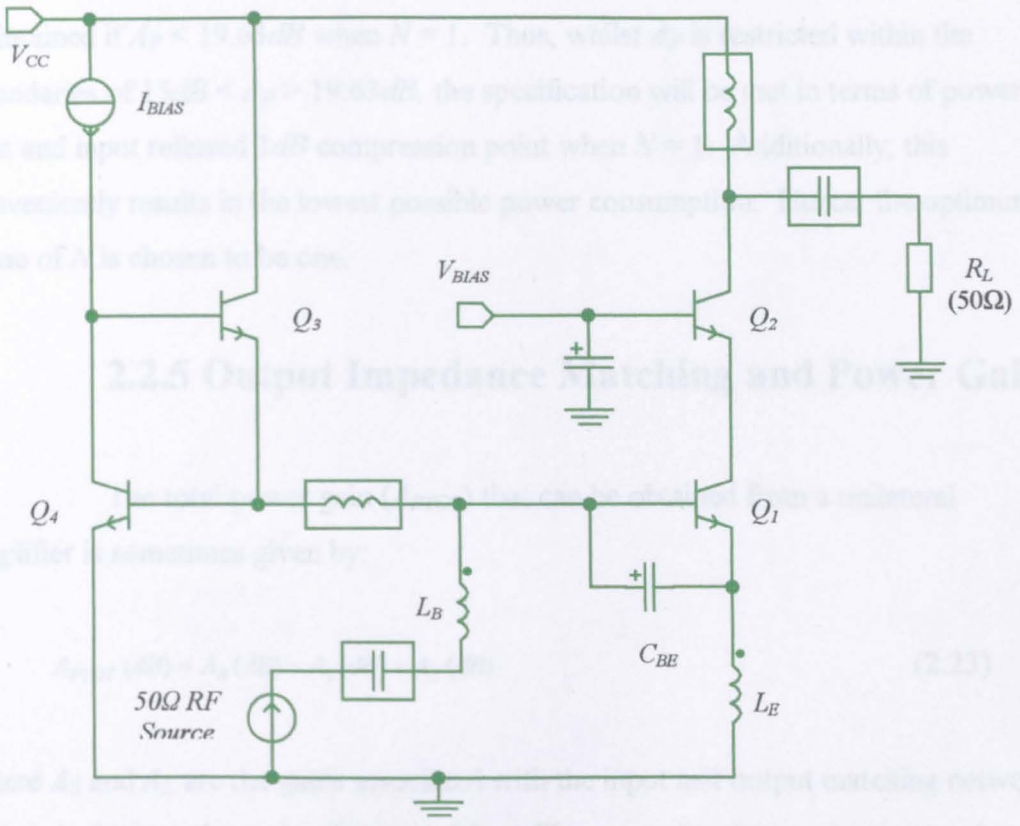

Figure 2.16 – Schematic of Test Circuit Used for Determination of ICP_{-1dB}

Therefore, a maximum value of A_P (A_{PMAX}) can now be determined that will result in the condition $ICP_{-1dB} = -15dBm$. These results are tabulated in Table 2.5.

N	C_{BE} (pF)	L_B (nH)	L_E (nH)	OCP_{-1dB} (dBm)	A_{PMAX} (dB)	P_{TOT} (mW)
1	0.43	4.8	0.92	4.629	19.629	7.5
2	0.39	3.07	0.76	9.654	24.654	15
3	0.21	2.45	0.67	11.791	26.791	22.5
4	0	2.09	0.62	12.860	27.860	30

Table 2.5 – $1dB$ Output Compression Point, Maximum Allowable Power Gain and Total Power Consumption when $N = 1$, $N = 2$, $N = 3$ and $N = 4$

From Table 2.5, it is clear that OCP_{-1dB} does indeed increase with N as expected. In order to meet the specification in Section 1.4, the LNA must provide a power gain of between $15dB$ and $20dB$ whilst maintaining an input referred $1dB$ compression point

in excess of $-15dBm$. The results indicate that the condition $ICP_{-1dB} \geq -15dBm$ will be maintained if $A_P < 19.63dB$ when $N = 1$. Thus, whilst A_P is restricted within the boundaries of $15dB < A_P > 19.63dB$, the specification will be met in terms of power gain and input referred $1dB$ compression point when $N = 1$. Additionally, this conveniently results in the lowest possible power consumption. Hence, the optimum value of N is chosen to be one.

2.2.5 Output Impedance Matching and Power Gain

The total power gain (A_{PTOT}) that can be obtained from a unilateral amplifier is sometimes given by:

$$A_{PTOT}(dB) = A_S(dB) + A_0(dB) + A_L(dB) \tag{2.23}$$

where A_S and A_L are the gains associated with the input and output matching networks and A_0 is the insertion gain of the amplifier. The network gains can be greater than unity. This may seem odd at first since they do not contain any active devices. However, significant power losses will result if the input and output impedances are not matched to their respective source or load. Therefore, the use of matching networks will result in additional gain. A_S, A_L and A_0 are themselves given by:

$$A_S(dB) = 10\log\frac{1}{1-|S_{11}|^2} \tag{2.24}$$

$$A_L(dB) = 10\log\frac{1}{1-|S_{22}|^2} \tag{2.25}$$

$$A_0(dB) = 10\log\ |S_{21}|^2 \tag{2.26}$$

The circuit of Figure 2.17 is simulated in order to obtain the S-parameters (i.e. S_{22} and S_{21}) and, hence, the gain values attributed to each part of the amplifier. In this case, the input impedance has already been matched to 50Ω using inductive degeneration.

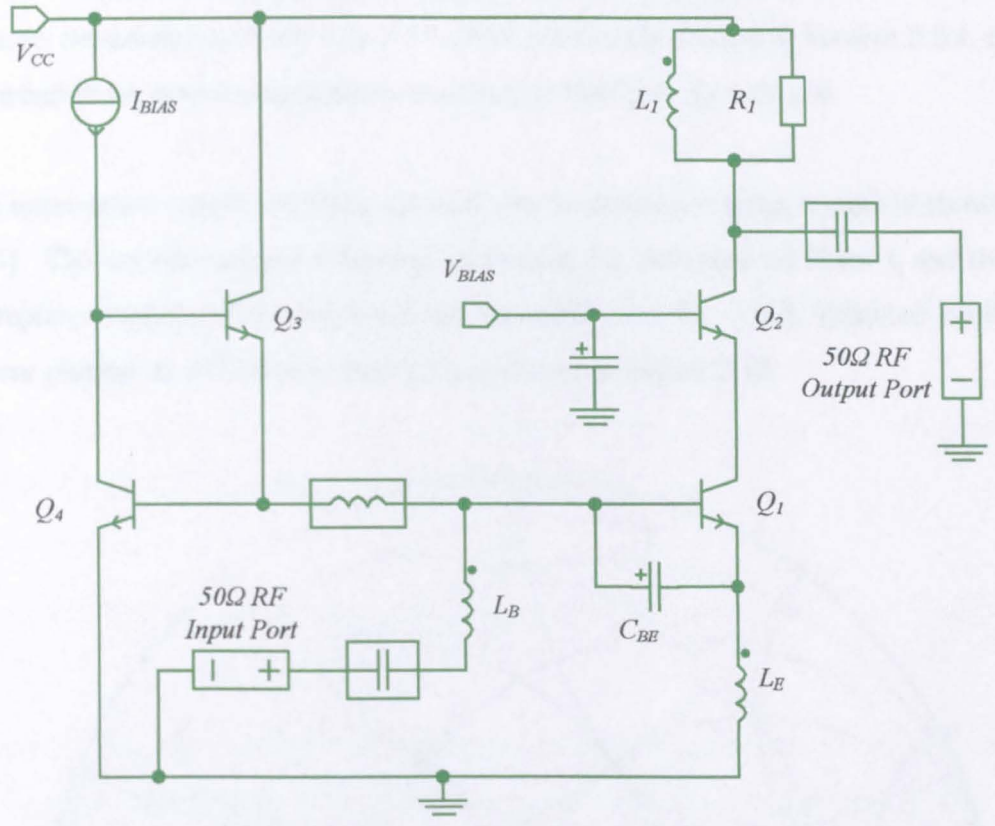

Figure 2.17 – Schematic of Test Circuit to Determine the LNA *S*-parameters

Therefore, $S_{11} \approx 0$ and little additional gain is available by improving the input matching network (i.e. $A_S \approx 0dB$). The resistor R_1 is used to control A_{PTOT} by reducing the quality factor of L_1. As R_1 is decreased, the magnitudes of S_{22} and, albeit to a much smaller extent, S_{21} also decrease. This in turn decreases A_{PTOT} by reducing the gain available from A_L and A_0. The *S*-parameter and gain values obtained via simulation at $2140MHz$, whilst $L_1 = 4.8nH$ and $R1 = 1K\Omega$, are presented in Table 2.6.

$\|S_{22}\|$	$\|S_{21}\|$	$A_0\,(dB)$	$A_L\,(dB)$	$A_{PTOT}\,(dB)$
0.938	2.565	8.181	9.194	17.375

Table 2.6 – *S*-parameter and Maximum Available Gain Values when $L_1 = 4.8nH$ and $R1 = 1K\Omega$

The results indicate that, without output matching, the cascode LNA of Figure 2.17 provides a power gain of $8.181dB$. If the output impedance is matched to 50Ω then

the power gain will increase by $9.194dB$, thus, providing a total gain of $17.375dB$. Hence, the condition $15dB < A_P > 19.63dB$, previously defined in Section 2.2.4, is satisfied if the output impedance is matched to 50Ω (i.e. $A_P = A_{PTOT}$).

An appropriate output matching network can be developed using a method shown in [15]. The amplifier output reflection coefficient S_{22}, indicated via Point 1, and the complex conjugate of the required load impedance (i.e. $50 - j0\Omega$), indicated via Point 3, are plotted on a *ZY* Smith chart [16] as shown in Figure 2.18.

Figure 2.18 – Output Matching Network Development using a *ZY* Smith Chart (Point 1 = S_{22}, Point 2 = Point of Intersection Between Constant Resistance and Constant Conductance Circles, Point 3 = Z_L^*)

Point 2 marks the point of intersection between the constant resistance circle, which passes through Point 1, and the constant conductance circle, which passes through

Point 3. The impedance (Z_X) and admittance (Y_X) values of each point are shown in Table 2.7.

Z_1 (Ω)	Z_2 (Ω)	Z_3 (Ω)	Y_1 (S)	Y_2 (S)	Y_3 (S)
4.5 + j66.8	4.5 + j14.3	50 – j0	0.001 – j0.0149	0.02 – j0.0636	0.2 + j0

Table 2.7 – Impedance and Admittance Values of Points 1, 2 and 3 on Figure 2.17

The output impedance of the LNA is transformed from Z_1 to Z_2 by the addition of a series capacitor. The value of which is given by:

$$C = \frac{1}{\omega(X_1 - X_2)} = \frac{1}{2\pi \times 2.14E9 \times (66.8 - 14.3)} = 1.42pF \qquad (2.27)$$

where X_1 and X_2 are the reactive imaginary components of Z_1 and Z_2, respectively. The output impedance of the LNA is then transformed from Z_2 to Z_3 (i.e. 50Ω) by the addition of a parallel or shunt capacitor. The value of which is given by:

$$C = \frac{B_2 - B_3}{\omega} = \frac{0.0636 - 0}{2\pi \times 2.14E9} = 4.73pF \qquad (2.28)$$

where B_2 and B_3 are the susceptive imaginary components of Y_2 and Y_3, respectively. The resulting output matching network is shown in Figure 2.19.

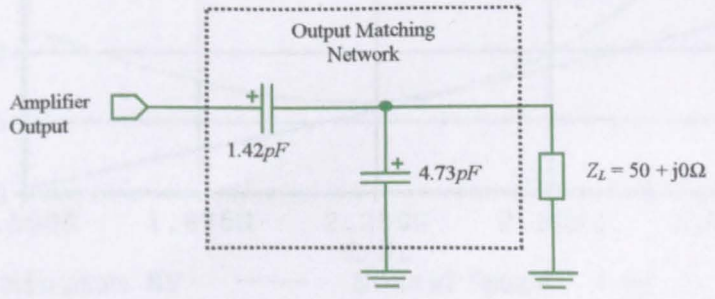

Figure 2.19 – Output Matching Network

2.2.6 Initial LNA Performance

The initial results for the complete LNA circuit, shown in Figure 2.20, are presented overleaf in Table 2.8. Plots illustrating noise performance, power gain,

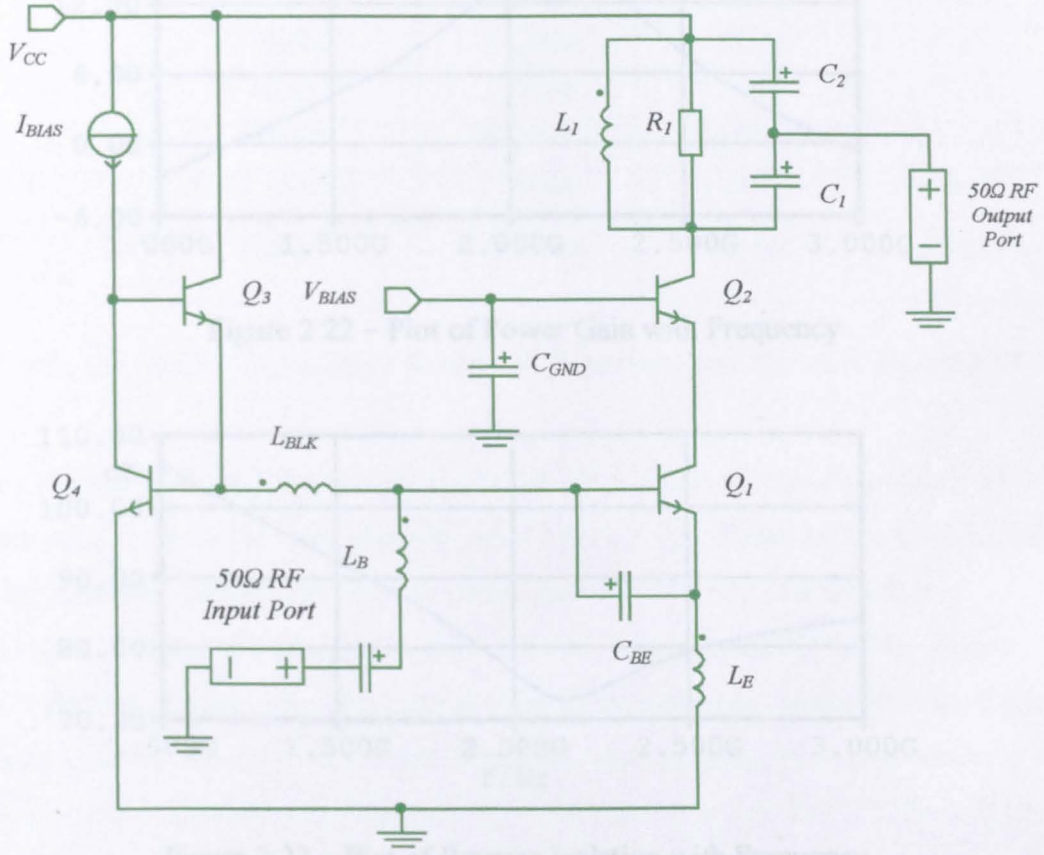

Figure 2.20 – Initial Design of a Complete LNA

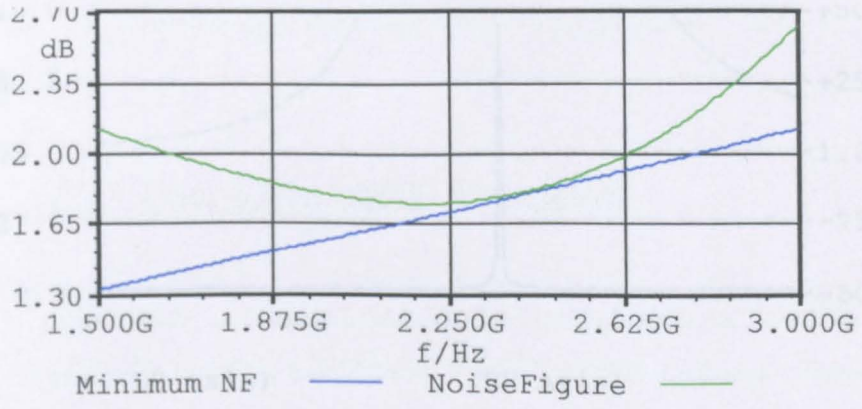

Figure 2.21 – Plot of LNA Noise Performance with Frequency

reverse isolation and the stability factor with frequency are presented in Figures 2.21, 2.22, 2.23 and 2.24, respectively.

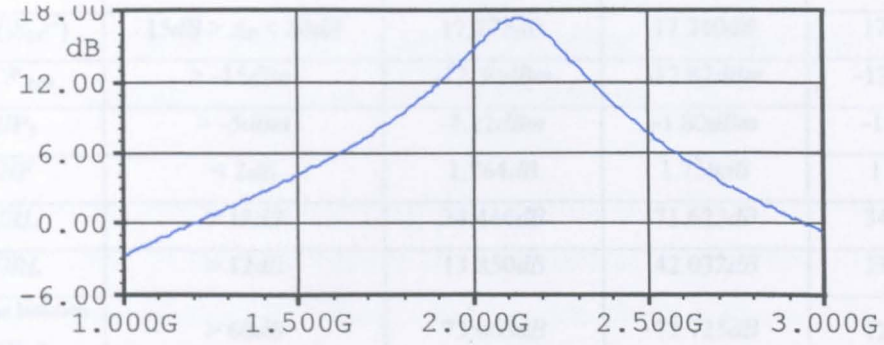

Figure 2.22 – Plot of Power Gain with Frequency

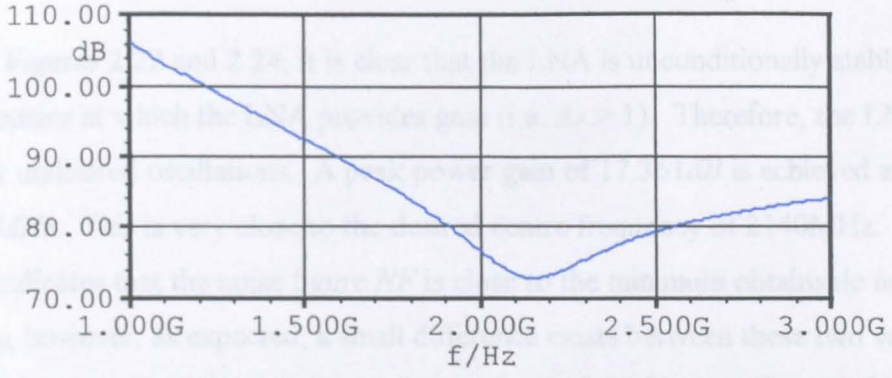

Figure 2.23 – Plot of Reverse Isolation with Frequency

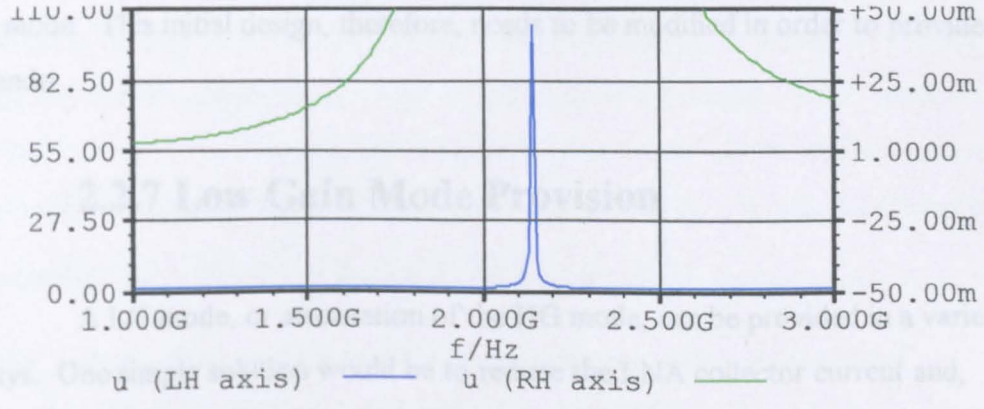

Figure 2.24 – Plot of Stability Factor μ with Frequency

LNA Parameters	Targeted Values (2110*MHz* - 2170*MHz*)	Simulated Results (27°C)		
		2110*MHz*	2140*MHz*	2170*MHz*
Z_{IN}	50 + j0Ω	50.082-j1.895Ω	50.005+j0.026Ω	49.945+j1.920Ω
Z_{OUT}	50 + j0Ω	37.006+j12.217Ω	50.567-j0.559Ω	51.161-j22.118Ω
A_P ($\|S_{21}\|^2$)	15*dB* > A_P < 20*dB*	17.272*dB*	17.340*dB*	17.021*dB*
ICP_{-1dB}	> -15*dBm*	-12.30*dBm*	-12.82*dBm*	-12.80*dBm*
IIP_3	> -5*dBm*	-2.12*dBm*	-1.80*dBm*	-1.07*dBm*
NF	< 2*dB*	1.764*dB*	1.759*dB*	1.756*dB*
IRL	> 12*dB*	34.446*dB*	71.623*dB*	34.325*dB*
ORL	> 12*dB*	13.850*dB*	42.032*dB*	13.396*dB*
Reverse Isolation -(S_{12})	> 60*dB*	73.063*dB*	72.725*dB*	72.778*dB*

Table 2.8 – Initial Performance Results of Complete LNA Shown in Figure 2.19

From Figures 2.22 and 2.24, it is clear that the LNA is unconditionally stable at all frequencies at which the LNA provides gain (i.e. $A_P > 1$). Therefore, the LNA is free of any undesired oscillations. A peak power gain of 17.361*dB* is achieved at 2133*MHz*. This is very close to the desired centre frequency of 2140MHz. Figure 2.21 indicates that the noise figure *NF* is close to the minimum obtainable noise figure NF_{MIN}, however, as expected, a small difference exists between these two values. This is because $X_{IN} \neq X_{OPT}$ as illustrated previously in Table 2.4. From Table 2.8, it is clear that the LNA exceeds the targeted parameter values. However, the original LNA specification from Chapter 1 expressed the need for an additional Low Gain (LG) mode. This initial design, therefore, needs to be modified in order to provide a LG mode.

2.2.7 Low Gain Mode Provision

A LG mode, or attenuation of the HG mode, can be provided in a variety of ways. One simple solution would be to reduce the LNA collector current and, hence, the transconductance g_m. This, in turn, causes the voltage and power gain to also decrease (e.g. A_v (*dB*) = A_p (*dB*) when the source and load reflection coefficients

are reduced to zero as a result of impedance matching) since the voltage gain of an amplifier is dependent on g_m. However, reducing the collector current will also alter the amplifier input capacitance and, hence, the input impedance. In addition, the transition frequency f_T will also change. Therefore, it becomes highly problematic to develop a matching network that can provide impedance matching in both LG and HG modes. For this reason, alternative methods are required.

The three most common LG mode implementations seen in the technical literature are based on techniques known as resistor chain attenuation [17], amplifier bypassing [18] and current steering [17]. These techniques are shown in Figure 2.25.

Figure 2.25 – Common Methods of LG Mode Provision (DC biasing not shown)
(a) Resistor Chain Attenuation (b) Amplifier Bypassing (c) Current Steering

In Figure 2.25(a) Q_1 provides low noise matching in both HG and LG modes. In HG mode V_{HG} is set high (2.5V) and V_{LG} is set low (1V), thus, Q_2 is turned on whilst Q_3 remains off and the amplified signal appears directly at the output. In LG mode V_{HG} is set low (1V) and V_{LG} is set high (2.5V), thus, Q_2 is turned off whilst Q_3 is turned on. In this case the amplified signal appears at the collector of Q_3. It is then attenuated by the potential divider formed by R_1 and R_2, by a factor of $\frac{R_2}{R_1}$, before appearing at the amplifier output. However, the resistor chain technique suffers from several drawbacks. For example, R_1 must be large (i.e. the condition $R_1 >> \omega_0 L_1$ must be satisfied) in order to preserve high power gain in HG mode. In addition, the output

swing of Q_3 is limited by R_2I_{C3}. Thus, circuit linearity is reduced in LG mode and a tradeoff exists between A_P, in HG mode, and ICP_{-1dB} in LG mode.

In Figure 2.25(b) Q_1 provides low noise matching in HG mode. The switch is left open and the signal is amplified as per the previous circuit. However, in LG mode, the switch is closed. The signal then flows directly through the switch, thus, completely bypassing the LNA. This enables the LNA to be powered down in LG mode, thus, dramatically reducing power consumption. However, A_P cannot be greater than unity or $0dB$ in LG mode. Furthermore, it can be highly problematic to provide simultaneous input and output matching in LG and HG modes.

In Figure 2.25(c) Q_1 again provides low noise matching in both HG and LG modes. In HG mode V_{HG} is set high (2.5V) and V_{LG} is set low (1V), thus, Q_2 is turned on whilst Q_{3A}, Q_{3B} and Q_{3C} remains off and the amplified signal appears directly at the output. In LG mode V_{HG} remains high (2.5V) whilst V_{LG} is also set high (2.5V), thus, Q_2, Q_{3A}, Q_{3B} and Q_{3C} are all turned on. In this case a proportion of the signal at the collector of Q_1 is dumped on to the power supply. This results in attenuation. The amplified signal present at the collector of Q_2 is attenuated by a factor of $\frac{A_{E2}+A_{E3}}{A_{E2}}$ where A_{E2} and A_{E3} are the emitter areas of Q_2 and Q_3, respectively. In this case, $\frac{A_{E2}+A_{E3}}{A_{E2}}=\frac{3+1}{1}=4$ since Q_3 consists of three unity devices in parallel. Current steering has negligible effect on the input and output impedances of the LNA, thus, simultaneous impedance matching can be achieved in both HG and LG modes. In addition, linearity is enhanced in LG mode whilst preserving a reasonable NF. For this reason, current steering is chosen as the most suitable approach. Referring to the original LNA specification of Section 1.4, the power gain in LG mode should be $12dB$ less than that of the HG mode. This gain attenuation A_{PATT} (dB) is given by:

$$A_{PATT} = 20\log_{10}\frac{A_{E2}}{A_{E2}+A_{E3}} \tag{2.29}$$

Thus, $A_{PATT} = 12dB$ when $A_{E2} = 1$ and $A_{E3} = 3$. In other words, if Q_2 and Q_3 consist of one and three unity devices, respectively, the power gain in LG mode will be $12dB$ less than that in HG mode. The final LNA design is illustrated in Figure 2.26.

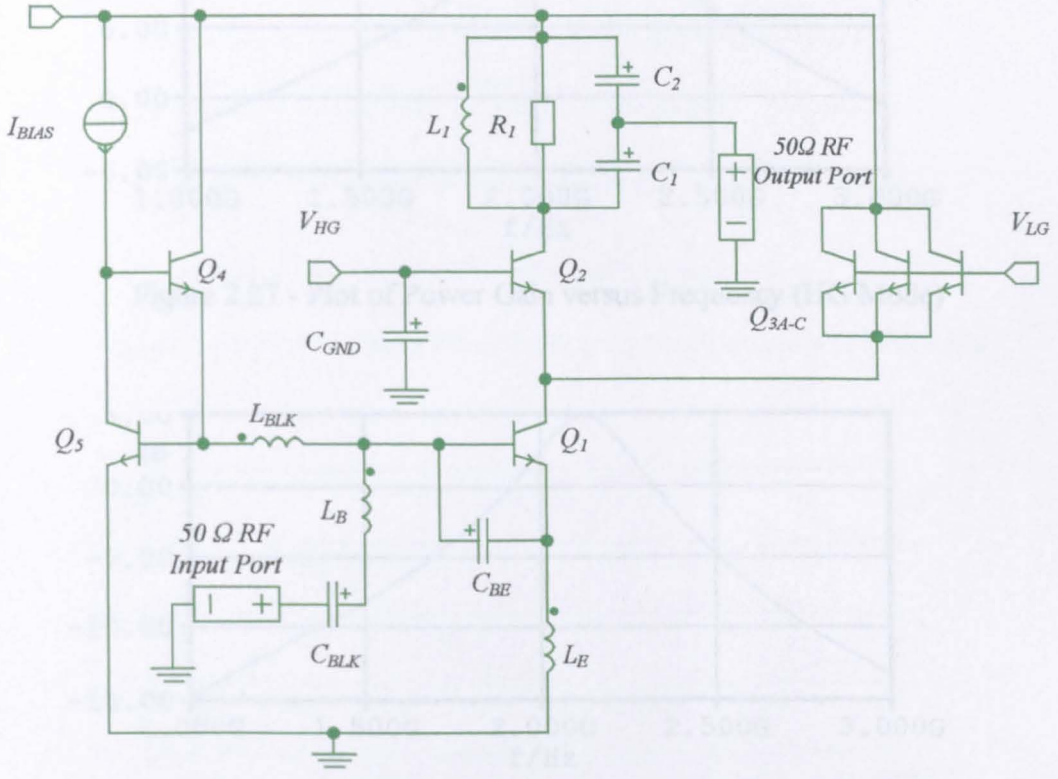

Figure 2.26 – Final Design of Complete LNA with Additional Low Gain Mode

2.2.8 Final LNA Performance

The key performance parameter values for the complete LNA circuit, shown in Figure 2.26, are presented overleaf in Table 2.9.

Plots illustrating power gain, noise performance, reverse isolation and the stability factor with frequency, in both HG and LG modes, are presented in Figures 2.27 to 2.34.

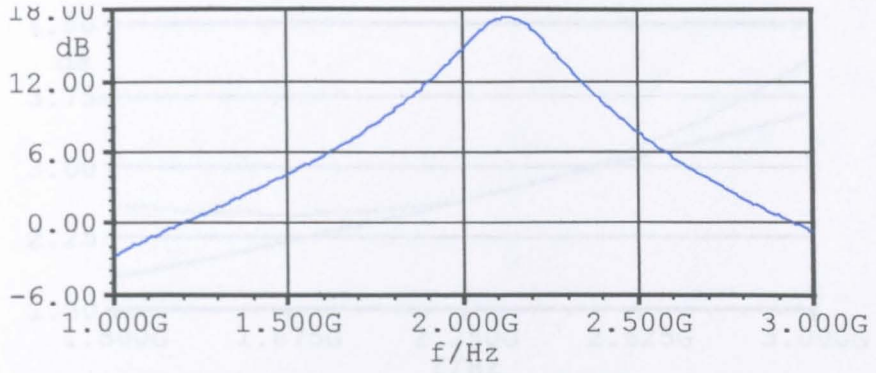

Figure 2.27 - Plot of Power Gain versus Frequency (HG Mode)

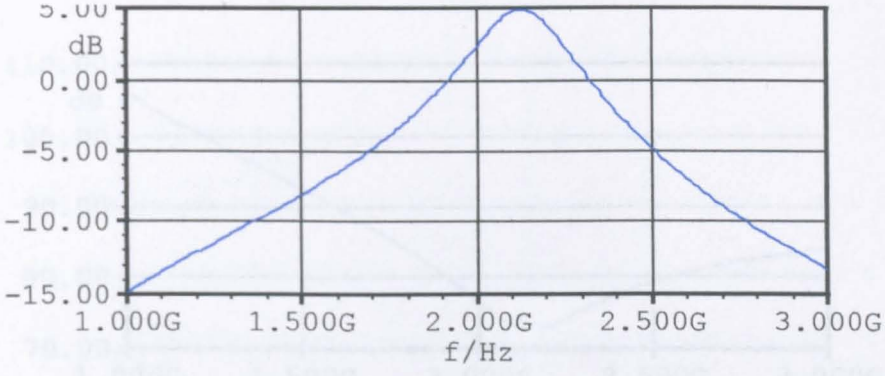

Figure 2.28 – Plot of Power Gain versus Frequency (LG Mode)

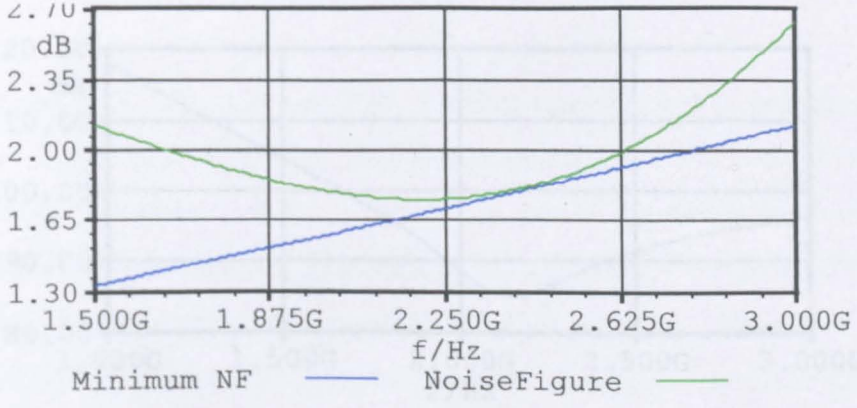

Figure 2.29 – Plot of Noise Performance versus Frequency (HG Mode)

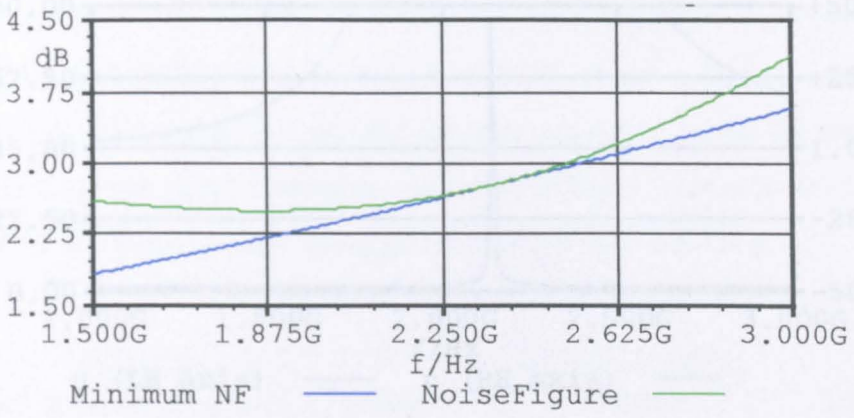

Figure 2.30 Plot of Noise Performance versus Frequency (LG Mode)

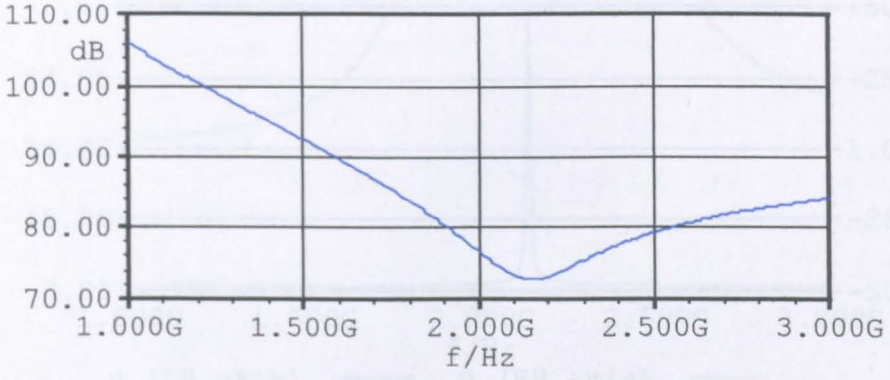

Figure 2.31 – Plot of Reverse Isolation versus Frequency (HG Mode)

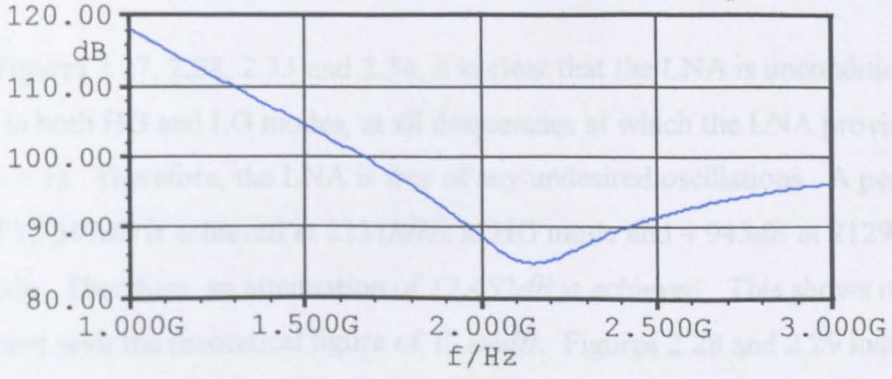

Figure 2.32 – Plot of Reverse Isolation versus Frequency (LG Mode)

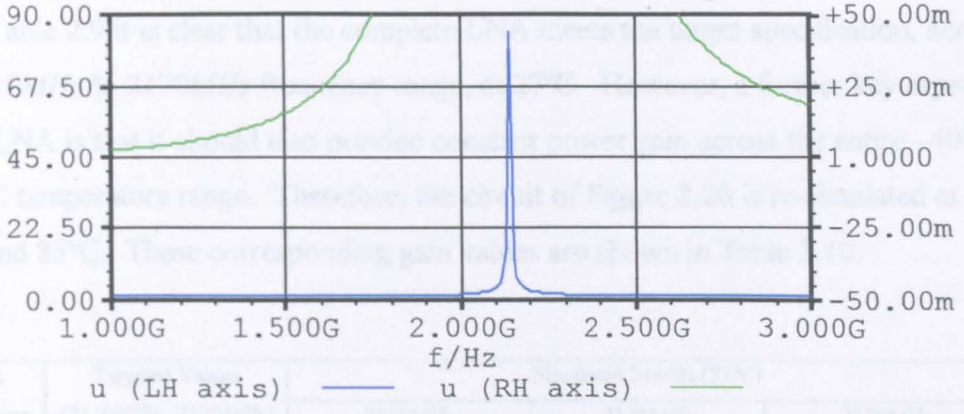

Figure 2.33 – Plot of Stability Factor μ versus Frequency (HG Mode)

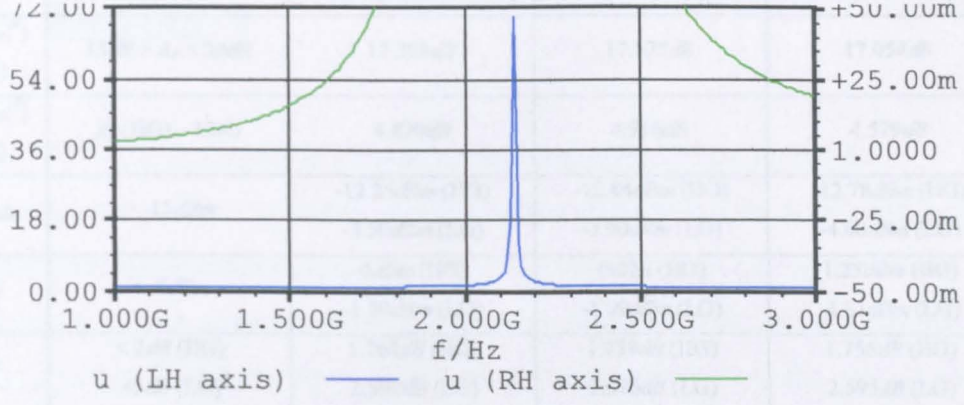

Figure 2.34 – Plot of Stability Factor μ versus Frequency (LG Mode)

From Figures 2.27, 2.28, 2.33 and 2.34, it is clear that the LNA is unconditionally stable, in both HG and LG modes, at all frequencies at which the LNA provides gain (i.e. $A_P > 1$). Therefore, the LNA is free of any undesired oscillations. A peak power gain of 17.397*dB* is achieved at 2131*MHz* in HG mode and 4.945*dB* at 2129*MHz* in LG mode. Therefore, an attenuation of 12.452*dB* is achieved. This shows reasonable agreement with the theoretical figure of 12.04*dB*. Figures 2.28 and 2.29 indicate that the noise figure *NF* is close to the minimum obtainable noise figure NF_{MIN}, in both HG and LG mode. However, as expected, a small difference exists between these two values. This is again because $X_{IN} \neq X_{OPT}$ as illustrated previously in Table 2.4. *NF* is

higher in LG mode. This can be explained because a large proportion of the signal is dumped on to the power supply, thus, reducing the overall signal to noise ratio. From Table 2.9 it is clear that the complete LNA meets the target specification, across the 2110*MHz* to 2170*MHz* frequency range, at 27°C. However, a further key aspect of the LNA is that it should also provide constant power gain across the entire –40°C to 85°C temperature range. Therefore, the circuit of Figure 2.26 is re-simulated at –40°C and 85°C. These corresponding gain values are shown in Table 2.10.

LNA Parameters	Targeted Values (2110*MHz* - 2170*MHz*)	Simulated Results (27°C)		
		2110*MHz*	2140*MHz*	2170*MHz*
Z_{IN}	50 + j0Ω	50.251-j1.750Ω (HG) 51.321-j2.015Ω (LG)	50.178+j0.174Ω (HG) 51.251-j0.119Ω (LG)	50.122+j2.070Ω (HG) 51.193+j1.751Ω (LG)
Z_{OUT}	50 + j0Ω	37.164+j12.315Ω (HG) 37.281+j11.650Ω (LG)	50.823-j0.602Ω (HG) 50.335-j1.392Ω (LG)	51.304+j22.346Ω (HG) 50.375-j22.509Ω (LG)
$A_P(\|S_{21}\|^2)$ (HG)	$15dB > A_P < 20dB$	17.308*dB*	17.375*dB*	17.054*dB*
$A_P(\|S_{21}\|^2)$ (LG)	A_P(HG) – 12*dB*	4.870*dB*	4.916*dB*	4.579*dB*
ICP_{-1dB}	> -15*dBm*	-12.25*dBm* (HG) -3.50*dBm* (LG)	-12.84*dBm* (HG) -3.90*dBm* (LG)	-12.78*dBm* (HG) -4.00*dBm* (LG)
IIP_3	> -5*dBm*	0*dBm* (HG) -1.80*dBm* (LG)	0*dBm* (HG) -1.09*dBm* (LG)	1.25*dBm* (HG) -1.81*dBm* (LG)
NF	< 2*dB* (HG) <5*dB* (LG)	1.764*dB* (HG) 2.559*dB* (LG)	1.759*dB* (HG) 2.576*dB* (LG)	1.756*dB* (HG) 2.595*dB* (LG)
IRL	> 12*dB*	35.072*dB* (HG) 32.472*dB* (LG)	52.090*dB* (HG) 38.083*dB* (LG)	33.678*dB* (HG) 33.585*dB* (LG)
ORL	> 12*dB*	13.890*dB* (HG) 14.160*dB* (LG)	39.899*dB* (HG) 36.913*dB* (LG)	13.320*dB* (HG) 13.197*dB* (LG)
Reverse Isolation ($-S_{12}$)	> 60*dB*	73.027*dB* (HG) 85.183*dB* (LG)	72.690*dB* (HG) 84.858*dB* (LG)	72.746*dB* (HG) 84.920*dB* (LG)

Table 2.9 – Performance Results of the Complete LNA with Additional LG Mode

From Table 2.10, the results show that the actual gain varies by 1.488*dB*, 1.5*dB* and 1.514*dB* at 2110*MHz*, 2140*MHz* and 2170*MHz*, respectively, between –40°C and 85°C. Therefore, a temperature compensation scheme must be employed in order to minimise gain variations with temperature. This is discussed in subsequent chapters.

Mode	Frequency (*MHz*)	A_P @ -40°C (*dB*)	A_P @ 27°C (*dB*)	A_P @ 85°C (*dB*)	Total A_P Variation (*dB*)
HG	2110	18.112	17.308	16.624	1.488
	2140	18.190	17.375	16.690	1.500
	2170	17.880	17.054	16.366	1.514
LG	2110	5.775	4.870	4.100	1.675
	2140	5.828	4.916	4.146	1.682
	2170	5.500	4.579	3.808	1.692

Table 2.10 – Gain Variation Across the –40°C to 85°C Temperature Range

2.3 Summary

Section 2.1 discussed possible LNA input stages in terms of noise performance. It was found that the common-emitter topology offered the best noise performance when compared against the common-base and common-collector topologies. However, several disadvantages associated with the common emitter configuration often prevent its use as an LNA in its basic form. These disadvantages stem from the presence of the base-collector capacitance C_μ. Firstly, C_μ causes the input capacitance to increase due to the Miller Effect [3], which in turn, causes a reduction in the circuit bandwidth. Secondly, C_μ allows coupling between the input and output ports. This coupling can create difficulties in providing simultaneous input and output impedance matching and often leads to instability.

Subsection 2.1.1 reviewed a neutralisation technique that can be employed to overcome these disadvantages. The aim of neutralisation is to cancel or 'neutralise' the coupling from the output port to input port. This is achieved by creating an additional coupling path with equal magnitude and opposite phase. Therefore, the overall or 'net' coupling between the two ports becomes equal to zero. Several neutralisation schemes were considered. However, in order to achieve precise neutralisation, the value of C_μ must be known. Unfortunately, C_μ is somewhat voltage

dependent. Therefore, precise cancellation is difficult particularly when dealing with additional variability in process parameters. Hence, neutralisation has been largely neglected in recent times and is not considered further in this thesis.

Subsection 2.1.2 reviewed a unilateralisation technique that can also be used to overcome the disadvantages associated with the common-emitter configuration. Unilateralisation decreases reverse signal flow and, thus, coupling between the output and input ports of an amplifier. This is most commonly achieved by means of a cascode amplifier or emitter-coupled amplifier (a combination of a common-collector stage with a common-base stage). In both cases, the common-base stage isolates the output from the input. These topologies are considered unilateral, since, signal flow only exists from input to output. This results in increased stability and allows for simplified impedance matching network design. Unilateralisation is much less prone to process parameter variation and is therefore generally considered to be the preferred technique for LNA design. The cascode configuration was selected for use in the final LNA design since it offers superior noise performance compared with the emitter-coupled configuration.

Section 2.2 outlined a methodical approach to LNA design. Firstly, the optimum collector current, at which the lowest minimum noise figure can be achieved, is determined in Subsection 2.2.1. Secondly in Subsection 2.2.2, the resistive real component of the optimum noise impedance (i.e. the input impedance at which the minimum noise figure is obtained) is manipulated, by combination of transistor sizing and the introduction of additional base-emitter capacitance, to equal the actual source impedance (50Ω). This allows simultaneous impedance and noise matching, thus, enabling maximum input power transfer whilst also maximising noise performance. The current 'state of the art' input impedance matching technique, known as inductive degeneration, is discussed in Subsection 2.2.3. Optimal selection of transistor size is determined in Subsection 2.2.4 so that sufficient linearity performance is maintained at the lowest possible power consumption. In Subsection 2.2.5, the maximum achievable power gain is manipulated by appropriate resistor selection. The actual power gain is then made equal to the maximum achievable value. This is achieved by matching the output impedance to the load impedance (50+j0Ω). A series-shunt

capacitor network provides output matching. The initial LNA design, formed using the predetermined values calculated in Subsections 2.2.1 to 2.2.5, is then simulated in Subsection 2.2.6. The results indicate that this initial design satisfies many of the specified target parameters defined in Chapter 1. However, at this stage a low gain mode is not provided. The provision of a low gain mode is addressed in Subsection 2.2.7. Current steering is chosen as the adopted technique and appropriate cascode transistor sizing allows a gain reduction of approximately $12dB$ in low gain mode. The final LNA design is simulated in Subsection 2.2.8. This is found to fully satisfy the specification defined in Chapter 1 at 27°C. However, the LNA should also provide constant gain across the entire –40°C to 85°C temperature range. Furthermore, the actual gain varies by $1.488dB$, $1.5dB$ and $1.514dB$ at $2110MHz$, $2140MHz$ and $2170MHz$, respectively, between –40°C and 85°C. Therefore, a temperature compensation scheme must be employed in order to minimise gain variations with temperature. This is addressed in subsequent chapters.

2.4 References

[1] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 783-788.

[2] J. M. Miller. 'Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit,' *Scientific Papers of the Bureau of Standards*,15(351), 1920, pp. 367-385.

[3] R. Ludwig and P. Bretchko, '*RF Circuit Design: Theory and Applications*,' Prentice Hall, Upper Saddle River, 2000, pp. 492.

[4] R. Ludwig and P. Bretchko, '*RF Circuit Design: Theory and Applications*,' Prentice Hall, Upper Saddle River, 2000, pp. 492-511.

[5] T. H. Lee, '*The Design of Radio-Frequency Integrated Circuits*,' Cambridge, UK, Cambridge University Press, 1998, pp. 205.

[6] D. J. Cassan and J. R. Long, 'A 1V Transformer-Feedback Low-Noise Amplifier for 5GHz Wireless LAN in 0.18um CMOS,' *IEEE Journal of Solid State Circuits*, Vol. 38, No. 3, March 2003, pp. 427-435.

[7] J. R. Long, 'Monolithic Transformers for Silicon RFIC Design,' *IEEE Journal of Solid State Circuits*, Vol. 35, September 2000, pp. 1368-1382.

[8] T. H. Lee, '*The Design of Radio-Frequency Integrated Circuits*,' Cambridge, UK, Cambridge University Press, 1998. pp, 206.

[9] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 260-262.

[10] S. Voinigescu *et al*, 'A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design,' *IEEE Journal of Solid State Circuits*, Vol. 32, No. 9, September 1997, pp. 1430-1439.

[11] G. Girlando, E. Ragonese, A. Italia and G. Palmisano, 'Bipolar LNA Design at Different Operating Frequencies,' *Proceedings of IEEE International Symposium of Circuits and Systems* (ISCAS), 25th-28th May 2003, Vol.1, pp.213-216.

[12] S. K. Alam, and J. DeGroat, 'A 1.5V 2.4GHz Differential CMOS Low Noise Amplifier for Bluetooth and Wireless LNA Applications,' *Proceedings of IEEE International North East Workshop of Circuits and Systems* (NEWCAS), 18th-21st June, 2006, pp. 13-16.

[13] G. Girlando and G. Palmisano, 'Noise Figure and Impedance Matching in RF Cascode Amplifiers,' *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, Vol. 46, No. 11, November 1999, pp. 1388-1396.

[14] M. K. Raja, T. T. C. Boon, K. N. Kumar and W. S. Jau, 'A Fully Integrated Variable Gain 5.75GHz LNA with on chip Active Balun for WLAN,' *IEEE Radio Frequency Integrated Circuits Symposium*, 2003, pp. 439-442.

[15] R. Ludwig and P. Bretchko, '*RF Circuit Design: Theory and Applications*,' Prentice Hall, Upper Saddle River, 2000, pp. 405-426.

[16] R. Ludwig and P. Bretchko, '*RF Circuit Design: Theory and Applications*,' Prentice Hall, Upper Saddle River, 2000, pp. 101-133.

[17] K. L. Fong, 'Dual-Band High-Linearity Variable Gain Low Noise Amplifiers for Wireless Applications,' *Proceedings of IEEE International Solid-State Circuits Conference* (ISSCC), 1999, pp. 224-225.

[18] Kumar, S. Vice, H. Morkner and W. Lam, 'Enhancement mode GaAs PHEMT LNA with linearity control (IP3) and phased matched mitigated bypass switch and differential active mixer,' *IEEE International Microwave Symposium Digest*, 8th-13th June 2003, Vol. 3, pp. 1577-1580.

CHAPTER 3

Constant Gain Bias Circuit Techniques

Chapter 3 concerns the investigation and analysis of traditional circuit techniques that can be used to bias the LNA of Chapter 1 in such a way that constant gain is achieved over a wide temperature range. A comparison of numerous circuit variations is conducted; particularly with regards to the temperature coefficient and sensitivity of the output current to power supply variations.

As previously mentioned in Chapter 1, a key aspect of any commercial LNA is that it should operate within specification over a wide temperature range. Common temperature range standards are detailed in [1] and are reproduced in Table 3.1 below.

Class	Lower Limit °C	Upper Limit °C
Military	-55	+125
Extended	-40	+125
Industrial	-40	+85
Commercial	0	+70

Table 3.1 – Temperature Range Standards

The LNA designs discussed within this thesis are intended for use in a portable cellular handset and could, theoretically, be used in any climatic condition across the globe. Therefore, it seems plausible that such designs should be able to operate across the entire Industrial Temperature Range (ITR) as this offers the best fit for any known climate. Hence, the gain of the LNA should remain as constant as possible between -40°C and +85°C.

3.1 Constant Voltage Gain

The small-signal voltage gain (A_v) of a bipolar transistor, connected in common-emitter configuration, can be expressed as:

$$A_v = g_m Z_L \tag{3.1}$$

where g_m and Z_L are the transconductance and load impedance of the transistor respectively. The transconductance is given by the well-known equation,

$$g_m = \frac{Ic}{V_T} = \frac{qIc}{kT} \tag{3.2}$$

where I_C is the collector current, V_T is the thermal voltage, q is the charge on an electron (1.602×10^{-19} C), k is Boltzmann's constant (1.3807×10^{-23} JK^{-1}) and T is temperature in degrees Kelvin (°K). Equations (3.1) and (3.2) show clearly that the transconductance and voltage gain are both dependent on temperature. In order to demonstrate how to eliminate this inherent temperature dependence we must first derive the transconductance temperature coefficient (TC_{gm}). By partial differentiation of (3.2) with respect to temperature:

$$\frac{\partial g_m}{\partial T} = \frac{V_T \frac{\partial Ic}{\partial T} - Ic \frac{\partial V_T}{\partial T}}{V_T^2} \tag{3.3}$$

This can be simplified to:

$$\frac{\partial g_m}{\partial T} = \frac{Ic}{V_T}\left(\frac{1}{Ic}\frac{\partial Ic}{\partial T} - \frac{1}{V_T}\frac{\partial V_T}{\partial T}\right) \tag{3.4}$$

Substituting (3.2) into (3.4) gives:

$$TC_{gm} = \frac{1}{g_m}\frac{\partial g_m}{\partial T} = \frac{1}{Ic}\frac{\partial Ic}{\partial T} - \frac{1}{V_T}\frac{\partial V_T}{\partial T} \tag{3.5}$$

In order to eliminate any voltage gain variations with temperature we must ensure that $TC_{gm} = 0$. Thus, the following condition must be met:

$$\frac{1}{Ic}\frac{\partial Ic}{\partial T} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} \tag{3.6}$$

This can also be expressed as:

$$TC_{Ic} = TC_{VT} \tag{3.7}$$

where TC_{IC} and TC_{VT} represent the temperature coefficients of I_C and V_T respectively. A numerical value for TC_{VT} can easily be derived. This is shown overleaf.

$$TC_{VT} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} = \frac{1}{V_T}\frac{V_T}{T} = \frac{1}{T} \tag{3.8}$$

Assuming operation at room temperature (27°C or 300.15°K):

$$TC_{VT} = \frac{1}{300.15} = 3332 ppm/°C \tag{3.9}$$

From (3.8) we see that the temperature coefficient of V_T is inversely Proportional To Absolute Temperature (PTAT) and also, from (3.9), that it has a value of 3332 ppm/°C. Referring back to (3.7), it is apparent that in order to ensure minimum voltage gain variation with temperature, the collector current temperature coefficient for a bipolar transistor should equal that of the thermal voltage (i.e. $TC_{IC} = TC_{VT} =$ 3332 ppm/°C). Thus, it follows that the collector current must also be PTAT.

3.2 Basic PTAT Current Reference Circuits

In order to develop a PTAT current it is necessary, first, to understand the workings of a simple Widlar Current Source [2,3]. This circuit or a derivative is found at the heart of all PTAT reference circuit designs.

3.2.1 The Basic Widlar Current Source

Figure 3.1 shows the simplest form of a Widlar Current Source. An expression for the output current can easily be derived by inspection.

Applying Kirchhoff's Voltage Law (KVL) to the base-emitter loop it follows that:

$$V_{BE1} - V_{BE2} - \frac{\beta_2 + 1}{\beta_2} I_{out} R_1 = 0 \tag{3.10}$$

where V_{BE1} and V_{BE2} are the base-emitter voltages of Q_1 and Q_2, respectively, and β_2 is the DC current gain of Q_2. According to [4], the collector current of a bipolar transistor that is operated in forward active mode under low-level injection conditions but at terminal currents well in excess of leakage levels, can be expressed as:

$$I_C = I_S . e^{\left[\left(\frac{V_{BE}}{V_T}\right) + \left(\frac{V_{CE}}{V_{AQ}}\right)\right]} \tag{3.11}$$

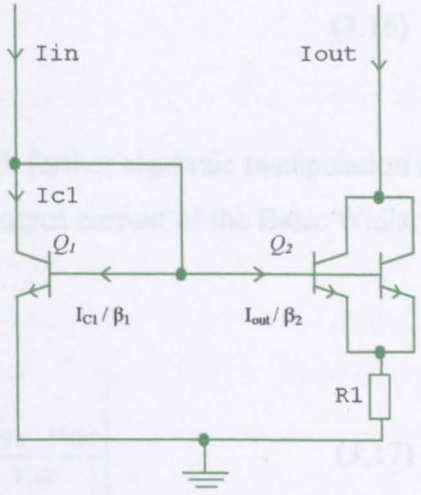

Figure 3.1 – A Basic Widlar Current Source

I_S is the base characteristic saturation current, V_{CE} is the collector-emitter voltage and V_{AQ} represents the Early voltage, the subscript for Q (N or P) indicating the device type (*NPN* or *PNP*). Thus it follows that:

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}} - \frac{V_T V_{CE1}}{V_{AN}} \tag{3.12}$$

and:

$$V_{BE2} = V_T \ln \frac{I_{out}}{I_{S2}} - \frac{V_T V_{CE2}}{V_{AN}} \tag{3.13}$$

Therefore by substituting (3.12) and (3.13) into (3.10) we obtain:

$$\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{out}}{I_{S2}} = \left[\frac{\beta_2 + 1}{\beta_2} I_{out} R_1 + V_T \frac{V_{CE1} - V_{CE2}}{V_{AN}} \right] \frac{1}{V_T} \tag{3.14}$$

By Kirchhoff's Current Law (KCL),

$$I_{in} = I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{out}}{\beta_2} \tag{3.15}$$

The expression above is easily rewritten in terms of the collector current:

$$I_{C1} = \frac{\beta_1}{\beta_1 + 1}\left(I_{in} - \frac{I_{out}}{\beta_2}\right) \tag{3.16}$$

I_{C1} can now be substituted back into (3.14). With further algebraic manipulation (see Appendix A), it is easily demonstrated that the output current of the Basic Widlar Current Source is given by:

$$I_{out} = \frac{\beta_2}{\beta_2 + 1}\frac{V_T}{R_1}\left[\ln\left[\frac{\left(\frac{\beta_1}{\beta_1 + 1}\right)\left(I_{in} - \frac{I_{out}}{\beta_2}\right)}{I_{out}}\frac{I_{S2}}{I_{S1}}\right] + \frac{V_{CE2} - V_{CE1}}{V_{AN}}\right] \tag{3.17}$$

If β_1 and β_2 are both >>1 then (3.17) simplifies to:

$$I_{out} = \frac{V_T}{R_1}\left[\ln\left(\frac{I_{in}}{I_{out}}\frac{I_{S2}}{I_{S1}}\right) + \frac{V_{CE2} - V_{CE1}}{V_{AN}}\right] \tag{3.18}$$

If $V_A >> \Delta V_{CE}$ then this result can be further simplified to give the well known equation [5]:

$$I_{out} = \frac{V_T}{R_1}\ln\left(\frac{I_{in}}{I_{out}}\frac{I_{S2}}{I_{S1}}\right) \tag{3.19}$$

From (3.19) it is clear that if the ratio of input current to output current is held constant then the resulting output current will be proportional to V_T. Or in other words, the output current will be PTAT. But how do we ensure that the ratio is indeed held constant? This is discussed later in Section 3.2.4.

By comparing (3.17) with (3.19), it can be seen that the actual expression for the output current differs somewhat from the simplified ideal expression. Thus, the Basic Widlar Current Source suffers from output current errors that are due to finite values of β and V_A along with mismatches in V_{CE1} and V_{CE2}. However, this limitation can be minimised with design techniques discussed in subsequent sections.

3.2.2 The Buffered Widlar Current Source

One common method for reducing the errors attributed to finite values of β is to replace the basic circuit with a Buffered Widlar Current Source. This is shown in Figure 3.2. Following a similar approach to that of the previous section, an expression for the output current is derived. The analysis of this circuit begins in an identical fashion to that of the Basic Widlar Current Source. The analysis from equation (3.10) to (3.14) is equally applicable to the Buffered Widlar Current Source except that in this case:

$$I_{C1} = I_{in} - I_{B3} \tag{3.20}$$

I_{B3} is the base current of Q_3, which in turn is given by:

$$I_{B3} = \frac{(\beta_1+1)I_{E2} + (\beta_2+1)I_{E1}}{(\beta_1+1)(\beta_2+1)(\beta_3+1)} \tag{3.21}$$

I_{E1} and I_{E2} are the emitter currents of Q_1 and Q_2 respectively. These, in turn, are given by:

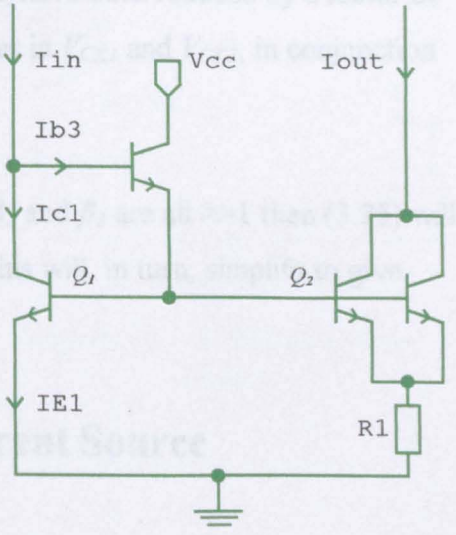

Figure 3.2 – A Buffered Widlar Current Source

$$I_{E1} = \frac{\beta_1+1}{\beta_1} I_{C1} \tag{3.22}$$

$$I_{E2} = \frac{\beta_2+1}{\beta_2} I_{out} \tag{3.23}$$

By combining (3.20), (3.21), (3.22) and (3.23) it is easily demonstrated that (See full derivation in Appendix A):

$$I_{C1} = \frac{I_{in}}{1+[1/\beta_1(\beta_3+1)]} - \frac{I_{out}}{\beta_2[(\beta_3+1)+1/\beta_1]} \tag{3.24}$$

This result can now be substituted back into (3.14). With a little algebraic manipulation, an expression for the output current of the Buffered Widlar Current Source can be arrived at. Thus:

$$I_{out} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\left[\ln\left[\frac{\left(\frac{I_{in}}{1+[1/\beta_1(\beta_3+1)]} - \frac{I_{out}}{\beta_2[(\beta_3+1)+1/\beta_1]}\right)}{I_{out}}\frac{I_{S2}}{I_{S1}}\right] + \frac{V_{CE2}-V_{CE1}}{V_{AN}}\right] \tag{3.25}$$

If (3.25) is compared with (3.17) then it can be seen that the output current errors due to finite values of β, in the square bracketed term, have been reduced by a factor of $(\beta+1)$. Unfortunately the error due to mismatches in V_{CE1} and V_{CE2}, in conjunction with a finite V_A value, remains unchanged.

As with the Basic Widlar Current Source, if β_1, β_2 and β_3 are all >>1 then (3.25) will reduce to (3.18). Similarly, if $V_A >> \Delta V_{CE}$ then this will, in turn, simplify to give (3.19).

3.2.3 The Wilson-based Current Source

An improved PTAT current source based on the use of a Wilson Current Mirror [6,7] is shown in Figure 3.3. The analysis of this circuit begins in a similar fashion to that of the Basic Widlar and Buffered Widlar Current Sources (Full derivation is given in Appendix A). The approach leading to equations (3.10) and (3.13) is equally applicable to the Wilson-based Current Source, except that in this case:

$$V_T \ln\frac{I_{C1}}{I_{S1}} - V_T \ln\frac{I_{C2}}{I_{S2}} + \frac{V_T V_{CE2}}{V_A} - \frac{V_T V_{CE1}}{V_A} - \frac{\beta_2+1}{\beta_2} I_{C2} R_1 = 0 \qquad (3.26)$$

The diode-connected transistor Q_4 acts as a level shift element which forces V_{BE4} and V_{BE3} to be equal if $I_{in} = I_{out}$. Thus it holds that $V_{CE1} \approx V_{CE2}$. Assuming this is so, (3.26) can be rewritten as:

$$V_T \ln\frac{I_{C1}}{I_{S1}} - V_T \ln\frac{I_{C2}}{I_{S2}} - \frac{\beta_2+1}{\beta_2} I_{C2} R_1 = 0 \qquad (3.27)$$

In this case it can be shown that:

$$I_{C1} = I_{in} - \frac{I_{out}}{\beta_3} \qquad (3.28)$$

and:

$$I_{C2} = \frac{\beta_2}{\beta_2+1}\left[\frac{\beta_3+1}{\beta_3} I_{out} - \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)\right] \qquad (3.29)$$

By substituting (3.28) and (3.29) back into (3.27), a little algebraic manipulation gives an expression for the output current:

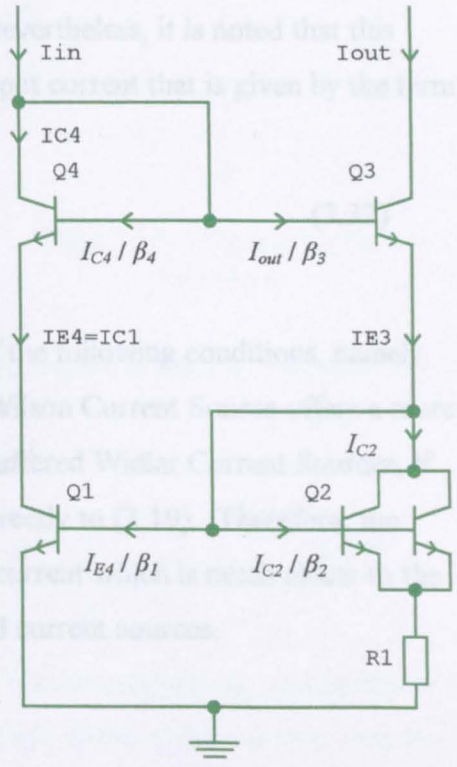

Figure 3.3 – A Wilson Current Source

$$I_{out} = \frac{\beta_3}{\beta_3+1}\frac{V_T}{R_1} \ln\left[\left(\frac{I_{in} - \frac{I_{out}}{\beta_3}}{\frac{\beta_2(\beta_3+1)}{\beta_3(\beta_2+1)} I_{out} - \frac{\beta_2}{\beta_1(\beta_2+1)}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)}\right)\frac{I_{S2}}{I_{S1}}\right] + \frac{\beta_3}{\beta_1(\beta_3+1)}\left(I_{in} - \frac{I_{out}}{\beta_3}\right) \qquad (3.30)$$

For the case $\beta_1=\beta_2=\beta_3=\beta_N$, (3.30) becomes:

$$I_{out} = \frac{\beta_N}{\beta_N+1}\frac{V_T}{R_1}\ln\left[\left(\frac{I_{in}-\frac{I_{out}}{\beta_N}}{I_{out}-\frac{1}{(\beta_N+1)}\left(I_{in}-\frac{I_{out}}{\beta_N}\right)}\right)\frac{I_{S2}}{I_{S1}}\right]+\frac{1}{(\beta_N+1)}\left(I_{in}-\frac{I_{out}}{\beta_N}\right) \qquad (3.31)$$

Again, if (3.31) is compared to (3.17) then it can be seen that the output current errors due to finite values of β, in the square bracketed term, have been significantly reduced. In addition, errors due to mismatches in V_{CE1} and V_{CE2} in conjunction with finite V_A values have been completely removed. Nevertheless, it is noted that this configuration gives rise to another error in the output current that is given by the term:

$$\frac{1}{(\beta_N+1)}\left(I_{in}-\frac{I_{out}}{\beta_N}\right) \qquad (3.32)$$

However, this term can be considered negligible if the following conditions, namely $I_{in} << \beta_N$ and $I_{out} << \beta_N$, are met. Therefore, the Wilson Current Source offers a more accurate output current. As with the Basic and Buffered Widlar Current Sources, if β_1, β_2 and β_3 are all >>1 then (3.31) will reduce directly to (3.19). Therefore, the Wilson Current Source offers an accurate output current which is much closer to the ideal than those offered by the previous mentioned current sources.

3.2.4 Bootstrap Biasing

In Section 3.2.1 it was stated that 'from (3.19) it is clear that if the ratio of input current to output current is held constant then the resulting output current will be proportional to V_T. Or, in other words, the output current will be PTAT.'

A technique that is often used, to ensure that the ratio is indeed held constant, was first proposed by Van Kessel and Van der Plaasche [8]. This method has been called bootstrap-biasing [9] or self-biasing. It commonly involves the use of an additional current mirror, of complementary polarity, and is illustrated in Figure 3.4. By connecting a current mirror as shown, the input current of the Widlar current source

(subsequent analysis is equally applicable to the Wilson Current Source) becomes dependent on its output current.

If the gain of the current mirror is set precisely to unity then $I_{out}=I_{in}$. The output current is then given by:

$$I_{out} = \frac{V_T}{R_1} \ln \frac{I_{S2}}{I_{S1}} \qquad (3.33)$$

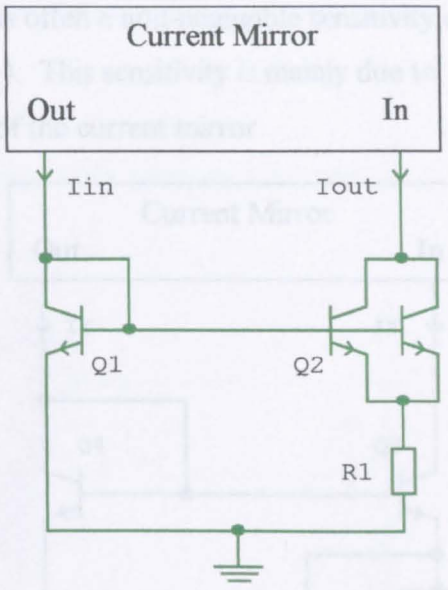

Figure 3.4 – Bootstrap Bias Technique

The ratio I_{S2}/I_{S1} is equal to the emitter area ratio Q_2/Q_1. Hence, in Figure 3.4, $I_{S2}/I_{S1} = 2$ since Q_2 comprises two transistors in parallel and, thus, has an emitter area twice as large as Q_1. Partial differentiation of (3.33) with respect to temperature gives the temperature coefficient of I_{out} (TC_{Iout}):

$$TC_{Iout} = \frac{1}{I_{out}} \frac{\partial I_{out}}{\partial T} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R_1} \frac{\partial R_1}{\partial T} \qquad (3.34)$$

From (3.34) it is apparent that TC_{Iout} is dependent on the temperature coefficients of both V_T and the resistor R_1. If temperature coefficient of the resistor is zero then the resulting temperature coefficient of I_{out} will meet the condition stated in (3.6). Thus I_{out} will be truly PTAT. In practice, resistors with zero temperature coefficients do not exist. However, external surface-mount resistors with temperature coefficients as low as 5ppm/°C [10] are readily available. Since this value is very close to ideal it is assumed for the remainder of this thesis that the temperature coefficient of R_1 is zero.

3.2.4.1 Theoretical Sensitivity to Power Supply Voltage Variations and Observed Simulation Results

PTAT current reference circuits must provide a current that is accurate and predictable across a wide range of power supply voltages. However, a practical

shortcoming of the method shown in Figure 3.4 is often a non-negligible sensitivity of I_{out} to variation in the power supply voltage (V_{CC}). This sensitivity is mainly due to variations in the current transfer ratio, $\lambda = I_Y/I_X$, of the current mirror.

It is now useful to determine the sensitivity of the Wilson current source shown in Figure 3.5. For simplicity (3.19) can be rewritten as:

$$Iout = \frac{V_T}{R1} \ln \lambda m \qquad (3.35)$$

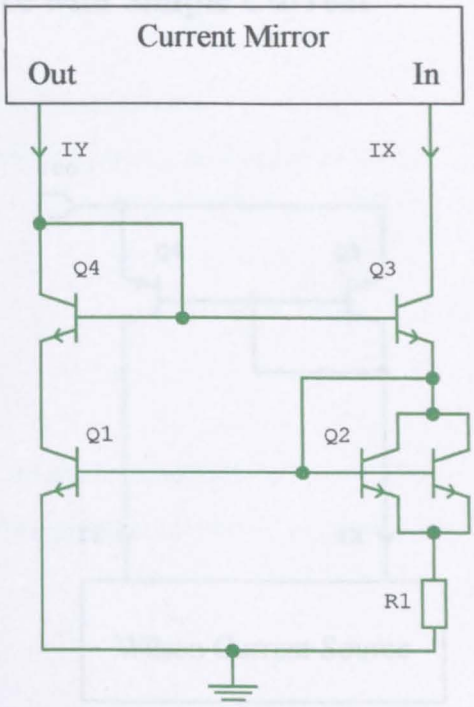

Figure 3.5 –PTAT Current Generator using a Wilson Current Source with a 1:m Emitter Area Ratio

From this result, it is clear that as V_{CC} changes then so does I_{out} because of a corresponding change in λ. Using (3.35), a further equation can be derived to give the sensitivity (S), to changes in V_{CC}, of a PTAT current generator circuit comprising of a Wilson current source and a generic current mirror. Again in [4], this is given as:

$$S = \frac{1}{\partial Iout} \frac{\partial Iout}{\partial Vcc} = \frac{\partial(\ln Iout)}{\partial Vcc} \qquad (3.36)$$

which can be rewritten (Full derivation is given in Appendix A) as:

$$S = \frac{1}{\ln \lambda m} \left(\frac{1}{\lambda} \frac{\partial \lambda}{\partial Vcc} \right) \qquad (3.37)$$

This result can now be applied to the analysis of different current mirror topologies that have $\lambda \approx 1$. This is necessary in order to determine how sensitive each current mirror topology is to changes in V_{CC} when used in place of the generic current mirror.

The performances of various current mirrors are compared in the subsequent sections of this chapter.

3.2.4.1.a Wilson Current Source with Simple Current Mirror (WCS+WCM)

According to [11], the current transfer ratio, $\lambda = I_Y/I_X$, of a simple current mirror with equal emitter area ratios can be defined as:

$$\lambda = \frac{1+(V_{BC4}-V_{BC5})/V_{AP}}{1+(2/\beta_P)} \qquad (3.38)$$

This expression can be rewritten as:

$$\lambda = \frac{1}{(1+2/\beta_P)}\left(1+\frac{V_{BC4}}{V_{AP}}\right) \qquad (3.39)$$

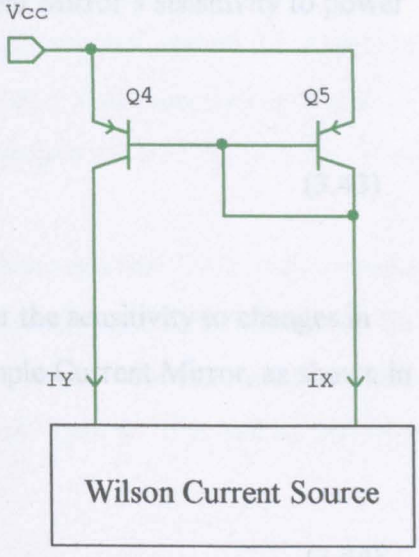

Figure 3.6 – Wilson Current Source with Simple Current Mirror

The $1/(1+2/\beta_P)$ term is constant and V_{BC4} varies directly with V_{CC}, so, this expression is easily differentiated with respect to V_{CC} to give:

$$\frac{\partial\lambda}{\partial V_{CC}} = \frac{\partial\lambda}{\partial V_{BC4}} = \left(\frac{1}{(1+2/\beta_P)}\right)\frac{1}{V_{AP}} \qquad (3.40)$$

Equation (3.39) and the reciprocal of (3.38) can now be combined to give an expression for the Simple Current Mirror's sensitivity to power supply variations. Thus:

$$\frac{1}{\lambda}\frac{\partial\lambda}{\partial V_{CC}} = \left(\frac{1}{(1+2/\beta_P)}\right)\left(\frac{1+2/\beta_P}{1+V_{BC4}/V_{AP}}\right)\frac{1}{V_{AP}} \qquad (3.41)$$

This result simplifies to:

$$\frac{1}{\lambda}\frac{\partial\lambda}{\partial Vcc}=\left(\frac{1}{1+V_{BC4}/V_{AP}}\right)\frac{1}{V_{AP}} \tag{3.42}$$

The bracketed term approximately equals unity for the usual case $V_{AP} >> V_{BC4}$. Therefore, it is reasonable to take the Simple Current Mirror's sensitivity to power supply variations as:

$$\frac{1}{\lambda}\frac{\partial\lambda}{\partial Vcc}=\frac{1}{V_{AP}} \tag{3.43}$$

By substituting (3.43) into (3.37), an expression for the sensitivity to changes in power supply of a Wilson Current Source with Simple Current Mirror, as shown in Figure 3.6, is defined as:

$$S(WCS+SCM)=\frac{1}{V_{AP}}\left(\frac{1}{\ln\lambda m}\right) \tag{3.44}$$

The result of (3.43) is very interesting because with a little intuitive thinking it seems that:

$$\frac{1}{\lambda}\frac{\partial\lambda}{\partial Vcc}\approx\frac{1}{I_T}\frac{\partial I_T}{\partial Vcc} \tag{3.45}$$

Thus, an alternative method can be developed to simplify the analysis of more complicated current mirror designs in subsequent sections. This is clearly demonstrated in the following analysis. From theory [11], the output resistance, R_{OUT}, of a Simple Current Mirror is given by:

$$R_{OUT}=\frac{V_{AP}}{I_T}=\frac{\partial V_{OUT}}{\partial I_T} \tag{3.46}$$

By replacing ∂V_{OUT} by ∂V_{CC}, a reasonable procedure because any change in V_{CC} will result in an equal change in V_{OUT}, and rearranging the previous equation we obtain:

$$\frac{1}{I_T}\frac{\partial I_T}{\partial V_{CC}} = \frac{1}{V_{AP}} \tag{3.47}$$

Thus, (3.47) gives an identical result to that of (3.43). This in turn shows that (3.45) is correct. Using the measured device parameters (V_{EB}=0.85V, β_P=65.27, V_{BE}=0.81V and β_N=177), Spice model data (V_{AP}=22V and V_{AN}=63V) and selecting m=2 and V_{CC}=5V, it is possible to calculate the theoretical values for λ and $S_{(WCS+SCM)}$. These are presented in Table 3.2 below.

Parameters	Theoretical Values
λ	1.082
$S_{(WCS+SCM)}$	58882 ppm/V

Table 3.2 – Theoretical Values for a Wilson Current Source with Simple Current Mirror

Table 3.2 illustrates that the current transfer ratio is expected to differ by 8.2% from the ideal case. Similarly, the output current should vary by 58882 ppm/V. This can be rewritten as 5.88 %/V.

Figure 3.7 shows the circuit diagram of the WCS+SCM PTAT Current Generator used for simulation. Initially, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V.

Table 3.3 shows the temperature performance of I_X, I_Y and λ at various power supply voltage values. The theoretical value of R_{PTAT} is given by:

$$R_{PTAT} = \frac{V_T}{I_X}\ln\lambda m = \frac{25.86mV}{50\mu A}\times\ln(1.082\times 2) = 399.26\Omega \tag{3.48}$$

However, the actual value of R_{PTAT} needed, in order that I_X = 50μA at 27°C, was found to be 443.63Ω. This is due to three things. Firstly, the formula used in (3.48) is a rearrangement of the simplified equation found in (3.35). A more accurate result could be obtained using a rearrangement of (3.31), however, this is much less straightforward.

Secondly, (3.48) assumes that the forward emission coefficient, n, of the NPN transistors is unity. Thus n does not appear in (3.48). More accurately the theoretical value of R_{PTAT} is given by:

$$R_{PTAT} = \frac{nV_T}{I_X} \ln \lambda m = \frac{1.094 \times 25.86mV}{50\mu A} \times \ln(1.082 \times 2) = 436.79\Omega \qquad (3.49)$$

where n is determined via a method given in Appendix A.

Thirdly, the theoretical value of λ =1.082 at 27°C calculated previously is slightly less than the actual simulated value of λ =1.111 at 27°C. Indeed, if λ =1.082 is substituted with λ =1.111 in (3.48) then the calculated value of R_{PTAT} becomes 451.75Ω which is much closer to the measured value of 443.63 Ω than that calculated in (3.48).

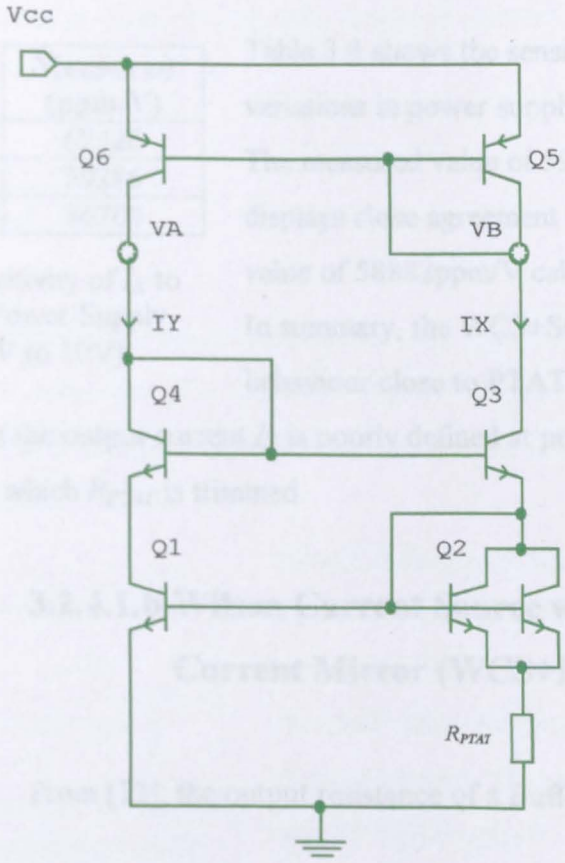

Figure 3.7 – Wilson Current Source + Simple Current Mirror PTAT Current Generator

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(µA)	I_Y(µA)	λ	I_X(µA)	I_Y(µA)	λ	I_X(µA)	I_Y(µA)	λ	(ppm/°C)
3	32.213	31.668	0.983	42.600	42.500	0.998	51.953	52.467	1.010	3716
4	35.327	36.859	1.043	46.406	48.965	1.055	56.299	59.961	1.107	3615
5	38.254	42.170	1.102	50.000	55.574	1.111	60.410	67.608	1.119	3545
6.5	42.340	50.316	1.188	55.038	65.702	1.194	66.200	79.325	1.198	3468
10	50.713	69.858	1.378	65.441	89.994	1.375	78.228	107.423	1.373	3364

Table 3.3 – Temperature Performance of I_X, I_Y and λ at Various Power Supply Voltage Values

From the results in Table 3.3 it is clear that I_X, I_Y and consequently λ are all highly sensitive to change in power supply. Thus, the design value of $I_X = 50\mu A$ at 27°C is only valid when V_{CC}=5V. However, as expected I_X exhibits behaviour close to PTAT between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) varies between 3364ppm/°C and 3716ppm/°C across the 3V to 10V power supply range. This shows good agreement with the theoretical value (3.9) of 3332ppm/°C.

Temperature (°C)	$S_{(WCS+SCM)}$ (ppm/V)
-40	62420
27	59286
85	56700

Table 3.4 - Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V)

Table 3.4 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V). The measured value of 59286ppm/V at 27°C displays close agreement with the theoretical value of 58882ppm/V calculated in Table 3.2. In summary, the WCS+SCM topology exhibits behaviour close to PTAT. However, a practical shortcoming is that the output current I_X is poorly defined at power supply voltages other than that for which R_{PTAT} is trimmed.

3.2.4.1.b Wilson Current Source with Buffered Current Mirror (WCS+BCM)

From [12], the output resistance of a Buffered Current Mirror is given by:

$$R_{OUT} = \frac{V_{AP}}{I_Y} = \frac{\partial V_{OUT}}{\partial I_Y} \tag{3.50}$$

Again, by replacing ∂V_{OUT} by ∂V_{CC} and rearranging the previous equation we obtain:

$$\frac{1}{I_Y}\frac{\partial I_Y}{\partial V_{CC}} = \frac{1}{V_{AP}} \approx \frac{1}{\lambda}\frac{\partial \lambda}{\partial V_{CC}} \qquad (3.51)$$

By substituting (3.51) into (3.37), an expression for the sensitivity to changes in power supply of a Wilson Current Source with Buffered Current Mirror, as shown in Figure 3.8, is defined as:

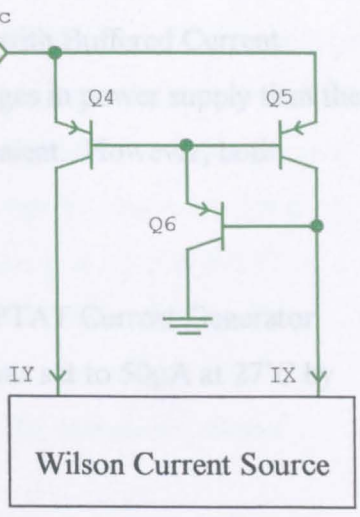

Figure 3.8 – Wilson Current Source with Buffered Current Mirror

$$S_{(WCS+BCM)} = \frac{1}{V_{AP}}\left(\frac{1}{\ln \lambda m}\right) \qquad (3.52)$$

where the current transfer ratio, $\lambda = I_Y/I_X$, of a Buffered Current Mirror with equal emitter area ratios can be defined as:

$$\lambda = \frac{1+(V_{EC4}-V_{EC5})/V_{AP}}{1+2/\beta_P(\beta_P+1)} \qquad (3.53)$$

As before, using the measured device parameters (V_{EB}=0.85V, β_P=65.27, V_{BE}=0.81V and β_N=177), Spice model data (V_{AP}=22V and V_{AN}=63V) and selecting m=2 and V_{CC}=5V, it is possible to calculate the theoretical values for λ and $S_{(WCS+BCM)}$. These are presented in Table 3.5 below.

Parameters	Theoretical Values
λ	1.076
$S_{(WCS+BCM)}$	59309 ppm/V

Table 3.5 – Theoretical Values for a Wilson Current Source with Buffered Current Mirror

Table 3.5 illustrates that the current transfer ratio is expected to differ by 7.6% from the ideal case. This is a slight improvement over the result calculated previously for the Simple Current Mirror. The output current should vary by 59309 ppm/V. This can be rewritten as 5.93 %/V.

In this case it can be said that the Wilson Current Source with Buffered Current Mirror topology should be slightly more sensitive to changes in power supply than the Wilson Current Source with Simple Current Mirror equivalent. However, both topologies are expected to produce very similar results.

Figure 3.9 shows the circuit diagram of the WCS+BCM PTAT Current Generator used for simulation. As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V.

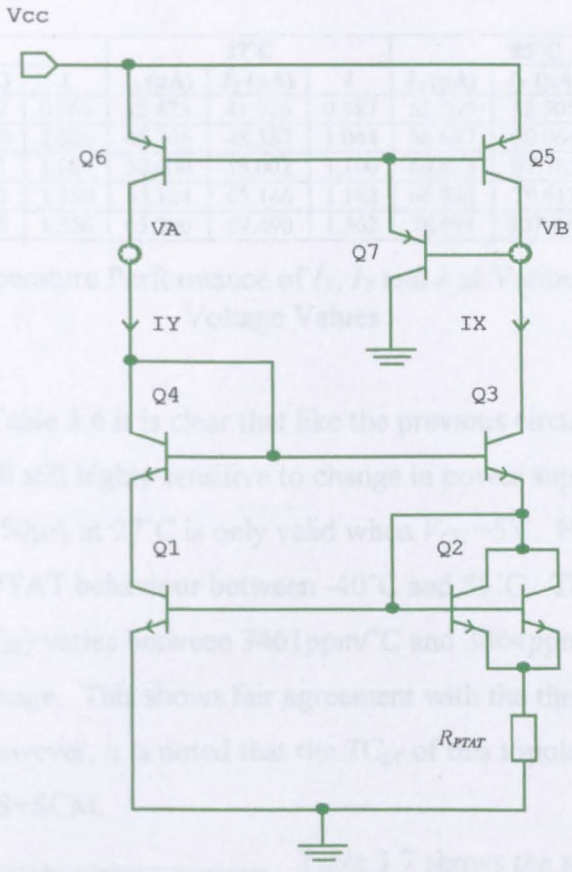

Figure 3.9 - Wilson Current Source + Buffered Current Mirror PTAT Current Generator

Table 3.6 shows the temperature performance of I_X, I_Y and λ at various power supply voltage values. The theoretical value of R_{PTAT} is given by:

$$R_{PTAT} = \frac{nV_T}{I_X} \ln \lambda m = \frac{1.094 \times 25.86mV}{50\mu A} \times \ln(1.076 \times 2) = 433.64\Omega \qquad (3.54)$$

However, the actual value of R_{PTAT} needed, in order that $I_X = 50\mu A$ at 27°C, was found to be 437.49Ω. Again, this can be attributed to the fact that the formula used in (3.54) is a rearrangement of the simplified equation found in (3.35). Using a rearrangement of (3.31) instead of (3.35) would lead to a more accurate result. However, this is much less straightforward. In addition, the theoretical value of $\lambda = 1.076$ at 27°C calculated previously is slightly less than the actual simulated value of $\lambda = 1.100$ at 27°C. Indeed, if $\lambda = 1.076$ is substituted with $\lambda = 1.100$ in (3.54) then the calculated value of R_{PTAT} becomes 446.12Ω which is much closer to the measured value of 437.49Ω.

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	(ppm/°C)
3	31.756	30.677	0.966	42.473	41.916	0.987	52.269	52.505	1.005	3864
4	34.923	35.819	1.026	46.346	48.387	1.044	56.687	60.064	1.060	3757
5	37.906	41.091	1.084	50.000	55.002	1.100	60.873	67.785	1.114	3675
6.5	42.056	49.172	1.169	55.124	65.146	1.182	66.762	79.613	1.192	3586
10	50.566	68.589	1.356	65.700	89.490	1.362	78.991	107.973	1.367	3461

Table 3.6 – Temperature Performance of I_X, I_Y and λ at Various Power Supply Voltage Values

From the results in Table 3.6 it is clear that like the previous circuit, I_X, I_Y and consequently λ are all still highly sensitive to change in power supply. Thus, the design value of $I_X = 50\mu A$ at 27°C is only valid when V_{CC}=5V. However, as expected I_X exhibits close to PTAT behaviour between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) varies between 3461ppm/°C and 3864ppm/°C across the 3V to 10V power supply range. This shows fair agreement with the theoretical value (3.9) of 3332 ppm/°C. However, it is noted that the TC_{IX} of this topology is slightly worse than that of the WCS+SCM.

Temperature (°C)	$S_{(WCS+BCM)}$ (ppm/V)
-40	63894
27	60194
85	57180

Table 3.7 - Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V)

Table 3.7 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V). The measured value of 60194ppm/V at 27°C demonstrates close agreement with the theoretical value of 59309ppm/V calculated in Section 3.2.5.b. However, as expected the measured sensitivity of I_X is in fact actually slightly worse than that of the WCS+SCM.

In summary, the WCS+BCM topology exhibits close to PTAT behaviour although the temperature coefficient is not as close to ideal as that of the WCS+SCM. Furthermore, the WCS+BCM suffers from the same practical shortcoming as the WCS+SCM. Namely, the output current I_X is poorly defined at power supply voltages other than that for which R_{PTAT} is trimmed. The only advantage that the WCS+BCM has over the WCS+SCM is a very small improvement in λ (i.e. λ is closer to unity).

3.2.4.1.c Wilson Current Source with Cascode Current Mirror (WCS+CCM)

From [13], the output resistance of a Cascode Current Mirror is given by:

$$R_{OUT} = \frac{\beta_P V_{AP}}{2I_Y} = \frac{\partial V_{OUT}}{\partial I_Y} \qquad (3.55)$$

Again, by replacing ∂V_{OUT} by ∂V_{CC} and rearranging the previous equation we obtain:

$$\frac{1}{I_Y}\frac{\partial I_Y}{\partial Vcc} = \frac{2}{\beta_P V_{AP}} \approx \frac{1}{\lambda}\frac{\partial \lambda}{\partial Vcc} \qquad (3.56)$$

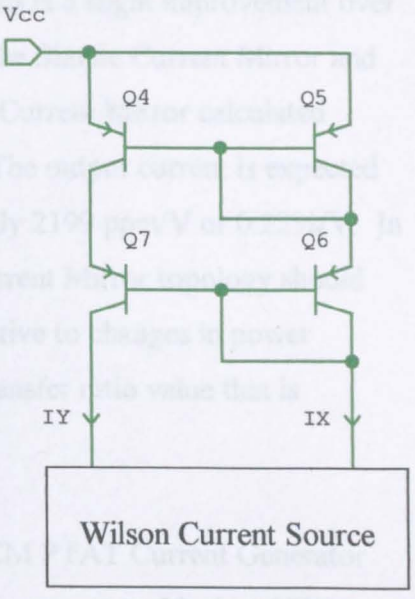

Figure 3.10 – Wilson Current Source with Cascode Current Mirror

By substituting (3.56) into (3.37), an expression for the sensitivity to changes in power supply of a Wilson Current Source with Cascode Current Mirror, as shown in Figure 3.10, is defined as:

$$S_{(WCS+CCM)} = \frac{2}{\beta_P V_{AP}}\left(\frac{1}{\ln \lambda m}\right) \qquad (3.57)$$

where the current transfer ratio, $\lambda = I_Y/I_X$, of a Cascode Current Mirror with equal emitter area ratios can be defined as:

$$\lambda = 1 - \frac{4\beta_P + 2}{\beta_P^2 + 4\beta_P + 2} \tag{3.58}$$

As before, using the measured device parameters (V_{EB}=0.85V, β_P=65.27, V_{BE}=0.81V and β_N=177), Spice model data (V_{AP}=22V and V_{AN}=63V) and selecting m=2 and V_{CC}=5V, it is possible to calculate the theoretical values for λ and $S_{(WCS+CCM)}$. These are presented in Table 3.8 below.

Parameters	Theoretical Values
λ	0.942
$S_{(WCS+CCM)}$	2199 ppm/V

Table 3.8 – Theoretical Values for a Wilson Current Source with Cascode Current Mirror

Table 3.8 illustrates that the current transfer ratio is expected to differ by 5.8% from the ideal case. This ia a slight improvement over that of both the Simple Current Mirror and the Buffered Current Mirror calculated previously. The output current is expected to vary by only 2199 ppm/V or 0.22%/V. In this case, the Wilson Current Source with Cascode Current Mirror topology should provide an output current that is significantly less sensitive to changes in power supply than both the previous circuits with a current transfer ratio value that is marginally closer to the ideal.

Figure 3.11 shows the circuit diagram of the WCS+CCM PTAT Current Generator used for simulation. As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V. The theoretical value of R_{PTAT} is given by:

$$R_{PTAT} = \frac{nV_T}{I_X} \ln \lambda m = \frac{1.094 \times 25.86mV}{50\mu A} \times \ln(0.942 \times 2) = 358.39\Omega \tag{3.59}$$

The actual value of R_{PTAT} needed, in order that I_X = 50μA at 27°C, was found to be 345.64Ω. This is fairly close to the theoretical value. A more accurate theoretical value could be obtained by using a rearrangement of (3.31) instead of (3.59), however, this is much less straightforward. Similarly, if the theoretical value of λ =0.942 at 27°C is replaced by the measured value of λ =0.937 at 27°C in (4.59) then

the calculated value of R_{PTAT} becomes 355.38Ω which is much closer to the measured value of 345.64Ω. Table 3.9 shows the temperature performance of I_X, I_Y and λ at various power supply voltage values.

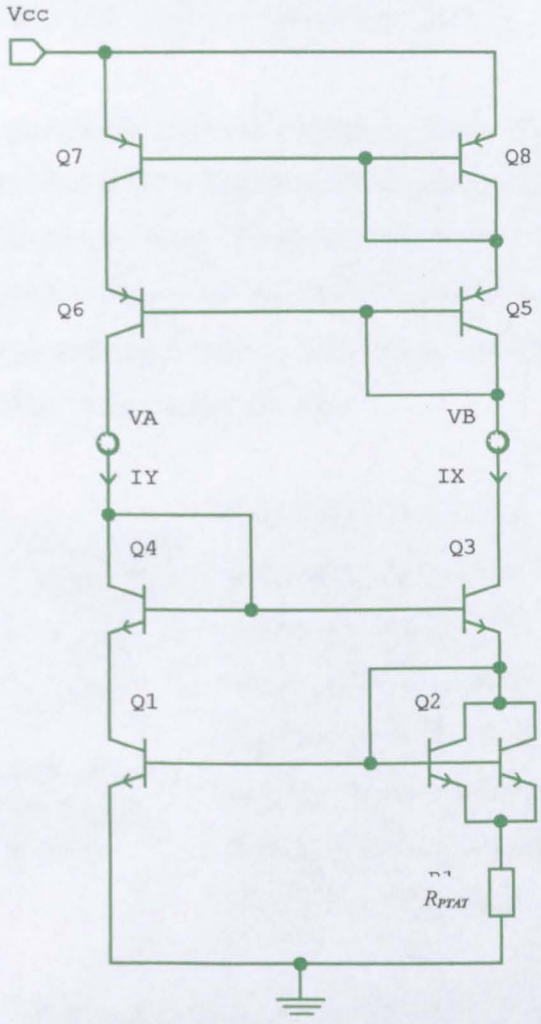

Figure 3.11 - Wilson Current Source + Cascode Current Mirror PTAT Current Generator

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	(ppm/°C)
3	38.109	35.435	0.930	49.560	46.249	0.933	59.624	55.803	0.936	3473
4	38.313	35.719	0.932	49.793	46.574	0.935	59.878	56.160	0.938	3465
5	38.484	35.959	0.934	50.000	46.865	0.937	60.108	56.483	0.940	3460
6.5	38.714	36.280	0.937	50.273	47.246	0.940	60.426	56.921	0.942	3455
10	39.132	36.862	0.942	50.781	47.955	0.944	60.981	57.702	0.946	3442

Table 3.9 – Temperature Performance of I_X, I_Y and λ at Various Power Supply Voltage Values (WCS+CCM)

I_X exhibits close to PTAT behaviour between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) varies between 3473 ppm/°C and 3442 ppm/°C across the 3V to 10V power supply range. This shows very close agreement with the theoretical value (3.9) of 3332 ppm/°C. Clearly in terms of temperature coefficient, this topology is superior to the WCS+SCM and WCS+BCM combinations.

Table 3.10 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V). The measured value of 3470 ppm/V at 27°C is larger than the theoretical value of 2199 ppm/V calculated previously. However, the difference between the theoretical and measured values is only 1271 ppm/V which is equivalent to 0.13 %/V. Obviously, this is a very small difference so it can be said that the measured result displays good agreement to the theoretical value.

Temperature (°C)	$S_{(WCS+CCM)}$ (ppm/V)
-40	3775
27	3470
85	3208

Table 3.10 - Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V)

In summary, the WCS+CCM topology demonstrates close to PTAT behaviour that is superior to that of both the WCS+SCM and WCS+BCM. Furthermore, the WCS+CCM is highly insensitive to fluctuations in the power supply voltage. Therefore, the output current I_X remains close to the design value over the entire (3V-10V) power supply voltage range.

3.2.4.1.d Wilson Current Source with Wilson Current Mirror (WCS+WCM)

The Wilson Current Mirror offers an improved transfer ratio over that of the Cascode Current Mirror by means of additional feedback [13], the output resistance of which is given by:

$$R_{OUT} = \frac{\beta_P V_{AP}}{2I_T} = \frac{\partial V_{OUT}}{\partial I_T} \qquad (3.60)$$

The output resistance is identical to that of the Cascode Current Mirror. Hence, following the same procedure as before, the sensitivity to changes in power supply of a Wilson Current Source with Wilson Current Mirror, as shown in Figure 3.12, is defined as:

$$S_{(WCS+WCM)} = \frac{2}{\beta_P V_{AP}} \left(\frac{1}{\ln \lambda m} \right) \qquad (3.61)$$

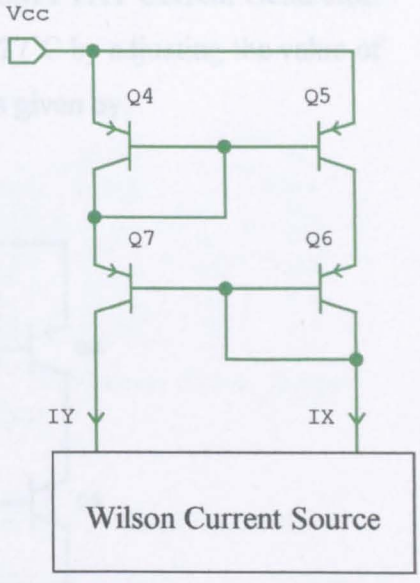

Figure 3.12 – Wilson Current Source with Wilson Current Mirror

where the current transfer ratio, $\lambda = I_Y/I_X$, of a Wilson Current Mirror with equal emitter area ratios can be defined as:

$$\lambda = 1 - \frac{2}{\beta_P^2 + 2\beta_P + 2} \qquad (3.62)$$

Again, using the measured device parameters (V_{EB}=0.85V, β_P=65.27, V_{BE}=0.81V and β_N=177), spice model data (V_{AP}=22V and V_{AN}=63V) and selecting m=2 and V_{CC}=5V, it is possible to calculate the theoretical values for λ and $S_{(WCS+WCM)}$. These are presented in Table 3.11 below.

Parameters	Theoretical Values
λ	0.9995
$S_{(WCS+CCM)}$	2011 ppm/V

Table 4.11 – Theoretical Values for a Wilson Current Source with Wilson Current Mirror

Table 3.5 illustrates that the current transfer ratio is expected to differ by only 0.05% from the ideal case! This is, in fact, significantly better than all the results calculated previously. Similarly, the output current is expected to vary by only 2011 ppm/V which equates to 0.2%/V. Thus, the Wilson Current Source with Wilson Current Mirror topology should be least sensitive to changes in power supply compared with the previous circuits, whilst, simultaneously providing a near unity current transfer ratio.

Figure 3.13 shows the circuit diagram of the WCS+WCM PTAT Current Generator. As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V. The theoretical value of R_{PTAT} is given by:

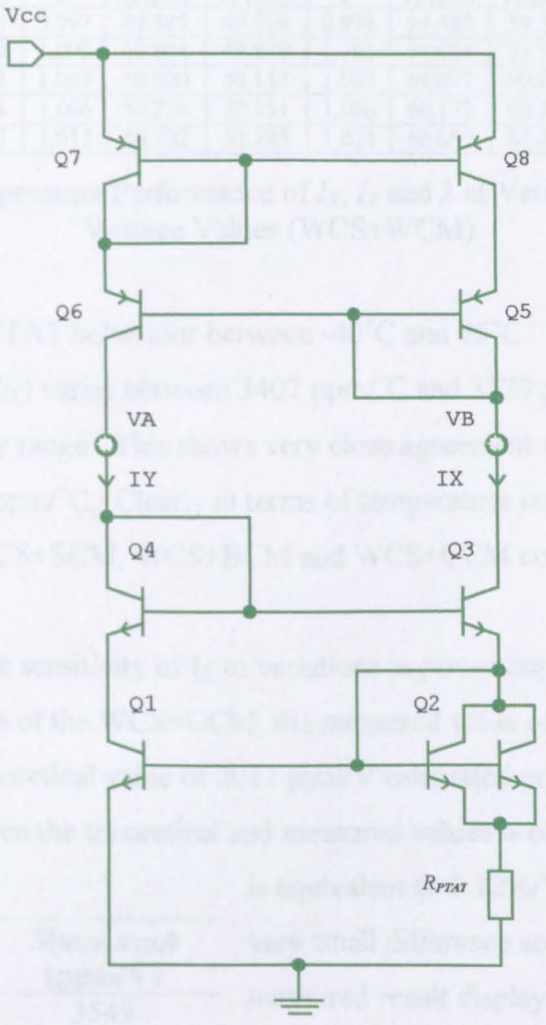

Figure 3.13 - Wilson Current Source + Wilson Current Mirror PTAT Current Generator

$$R_{PTAT} = \frac{nV_T}{I_X} \ln \lambda m = \frac{1.094 \times 25.86mV}{50\mu A} \times \ln(0.9995 \times 2) = 391.91\Omega \qquad (3.63)$$

The actual value of R_{PTAT} needed, in order that I_X = 50μA at 27°C, was found to be 384.38Ω. This small difference can largely be attributed to the fact that the formula used in (3.63) is a rearrangement of the simplified equation found in (3.35). Using a rearrangement of (3.31) instead of (3.35) would lead to a more accurate result.

Table 3.12 shows the temperature performance of I_X, I_Y and λ at various power supply voltage values.

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	(ppm/°C)
3	38.306	38.210	0.997	49.585	49.510	0.998	59.420	59.375	0.999	3407
4	38.492	38.480	1.000	49.804	49.849	1.001	59.684	59.772	1.001	3404
5	38.659	38.758	1.003	50.000	50.153	1.003	59.877	60.083	1.003	3395
6.5	38.875	39.094	1.006	50.256	50.551	1.006	60.173	60.536	1.006	3390
10	39.272	39.707	1.011	50.732	51.285	1.011	60.697	61.350	1.011	3379

Table 3.12 – Temperature Performance of I_X, I_Y and λ at Various Power Supply Voltage Values (WCS+WCM)

I_X exhibits close to PTAT behaviour between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) varies between 3407 ppm/°C and 3379 ppm/°C across the 3V to 10V power supply range. This shows very close agreement with the theoretical value (3.9) of 3332 ppm/°C. Clearly in terms of temperature coefficient, this topology is superior to the WCS+SCM, WCS+BCM and WCS+CCM combinations.

Table 3.13 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V). As in the case of the WCS+CCM, the measured value of 3260 ppm/V at 27°C is larger than the theoretical value of 2011 ppm/V calculated previously. However, the difference between the theoretical and measured values is only 1249 ppm/V which is equivalent to 0.12%/V. Obviously, this is a very small difference so it can be said that the measured result displays good agreement to the theoretical value. In addition, the sensitivity of I_X of this circuit is marginally better than that of the WCS+CCM. This is due to the improvement in λ (i.e. λ is closer to unity).

Temperature (°C)	$S_{(WCS+WCM)}$ (ppm/V)
-40	3549
27	3260
85	3032

Table 3.15 - Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V)

In summary, the WCS+WCM topology demonstrates close to PTAT behaviour that is superior to that of the WCS+SCM, WCS+BCM and WCS+CCM. Furthermore, the WCS+CCM is marginally more insensitive to variations in the power supply voltage

than the WCS+CCM. Thus, the output current, I_X, remains even closer to the design value over the entire (3V-10V) power supply voltage range.

3.2.4.1.e Wilson Current Source with Voltage Following Current Mirror (WCS+VFCM)

Figure 3.14 illustrates the Wilson Current Source with Voltage Following Current Mirror combination. The current transfer ratio of the Voltage Following Current Mirror, first proposed by Barker and Hart [14], is given by:

$$\lambda = \frac{1 - \frac{2}{\beta_N \beta_P} + \frac{1}{\beta_P}}{1 + \frac{1}{\beta_P}} \qquad (3.64)$$

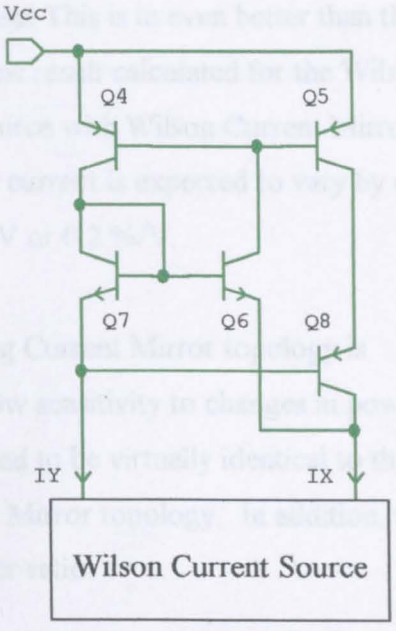

Figure 3.14 – Wilson Current Source with Voltage Following Current Mirror

The expression above can then be differentiated with respect to V_{CC} and multiplied by the reciprocal of (3.64) to give:

$$\frac{1}{\lambda}\frac{\partial \lambda}{\partial V_{CC}} = \frac{2}{\beta_P V_{AP}} + \frac{2}{\beta_P \beta_N}\left(\frac{1}{V_{AN}} + \frac{1}{V_{AP}}\right) \qquad (3.65)$$

By substituting (3.65) into (3.37), an expression for the sensitivity to changes in power supply of a Wilson Current Source with Voltage Following Current Mirror can be defined as:

$$S^{(WCS+VFCM)} = \left[\frac{2}{\beta_P V_{AP}} + \frac{2}{\beta_P \beta_N}\left(\frac{1}{V_{AN}} + \frac{1}{V_{AP}}\right)\right]\left(\frac{1}{\ln \lambda m}\right) \qquad (3.66)$$

Again, using the measured device parameters (V_{EB}=0.85V, β_P=65.27, V_{BE}=0.81V and β_N=177), Spice model data (V_{AP}=22V and V_{AN}=63V) and selecting m=2 and V_{CC}=5V, it is possible to calculate the theoretical values for λ and $S_{(WCS+VFCM)}$. These are presented in Table 3.16 below.

Parameters	Theoretical Values
λ	0.9998
$S_{(WCS+VFCM)}$	2025 ppm/V

Table 3.16 – Theoretical Values for a Wilson Current Source with Voltage Following Current Mirror

Table 3.16 illustrates that the current transfer ratio is expected to differ by only 0.02% from the ideal case! This is in even better than the previous best result calculated for the Wilson Current Source with Wilson Current Mirror. The output current is expected to vary by only 2025 ppm/V or 0.2 %/V.

The Wilson Current Source with Voltage Following Current Mirror topology is expected to offer an output current that has very low sensitivity to changes in power supply. In fact the degree of insensitivity is expected to be virtually identical to that of the Wilson Current Source with Wilson Current Mirror topology. In addition, this circuit should provide a near perfect current transfer ratio.

Figure 3.15 shows the circuit diagram of the WCS+VFCM PTAT Current Generator for simulation. As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V. The theoretical value of R_{PTAT} is given by:

$$R_{PTAT} = \frac{nV_T}{I_X} \ln \lambda m = \frac{1.094 \times 25.86mV}{50\mu A} \times \ln(0.9998 \times 2) = 392.08\Omega \qquad (3.67)$$

However, the actual value of R_{PTAT} needed, in order that I_X = 50μA at 27°C, was found to be 384.99Ω. Again, This small difference can largely be attributed to the fact that the formula used in (3.67) is a rearrangement of the simplified equation found in (3.35). Using a rearrangement of (3.31) instead of (3.35) would lead to a more accurate result. Table 3.17 shows the temperature performance of I_X, I_Y and λ at various power supply voltage values.

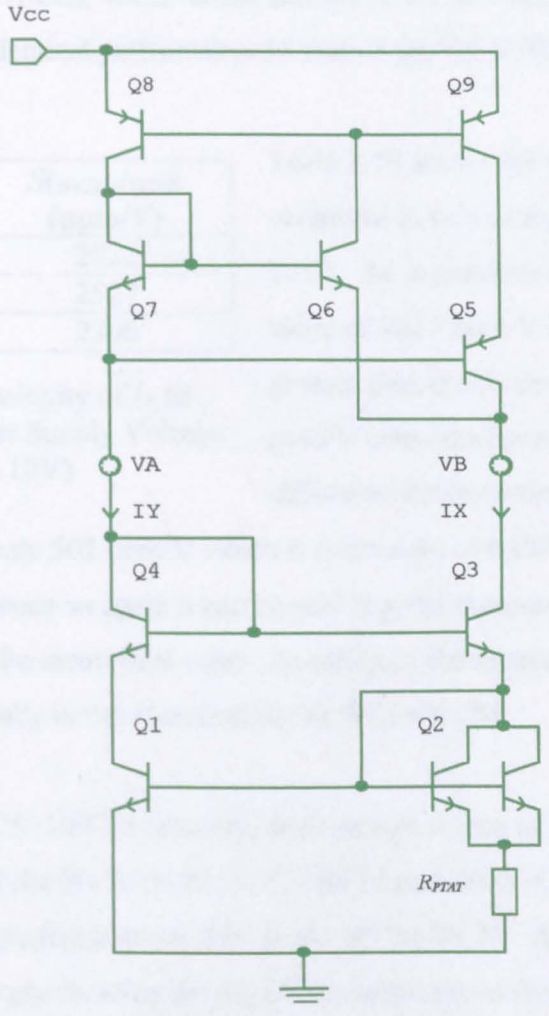

Figure 3.15 - Wilson Current Source + Voltage Following Current Mirror PTAT Current Generator

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(µA)	I_Y(µA)	λ	I_X(µA)	I_Y(µA)	λ	I_X(µA)	I_Y(µA)	λ	(ppm/°C)
3	38.367	38.339	0.999	49.670	49.693	1.000	59.525	59.605	1.001	3408
4	38.520	38.588	1.002	49.846	49.980	1.003	59.715	59.916	1.003	3402
5	38.655	38.809	1.004	50.000	50.234	1.005	59.882	60.191	1.005	3396
6.5	38.826	39.092	1.007	50.200	50.562	1.007	60.100	60.549	1.007	3390
10	39.134	39.599	1.012	50.558	51.155	1.012	60.495	61.201	1.012	3380

Table 3.17 – Temperature Performance of I_X, I_Y and λ at Various Power Supply Voltage Values (WCS+VFCM)

I_X demonstrates close to PTAT behaviour between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) varies between 3408ppm/°C and 3380ppm/°C across the 3V to 10V power supply range. This shows very close agreement with the theoretical value (3.9) of 3332 ppm/°C. Clearly in terms of temperature coefficient, this topology is

superior to the WCS+SCM, WCS+BCM and WCS+CCM combinations whilst offering practically identical performance to that of the WCS+WCM.

Temperature (°C)	$S_{(WCS+VFCM)}$ (ppm/V)
-40	2822
27	2527
85	2306

Table 3.18 - Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V)

Table 3.18 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V). As in previous cases, the measured value of 2527 ppm/V at 27°C is slightly greater than the theoretical value of 2025 ppm/V calculated previously. However, the difference between the theoretical and measured values is only 502 ppm/V which is equivalent to 0.05%/V. Obviously, this is a very small difference so again it can be said that the measured result displays good agreement to the theoretical value. In addition, the measured sensitivity of I_X for this circuit is marginally better than that of the WCS+WCM.

In summary, the WCS+VFCM topology demonstrates close to PTAT behaviour that is superior to that of the WCS+SCM, WCS+BCM and WCS+CCM whilst offering practically identical performance to that of the WCS+WCM. Additionally, the WCS+VFCM is marginally more insensitive to variations in the power supply voltage than the WCS+WCM. Thus, the output current I_X remains even closer to the design value over the entire (3V-10V) power supply voltage range.

3.2.4.1.f Buffered Widlar Current Source with Voltage Following Current Mirror (BWCS+VFCM)

In Section 3.2.2 it was shown that the output current of the Buffered Widlar Current Source suffers from errors due to V_{CE} mismatches (i.e. $V_{CE1} \neq V_{CE2}$). The output current equation (3.25) is repeated, for the benefit of the reader, below:

$$I_{out} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\ln\left[\left[\frac{\left(\frac{I_{in}}{1+[1/\beta_1(\beta_3+1)]}-\frac{I_{out}}{\beta_2[(\beta_3+1)+1/\beta_1]}\right)}{I_{out}}\frac{I_{S2}}{I_{S1}}\right]+\frac{V_{CE2}-V_{CE1}}{V_{AN}}\right] \quad (3.68)$$

If V_{CE1} and V_{CE2} are well matched (i.e. $V_{CE1} = V_{CE2}$) then (3.68) will simplify to give:

$$I_{out} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\ln\left[\frac{\left(\frac{I_{in}}{1+[1/\beta_1(\beta_3+1)]}-\frac{I_{out}}{\beta_2[(\beta_3+1)+1/\beta_1]}\right)}{I_{out}}\frac{I_{S2}}{I_{S1}}\right] \quad (3.69)$$

Now provided the following conditions are met, namely $\beta_N >> I_{out}$ and $\beta_N >> 1$, (3.69) will give a highly accurate result that is close to the ideal equation (3.19). However, this simplification is subject to the condition $V_{CE1} = V_{CE2}$. Fortunately, this condition can be ensured via use of a Voltage Following Current Mirror. Figure 3.16 illustrates the Wilson Current Source with Voltage Following Current Mirror combination.

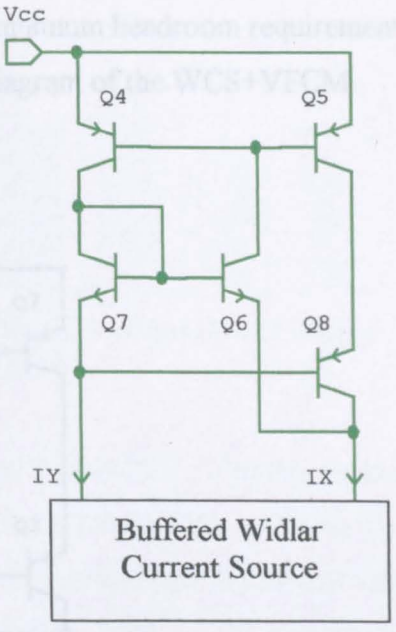

Figure 3.16 – Buffered Widlar Current Source with Voltage Following Current Mirror

The current transfer ratio, λ, of this configuration is given as [4]:

$$\lambda = 1+\frac{2}{\beta P}-\left[\left(1+\frac{1}{\beta N}\right)\frac{2}{\beta P}\right] \quad (3.70)$$

Similarly, an expression for the sensitivity to changes in power supply of a Buffered Widlar Current Source with Voltage Following Current Mirror can be defined as [4]:

$$S(_{BWCS+VFCM}) = \left[\frac{2}{\beta_P V_{AP}}+\frac{2}{\beta_P \beta_N}\left(\frac{1}{V_{AN}}+\frac{1}{V_{AP}}+\frac{V_T}{V_{AN}V_{AP}}\right)\right]\left(\frac{1}{\ln \lambda m}\right) \quad (3.71)$$

Again, using the measured device parameters (V_{EB}=0.85V, β_P=65.27, V_{BE}=0.81V and β_N=177), Spice model data (V_{AP}=22V and V_{AN}=63V) and selecting m=2 and V_{CC}=5V, it is possible to calculate the theoretical values for λ and $S_{(BWCS+VFCM)}$. These are presented in Table 3.19 below.

Parameters	Theoretical Values
λ	0.9998
$S_{(BWCS+VFCM)}$	2025 ppm/V

Table 3.19 – Theoretical Values for a Buffered Widlar Current Source with Voltage Following Current Mirror

Table 3.19 illustrates that this configuration should offer identical results to that of the Wilson Current Source with Voltage Following Current Mirror in terms of current transfer ration and power supply sensitivity. However, this configuration should operate at lower supply voltages than the previous circuit because the minimum headroom requirement is one V_{BE} drop less. Figure 3.17 shows the circuit diagram of the WCS+VFCM PTAT Current Generator used for simulation.

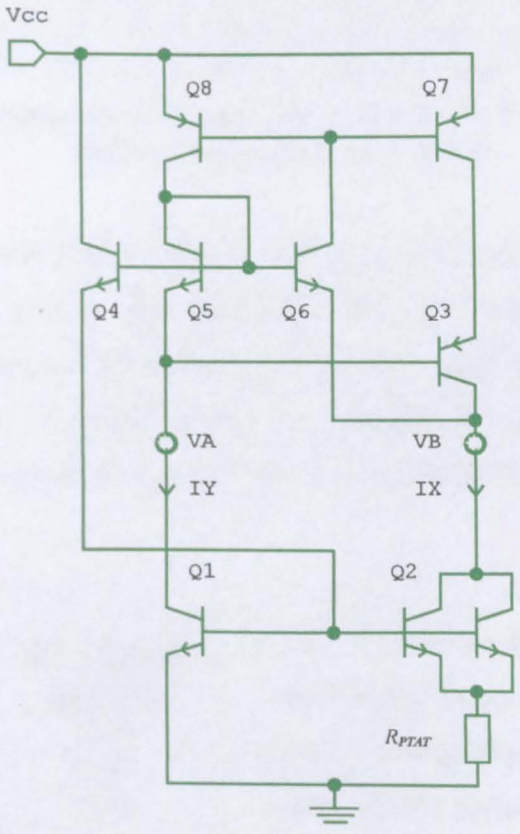

Figure 3.17 – Buffered Widlar Current Source with Voltage Following Current Mirror

As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V. The theoretical value of R_{PTAT} is given by:

$$R_{PTAT} = \frac{nVT}{Ix} \ln \lambda m = \frac{1.094 \times 25.86mV}{50\mu A} \times \ln(0.9998 \times 2) = 392.08\Omega \qquad (3.72)$$

However, the actual value of R_{PTAT} needed, in order that I_X = 50μA at 27°C, was found to be 384.86Ω. Again, This small difference can largely be attributed to the fact that the formula used in (3.72) is a rearrangement of the simplified equation found in (3.35). Using a rearrangement of (3.31) instead of (3.35) would lead to a more accurate result. Table 3.20 shows the temperature performance of I_X, I_Y and λ at various power supply voltage values.

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	(ppm/°C)
3	38.389	38.453	0.998	49.706	49.830	0.998	59.580	59.764	0.997	3411
4	38.522	38.673	0.996	49.862	50.086	0.996	59.751	60.044	0.995	3406
5	38.640	38.866	0.994	50.000	50.313	0.994	59.904	60.293	0.994	3402
6.5	38.793	39.119	0.992	50.181	50.610	0.992	60.104	60.622	0.991	3397
10	39.069	39.575	0.987	50.510	51.152	0.987	60.471	61.227	0.988	3390

Table 3.20 – Temperature Performance of I_X, I_Y and λ at Various Power Supply Voltage Values (BWCS+VFCM)

I_X demonstrates close to PTAT behaviour between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) varies between 3411ppm/°C and 3390ppm/°C across the 3V to 10V power supply range. This shows very close agreement with the theoretical value (3.9) of 3332 ppm/°C. However, in terms of temperature coefficient, this topology offers marginally worse performance to that of both the WCS+WCM and WCS+VFCM.

Temperature (°C)	$S_{(BWCS+VFCM)}$ (ppm/V)
-40	2504
27	2289
85	2118

Table 3.21 - Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V)

Table 3.21 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V). As in previous cases, the measured value of 2289 ppm/V at 27°C is slightly greater than the theoretical value of 2025 ppm/V calculated previously. However, the

difference between the theoretical and measured values is only 264 ppm/V which is equivalent to 0.0264%/V. Obviously, this is a very small difference so again it can be said that the measured result displays good agreement to the theoretical value. In addition, the measured sensitivity of I_X for this circuit is 238 ppm/V better than that of the WCS+VFCM (the previous least sensitive circuit topology).

In summary, the BWCS+VFCM topology demonstrates close to PTAT behaviour that is superior to that of the WCS+SCM, WCS+BCM and WCS+CCM whilst offering practically identical performance to that of both the WCS+WCM and WCS+VFCM.

Additionally, the BWCS+VFCM is marginally more insensitive to variations in the power supply voltage than the WCS+VFCM. Thus, the output current I_X remains even closer to the design value over the entire (3V-10V) power supply voltage range.

3.2.4.2 Circuit Performance Comparison

Table 3.22 summarises the temperature coefficient of I_X that was measured for each circuit topology.

V_{CC} (V)	TC_{IX} ($_{IDEAL}$) (ppm/°C)	TC_{IX} ($_{WCS+SCM}$) (ppm/°C)	TC_{IX} ($_{WCS+BCM}$) (ppm/°C)	TC_{IX} ($_{WCS+CCM}$) (ppm/°C)	TC_{IX} ($_{WCS+WCM}$) (ppm/°C)	TC_{IX} ($_{WCS+VFCM}$) (ppm/°C)	TC_{IX} ($_{BWCS+VFCM}$) (ppm/°C)
3	3332	3716	3864	3473	3407	3408	3411
5	3332	3545	3675	3460	3395	3396	3402
10	3332	3364	3461	3442	3379	3380	3390

Table 3.22 – Temperature Coefficient of I_X for Each Circuit Topology

The WCS+SCM topology offers a temperature coefficient of 3364 ppm/°C when V_{CC} =10V which is very close to the ideal of 3332 ppm/°C. However, TC_{IX} deviates grossly from this initial value by 181 ppm/°C when V_{CC}=5V and 352 ppm/°C when V_{CC}=3V! Clearly, TC_{IX} is significantly power supply dependent for the WCS+SCM topology. This is also true, albeit to an even worse extent, of the WCS+BCM topology. The WCS+CCM offers improved sensitivity of TC_{IX} to changes in power supply voltage.

However, the actual 'best-case' value of TC_{IX}, measured when V_{CC}=10V, is still 110 ppm/°C larger than the ideal value. Both the WCS+WCM and WCS+VFCM combinations offer virtually identical and superior performance in terms of TC_{IX}. The total change in TC_{IX} across the 3V to 10V power supply range is only 28 ppm/°C. In addition, the actual 'best-case' value of TC_{IX} differs by only 47 ppm/°C from the ideal whilst the 'worst-case' value of TC_{IX} differs by only 75 ppm/°C! The BWCS+VFCM combination offers performance in terms of TC_{IX} that is marginally worse than but still very close to that of both the WCS+WCM and WCS+VFCM combinations.

Table 3.23 illustrates the sensitivity of I_X to changes in V_{CC} for each circuit topology. From the table it is clear that, in the case of the WCM+SCM and WCS+BCM topologies, I_X is highly sensitive to V_{CC}. This results in a poorly defined current at power supply voltages other than that for which R_{PTAT} is trimmed.

Temperature (°C)	$S_{(WCS+SCM)}$ (ppm/V)	$S_{(WCS+BCM)}$ (ppm/V)	$S_{(WCS+CCM)}$ (ppm/V)	$S_{(WCS+WCM)}$ (ppm/V)	$S_{(WCS+VFCM)}$ (ppm/V)	$S_{(BWCS+VFCM)}$ (ppm/V)
-40	62420	63894	3775	3549	2822	2504
27	59286	60194	3470	3260	2527	2289
85	56700	57180	3208	3032	2306	2118

Table 3.23 – Measured Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V) for Each Circuit Topology

The WCS+CCM, WCS+WCM and WCS+VFCM combinations offer improved performance. However, the BWCS+VFCM topology is least sensitive to changes in V_{CC}. Thus, the output current I_X remains very close to the design value over the entire (3V-10V) power supply voltage range. In summary, the BWCS+VFCM achieves the best overall performance using the 'Bootstrap-Bias Technique'.

3.2.4.3 Start-Up Circuit Development

Fundamentally, all of the previously described circuits used for generating a PTAT current operate by ensuring that the input current is made to depend upon the output current. This concept is shown in Figure 3.18. The relationship between I_{IN} and I_{OUT} is governed by the 'Widlar type' current source and

the current transfer ratio of the current mirror. From the point of view of the 'Widlar type' current source, I_{OUT} is almost independent of I_{IN} for a wide range of input

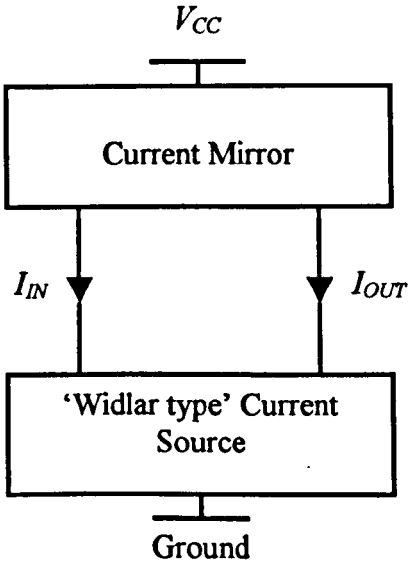

Figure 3.18 – Block Diagram of a 'Bootstrap Biased' Circuit

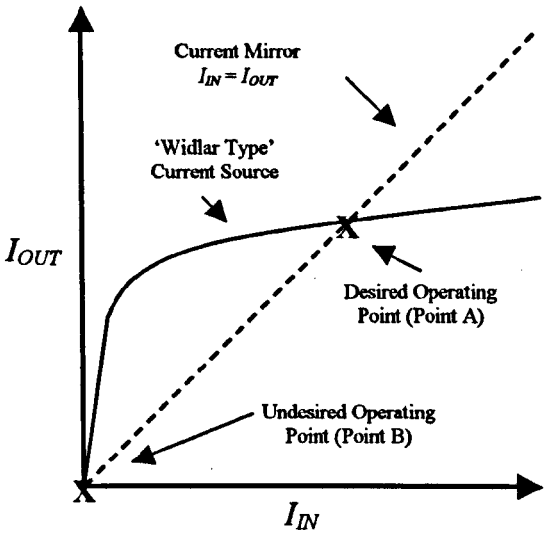

Figure 3.19 – Possible Operating Points of a 'Bootstrap Biased' Circuit

currents as shown in Figure 3.19. From the point of view of the output current current, $I_{IN} = I_{OUT}$ assuming the current mirror transfer ratio is set to unity. Therefore, the operating point of these circuits must satisfy both constraints simultaneously and hence is the intersection of the two characteristics [15]. Figure 3.19 also demonstrates two possible operating points. Point A is the desired operating point and Point B is the undesired operating point where $I_{IN} = I_{OUT} = 0$. Thus, unless precautions are taken the circuit may operate in the zero-current condition! This zero-current state can be avoided by employing a 'start-up circuit' to ensure that some current always flows in the transistors of the PTAT reference circuit. However, the start-up circuit should not interfere with the normal operation of the PTAT reference circuit once the desired operating condition is reached.

A start-up circuit, based on previous work by Hart and Barker [16], adapted for use with the BWCS+VFCM circuit is shown in Figure 3.20. This circuit, with minor alterations, is suitable for use with all of the previously mentioned PTAT current generator circuits described in this chapter. Circuit operation is as follows.

R_{START2}, Q_9 and Q_{10} form a 'Bipolar Peaking Current Source' [17]. The purpose of which is to provide a small output current, $I_{STARTOUT}$, that is in the order of a few μA. In this case Q_9 and Q_{10} are assumed identical, therefore, $I_{STARTOUT}$ is given by the well-known equation:

$$I_{STARTOUT} = I_{STARTIN}.e^{\left(-\frac{ISTARTIN.RSTART2}{VT}\right)} \tag{3.73}$$

When the power supply (V_{CC}) is turned on, $I_{STARTOUT}$ charges the effective capacitance associated with the collector circuit of Q_{11} until the emitter of the diode connected transistor Q_{12} becomes two junction drops below V_{CC}. Conduction current now flows from the bases of Q_7 and Q_8 (turning them on) through the diode Q_{12}. Current can now flow, via the collector of Q_8, into the bases of Q_4, Q_5 and Q_6, thus, also turning them on. This in turn allows current flow in the remaining devices, thus, having the effect of 'starting-up' the PTAT generator circuit and driving it into the desired point of operation.

Now, the steady 'on' current of Q_4 is approximately equal to $(I_X + I_Y) / (\beta_N + 1)$. This flows from the base of Q_{11} causing it to saturate and, in turn, forcing Q_{12} to become reverse biased provided that:

$$\beta_P(sat) > \left(\frac{I_{STARTOUT}}{Ix + Ir}\right)(\beta_N + 1) \tag{3.74}$$

Thus, the diode formed by Q_{13} is now turned off which in turn disconnects the 'start-up circuit' from the PTAT current generator.

This 'start up circuit' is particularly efficient because Q_4 is used for the dual purpose of (a) providing the base currents of Q_1 and Q_2 whilst also ensuring that (b) the 'start-up circuit' becomes disconnected from the PTAT generator under normal operating conditions. When desired operating point is reached and the 'start-up circuit' is disconnected, zero current should flow through the diode formed by Q_{12}. Thus, $I_{STARTDIODE} \leq 0$. This is proved via the simulation results shown in Table 3.24.

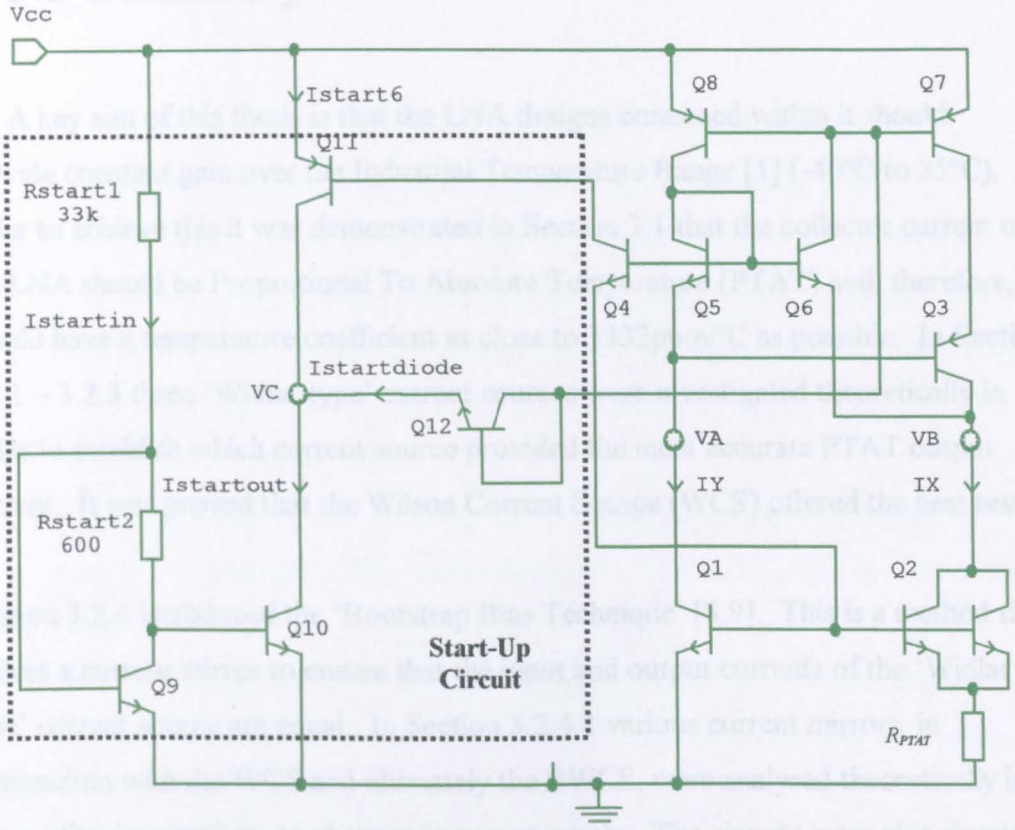

Figure 3.20 – BWCS+VFCM PTAT Current Generator Circuit with Start-Up Circuit

V_{CC} (V)	$I_{STARTDIODE}$ (-40°C) (pA)	$I_{STARTDIODE}$ (27°C) (pA)	$I_{STARTDIODE}$ (85°C) (pA)
3	-39.6	-41.4	-43.2
5	-94.5	-97.1	-99.6
10	-353.6	-359.5	-364.7

Table 3.24 – Current Flow Through Q_{12} After the Desired Operating Point is Reached

3.3 Summary

A key aim of this thesis is that the LNA designs contained within it should provide constant gain over the Industrial Temperature Range [1] (-40°C to 85°C). In order to achieve this it was demonstrated in Section 3.1 that the collector current of the LNA should be Proportional To Absolute Temperature (PTAT) and, therefore, should have a temperature coefficient as close to 3332ppm/°C as possible. In Sections 3.2.1 – 3.2.3 three 'Widlar type' current sources were investigated theoretically in order to establish which current source provided the most accurate PTAT output current. It was proved that the Wilson Current Source (WCS) offered the best results.

Section 3.2.4 introduced the 'Bootstrap Bias Technique' [8,9]. This is a method that utilises a current mirror to ensure that the input and output currents of the 'Widlar type' current source are equal. In Section 3.2.4.1 various current mirrors, in conjunction with the WCS and ultimately the BWCS, were analysed theoretically in terms of their sensitivity to changes in power supply. The circuits were also simulated using the software package APLAC. It was found that the BWCS+VFCM topology provided an accurate output current that exhibited close to ideal PTAT behaviour compared with the other 'Bootstrap Bias' circuits. Furthermore, the BWCS+VFCM topology also produced the output current that exhibited the highest degree of insensitivity to changes in the power supply voltage. This meant that the output current remained close to the nominal design value over the entire (3V-10V) power supply voltage range.

Finally Section 3.4 discussed the need for a 'start-up circuit' in order to ensure that all 'Bootstrap Bias' type circuits are driven out of the undesired operating condition $I_{IN} = I_{OUT} = 0$. One such circuit is presented that with minor alterations, is suitable for use with all of the previously mentioned PTAT current generator circuits described in this chapter.

3.4 References

[1] Temperature Range Standards, Retrieved 6th April, 2006, from http://www.interfacebus.com/Logic_Prefix_Temp_Range.html

[2] R. J. Widlar, 'Some Circuit Design Techniques for Linear Integrated Circuits', *IEEE Trans. Circuit Theory*, vol. CT-12, Dec. 1965, pp. 586-590.

[3] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 299-301.

[4] R. W. J Barker and B. L. Hart, 'Low-Voltage Rail-Supply-Insensitive PTAT current Generator', *IEE Proceedings Part G*, Vol. 131, No. 6, Dec. 1984, pp. 242-244.

[5] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 314.

[6] A. S. Sedra and K. C. Smith, *Microelectronic Circuits (Fifth Edition)*, Oxford University Press, Oxford, 2004, pp. 651-652.

[7] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 274-277.

[8] T. J. Van Kessel and R. J. Van der Plaasche, 'Integrated Linear Basic Circuits', *Phillips Technical Review*, Vol. 32, 1971, pp. 1-12.

[9] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 309-317.

[10] Welwyn, '*Precision Surface Mount Resistor: PCF Series*', Welwyn Components Ltd., Bedlington, Northumberland NE22 &AA, UK, Issue C, February 2004.

[11] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 255-257.

[12] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 260-262.

[13] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 263-266.

[14] R. W. J Barker and B. L. Hart, 'Modified Current Mirror with a Voltage Following Capability', *Electronic Letters*, Vol. 18, No. 22, Oct. 1982, pp. 970-972.

[15] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 309-311.

[16] B.L. Hart and R.W.J. Barker, 'Automatic Start-up Technique for Complementary PTAT Current Generators', *Electronics Letters*, 1982, 18, pp. 776-777.

[17] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 303-304.

CHAPTER 4

Improved Constant Gain Bias Circuit Techniques

The previously discussed 'Bootstrap Bias Technique' depends on a current mirror to force the input and output currents of a 'Widlar' type current source to be equal. As seen in Chapter 3, these circuits are inherently power supply dependent, thus, they exhibit output current inaccuracies. In order to improve performance it is necessary to improve the current mirror performance.

Chapter 4 concerns the investigation and analysis of a novel alternative circuit technique that can be used to bias the LNA of Chapter 1 in such a way that constant gain is achieved over a wide temperature range. A comparison of two circuit variations is conducted; particularly with regards to the temperature coefficient and sensitivity of the output current to power supply variations. These results are compared with those obtained using the 'Bootstrap Bias Technique' in Chapter 3.

4.1 An Improved PTAT Current Reference Circuit

In 1985 Nauta and Nordholt [1] proposed a new class of PTAT Current Generator that avoided the use of current mirrors, thereby alleviating the pain of improving their performance. Instead, two identical current sources are used in-place of a current mirror. These current sources are controlled via a simple loop amplifier so that equal bias conditions are maintained with large changes in power supply voltage. Although they presented impressive performance figures for this configuration, Nauta and Nordholt gave no theoretical analysis. This is done in the sections that follow.

4.1.1 Basic Nauta and Nordholt (BNN) Circuit

A basic implementation of this improved class of PTAT current reference circuit is shown in Figure 4.1. Circuit operation is as follows. A single transistor Q_3 in common emitter configuration forms a simple loop amplifier. This amplifier forces equal currents through Q_1 and Q_6 by sensing any difference in these currents and feeding it back to the current sources Q_5 and Q_6. Q_1 and Q_2 have identical collector-

base voltages, as do Q_5 and Q_6. Thus, it follows that the collector currents of Q_5 and Q_6 are equal. This in turn means that the collector currents of Q_1 and Q_2 are also equal which provides the necessary condition for the output current to be completely determined by any difference between V_{BE1} and V_{BE2}. Thus:

$$I_{out} = I_X = \frac{V_T}{R_1} \ln \lambda m \tag{4.1}$$

This result is identical to the simplified expression (3.19) derived for the output current of a 'bootstrap-bias' type circuit.

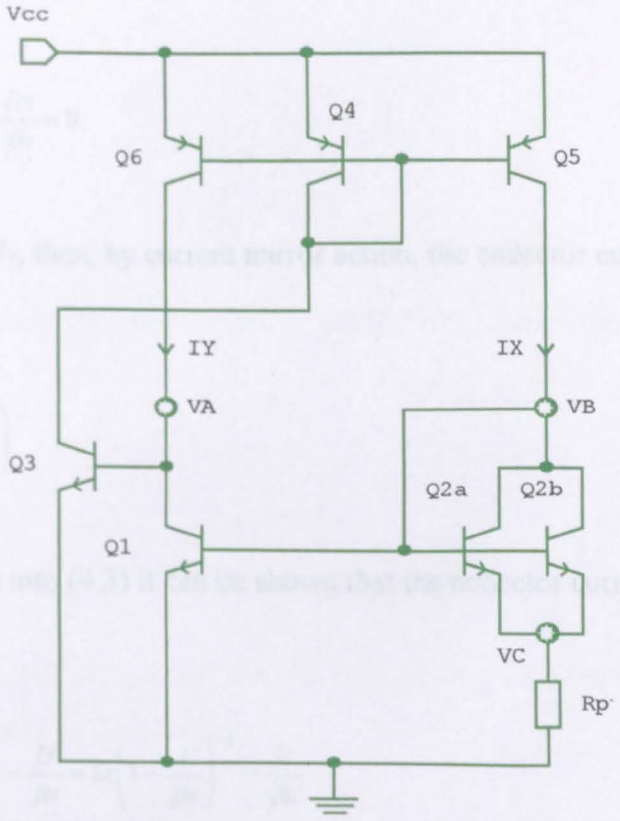

Figure 4.1 – Basic Implementation of the Nauta and Nordholt PTAT Current Generator

4.1.1.1 Theoretical Sensitivity of the BNN to Power Supply Voltage Variations and Observed Simulation Results

It is useful to derive an expression for the sensitivity of the basic implementation to changes in the power supply voltage. Referring to Figure 4.1, it can be said that:

$$Ir - Ic1 - \frac{Ic3}{\beta N} = 0 \tag{4.2}$$

and:

$$Ix - Ic2 - \frac{Ic2}{\beta N} - \frac{Ic1}{\beta N} = 0 \tag{4.3}$$

Assuming that $I_{C3} \approx I_Y$, then, by current mirror action, the collector current of Q_1 is given by:

$$Ic1 \approx Ir\left(1 - \frac{1}{\beta N}\right) \tag{4.4}$$

By substituting (4.4) into (4.3) it can be shown that the collector current of Q_2 is given by:

$$Ic2 = \frac{Ix}{\left(1 - \frac{1}{\beta N}\right)} - \frac{Ir}{\beta N} = Ix\left(1 - \frac{1}{\beta N}\right)^{-1} - \frac{Ir}{\beta N} \tag{4.5}$$

Since it has already been stated in the previous section that the collector currents of Q_5 and Q_6 are equal (i.e. $I_Y \approx I_X$), then, it is fair to say that:

$$Ic2 \cong Ix \tag{4.6}$$

Applying KVL around the base-emitter loop of Q_1 and Q_2, bearing in mind the simplification made in (4.6), it is clear that:

$$V_{BE1} - V_{BE2} - \frac{\beta_N + 1}{\beta_N} I_X R_1 = 0 \tag{4.7}$$

A common identity for collector current [2] is shown below:

$$I_C = I_S\left(1 + \frac{V_{CE}}{V_A}\right)e^{\left(\frac{V_{BE}}{V_T}\right)} \tag{4.8}$$

Using a rearrangement of (4.8), it can be shown that:

$$V_{BE1} - V_{BE2} = \frac{\beta_N + 1}{\beta_N} I_X = \Delta V = V_T \ln\left[m\left(\frac{I_{C1}}{I_{C2}}\right)\frac{\left(1 + \frac{V_{CE2}}{V_A}\right)}{\left(1 + \frac{V_{CE1}}{V_A}\right)}\right] \tag{4.9}$$

where $m = I_{S2}/I_{S1}$. Using the results of (4.4) and (4.6), the I_{C1}/I_{C2} term can be rewritten as:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_Y\left(1 - \frac{1}{\beta_N}\right)}{I_X} \tag{4.10}$$

Using the previously defined identity (4.8) for collector current, and applying it to the case of a PNP transistor, it follows that:

$$I_X = I_{S5}\left(1 + \frac{V_{EC5}}{V_{AP}}\right)e^{\left(\frac{V_{EB5}}{V_T}\right)} \tag{4.11}$$

$$I_Y = I_{S6}\left(1 + \frac{V_{EC6}}{V_{AP}}\right)e^{\left(\frac{V_{EB6}}{V_T}\right)} \tag{4.12}$$

Therefore, (4.10) can be rewritten as:

$$\frac{Ic1}{Ic2}=\frac{Is6\left(1+\frac{VEC6}{VAP}\right)\left(1-\frac{1}{\beta N}\right)e^{\left(\frac{VEB6}{VT}\right)}}{Is5\left(1+\frac{VEC5}{VAP}\right)e^{\left(\frac{VEB5}{VT}\right)}} \tag{4.13}$$

This result can now be substituted into (4.9) to give:

$$\Delta V=VT\ln\left[m\frac{Is6\left(1+\frac{VEC6}{VAP}\right)\left(1-\frac{1}{\beta N}\right)\left(1+\frac{VCE2}{VAN}\right)}{Is5\left(1+\frac{VEC5}{VAP}\right)\left(1+\frac{VCE1}{VAN}\right)}\right] \tag{4.14}$$

Using some algebraic manipulation, the above result can now be rewritten as:

$$\Delta V=VT\ln\left[m\frac{Is6\left(1-\frac{1}{\beta N}\right)\left(1+\frac{VCE2}{VAN}\right)}{Is5\left(1+\frac{VCE1}{VAN}\right)}\right]+VT\ln\left[\frac{\left(1+\frac{VEC6}{VAP}\right)}{\left(1+\frac{VEC5}{VAP}\right)}\right] \tag{4.15}$$

The emitter-collector voltages, V_{EC5} and V_{EC6}, are dependent on the power supply voltage (V_{CC}). However, all the other parameters do not alter (significantly) with V_{CC}. Hence, the second term is the only part of (4.15) that varies with V_{CC}. Therefore:

$$\frac{\partial(\Delta V)}{\partial Vcc}=\frac{\partial}{\partial Vcc}VT\left[\ln\left(1+\frac{VEC6}{VAP}\right)-\ln\left(1+\frac{VEC5}{VAP}\right)\right] \tag{4.16}$$

$$\frac{\partial(\Delta V)}{\partial Vcc}=\left(R1\frac{\beta N+1}{\beta N}\right)\frac{\partial Ix}{\partial Vcc}=VT\left[\frac{\partial}{\partial Vcc}\ln\left(1+\frac{VEC6}{VAP}\right)-\frac{\partial}{\partial Vcc}\ln\left(1+\frac{VEC5}{VAP}\right)\right] \tag{4.17}$$

However, in this case $\frac{\partial VEC}{\partial Vcc}\approx 1$ and $\frac{\partial}{\partial x}(\ln x)=\frac{1}{x}$. Therefore, (4.17) becomes:

$$\left(R_1\frac{\beta_N+1}{\beta_N}\right)\frac{\partial Ix}{\partial Vcc}=V_T\left[\frac{1}{V_{AP6}\left(1+\frac{V_{EC6}}{V_{AP6}}\right)}-\frac{1}{V_{AP5}\left(1+\frac{V_{EC5}}{V_{AP5}}\right)}\right] \tag{4.18}$$

An expression for the sensitivity of I_X to changes in the power supply voltage can now be defined as:

$$S(_{BNN})=\frac{1}{Ix}\frac{\partial Ix}{\partial Vcc}=\frac{\beta_N}{\beta_N+1}\frac{V_T}{IxR_1}\left(\frac{1}{V_{AP6}+V_{EC6}}-\frac{1}{V_{AP5}+V_{EC5}}\right) \tag{4.19}$$

The operation of the circuit ensures that the emitter-collector voltages of Q_5 and Q_6 are equal (i.e. $V_{EC6} = V_{EC5}$). Thus, it is obvious that if the Early voltages of Q_5 and Q_6 are equal (i.e. $V_{AP5} = V_{AP6}$) then the output current of this circuit will be completely insensitive to changes in the power supply voltage (i.e. $\frac{1}{Ix}\frac{\partial Ix}{\partial Vcc}=0$).

Figure 4.1 shows the basic implementation of the Nordholt and Nauta (BNN) PTAT Current Generator used for simulation. As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V.

Table 4.1 shows the temperature performance of I_X, I_Y and λ at various power supply voltage values.

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	(ppm/°C)
3	38.641	38.642	1.000	49.918	49.921	1.000	59.719	59.725	1.000	3378
4	38.675	38.679	1.000	49.962	49.971	1.000	59.775	59.787	1.000	3378
5	38.705	38.714	1.000	50.000	50.013	1.000	59.825	59.844	1.000	3378
6.5	38.745	38.756	1.000	50.051	50.071	1.000	59.875	59.908	1.000	3377
10	38.816	38.832	1.000	50.140	50.167	1.001	59.981	60.018	1.001	3377

Table 4.1 – Temperature Performance of I_X, I_Y and λ for the BNN with Variations in V_{CC}

I_X exhibits close to PTAT behaviour between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) varies by only 1ppm/°C (3378ppm/°C to 3377ppm/°C) across the 3V to 10V power supply range! This shows close agreement with the theoretical

value (3.9) of 3332ppm/°C. In addition, the current transfer ratio is virtually perfect (λ = 1) across both the afore-mentioned temperature and voltage ranges.

Table 4.2 shows the sensitivity of I_X to variations in V_{CC} (3V to 10V). The measured value of 634ppm/V at 27°C is greater than the theoretical value of 0ppm/V calculated previously. However, the difference between the theoretical and measured values is only equivalent to 0.0634%/V. Obviously, this is very small so it can be said that the measured result displays good agreement to the theoretical value.

Temperature (°C)	$S_{(BNII)}$ (ppm/V)
-40	645
27	634
85	625

Table 4.2 - Sensitivity of I_X to Variations in V_{CC} (3V to 10V)

In summary, the BNN topology demonstrates behaviour close to PTAT that is superior to that of the best 'Bootstrap Bias' type circuits from Chapter 3. Additionally, the BNN is approximately three times less sensitive to variations in V_{CC} than that of the BWCS+VFCM. Thus, the output current I_X remains extremely close (as seen in Table 4.1) to the design value over the entire (3V-10V) power supply voltage range under consideration.

4.1.2 High Performance Nauta and Nordholt (HPNN) Circuit

A high performance implementation of this improved class of PTAT current reference circuit, first seen in [1], is shown in Figure 4.2. Circuit operation is similar to that of the basic implementation, except in this case, the simple loop amplifier is replaced with a symmetrical loop amplifier formed by Q_4, Q_5, Q_8 and Q_9.

The reason for using the symmetrical loop amplifier is twofold. Firstly, in the analysis of section 4.1.1.1 it was assumed, for simplicity, that $I_{C2} = I_X$ (4.6), however, this is not quite the case as demonstrated in (4.5). Secondly, it is assumed in the same analysis that the simple loop amplifier ensures the condition $I_X = I_Y$. This is a fairly accurate assumption but it can be seen from Table 4.1 that I_X and I_Y are never exactly

equal. Ultimately, inaccuracies in both these assumptions contribute to the observed difference between the calculated and measured sensitivity values of I_X for the basic implementation. Therefore, the symmetrical loop amplifier is used to ensure that these assumptions become even more applicable.

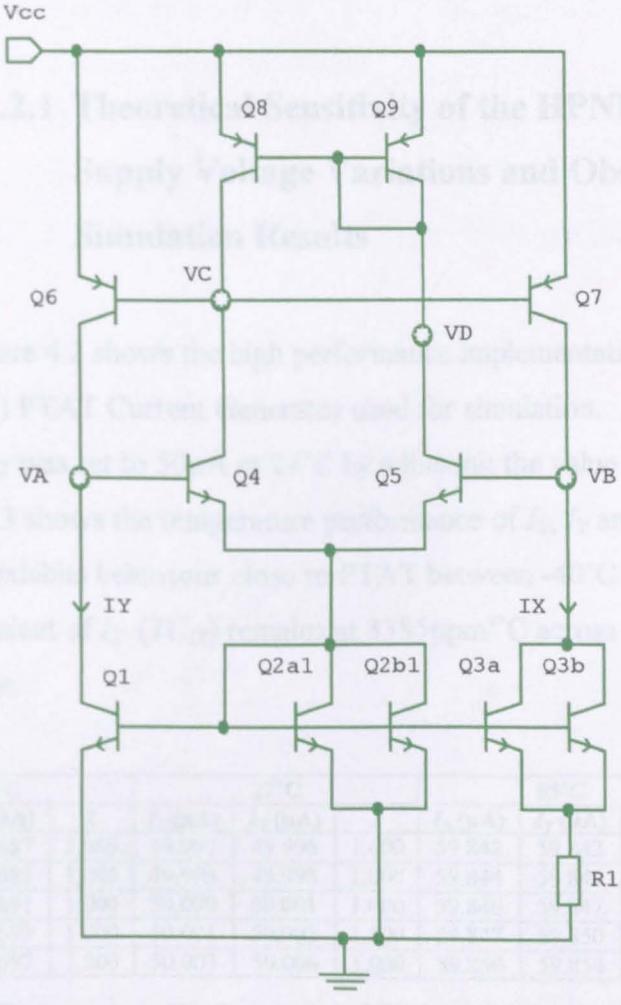

Figure 4.2 – High Performance Implementation of the Nauta and Nordholt PTAT Current Generator

The sensitivity analysis of section 4.1.1.1 is equally applicable to the high performance circuit considered here. Thus, it can be shown that the sensitivity of I_X to V_{CC} is given by:

$$S(_{HPNN}) = \frac{1}{Ix}\frac{\partial Ix}{\partial Vcc} = \frac{\beta_N}{\beta_N + 1}\frac{V_T}{IxR1}\left(\frac{1}{V_{AP7} + V_{EC7}} - \frac{1}{V_{AP6} + V_{EC6}}\right) \qquad (4.20)$$

As in the case of the basic implementation, the operation of the circuit ensures that the emitter-collector voltages of Q_6 and Q_7 are equal (i.e. $V_{EC6} = V_{EC7}$). Thus, it is apparent that as long as the Early voltages of Q_6 and Q_7 are equal (i.e. $V_{AP6} = V_{AP7}$) the output current of this circuit will be insensitive to changes in the power supply voltage (i.e. $\frac{1}{Ix}\frac{\partial Ix}{\partial Vcc} = 0$).

4.1.2.1 Theoretical Sensitivity of the HPNH to Power Supply Voltage Variations and Observed Simulation Results

Figure 4.2 shows the high performance implementation of the Nordholt and Nauta (HPNN) PTAT Current Generator used for simulation. As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V. Table 4.3 shows the temperature performance of I_X, I_Y and λ at various values of V_{CC}. I_X exhibits behaviour close to PTAT between -40°C and 85°C. The temperature coefficient of I_X (TC_{IX}) remains at 3385ppm/°C across the 3V to 10V power supply range.

V_{CC}	-40°C			27°C			85°C			TC_{IX}
(V)	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	I_X(μA)	I_Y(μA)	λ	(ppm/°C)
3	38.688	38.687	1.000	49.997	49.996	1.000	59.842	59.842	1.000	3385
4	38.689	38.689	1.000	49.998	49.998	1.000	59.844	59.844	1.000	3385
5	38.690	38.691	1.000	50.000	50.001	1.000	59.846	59.847	1.000	3385
6.5	38.691	38.693	1.000	50.001	50.003	1.000	59.847	59.850	1.000	3385
10	38.694	38.697	1.000	50.003	50.006	1.000	59.850	59.854	1.000	3385

Table 4.3 – Temperature Performance of I_X, I_Y and λ for the HPNN with Variations in V_{CC}

This shows close agreement with the theoretical value (3.9) of 3332ppm/°C but is slightly worse than that of the BNN. In addition, the current transfer ratio is virtually perfect (λ = 1) across both the afore-mentioned temperature and voltage ranges.

Table 4.4 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V). The measured value of 17ppm/V at 27°C shows close agreement with the theoretical value of 0ppm/V calculated previously.

In summary, the HPNN topology demonstrates behaviour close to PTAT that is superior to that of the best 'bootstrap-bias' type circuits from Chapter 3. Additionally, the HPNN is almost completely insensitive to variations in the power supply voltage. Thus, the output current I_X remains very close (see Table 4.3) to the design value over the entire (3V-10V) power supply voltage range.

Temperature (°C)	$S_{(HPNH)}$ (ppm/V)
-40	22
27	17
85	19

Table 4.4 - Sensitivity of I_X to Variations in V_{CC} (3V to 10V)

4.1.2.2 Effect of Early Voltage Mismatches

In modern simulation software all similar devices have identical characteristics. However, in reality this is not the case. Therefore, it is important to consider the case where the Early voltages are slightly mismatched. Following on from the equation derived for the sensitivity of I_X (4.20) for the high performance circuit, let $V_{AP7} = V_{AP}$ and $V_{AP6} = \Delta V_{AP}$ ($|\Delta V_{AP}| << V_{AP}$). Then:

$$S_{(HPNN)} = \frac{1}{Ix}\frac{\partial Ix}{\partial Vcc} = \frac{\beta_N}{\beta_N + 1}\frac{V_T}{IxR_1}\left(\frac{1}{V_{AP} + V_{EC7}} - \frac{1}{(V_{AP} + \Delta V_{AP}) + V_{EC6}}\right) \qquad (4.21)$$

$$S_{(HPNN)} = \frac{1}{Ix}\frac{\partial Ix}{\partial Vcc} = \frac{\beta_N}{\beta_N + 1}\frac{V_T}{IxR_1}\left(\frac{\Delta V_{AP}}{(V_{AP} + V_{EC7})(V_{AP} + \Delta V_{AP} + V_{EC6})}\right) \qquad (4.22)$$

But $\Delta V_{AP} << V_{AP}$, so assuming $V_{EC7} = V_{EC6} = V_{EC}$ and $V_{EC} << V_{AP}$, the sensitivity of I_X to changes in V_{CC} is now given by:

$$S_{(HPNN)} = \frac{1}{Ix}\frac{\partial Ix}{\partial Vcc} = \frac{\beta_N}{\beta_N + 1}\frac{V_T}{IxR_1}\left(\frac{\Delta V_{AP}}{V_{AP}^2}\right) = \frac{\beta_N}{\beta_N + 1}\frac{V_T}{IxR_1}\frac{1}{V_{AP}}\left(\frac{\Delta V_{AP}}{V_{AP}}\right) \qquad (4.23)$$

Using the measured device parameter (β_N=177), SPICE model data (V_{AP}=22V) and noting that I_X= 50μA at 27°C, V_T= 25.86mV and R_1 = 380Ω, it is possible to calculate the theoretical values for $S_{(HPNN)}$ when the Early voltages are mismatched by 1%, 5% and 10%. Then,

$$\frac{\Delta V_{AP}}{V_{AP}} = \frac{(V_{AP} \times 1.01) - V_{AP}}{V_{AP}} = \frac{(22 \times 1.01) - 22}{22} = 0.01 \quad \text{(1\% mismatch)} \quad (4.24)$$

$$\frac{\Delta V_{AP}}{V_{AP}} = \frac{(V_{AP} \times 1.05) - V_{AP}}{V_{AP}} = \frac{(22 \times 1.05) - 22}{22} = 0.05 \quad \text{(5\% mismatch)} \quad (4.25)$$

$$\frac{\Delta V_{AP}}{V_{AP}} = \frac{(V_{AP} \times 1.1) - V_{AP}}{V_{AP}} = \frac{(22 \times 1.1) - 22}{22} = 0.1 \quad \text{(10\% mismatch)} \quad (4.26)$$

The theoretical values of $S(_{HPNN})$ at 27°C are presented in Table 4.5 below.

V_{AP} Mismatch	$S(_{HPNH})$ (ppm/V)
1%	615
5%	3076
10%	6152

Table 4.5 - Theoretical Values of $S(_{HPNN})$ at 27°C for Various Degrees of Mismatch in V_{AP}

The maximum amount of Early voltage mismatch that can be tolerated, before the sensitivity of the HPNH circuit exceeds that of the best 'Bootstrap Bias' type circuit (i.e. BWCS+WCS), can be calculated via a rearrangement of (4.23). Thus:

$$\left[S(_{BWCS+WCS}) \left(\frac{\beta_N + 1}{\beta_N} \frac{I_X R_1}{V_T} \right) V_{AP} \right] \times 100 = \left(\frac{\Delta V_{AP}}{V_{AP}} \right) \quad (in\ \%) \quad (4.27)$$

Therefore, using previous values, the theoretical maximum value of Early voltage mismatch that can be tolerated is 4.1%.

The high performance circuit was re-simulated to take into account Early voltage mismatches. As before, the reference current I_X was set to 50μA at 27°C by adjusting the value of R_{PTAT} whilst V_{CC}=5V. However, this time the Early voltage of Q_7 is initially increased successively by 1%, then 5% and finally 10%. Table 5.6 shows the temperature coefficient of I_X at various values of V_{CC}.

V_{CC} (V)	TC_{IX} (ppm/°C) (1% V_{AP} mismatch)	TC_{IX} (ppm/°C) (5% V_{AP} mismatch)	TC_{IX} (ppm/°C) (10% V_{AP} mismatch)
3	3388	3398	3410
5	3386	3391	3397
10	3385	3383	3381

Table 4.6 - Simulated Values of TC_{IX} for Various Degrees of V_{AP} Mismatch

The results above indicate that the output current of the high performance circuit displays behaviour close to PTAT. However, as the Early voltage mismatches increase the temperature coefficient becomes increasingly sensitive to the power supply voltage.

Table 4.7 shows the sensitivity of I_X to variations in power supply voltage (3V to 10V).

V_{AP} Mismatch (%)	$S_{(HPNN)}$ (ppm/V) (-40°C)	$S_{(HPNN)}$ (ppm/V) (27°C)	$S_{(HPNN)}$ (ppm/V) (85°C)
1	653	614	594
5	3057	2899	2770
10	5782	5478	5248

Table 4.7 - Simulated Values of TC_{IX} with Various Degrees of V_{AP} Mismatch

As predicted by the theory above, the results clearly illustrate that as the Early voltages of Q_6 and Q_7 become increasingly mismatched, I_X becomes increasingly sensitive to variation in V_{CC}. The simulated results show fair agreement with the theoretical values shown in Table 4.5, particularly for $V_{CC} \leq 5V$. In fact the calculated values err on the side of safety, a useful feature for engineering design equations!

Figure 4.3 illustrates the measured sensitivity of I_X to changes in V_{CC} for varying degrees of Early Voltage Mismatch.

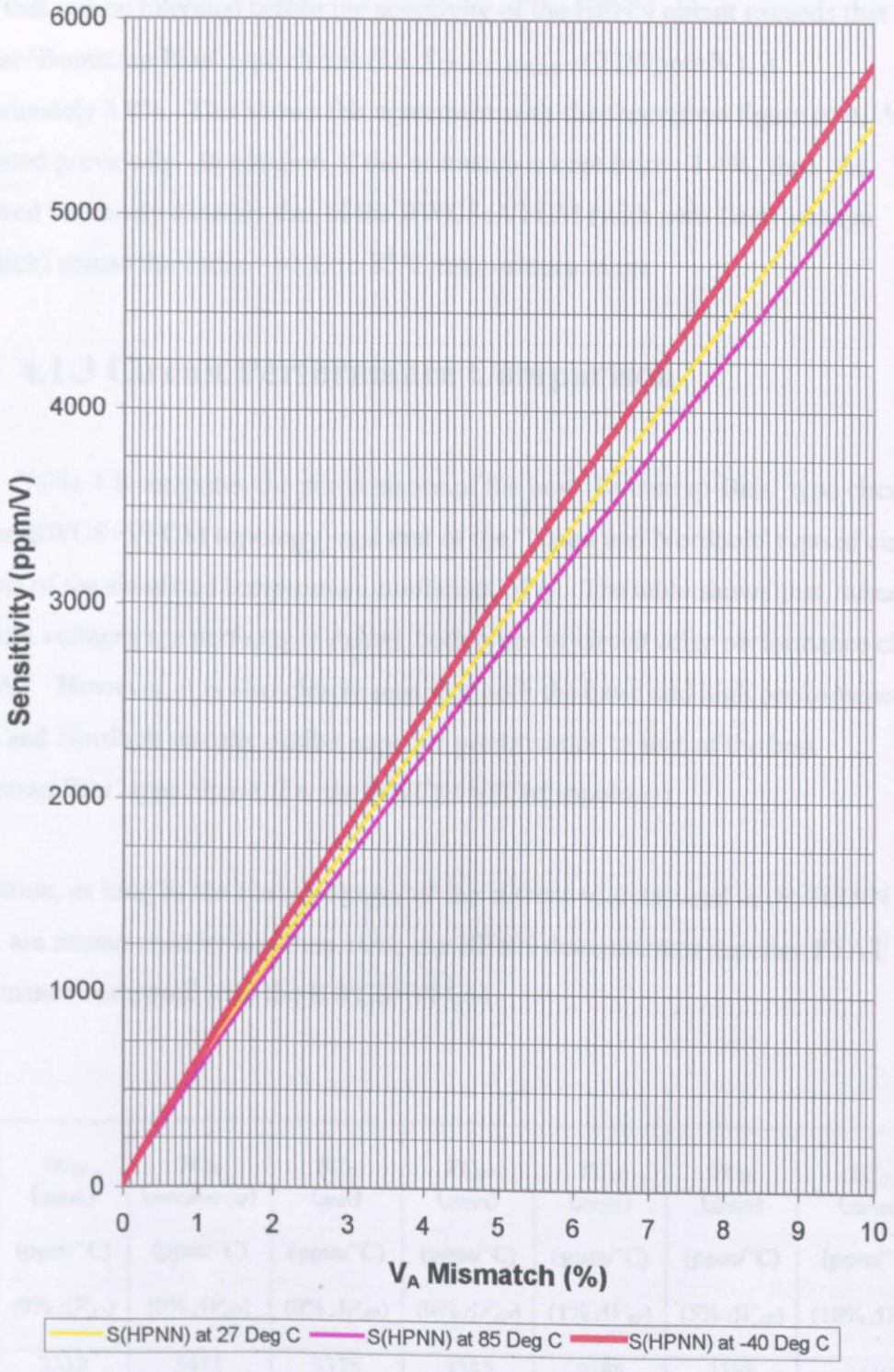

Figure 4.3 – Measured Sensitivity of I_X to Changes in V_{CC} for Varying Degrees of Early Voltage Mismatch

From Figure 4.3 it is clear that the maximum amount of Early voltage mismatch, at 27°C, that can be tolerated before the sensitivity of the HPNN circuit exceeds that of the best 'Bootstrap Bias' type circuit (i.e. $S_{(BWCS+VFCM)}$ = 2289ppm/V), is approximately 3.8%. This shows fair agreement with the theoretical figure of 4.1% calculated previously. In addition, if the mismatch is kept below 3.4%, then, the measured sensitivity exceeds that of the BWCS+VFCM (with zero Early voltage mismatch) across the entire –40°C to 85°C temperature range.

4.1.3 Circuit Performance Comparison

Table 4.8 compares the performance of the best 'Bootstrap-Bias' type circuit (i.e. the BWCS+VFCM topology) and that of the 'Nauta and Nordholt' type of circuit, in terms of the simulated temperature coefficient of I_X. The table shows that, when the Early voltages are perfectly matched, both types of circuit offer performance close to PTAT. However, it is also clearly seen that both the basic and high performance Nauta and Nordholt circuits exhibit superior performance to that of the best 'Bootstrap Bias' type circuit (i.e. the BWCS+VFCM topology).

In addition, as long as the Early voltages of the current sources used in the HPNN circuit are mismatched by less than 10%, the HPNN demonstrates superior PTAT performance compared with the BWCS+VFCM.

V_{CC} (V)	TC_{IX} ($_{IDEAL}$) (ppm/°C) (0% ΔV_{AP})	TC_{IX} ($_{BWCS+VFCM}$) (ppm/°C) (0% ΔV_{AP})	TC_{IX} ($_{BNN}$) (ppm/°C) (0% ΔV_{AP})	TC_{IX} ($_{HPNN}$) (ppm/°C) (0% ΔV_{AP})	TC_{IX} ($_{HPNN}$) (ppm/°C) (1% ΔV_{AP})	TC_{IX} ($_{HPNN}$) (ppm/°C) (5% ΔV_{AP})	TC_{IX} ($_{HPNN}$) (ppm/°C) (10% ΔV_{AP})
3	3332	3411	3378	3385	3388	3398	3410
5	3332	3402	3378	3385	3386	3391	3397
10	3332	3390	3377	3385	3385	3383	3381

Table 4.8 –Temperature Coefficient Comparison of I_X for Each Circuit Topology

Table 4.9 offers a comparison of the best 'Bootstrap-Bias' type circuit (i.e. the BWCS+VFCM topology) and that of the Nauta and Nordholt type of circuit in terms of the sensitivity of I_X to changes in V_{CC}.

Temp (°C)	$S_{(BWCS+VFCM)}$ (ppm/V) (0% ΔV_{AP})	$S_{(BNN)}$ (ppm/V) (0% ΔV_{AP})	$S_{(HPNN)}$ (ppm/V) (0% ΔV_{AP})	$S_{(HPNN)}$ (ppm/V) (1% ΔV_{AP})	$S_{(HPNN)}$ (ppm/V) (5% ΔV_{AP})	$S_{(HPNN)}$ (ppm/V) (10% ΔV_{AP})
-40	2504	645	22	653	3057	5782
27	2289	634	17	614	2899	5478
85	2118	625	19	594	2770	5248

Table 5.9 – Measured Sensitivity of I_X to Variations in Power Supply Voltage (3V to 10V) for Each Circuit Topology

The tabulated results above indicate that when the Early voltages are perfectly matched, the output current of both types of circuit is significantly insensitive to changes in the power supply voltage. However, it is clear that both the basic and high performance Nauta and Nordholt circuits exhibit superior performance to that of the best 'Bootstap-Bias' type circuit (i.e. the BWCS+VFCM topology). Indeed, the output current of the HPNN circuit is almost completely insensitive to the power supply voltage! This means that the output current I_X remains very close to the design value over the entire (3V-10V) power supply voltage range.

Furthermore, as long as the Early voltages of the current sources used in the HPNN circuit are mismatched by less than approximately 3.4%, the HPNN demonstrates superior performance compared with that of the WCS+VFCM. In summary, the HPNN achieves the best overall performance of all the PTAT generator circuits described in Chapter 4. The BNN circuit also offers very good performance and has the advantage of a lower headroom requirement. Thus the BNN may be useful in low voltage systems.

4.1.4 Start-Up Circuit Development

Fundamentally, both of the previously described (Nauta and Nordholt) circuits for generating a PTAT current operate by ensuring that the input current is made to depend upon the output current. This concept is identical to that shown in Chapter 3 except that, in this case, the relationship between I_{IN} and I_{OUT} is governed by the 'Widlar type' current source and the use of identical current sources controlled via a loop amplifier. Following from the discussion in Chapter 3, precautions must be taken to ensure that the circuit does not operate in the zero-current condition (i.e. $I_{IN} = I_{OUT} = 0$)!

Again, this zero-current state can be avoided by employing a 'start-up circuit' to ensure that some current always flows in the transistors of the PTAT reference circuit. However, the start-up circuit should not interfere with the normal operation of the PTAT reference circuit once the desired operating condition is reached.

A similar start-up circuit to that described previously in Chapter 3, based on previous work by Hart and Barker [3], is adapted for use with the HPNN circuit. This is shown in Figure 4.4. This circuit, with minor alterations, is suitable for use with all of the previously mentioned PTAT current generator circuits described in this chapter. Circuit operation is as follows.

R_{START2}, Q_{12} and Q_{13} form a 'Bipolar Peaking Current Source' [4]. The purpose of which is to provide a small output current, $I_{STARTOUT}$, that is in the order of a few μA. In this case Q_{12} and Q_{13} are assumed identical, therefore, $I_{STARTOUT}$ is given by the equation:

$$I_{STARTOUT} = I_{STARTIN}\, e^{\left(\frac{ISTARTIN.RSTART2}{VT}\right)} \qquad (4.28)$$

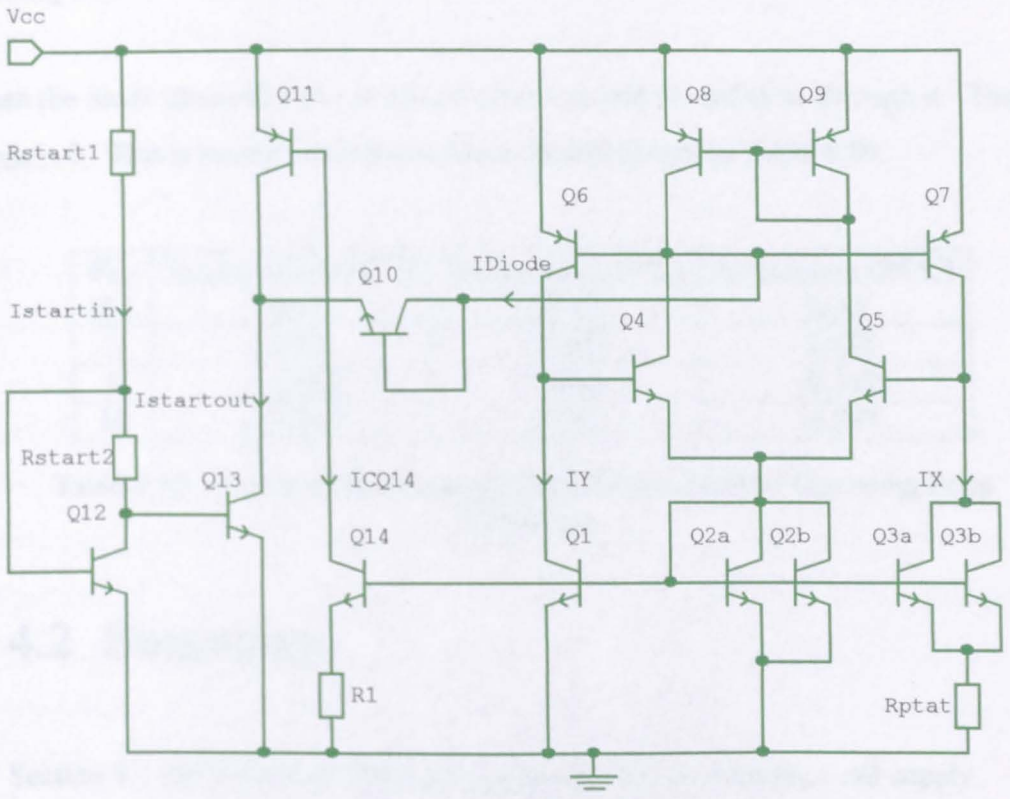

Figure 4.4 – Start-Up Circuit Adapted For Use With The High Performance Nauta and Nordholt PTAT Current Generator

When the power supply (V_{CC}) is switched on, $I_{STARTOUT}$ charges the effective capacitance associated with the collector circuit of Q_{11} until the emitter of the diode connected transistor Q_{10} becomes two junction drops below V_{CC}. Conduction current now flows from the bases of Q_6 and Q_7 (turning them on) through the diode Q_{10}. Current can now flow, via the collectors of Q_6 and Q_7, into the bases of Q_4 and Q_5, thus, also turning them on. This, in turn, allows current flow in the remaining devices, thus 'starting-up' the PTAT generator circuit and driving it into the desired condition of operation.

Now, the steady 'on' current of Q_{14} (I_{CQ14}) flows from the base of Q_{11} causing it to saturate, in turn, forcing Q_{10} to become reverse biased. Thus, the diode formed by Q_{10} is now turned off disconnecting the 'start-up circuit' from the PTAT current generator. R_1 is chosen to minimise I_{CQ14} in order to reduce the overall power

consumption.

When the diode formed by Q_{13} is turned off no current should flow through it. Thus, $I_{DIODE} \leq 0$. This is proved via the simulation results shown in Table 4.10.

V_{CC} (V)	$I_{STARTDIODE}$ (-40°C) (pA)	$I_{STARTDIODE}$ (27°C) (pA)	$I_{STARTDIODE}$ (85°C) (pA)
3	-10.931	-9.483	-8.275
5	-11.093	-9.604	-8.347
10	-11.119	-9.782	-8.587

Table 4.10 – Current Flow through Q_{10} After the Desired Operating Point is Reached

4.2 Summary

Section 4.1 introduced an alternative method [1] of developing a rail supply insensitive PTAT current that was first proposed by Nauta and Nordholt. This method uses a loop amplifier with identical current sources to ensure that the input and output currents of a 'Widlar type' current source are equal. Two different implementations of this technique were analysed in Sections 4.1.1 and 4.1.2 to determine their sensitivity to changes in power supply and overall temperature performance. It was found that, in theory, both of the 'Nauta and Nordholt' (NN) type circuits offered higher degrees of insensitivity to changes in the power supply voltage than that obtainable from the best 'Bootstrap Bias' type circuit (i.e. the BWCS+VFCM) discussed in Chapter 3. However, the High Performance Nauta and Nordholt (HPNN) circuit provided the highest theoretical degree of insensitivity.

The HPNN circuit was then investigated further to take into account Early voltage mismatches. This resulted in a degradation of the previously calculated power supply insensitivity. It was found that both implementations out-performed the BWCS+VFCM both in terms of power supply insensitivity and PTAT behaviour when the Early voltages were perfectly matched. Indeed, it was found that if the

Early voltages were mismatched by less than 3.4% then the HPNN still out-performed the WCS+VFCM with perfectly matched Early voltages!

Finally, Section 4.1.4 discussed the need for a start-up circuit in order to ensure that the NN type of circuit is driven out of the undesired operating condition $I_{IN} = I_{OUT} = 0$. One such circuit is presented that, with minor alterations, is suitable for use with all of the previously mentioned PTAT current generator circuits described in this chapter.

In summary, both circuits discussed in this chapter offer considerable performance advantages over all of the 'Bootstrap Bias' circuits discussed in Chapter 3. The HPNN topology offers the highest degree of insensitivity to changes in power supply but that is at the expense of increased circuit complexity and a headroom requirement that is one junction drop higher than that of the BNN topology. Therefore, it is left to the designer to weigh-up these pros and cons and choose the appropriate topology for the desired application.

4.3 References

[1] H. C. Nauta and E. H. Nordholt, 'A New Class of High-Performance PTAT Current Generators', *Electronic Letters*, Vol. 21, No. 9, Apr. 1985, pp. 384-386.

[2] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 16.

[3] B.L. Hart and R.W.J. Barker, 'Automatic Start-up Technique for Complementary PTAT Current Generators', *Electronics Letters*, 1982, 18, pp. 776-777.

[4] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 303-304.

CHAPTER 5

Novel Reference Current Amplification Circuits and Techniques

It is desirable to bias bipolar amplifiers with a collector current that is PTAT in order to minimise variation in voltage gain, that would normally arise, with change in temperature. Previously Chapters 3 and 4 discussed a variety of PTAT current generator circuits. However, bipolar amplifiers often require a collector current that has a value of several *mA* in order to produce significant voltage gain and maintain sufficient linearity. Unfortunately, PTAT current generator circuits are usually used to develop currents that are in the μA range because it can be problematic to produce accurate *m*A level currents. The reasoning behind this is threefold. Firstly, there can be difficulty in fabricating on-chip close tolerance resistors of low ohmic value (<100Ω). However, this could be overcome by using an off-chip resistor. Secondly, by referring to (5.1) and Table 5.1, it is clearly seen that the output current of a PTAT current generator becomes less accurate at large (*mA* level) currents. This is because the measured values of β decrease as the transistor collector current increases due to the effect of high-level injection [1].

$$I_{out} = \frac{\beta}{\beta+1}\frac{V_T}{R_1}\ln \lambda m \qquad (5.1)$$

V_{CE} (V)	I_C	β
5	10μA	188.754
5	50μA	184.335
5	100μA	181.104
5	500μA	163.783
5	1*mA*	147.479
5	2*mA*	123.054
5	3*mA*	105.329

Table 5.1 – Measured Values of β at Varying Collector Currents (T=27°C, V_{CE}=5V)

Thirdly and more importantly, developing large PTAT currents directly from a reference circuit before mirroring them to bias an amplifier is hugely wasteful in terms of power consumption.

Clearly, there is a need for some form of current converter / amplifier that can scale-up a reference current, accurately, and without introducing any significant additional temperature coefficient.

Thus, Chapter 5 begins with a brief discussion of several classical approaches to provide current conversion / amplification whilst highlighting their associated disadvantages. Finally culminating in the development and presentation of a novel current controlled current source providing temperature independent current gain.

5.1 Traditional VCCS Techniques

Large output currents can be achieved via a Voltage Controlled Current Source (VCCS) [2], also known as a Voltage to Current (V-I) Converter or transconductance amplifier. The input or control voltage could be taken directly from the PTAT circuit. Alternatively, a PTAT current could be mirrored from the PTAT generator and fed into a resistor to create a control/input PTAT voltage. A common form of VCCS is shown in Figure 5.1. This circuit employs an Operational Amplifier (OA) with Q_1 as a feedback element or load. All three terminals of Q_1 are uncommitted to any particular potential, therefore, this circuit is said to be a 'floating load' VCCS. In this case the output current is given by the well-known equation:

$$I_{out} = \frac{V_{in}}{R_1} \tag{5.2}$$

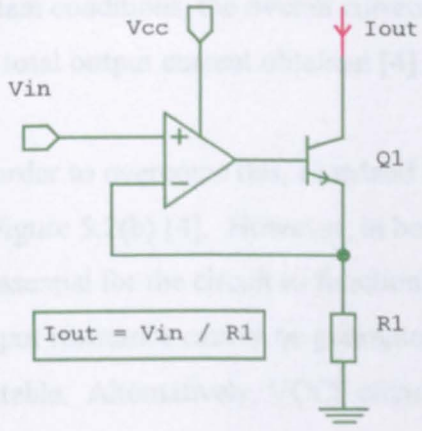

Figure 5.1 – A Simple 'Floating Load' VCCS Using an OA

The circuit of Figure 5.1 has the advantage that Q_1 could also form the input stage of a LNA. However, the emitter of Q_1 is not grounded which could present problems in designing the matching network especially if inductive degeneration is desired. Furthermore, the minimum allowable voltage at the collector of Q_1 is given by:

$$V_m = V_{in} + V_{BE1} \tag{5.3}$$

If a cascode stage were added the minimum voltage requirement will increase to:

$$V_m = V_{in} + 2V_{BE} \tag{5.4}$$

Obviously, if V_{in} is large then this circuit may require a large power supply voltage in order to operate satisfactorily.

Figure 5.2 shows two 'grounded load' VCCS circuits proposed by Howland [3,4].

Figure 5.2 – (a) Howland VCCS (b) Improved Howland VCCS

The basic circuit, shown in Figure 5.2(a), utilises an OA with a combination of both positive and negative feedback. This results in a high output resistance as required for true current source behaviour. As in the previous circuit, the output current is given by (5.2) when R_1=R_3. However, the Howland circuit can be very inefficient as, under certain conditions, the overall current consumption will be very high compared with the total output current obtained [4].

In order to overcome this, Howland introduced an improved current source as shown in Figure 5.2(b) [4]. However, in both circuits, a precisely matched resistor network is essential for the circuit to function properly. Mismatches mean that a very high output resistance cannot be guaranteed, and the Howland circuit may become unstable. Alternatively, VCCS circuits can be constructed from Current Conveyors (CCs) [5], an example of which is shown below in Figure 5.3.

Figure 5.3 - Basic VCCS using a Current Conveyor

However, one key disadvantage of all VCCS designs is that the temperature coefficient of the VCCS will be inversely related to the temperature coefficient of R_1. If R_1 is to be integrated, this

places a stringent requirement on production of a resistor with an extremely low temperature coefficient.

5.2 Traditional CCCS Techniques

An alternative approach in realising large output currents, which offers some advantages in removing the requirement of a very low temperature coefficient resistor, is to take a low amplitude precise reference current and scale it directly using a Current Controlled Current Source (CCCS) [6] to generate the required higher level of current output. One of the simplest CCCS designs commonly used in integrated circuits is the current-mirror [7]. However, in order to achieve large current gain ratios the current-mirror must be constructed from devices with equally large emitter area. This is often undesirable, particularly in terms of required chip area. In addition, current mirrors do not exhibit inherently low temperature coefficients without the use of significant emitter degeneration, which in turn can prevent low voltage operation. Two common CCCS designs are shown below in Figure 5.4.

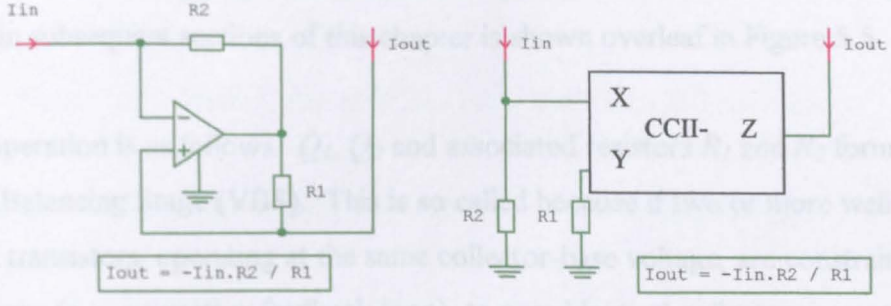

Figure 5.4 - Two common CCCS designs using (a) an Operational Amplifier (b) a Current Conveyor

The circuit of Figure 5.4(a) uses an OA and is similar to the Howland VCCS design in that it employs a combination of both positive and negative feedback. Figure 5.4(b) illustrates a CC based CCCS. It should be noted that as long as the temperature coefficients of R_1 and R_2 in either design are matched then both CCCS circuits are

inherently temperature independent, and hence of the two approaches, VCCS or CCCS, the latter appears to be more attractive.

5.3 A Novel CCCS Technique

Regardless of which approach is adopted, the designer must first develop an integrated OA or CC. If designing from scratch this represents a non-trivial task. In industry, standard circuit blocks may be available that will function adequately. However, this method often results in an overly elaborate circuit with a comparatively high component count. This in turn, may waste valuable chip area and result in a circuit that typically is not able to operate at low supply voltages. Clearly there is a need for an alternative form of CCCS that offers accurate performance without relying on an OA or CC.

5.3.1 Basic Concept of the Novel CCCS

The basic concept behind the development of the novel CCCS designs detailed in subsequent sections of this chapter is shown overleaf in Figure 5.5.

Circuit operation is as follows. Q_1, Q_2 and associated resistors R_1 and R_2 form a Voltage Balancing Stage (VBS). This is so called because if two or more well-matched transistors, operating at the same collector-base voltage, are constrained by some means (e.g. a negative feedback loop), to pass identical collector currents then their emitter currents and base-emitter voltages are, respectively, equal or 'balanced'.

For simplicity, assume that I_Y is negligible and $\beta_P >> 1$. Now, since the bases of Q_1 and Q_2 have a common potential, it follows that the potential difference across the resistor R_1 is equal to the potential difference across resistor R_2.

The potential difference across R_1 is given by:

$$V_1 = I_0 R_1 \qquad (5.5)$$

While the potential difference across R_2 is given by:

$$V_2 = (I_0 + I)R_2 \tag{5.6}$$

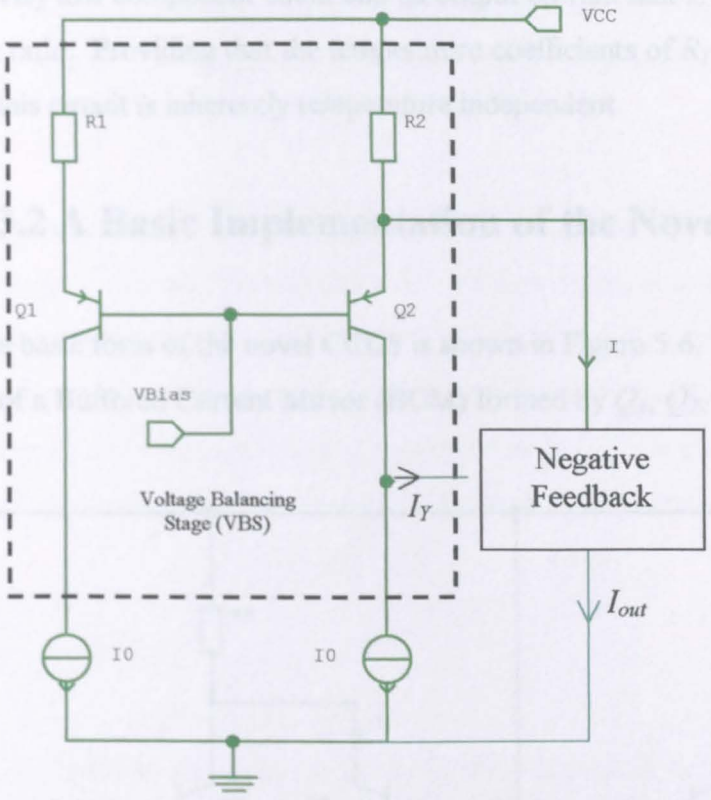

Figure 5.5 – Basic Concept Behind the Novel CCCS Technique

Equating (5.5) and (5.6) gives the relationship between I and I_0, namely:

$$I = I_0\left(\frac{R_1}{R_2} - 1\right) \tag{5.7}$$

Since I_Y is negligible it follows that:

$$I_{out} = I_0\left(\frac{R_1}{R_2} - 1\right) \tag{5.8}$$

Therefore, the current gain, A_I, of this circuit is given by:

$$A_I = \frac{I_{out}}{I_0} = \frac{R_1}{R_2} - 1 \qquad (5.9)$$

From the result above, it can be easily seen that this novel CCCS configuration provides relatively low component count and an output current that is defined by a simple resistor ratio. Providing that the temperature coefficients of R_1 and R_2 are matched then this circuit is inherently temperature independent.

5.3.2 A Basic Implementation of the Novel CCCS

The basic form of the novel CCCS is shown in Figure 5.6. In this case, the VBS consists of a Buffered Current Mirror (BCM) formed by Q_1, Q_2, Q_3 and

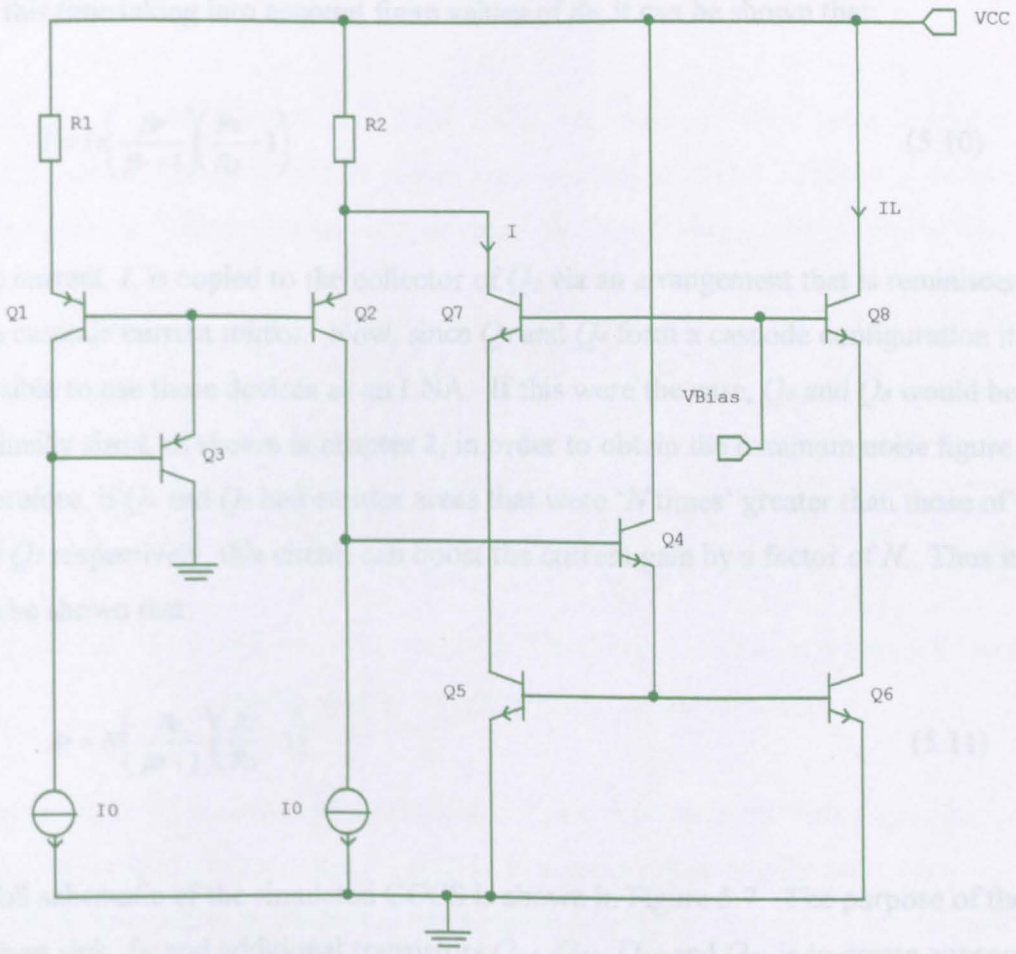

Figure 5.6 – Basic Implementation of the Proposed Novel CCCS

associated resistors R_1, R_2. Here a feedback loop, formed by Q_4, Q_5 and Q_7, forces the collector current of Q_2 to be equal to that of Q_1.

Circuit operation is as follows. The base current of the emitter follower Q_3 is much smaller than I_o. Similarly, the base current of the emitter follower Q_4 is also very small compared with I_o. Therefore, the collector currents of Q_1 and Q_2 are effectively equal to I_o.

Since the collector currents of Q_1 and Q_2 are equal. This in turn means that their emitter base voltages, V_{EB1} and V_{EB2} respectively, are also equal, as are their emitter currents. Since the bases of Q_1 and Q_2 have a common potential, it follows that the potential difference across the resistor R_1 is equal to the potential difference across resistor R_2. Thus by following an identical procedure as that in the previous section, but this time taking into account finite values of β_P, it can be shown that:

$$I = I_o\left(\frac{\beta_P}{\beta_P+1}\right)\left(\frac{R_1}{R_2}-1\right) \tag{5.10}$$

The current, I, is copied to the collector of Q_8 via an arrangement that is reminiscent of a cascode current mirror. Now, since Q_6 and Q_8 form a cascode configuration it is possible to use these devices as an LNA. If this were the case, Q_6 and Q_8 would be optimally sized, as shown in chapter 2, in order to obtain the minimum noise figure. Therefore, if Q_6 and Q_8 had emitter areas that were 'N times' greater than those of Q_5 and Q_7 respectively, this circuit can boost the current gain by a factor of N. Thus it can be shown that:

$$A_I = N\left(\frac{\beta_P}{\beta_P+1}\right)\left(\frac{R_1}{R_2}-1\right) \tag{5.11}$$

A full schematic of the simulated CCCS is shown in Figure 5.7. The purpose of the current sink, I_3, and additional transistors Q_{24}, Q_{25}, Q_{26} and Q_{27} is to create appropriate bias conditions for Q_{21} and Q_{23}. Initially I_1, I_2 and I_3 were set give a constant 50μA across the entire -40°C to 85°C temperature range. Assuming $\beta_P >> 1$, the values for

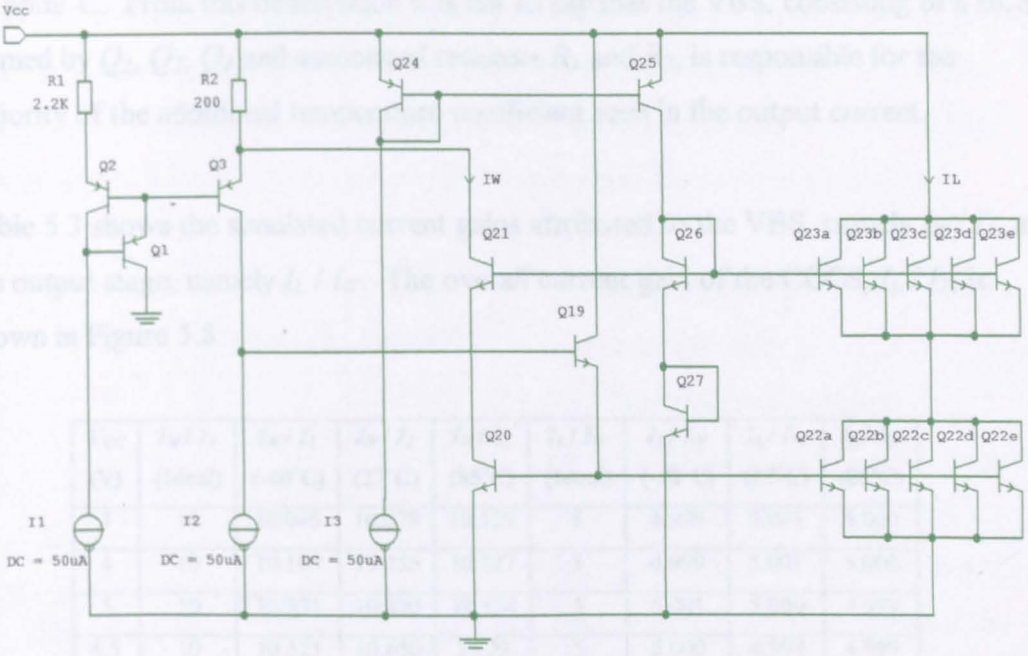

Figure 5.7 – Full Schematic of the Novel CCCS (Basic Implementation) Used for Simulation Tests

R_1, R_2 and N were chosen to be $2.2K\Omega$, 200Ω and 5 respectively in order to give an overall current gain of 50 and an output current equal to $2.5mA$. Table 5.2 shows the temperature performance of significant currents with varying power supply values.

V_{CC} (V)	I_1=I_2=I_3 (µA)	-40°C		27°C		85°C		$TC_{(IW)}$ (ppm/°C)	$TC_{(IL)}$ (ppm/°C)
		I_W (µA)	I_L (mA)	I_W (µA)	I_L (mA)	I_W (µA)	I_L (mA)		
3	50	502.288	2.511	503.922	2.520	506.445	2.532	66	67
4	50	509.666	2.548	512.747	2.564	516.361	2.582	104	106
5	50	516.543	2.583	521.008	2.605	525.677	2.628	140	138
6.5	50	526.052	2.630	532.488	2.662	538.673	2.693	190	189
10	50	545.273	2.726	555.880	2.779	565.317	2.827	288	290

Table 5.2 - Temperature Performance of Significant Currents at Various Values of Power Supply Voltage (Basic Implementation)

From Table 5.2 it is clearly seen that I_W and I_L are dependent on both temperature and V_{CC}. The input currents, I_1 and I_2, both have a temperature coefficient of zero. However, I_W exhibits an additional temperature coefficient that is between 66 ppm/°C and 288 ppm/°C across the 3V to 10V power supply range. I_L also exhibits an additional temperature coefficient but this differs from that of I_W by no greater than

±2 ppm/°C. From this observation it is fair to say that the VBS, consisting of a BCM formed by Q_1, Q_2, Q_3 and associated resistors R_1 and R_2, is responsible for the majority of the additional temperature coefficient seen in the output current.

Table 5.3 shows the simulated current gains attributed to the VBS, namely I_W / I_1, and the output stage, namely I_L / I_W. The overall current gain of the CCCS, I_L / I_1, is shown in Figure 5.8.

V_{CC} (V)	I_W / I_1 (Ideal)	I_W / I_1 (-40°C)	I_W / I_1 (27°C)	I_W / I_1 (85°C)	I_L / I_W (Ideal)	I_L / I_W (-40°C)	I_L / I_W (27°C)	I_L / I_W (85°C)
3	10	10.046	10.078	10.129	5	4.999	5.001	5.000
4	10	10.193	10.255	10.327	5	4.999	5.001	5.000
5	10	10.331	10.420	10.514	5	5.001	5.000	4.999
6.5	10	10.521	10.650	10.73	5	5.000	4.999	4.999
10	10	10.905	11.176	11.306	5	5.001	4.999	5.001

Table 5.3 – Simulated Current Gains Attributed to the VBS and the Output Stage of the Novel CCCS (Basic Implementation)

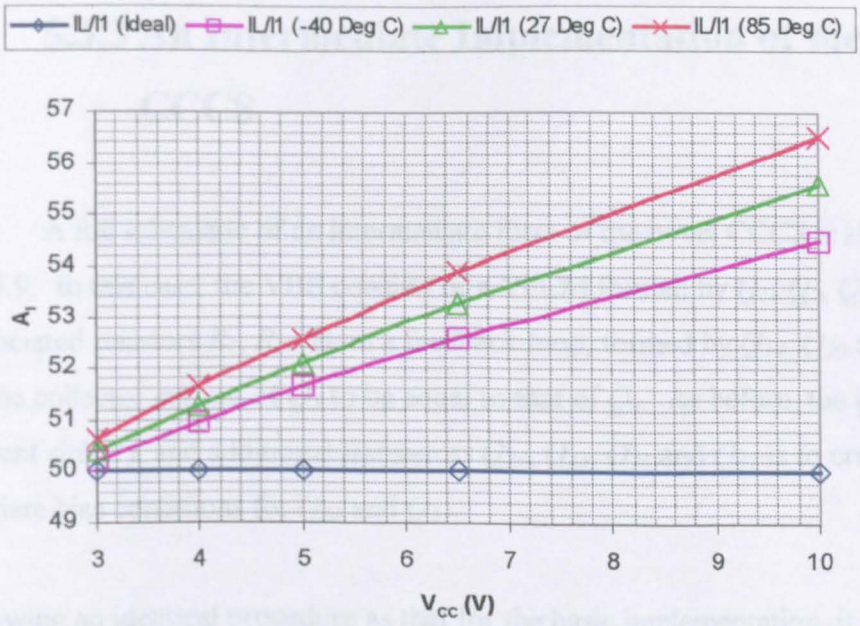

Figure 5.8 – Overall Current Gain with Temperature at Various Values of Power Supply Voltage (Basic Implementation)

Table 5.3 indicates that the current gain of the output stage is virtually power supply and temperature independent and, therefore, remains extremely close to the ideal design value. Clearly, the current gain of the VBS is particularly sensitive to the power supply voltage. As is the overall current gain illustrated in Figure 5.8.

Temperature (°C)	$S_{(IW)}$ (ppm/V)	$S_{(IL)}$ (ppm/V)
-40	11673	11678
27	13939	13899
85	15613	15649

Table 5.4 – Sensitivity of I_W and I_L to Changes in Power Supply Voltage (Basic Implementation)

The sensitivity of I_W and I_L to changes in power supply voltage is shown in Table 5.4. Since the sensitivity of I_L is virtually identical to that of I_W, it seems reasonable that the overall sensitivity of the entire CCCS is defined by the VBS. Thus, if the VBS were improved, by replacing the BCM with a 'high quality' current mirror such as the VFCM defined in Chapter 3, then the current gain, sensitivity to power supply voltage and temperature coefficient of the entire novel CCCS would also improve.

5.3.3 An Intermediate Implementation of the Novel CCCS

A full schematic of an intermediate form of the novel CCCS is shown in Figure 5.9. In this case, the VBS consists of a VFCM formed by Q_1, Q_2, Q_3, Q_4, Q_5 and associated resistors R_1, R_2. Here a feedback loop, formed by Q_{19}, Q_{20} and Q_{21}, forces the collector current of Q_5 to be equal to that of Q_4. As before, the purpose of the current sink, I_3, and additional transistors Q_{24}, Q_{25}, Q_{26} and Q_{27} is to create appropriate bias conditions for Q_{21} and Q_{23}.

By following an identical procedure as that for the basic implementation, it can be demonstrated that the overall current gain is given by:

$$A_I = N\left(\frac{R_1}{R_2} - 1\right) \tag{5.12}$$

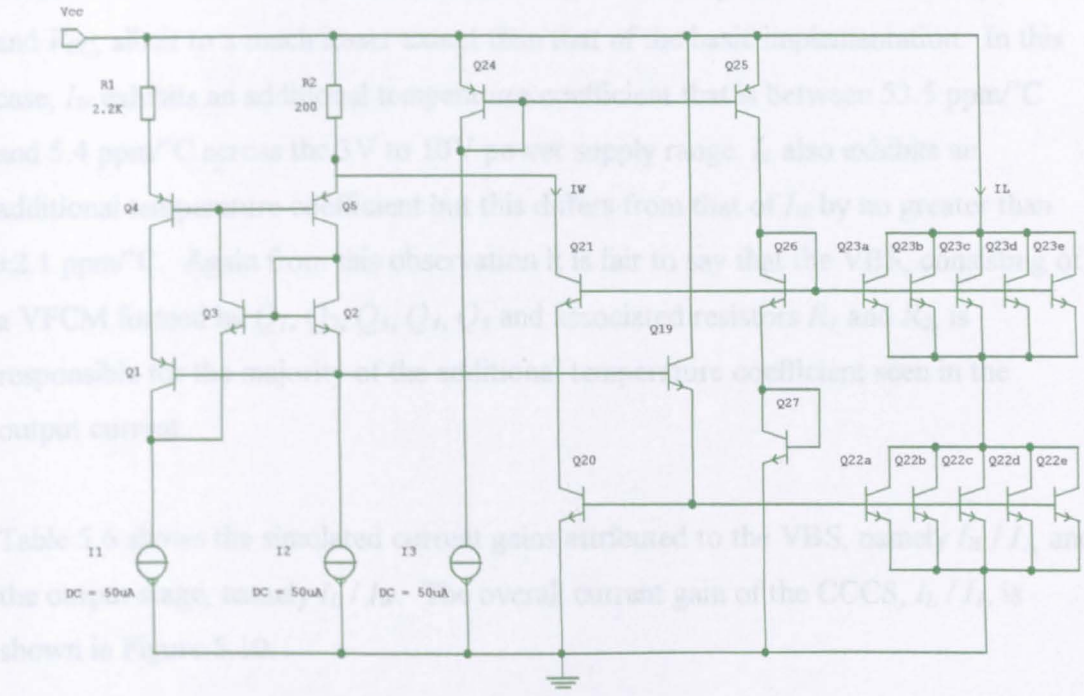

Figure 5.9 – Full Schematic of the Novel CCCS (Intermediate Implementation)

As before, I_1, I_2 and I_3 were set to give a constant 50μA across the entire -40°C to 85°C temperature range. The values for R_1, R_2 and N were chosen to be $2.2K\Omega$, 200Ω and 5 respectively in order to give an overall current gain of 50 and an output current equal to $2.5mA$.

Table 5.5 shows the temperature performance of significant currents with varying power supply values.

V_{CC}	I_1=I_2=I_3	-40°C		27°C		85°C		$TC_{(IW)}$	$TC_{(IL)}$
(V)	(μA)	I_W (μA)	I_L (mA)	I_W (μA)	I_L (mA)	I_W (μA)	I_L (mA)	(ppm/°C)	(ppm/°C)
3	50	496.001	2.480	498.892	2.495	499.338	2.497	53.5	54.5
4	50	499.589	2.498	500.019	2.500	500.388	2.502	12.0	12.8
5	50	500.640	2.503	501.002	2.505	501.312	2.507	10.7	12.8
6.5	50	501.975	2.510	502.263	2.511	502.506	2.513	8.5	9.6
10	50	504.309	2.522	504.500	2.523	504.650	2.523	5.4	3.2

Table 5.5 - Temperature Performance of Significant Currents at Various Values of Power Supply Voltage (Intermediate Implementation)

From Table 5.5 it is clearly seen that I_W and I_L are still dependent on both temperature and V_{CC}, albeit to a much lesser extent than that of the basic implementation. In this case, I_W exhibits an additional temperature coefficient that is between 53.5 ppm/°C and 5.4 ppm/°C across the 3V to 10V power supply range. I_L also exhibits an additional temperature coefficient but this differs from that of I_W by no greater than ±2.1 ppm/°C. Again from this observation it is fair to say that the VBS, consisting of a VFCM formed by Q_1, Q_2, Q_3, Q_4, Q_5 and associated resistors R_1 and R_2, is responsible for the majority of the additional temperature coefficient seen in the output current.

Table 5.6 shows the simulated current gains attributed to the VBS, namely I_W / I_1, and the output stage, namely I_L / I_W. The overall current gain of the CCCS, I_L / I_1, is shown in Figure 5.10.

V_{CC} (V)	I_W / I_1 (Ideal)	I_W / I_1 (-40°C)	I_W / I_1 (27°C)	I_W / I_1 (85°C)	I_L / I_W (Ideal)	I_L / I_W (-40°C)	I_L / I_W (27°C)	I_L / I_W (85°C)
3	10	9.920	9.978	9.987	5	5.000	5.001	5.001
4	10	9.992	10.000	10.008	5	5.000	5.000	5.000
5	10	10.013	10.020	10.026	5	5.000	5.000	5.001
6.5	10	10.040	10.045	10.050	5	5.000	4.999	5.001
10	10	10.086	10.090	10.093	5	5.001	5.001	5.000

Table 5.6 – Simulated Current Gains Attributed to the VBS and the Output Stage of the Novel CCCS (Intermediate Implementation)

Table 5.6 indicates that the current gain of the output stage is virtually power supply and temperature independent and, therefore, remains extremely close to the ideal design value. In this case, the current gain of the VBS is greatly improved (i.e. I_W / I_1 is much closer to ideal) over the entire 3V to 10V power supply voltage range compared to that of the basic implementation. This in turn means that I_W and I_L are much less sensitive to the power supply voltage. Therefore, the overall current gain of the CCCS now remains much closer to the design value as illustrated in Figure 5.10.

The simulated sensitivity of I_W and I_L to changes in power supply voltage is shown in Table 5.7.

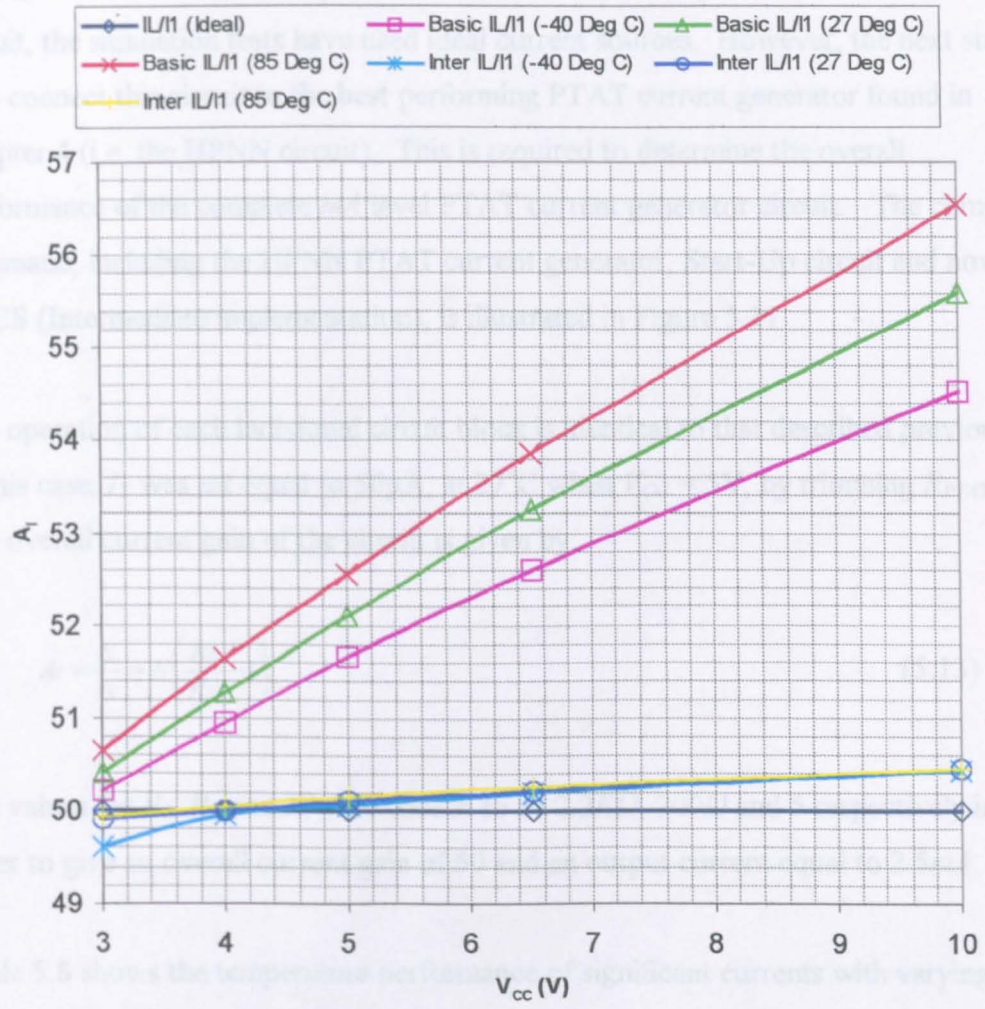

Figure 5.10 - Overall Current Gain (Intermediate Implementation) with Temperature at Various Values of Power Supply Voltage Compared Against Previous Results (Basic Implementation)

Temperature (°C)	$S_{(IW)}$ (ppm/V)	$S_{(IL)}$ (ppm/V)
-40	2364	2390
27	1595	1593
85	1510	1478

Table 5.7 – Sensitivity of I_W and I_L to Changes in Power Supply Voltage (Intermediate Implementation)

It is noted that the sensitivity of both I_W and I_L is significantly worse at -40°C than at any other temperature. This is due to the fact that when the power supply is reduced to 3V at -40°C the circuit is nearing saturation. Thus, this circuit should be operated under the condition $V_{CC} > 3$V if accurate circuit operation down to -40°C is required.

So far, in order to isolate the performance attributed directly to the Intermediate circuit, the simulation tests have used ideal current sources. However, the next stage is to connect this circuit to the best performing PTAT current generator found in Chapter 4 (i.e. the HPNN circuit). This is required to determine the overall performance of the complete *mA* level PTAT current generator circuit. The complete schematic, including the HPNN PTAT current generator, Start-Up circuit and novel CCCS (Intermediate implementation), is illustrated in Figure 5.11.

The operation of each individual circuit block is identical to that described previously. In this case, I_X was set equal to 50μA, at 27°C when $V_{CC} = 5V$, by trimming R_{PTAT}. The overall current gain of the circuit is given by:

$$A_I = \frac{I_L}{I_X} = N\left(\frac{R_2}{R_X} - 1\right) \tag{5.13}$$

The values for R_2, R_X and N were chosen to be $2.2K\Omega$, 200Ω and 5 respectively in order to give an overall current gain of 50 and an output current equal to $2.5mA$.

Table 5.8 shows the temperature performance of significant currents with varying power supply values.

V_{CC}	I_X	-40°C		27°C		85°C		$TC_{(I_W)}$	$TC_{(I_L)}$
(V)	(μA)	I_W (μA)	I_L (mA)	I_W (μA)	I_L (mA)	I_W (μA)	I_L (mA)	(ppm/°C)	(ppm/°C)
3	49.998	386.620	1.933	500.645	2.503	600.111	3.001	3411	3414
4	49.999	387.743	1.939	501.830	2.509	601.393	3.007	3406	3405
5	50	388.619	1.943	502.873	2.514	602.533	3.013	3403	3405
6.5	50.002	389.747	1.949	504.207	2.521	603.995	3.020	3399	3399
10	50.004	391.729	1.959	506.561	2.533	606.636	3.033	3394	3392

Table 5.8 - Temperature Performance of Significant Currents at Various Values of Power Supply Voltage (Complete Intermediate *mA* Level PTAT Generator Circuit)

As expected, Table 5.8 clearly illustrates that I_W and I_L exhibit close to PTAT behaviour. Thus, the temperature coefficients are close to the ideal figure of 3332ppm/°C defined in Chapter 3.

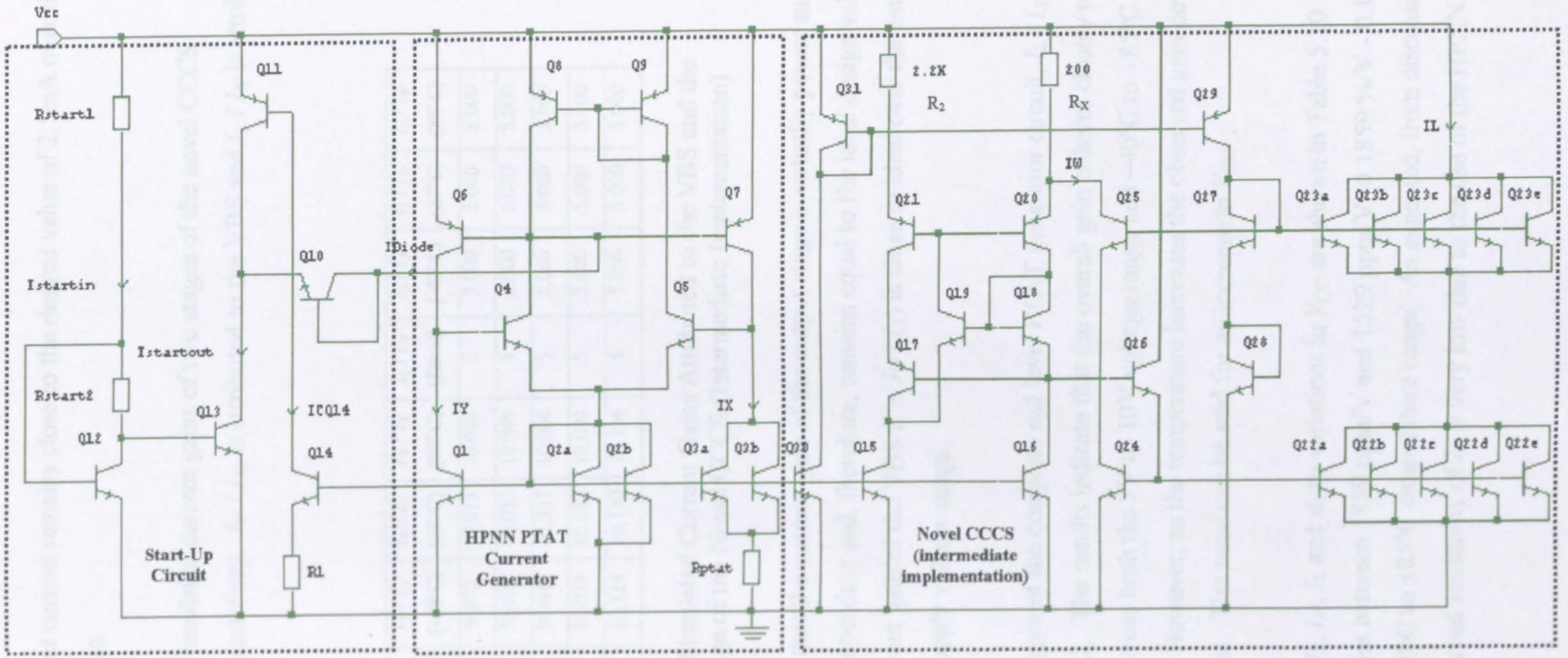

Figure 5.11 - Complete Schematic of a *mA* Level PTAT Current Generator Formed via the Interconnection of the HPNN PTAT Current Generator (with associated Start-Up circuit) and the Novel CCCS (Intermediate Implementation)

In addition, the output current remains close to the desired value of 2.5mA over the 3V-10V voltage range.

Table 5.9 shows the simulated current gains of two stages of the novel CCCS (intermediate implementation). I_W / I_X, is attributed to the VBS and I_L / I_W is attributed to the output stage.

V_{CC} (V)	I_W / I_X (Ideal)	I_W / I_X (-40°C)	I_W / I_X (27°C)	I_W / I_X (85°C)	I_L / I_W (Ideal)	I_L / I_W (-40°C)	I_L / I_W (27°C)	I_L / I_W (85°C)
3	10	9.993	10.013	10.028	5	5.000	5.000	5.000
4	10	10.022	10.037	10.049	5	5.000	5.000	5.000
5	10	10.044	10.057	10.068	5	5.000	5.000	5.000
6.5	10	10.073	10.084	10.092	5	5.000	5.000	5.000
10	10	10.124	10.130	10.136	5	5.000	5.000	5.000

Table 5.9 – Simulated Current Gains Attributed to the VBS and the Output Stage of the Novel CCCS (Intermediate Implementation)

The results indicate that the current gain of the output stage is virtually power supply and temperature independent and, therefore, remains equal to the ideal design value. In this case, the current gain of the VBS (i.e. I_W / I_X) is close to ideal over the entire 3V to 10V power supply voltage range.

The overall current gain of the complete *mA* level PTAT generator circuit, I_L / I_X, is shown in Figure 5.12. The results indicate that the overall gain coheres closely to the ideal figure of 50, across both the 3V to 10V voltage range and –40°C to +85°C temperature range. However, as the temperature increases the observed gain deviates further from the ideal. The same can be said for an increase in V_{CC}.

The sensitivities of I_X, I_W, I_L and A_I to variations in V_{CC} are shown in Table 5.10. The sensitivity of A_I varies between 1859 ppm/V and 1529 ppm/V (0.1859 %/V - 0.1529 %/V) across the –40°C to +85°C temperature range. As expected, from discussions in Chapter 4, the observed sensitivity of I_X is very low due to the use of the HPNN circuit.

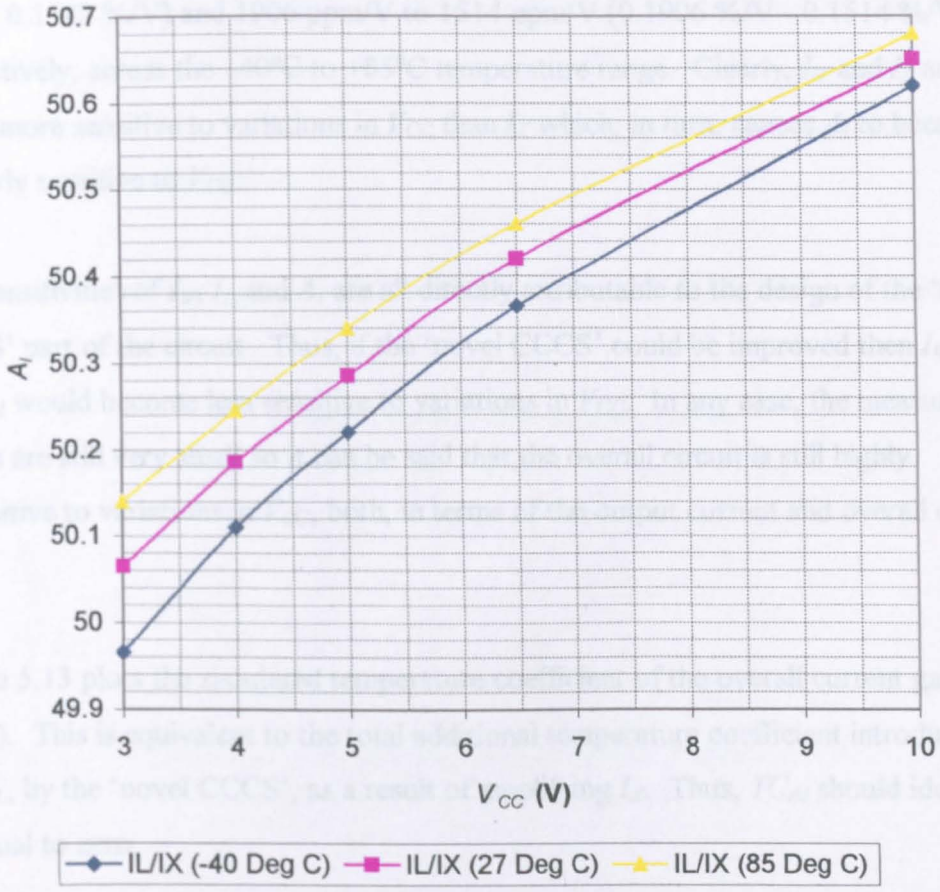

Figure 5.12 – Overall Current Gain of the Complete *mA* Level PTAT Generator Circuit

Temperature (°C)	$S_{(IX)}$ (ppm/V)	$S_{(IW)}$ (ppm/V)	$S_{(IL)}$ (ppm/V)	$S_{(AI)}$ (ppm/V)
-40	18	1873	1906	1859
27	17	1676	1700	1658
85	21	1543	1514	1529

Table 5.10 – Sensitivity of I_X, I_W, I_L and A_I to Variations in V_{CC} (Complete Intermediate PTAT Current Generator)

The sensitivity of I_W and I_L ranges between 1873 ppm/V and 1543 ppm/V (0.1873 %/V - 0.1543 %/V) and 1906 ppm/V to 1514 ppm/V (0.1906 %/V - 0.1514 %/V), respectively, across the –40°C to +85°C temperature range. Clearly, I_W and I_L are much more sensitive to variations in V_{CC} than I_X which, in turn, causes A_I to become similarly sensitive to V_{CC}.

The sensitivities of I_W, I_L and A_I are all directly attributable to the design of the 'novel CCCS' part of the circuit. Thus, if the 'novel CCCS' could be improved then I_W, I_L and A_I would become less sensitive to variations in V_{CC}. In any case, the measured values are still very small so it can be said that the overall circuit is still highly insensitive to variations in V_{CC}, both, in terms of the output current and overall current gain.

Figure 5.13 plots the simulated temperature coefficient of the overall current gain (TC_{AI}). This is equivalent to the total additional temperature coefficient introduced into I_L, by the 'novel CCCS', as a result of amplifying I_X. Thus, TC_{AI} should ideally be equal to zero.

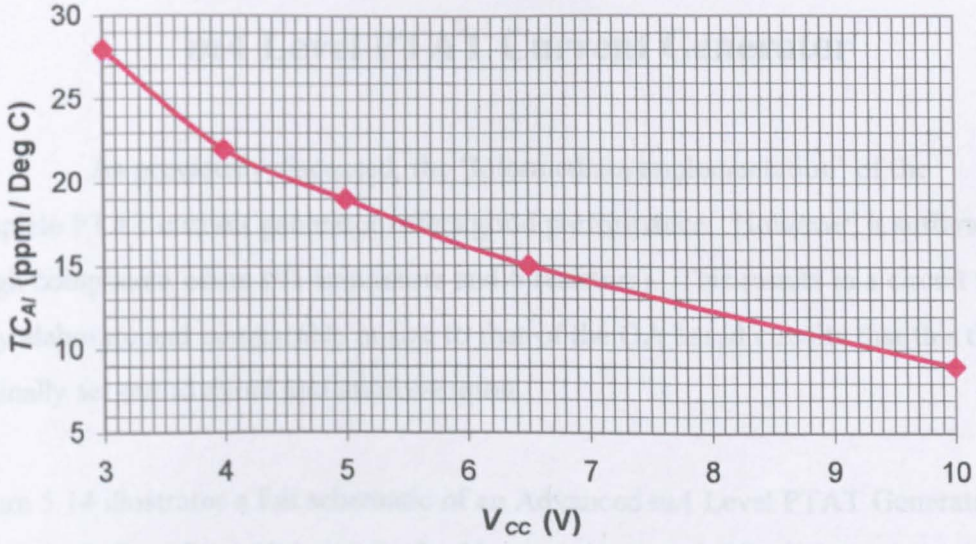

Figure 5.13 - Additional Temperature Coefficient Introduced into I_L (Complete Intermediate PTAT Current Generator)

From Figure 5.13 it is seen that the Intermediate form of the novel CCCS introduces an additional temperature coefficient of between 28 ppm/°C and 9 ppm/°C across the 3V to 10V voltage range. These values are very small and exhibit close proximity to the ideal figure. Thus, it can be said that the current gain of the overall circuit is highly temperature insensitive.

Finally, the overall power consumption of the circuit is tabulated below in Table 5.11.

V_{CC}	**Total Power Consumption (*mW*)**		
(V)	**-40°C**	**27°C**	**85°C**
3	8.165	10.532	12.596
5	13.976	17.934	21.329
10	29.813	37.774	44.720

Table 5.11 – Total Power Consumption (Complete Intermediate PTAT Current Generator)

5.3.4 An Advanced Implementation of a Complete *mA* Level PTAT Current Generator

As previously discussed, the 'Intermediate implementation' of the complete PTAT current generator offers good performance. However, it suffers from a high component count (41 transistors and 6 resistors). This results in a circuit that is fairly elaborate and comparable in size to that of the OA based circuits that this thesis originally set out to avoid and improve upon.

Figure 5.14 illustrates a full schematic of an Advanced *mA* Level PTAT Generator Circuit including 'Start-Up' circuit. In this case, the 'novel CCCS' is integrated directly into the BNN PTAT generator discussed in Chapter 4. This results in a more elegant and simplified circuit with a reduced component count (33 transistors and 8 resistors).

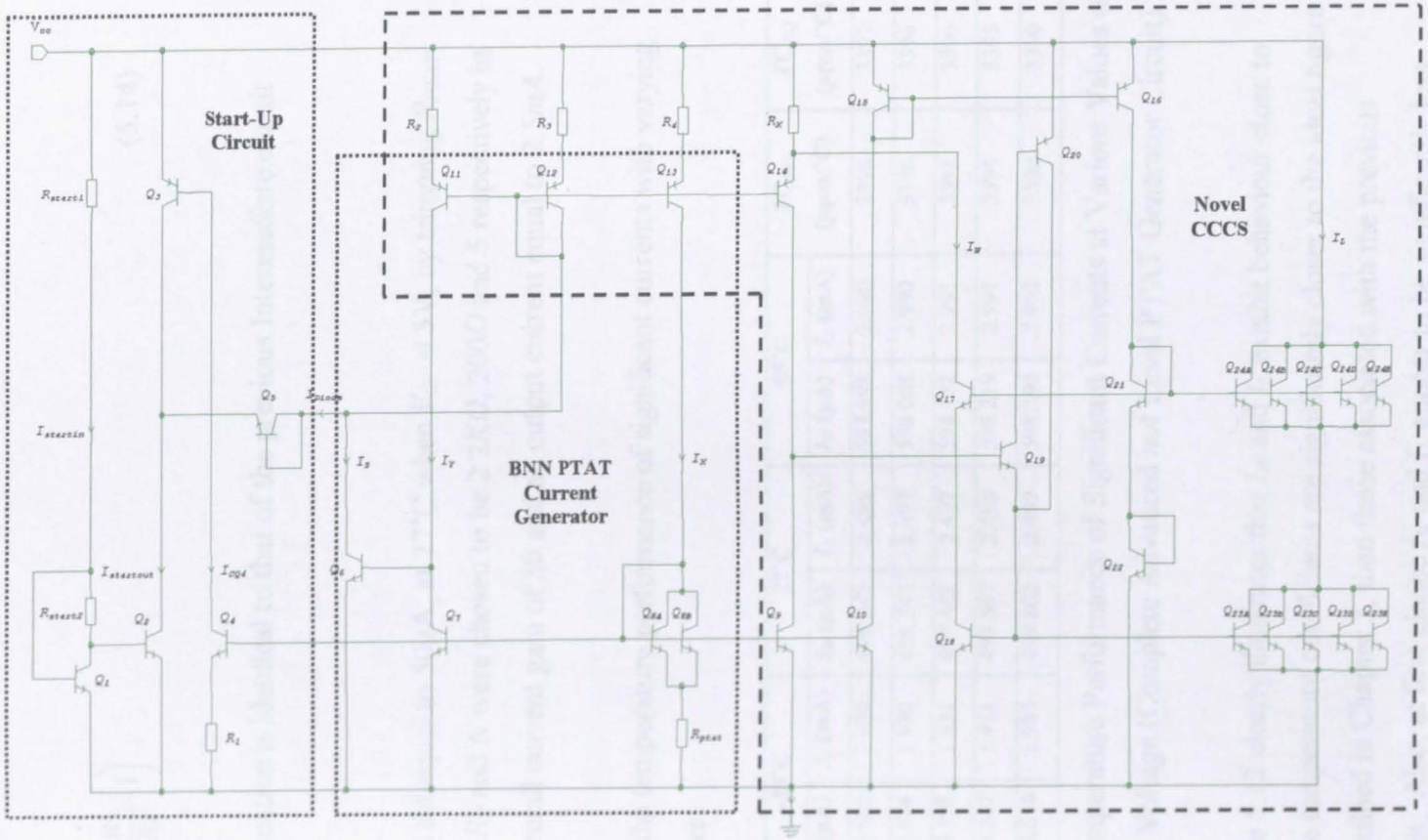

Figure 5.14 - Full Schematic of a *mA* Level PTAT Current Generator (Advanced Implementation) Formed by Integrating the BNN PTAT Current Generator (with associated Start-Up circuit) and the Novel CCCS

The operation of each individual circuit block is identical to that described previously. The overall current gain of the circuit, provided the condition $R_2 = R_3 = R_4$ is met, is given by:

$$Ai = \frac{I_L}{Ix} = N\left(\frac{R2}{Rx} - 1\right) \tag{5.14}$$

Note, the above equation is identical to that of the previous Intermediate circuit (5.13).

In this case, I_X was set equal to 50μA, at 27°C when V_{CC} = 5V, by trimming R_{PTAT}. The values for R_2, R_X and N were chosen to be $2.2K\Omega$, 200Ω and 5 respectively in order to give an overall current gain of 50 and an output current equal to $2.5mA$.

Table 5.12 shows the temperature performance of significant currents with varying power supply values.

V_{CC}	I_X	-40°C		27°C		85°C		$TC_{(IW)}$	$TC_{(IL)}$
(V)	(μA)	I_W (μA)	I_L (mA)	I_W (μA)	I_L (mA)	I_W (μA)	I_L (mA)	(ppm/°C)	(ppm/°C)
3	49.966	385.955	1.930	499.242	2.496	597.998	2.990	3398	3397
4	49.983	386.084	1.930	499.347	2.497	598.068	2.990	3396	3396
5	50.000	386.198	1.931	499.442	2.497	598.132	2.991	3395	3396
6.5	50.023	386.267	1.931	499.567	2.498	598.219	2.991	3394	3395
10	50.067	386.619	1.933	499.802	2.499	598.390	2.992	3390	3390

Table 5.12 - Temperature Performance of Significant Currents at Various Values of Power Supply Voltage (Complete Advanced *mA* Level PTAT Generator Circuit)

As expected, Table 5.12 clearly illustrates that I_W and I_L exhibit behaviour close to PTAT. In fact, the temperature coefficients are significantly closer to the ideal figure of 3332ppm/°C, defined in Chapter 3, than those associated with the previous Intermediate circuit. Also, at first glance I_W and I_L appear to be significantly less sensitive to changes in V_{CC} compared with the Intermediate circuit. This will be confirmed later. In addition, the output current remains very close to the design value (i.e. within $4\mu A$) of 2.5mA over the entire 3V to 10V voltage range.

Table 5.13 shows the simulated current gains of two stages of the Advanced PTAT current generator. I_W / I_X, is attributed to the VBS and I_L / I_W is attributed to the output stage.

V_{CC} (V)	I_W / I_X (Ideal)	I_W / I_X (-40°C)	I_W / I_X (27°C)	I_W / I_X (85°C)	I_L / I_W (Ideal)	I_L / I_W (-40°C)	I_L / I_W (27°C)	I_L / I_W (85°C)
3	10	9.966	9.992	10.013	5	5.000	5.000	5.000
4	10	9.965	9.990	10.011	5	5.000	5.000	5.000
5	10	9.965	9.989	10.009	5	5.000	5.000	5.000
6.5	10	9.962	9.987	10.006	5	5.000	5.000	5.000
10	10	9.962	9.983	10.000	5	5.000	5.000	5.000

Table 5.13 – Simulated Current Gains Attributed to the VBS and the Output Stage of the Advanced Circuit

The results indicate that the current gain of the output stage is virtually power supply and temperature independent and, therefore, remains equal to the ideal design value. In this case, the current gain of the VBS (i.e. I_W / I_1) is even closer to ideal over the entire 3V to 10V power supply voltage range than that of the Intermediate circuit.

The overall current gain of the complete Advanced *mA* level PTAT generator circuit, I_L / I_1, is shown in Figure 5.15. The results indicate that the overall gain coheres closely to the ideal figure of 50, across both the 3V to 10V voltage range and –40°C to +85°C temperature range. If Figure 5.15 is compared with Figure 5.12, it can be seen that the overall gain of the advanced circuit demonstrates much closer agreement with the ideal design value of 50 than that of the previous intermediate circuit.

The sensitivities of I_X, I_W, I_L and A_I to variations in V_{CC} are shown in Table 5.14. The sensitivity of A_I varies between -54 ppm/V and -186 ppm/V (-0.0054 %/V and -0.0186 %/V) across the –40°C to +85°C temperature range. These results indicate that the current gain is much less sensitive to changes in V_{CC} compared with that of previous circuits. The observed sensitivity of I_X is greater than that of the Intermediate circuit, due to the use of the BNN configuration, however, the output current (I_L) is significantly less sensitive to changes in V_{CC} than that of any previous circuit.

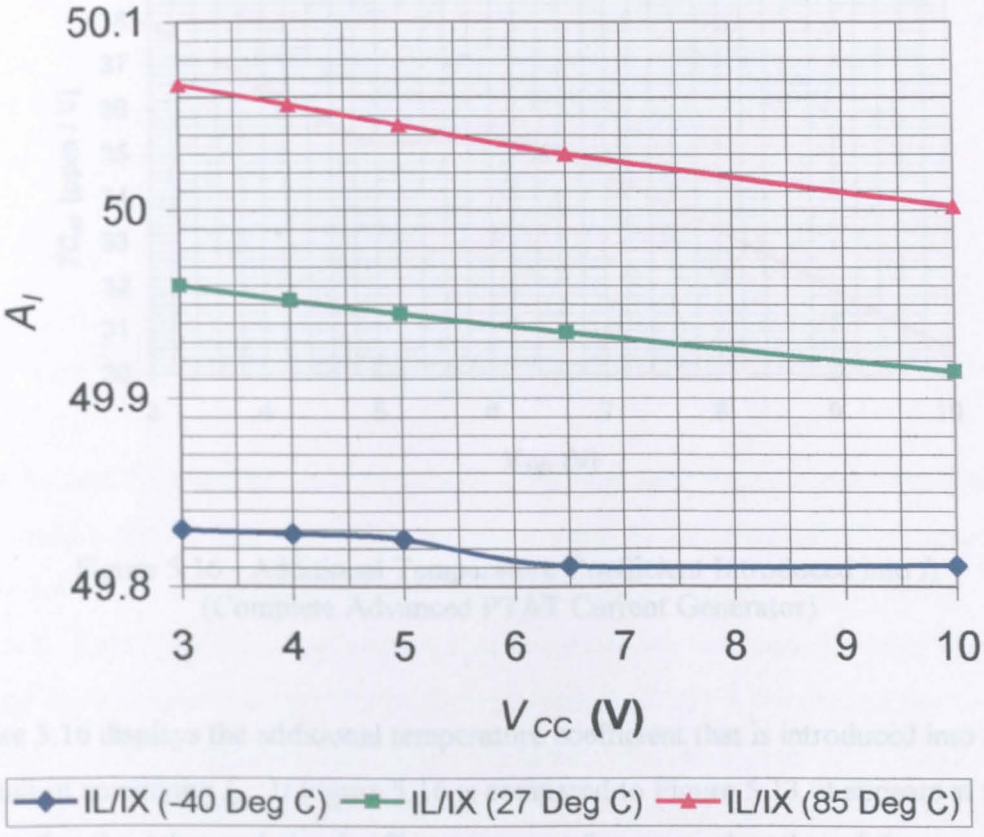

Figure 5.15 - Overall Current Gain of the Complete Advanced *mA* Level PTAT Generator Circuit

Temperature (°C)	$S_{(IX)}$ (ppm/V)	$S_{(IW)}$ (ppm/V)	$S_{(IL)}$ (ppm/V)	$S_{(AI)}$ (ppm/V)
-40	298	246	222	-54
27	288	160	172	-132
85	282	94	96	-186

Table 5.14 – Sensitivity of I_X, I_W, I_L and A_I to Variations in V_{CC} (Complete Advanced PTAT Current Generator)

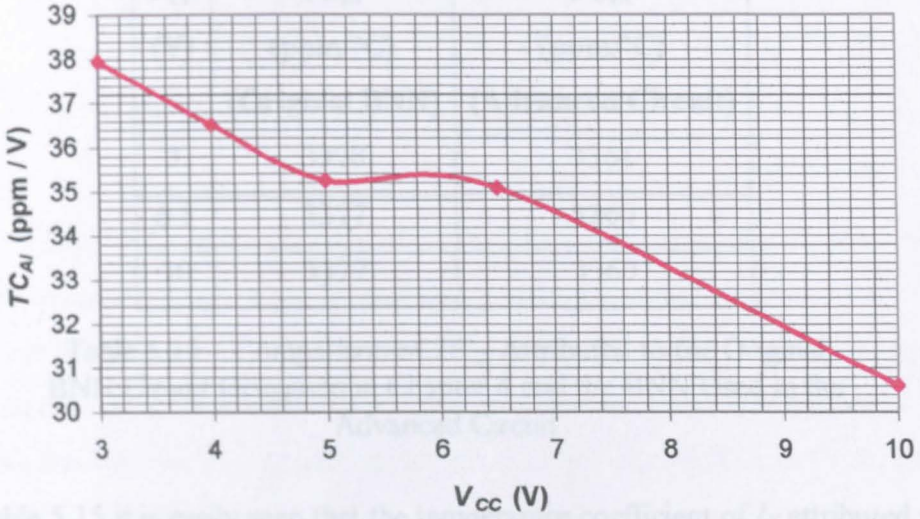

Figure 5.16 - Additional Temperature Coefficient Introduced into I_L
(Complete Advanced PTAT Current Generator)

Figure 5.16 displays the additional temperature coefficient that is introduced into I_L as a result of amplifying I_X. If Figure 5.16 is compared to Figure 5.13, it appears at first glance that the Advanced circuit offers poorer performance, than that of the Intermediate circuit, in terms of the magnitude of the additional temperature coefficient.

However, previous results have already shown that "the temperature coefficients (of I_L and I_W) are significantly closer to the ideal figure of 3332ppm/°C, defined in Chapter 3, than those associated with the previous Intermediate circuit". This can be clearly seen by comparing Table 5.12 with Table 5.8. Thus, TC_{IX} of the Advanced circuit must be smaller than TC_{IX} of the Intermediate circuit. This is expected because the Intermediate circuit employs the HPNN PTAT current generator whereas the Advanced circuit utilises the BNN PTAT current generator and Chapter 4 (Tables 4.1 and 4.3) has already shown that TC_{IX} is superior for the BNN configuration.

Table 5.15 compares the temperature coefficient of the original BNN circuit (described in Chapter 4) at various values of V_{CC} with that of the BNN used in the Advanced circuit.

V_{CC} (V)	TC_{IX} (ppm/°C) (Original BNN)	TC_{IX} (ppm/°C) (Advanced Circuit)
3	3378	3361
6.5	3377	3360
10	3377	3360

Table 5.15 – Comparison of TC_{IX} Attributed to the Original BNN Circuit Discussed in Chapter 4 and the BNN Used in the Advanced Circuit

From Table 5.15 it is easily seen that the temperature coefficient of I_X attributed to the BNN used in the Advanced circuit is superior to that of the original BNN discussed in Chapter 4. However, if the schematic diagrams of each circuit (Figure 5.14 and Figure 5.1) are compared then it seems that there are only two discernable differences. Firstly, three additional currents are mirrored from the BNN in the case of the Advanced circuit. However, this should not affect the overall value of TC_{IX} as a unity current transfer ratio (I_Y/I_X) is still ensured via the loop amplifier. Secondly, the current sources Q_{11}, Q_{12} and Q_{13} of the BNN used in the Advanced circuit have significant resistive emitter degeneration as a result of combining the BNN PTAT current generator and novel CCCS stages. Thus, it is apparent that the emitter degeneration has the effect of reducing TC_{IX} so that it becomes closer to the ideal value. This, in turn, leads to improvement in the output current temperature coefficient (TC_{IL}).

Finally, the overall power consumption of the circuit is tabulated in Table 5.16.

V_{CC} (V)	Total Power Consumption (mW)		
	-40°C	27°C	85°C
3	7.931	10.216	12.206
5	13.528	17.341	20.666
10	28.738	36.364	43.011

Table 5.16 – Total Power Consumption (Complete Advanced PTAT Current Generator)

5.3.5 An Advanced Implementation of a Complete *mA* Level PTAT Current Generator with Reduced Resistor Count

The Advanced form of the *mA* level PTAT current generator offers many benefits in terms of improved performance and reduced component count over previous circuits. However, it suffers from one major drawback. Namely, it requires four resistors to form the novel CCCS and provide current gain. Unfortunately, this circuit requires two more resistors than the previously discussed OA or CC based circuits. Thus, if these resistors were to be integrated then the advanced circuit would require significant chip area to implement them, which may render this solution undesirable.

Figure 5.17 illustrates a full schematic of the complete Advanced Reduced Resistor Version (RRV) PTAT current generator, including 'Start-Up' circuit, that only requires two resistors to form the CCCS element. The total component count for the complete circuit is 37 transistors and 6 resistors.

The operation of each individual circuit block of the Advanced RRV circuit is identical to that of the Advanced circuit (see Figure 5.14). Except that, regarding the Advanced RRV circuit, the BNN PTAT current generator has been modified slightly so that the loop amplifier (Q_4) now controls two high-performance current sources formed from the outputs of a Wilson current mirror ($Q_{11} - Q_{18}$). In addition, R_2, R_3 and R_4 (shown in Figure 5.14) have been removed and replaced with a single new resistor R_N (see Figure 5.17), where R_N is given by:

$$R_N = R_2 // R_3 // R_4 \tag{5.15}$$

Since under normal conditions $R_2 = R_3 = R_4$, (5.15) can be re-expressed as:

$$R_N = \frac{R_2}{3} \tag{5.16}$$

Now, neglecting base currents, the overall current gain of the circuit is given by:

$$A_I = \frac{I_L}{I_X} = N\left(\frac{3R_N}{R_X} - 1\right) \tag{5.17}$$

The total value of resistance required to implement the novel CCCS in both the Advanced and Advanced RRV circuits, respectively, is given by:

$$R_{(Adv)} = 9R_N + R_X \tag{5.18}$$

$$R_{(Uti)} = R_N + R_X \tag{5.19}$$

Assuming these resistors are integrated using resistance squares of unity value. It can be shown that, in terms of the total area needed to implement the resistance attributed to the CCCS of both the Advanced RRV and Advanced circuits, the Advanced RRV circuit offers a Chip Area Saving (CAS) of:

$$CAS = \left(1 - \frac{R_{(AdvRRV)}}{R_{(Adv)}}\right) \times 100 = \left(1 - \frac{R_N + R_X}{9R_N + R_X}\right) \times 100 \quad (\%) \tag{5.20}$$

As before, I_X was set equal to $50\mu A$ at 27°C when V_{CC} = 5V, by trimming R_{PTAT}. The values for R_N, R_X and N were chosen to be 733.33Ω, 200Ω and 5 respectively in order to give an overall current gain of 50, an output current equal to $2.5mA$ and, more importantly, to remain consistent, in terms of voltage drop across the CCCS resistors, with the previous circuits.

Table 5.17 shows the temperature performance of significant currents with varying power supply values.

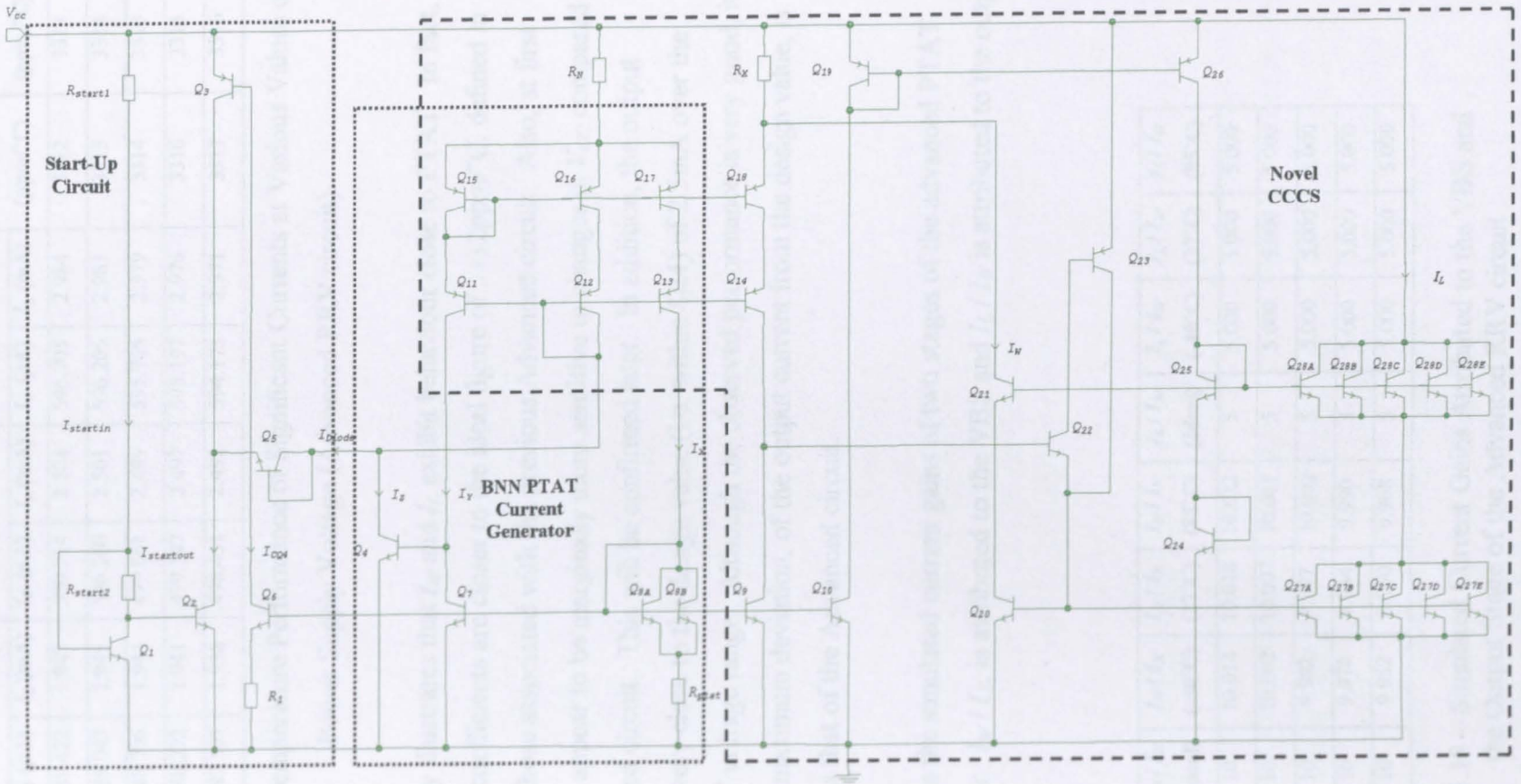

Figure 5.17 - Full Schematic of the Advanced RRV *mA* Level PTAT Current Generator Formed by Integrating the BNN PTAT Current Generator (with associated Start-Up circuit) and Novel CCCS

V_{CC} (V)	I_X (µA)	-40°C		27°C		85°C		$TC_{(IW)}$ (ppm/°C)	$TC_{(IL)}$ (ppm/°C)
		I_W (µA)	I_L (mA)	I_W (µA)	I_L (mA)	I_W (µA)	I_L (mA)		
3	49.980	389.422	1.947	500.714	2.504	596.705	2.984	3312	3313
4	49.990	389.043	1.945	500.260	2.501	596.206	2.981	3313	3314
5	50.000	388.706	1.944	499.861	2.499	595.766	2.979	3314	3313
6.5	50.014	388.272	1.941	499.347	2.497	595.197	2.976	3316	3315
10	50.041	387.507	1.938	498.431	2.492	594.173	2.971	3317	3316

Table 5.17 - Temperature Performance of Significant Currents at Various Values of Power Supply Voltage (Advanced RRV circuit)

Table 5.17 clearly illustrates that I_W and I_L exhibit behaviour close to PTAT. In fact, the temperature coefficients are closer to the ideal figure of 3332ppm/°C, defined in Chapter 3, than those associated with the previous Advanced circuit. Also, at first glance, I_W and I_L appear to be marginally more sensitive to changes in V_{CC} compared with the Advanced circuit. This will be confirmed later. In addition, the output current remains very close to the design value (i.e. within $8\mu A$) of 2.5mA over the entire 3V to 10V voltage range. Although the observed performance is very good, it is noted that the maximum deviation, of the output current from the design value, is twice as worse as that of the Advanced circuit.

Table 5.18 shows the simulated current gains of two stages of the advanced PTAT current generator. I_W / I_X, is attributed to the VBS and I_L / I_W is attributed to the output stage.

V_{CC} (V)	I_W / I_X (Ideal)	I_W / I_X (-40°C)	I_W / I_X (27°C)	I_W / I_X (85°C)	I_L / I_W (Ideal)	I_L / I_W (-40°C)	I_L / I_W (27°C)	I_L / I_W (85°C)
3	10	10.014	10.018	10.022	5	5.000	5.000	5.000
4	10	10.002	10.007	10.011	5	5.000	5.000	5.000
5	10	9.992	9.997	10.002	5	5.000	5.000	5.000
6.5	10	9.978	9.984	9.990	5	5.000	5.000	5.000
10	10	9.952	9.960	9.968	5	5.000	5.000	5.000

Table 5.18 – Simulated Current Gains Attributed to the VBS and the Output Stage of the Advanced RRV circuit

The results indicate that, as before, the current gain of the output stage is virtually power supply and temperature independent and, therefore, remains equal to the ideal design value. In this case, the current gain of the VBS (i.e. I_W / I_X) shows fair agreement with the ideal value over the entire 3V to 10V power supply voltage range but demonstrates more variation than that seen with the Advanced circuit.

The overall current gain of the complete *mA* level PTAT generator circuit, I_L / I_X, is shown in Figure 5.18.

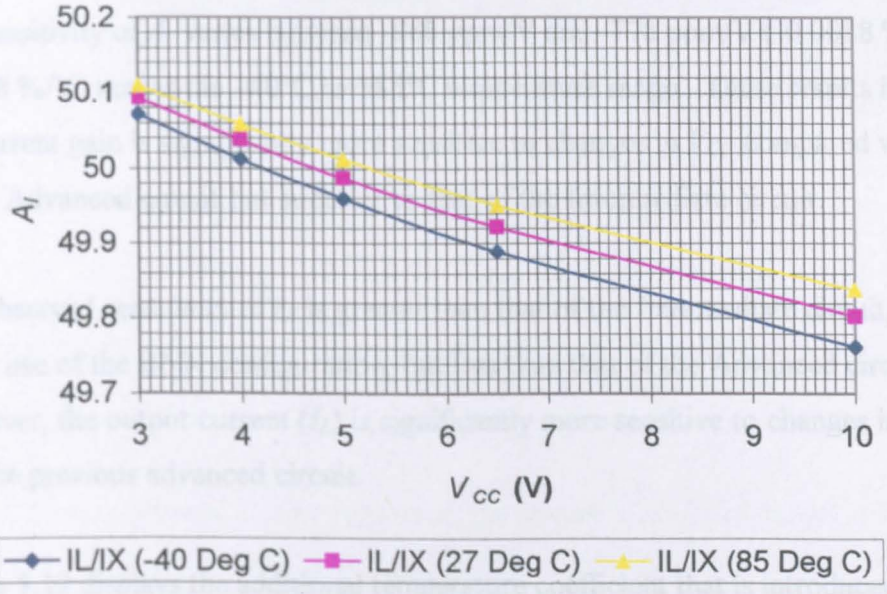

Figure 5.18 - Overall Current Gain of the Complete Advanced RRV *mA* Level PTAT Generator Circuit

The results indicate that the overall gain coheres closely to the ideal figure of 50, across both the 3V to 10V voltage range and –40°C to +85°C temperature range. However, if Figure 5.18 is compared with Figure 5.12 and Figure 5.15, it can be seen that the overall gain of the Advanced RRV circuit demonstrates much closer agreement with the ideal design value of 50 than that of the previous Intermediate circuit but shows worse agreement than that of the Advanced circuit.

The sensitivities of I_X, I_W, I_L and A_I to variations in V_{CC} are shown in Table 5.19.

Temperature (°C)	$S_{(IX)}$ (ppm/V)	$S_{(IW)}$ (ppm/V)	$S_{(IL)}$ (ppm/V)	$S_{(AI)}$ (ppm/V)
-40	180	-705	-662	-888
27	174	-653	-687	-830
85	170	-608	-624	-778

Table 5.19 – Sensitivity of I_X, I_W, I_L and A_I to Variations in V_{CC} for the Complete Advanced RRV PTAT Current Generator

The sensitivity of A_I varies between -888 ppm/V and -778 ppm/V (-0.0888 %/V and -0.0778 %/V) across the –40°C to +85°C temperature range. These results indicate that the current gain is significantly more sensitive to changes in V_{CC} compared with that of the Advanced circuit but superior to that of the Intermediate circuit.

The observed sensitivity of I_X is greater than that of the Intermediate circuit, again due to the use of the BNN configuration, but less than that of the Advanced circuit. However, the output current (I_L) is significantly more sensitive to changes in V_{CC} than that the previous advanced circuit.

Figure 5.19 displays the additional temperature coefficient that is introduced into I_L as a result of amplifying I_X. If Figure 5.19 is compared to Figure 5.13 and Figure 5.16, it is clear that the Advanced RRV circuit offers superior performance, than that of both the Intermediate circuit and Advanced circuit. Thus, the Advanced RRV circuit introduces the least additional temperature coefficient into the output current.

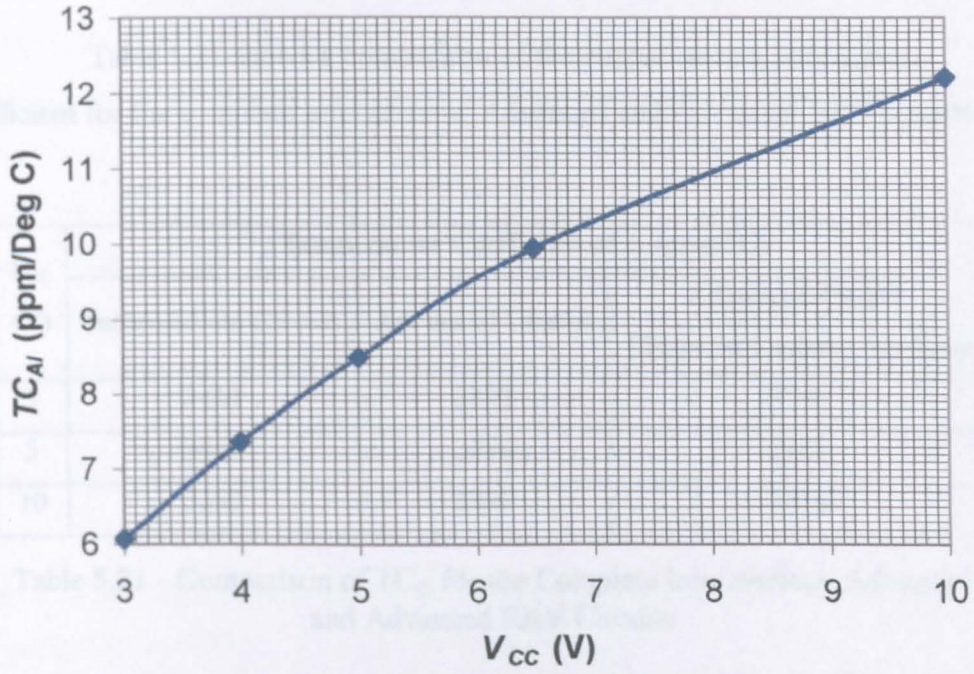

Figure 5.19 - Additional Temperature Coefficient Introduced into I_L for the Complete Advanced RRV PTAT Current Generator

Finally, the overall power consumption of the circuit is tabulated below in Table 5.20.

V_{CC}	**Total Power Consumption (*mW*)**		
(V)	**-40°C**	**27°C**	**85°C**
3	8.035	10.290	12.234
5	13.678	17.440	20.688
10	28.971	36.491	42.984

Table 5.20 – Total Power Consumption of the Complete Advanced RRV PTAT Current Generator

5.3.6 Circuit Performance Comparison

Table 5.21 shows a comparison of the output current temperature coefficient for the complete Intermediate, Advanced and Advanced RRV circuits.

V_{CC} (V)	Temperature Coefficient of I_L (ppm/°C)		
	Intermediate Circuit	**Advanced Circuit**	**Advanced Circuit (Reduced Resistor Version)**
3	3414	3397	3313
5	3405	3396	3313
10	3392	3390	3316

Table 5.21 - Comparison of TC_{IL} for the Complete Intermediate, Advanced and Advanced RRV Circuits

As calculated in Chapter 3, the ideal temperature coefficient of a PTAT current is 3332 ppm/°C. Thus, it is clear from the above results that the Advanced RRV circuit exhibits behaviour that is considerably closer to the ideal than that of the other two circuits. The Advanced circuit demonstrates the second best performance with the Intermediate circuit showing a poor third.

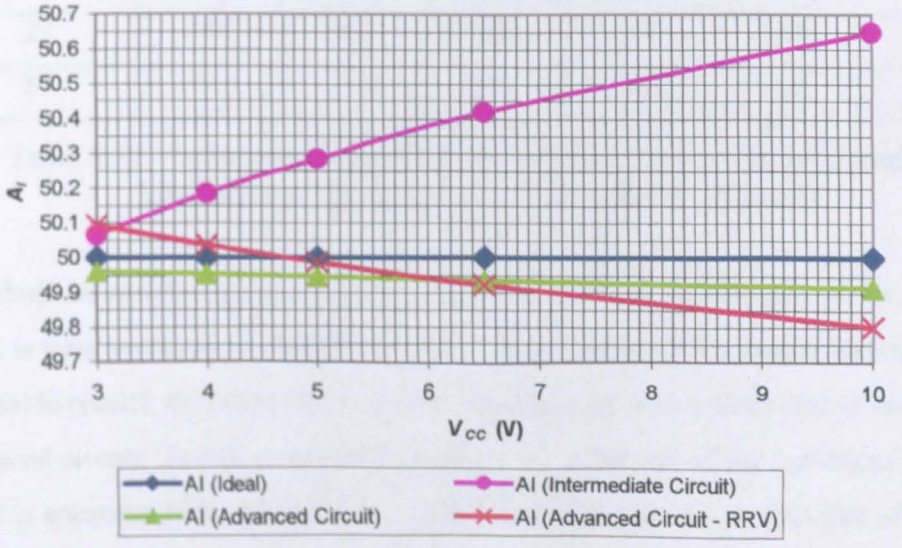

Figure 5.20 - Comparison of A_I at 27°C for the Complete Intermediate, Advanced and Advanced RRV Circuits

Figure 5.20 illustrates a comparison of current gain for the complete Intermediate, Advanced and Advanced RRV circuits. The current gain of the Advanced circuit is closest to the ideal design target of 50 across the 3V to 10V voltage range. The Advanced RRV circuit also offers good performance but is much more sensitive to the value of V_{CC}. The Intermediate circuit works as a proof of concept but, in comparison, is significantly more sensitive to changes in V_{CC} than the other two circuits. This is confirmed in Table 5.22 below. An interesting point of note is that the current gain of the Intermediate circuit increases with VCC. This contrasts with the current gain behaviour of the Advanced and Advanced RRV implementations, which decreases as VCC is increased. The exact mechanism behind this behaviour reversal is as yet unknown and requires further investigation.

Table 5.22 displays a comparison of the sensitivity of the current gain and output current to changes in V_{CC} (3V to 10V voltage range).

Temperature (°C)	Intermediate Circuit		Advanced Circuit		Advanced Circuit (Reduced Resistor Version)	
	$S_{(IL)}$ (ppm/V)	$S_{(AI)}$ (ppm/V)	$S_{(IL)}$ (ppm/V)	$S_{(AI)}$ (ppm/V)	$S_{(IL)}$ (ppm/V)	$S_{(AI)}$ (ppm/V)
-40	1906	1859	222	-54	-662	-888
27	1700	1658	172	-132	-687	-830
85	1514	1529	96	-186	-624	-778

Table 5.22 - Sensitivity of I_L and A_I to Variations in V_{CC} for the Complete Intermediate, Advanced and Advanced RRV Circuits

The tabulated results indicate that the output current and current gain of the Advanced circuit is least sensitive to changes in V_{CC}. The Advanced RRV circuit also provides reasonable results, however, these are still significantly worse than that of the Advanced circuit. For example, at 27°C the output current of the Advanced RRV circuit is approximately 4 times more sensitive to changes in V_{CC} than that of the Advanced circuit. Similarly, at 27°C the current gain of the Advanced RRV circuit is

approximately 6 times more sensitive to changes in V_{CC} than that of the Advanced circuit. Finally, it is clear from the table that the Intermediate circuit offers significantly poorer results than either of the other two circuits.

Table 5.23 demonstrates a comparison of the total DC power consumption at various temperature and V_{CC} values.

V_{CC}	Intermediate Circuit DC Power Consumption (mW)			Advanced Circuit DC Power Consumption (mW)			Advanced Circuit (Reduced Resistor Version) DC Power Consumption (mW)		
(V)	-40°C	27°C	85°C	-40°C	27°C	85°C	-40°C	27°C	85°C
3	8.165	10.532	12.596	7.931	10.216	12.206	8.035	10.290	12.234
5	13.976	17.934	21.329	13.528	17.341	20.666	13.678	17.440	20.688
10	29.813	37.774	44.720	28.738	36.364	43.011	28.971	36.491	42.984

Table 5.23 – Comparison of Total DC Power Consumption for the Complete Intermediate, Advanced and Advanced RRV Circuits

The results show that the total DC power consumption for each circuit is fairly constant. However, the Advanced circuit offers a small power saving over the other two circuits. The Advanced RRV circuit consumes marginally more power than the Advanced circuit. The Intermediate circuit is again the worst performer.

The resistor total required (including 'Start-Up' and PTAT Current Generator blocks) to implement each circuit is also of importance since each additional resistor increases the chip area required. These values are shown in Table 5.24.

Circuit	Total Resistors Required
Intermediate	6
Advanced	8
Advanced (RRV)	6

Table 5.24 – Total of Resistors Required to Implement the Complete Intermediate, Advanced and Advanced RRV Circuits (including 'Start-Up' and PTAT Current Generator blocks)

Finally, a marking scheme is employed in order to evaluate each circuit regarding each of the previously mentioned criteria in this section. Circuits are awarded three points for offering the best performance, two points for second best performance and one point for worst performance in a particular category. Table 5.25 illustrates the results.

Marking Criteria	Intermediate Circuit	Advanced Circuit	Advanced Circuit (RRV)
TC Closest to Ideal	1	2	3
Accuracy of A_I (V_{CC}=5V, T=27°C)	1	2	3
Sensitivity of A_I and I_L	1	3	2
Total DC Power Consumption	1	3	2
Total Resistors Required	3	1	3
Total	**7**	**11**	**13**

Table 5.25 – Performance Evaluation of the Complete Intermediate, Advanced and Advanced RRV Circuits

From the Table 5.25, it is clear that the Advanced RRV circuit offers the best overall performance, followed by the Advanced circuit and the Intermediate circuit. However, the Advanced circuit does also offer very good accuracy of A_I that is very close to that provided by the RRV circuit. If the sensitivity of I_L and A_I are considered more important than the other areas of performance, the Advanced circuit may provide the best results. It is left up to the designer to consider the 'pros and cons' and choose the appropriate topology.

5.4 Summary

This Chapter highlighted the need for a 'current converter / amplifier that can scale-up a reference current, accurately, and without introducing any significant additional temperature coefficient.' This was necessary in order to produce accurate mA level PTAT currents for biasing a bipolar LNA.

Section 5.1 reviewed a range of existing VCCS techniques, that relied on the use of OAs and CCs, which could be utilised to provide a *mA* level output current. Similarly, Section 5.2 discussed a range of common CCCS techniques that relied on the use of either current mirrors or OAs and CCs, which could also be utilised to provide a *mA* level output current. It was found that CCCS circuits are inherently temperature independent, and hence of the two approaches, VCCS or CCCS, the latter is more attractive. However, traditional methods often result in an overly elaborate circuit with a comparatively high component count. This in turn, may waste valuable chip area and result in a circuit that typically is not able to operate at low supply voltages. Thus, the need for a new form of CCCS was highlighted.

Sections 5.3 – 5.3.1introduced a novel form of CCCS proposed by the author. This new technique has been presented in technical literature [8-10] and has led to a patent application [11]. Subsequent Sections 5.3.2 to 5.3.5 discussed four different implementations of this technique and these are compared in terms of overall performance in Section 5.3.6.

An Advanced implementation of the novel CCCS was presented which produced an accurate output current, exhibiting close to ideal PTAT behaviour. In addition, the current gain and output current of this circuit demonstrated very high insensitivity to variations in power supply. Although, a drawback of this topology is that four resistors are required to define the current gain.

In order to overcome this disadvantage, a further reduced resistor version of the novel CCCS was presented. This required only two resistors to define the current gain (i.e. the same as traditional OA or CC based circuits) and produced an output current with improved PTAT behaviour. However, this was achieved at the expense of increased sensitivity of the current gain and output current to variations in power supply voltage.

It was found that the Advanced RRV circuit produce superior overall results. However, if the sensitivity of current gain and output current are considered high priority parameters then the Advanced circuit provides a very capable alternative.

5.5 References

[1] A. S. Grove, *Physics and Technology of Semiconductor Devices*, Wiley, New York, 1967, Chapter 7.

[2] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits (Third Edition)*, McGraw-Hill International Editions, 2002, pp. 63-71.

[3] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits (Third Edition)*, McGraw-Hill International Editions, 2002, pp. 66-70.

[4] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits (Third Edition)*, McGraw-Hill International Editions, 2002, pp. 70-71.

[5] C. Toumazou, F.J. Lidgey and D.G. Haigh, *Analogue IC Design: the current mode approach*, IEE Circuits and Systems Series 2, Peter Peregrinus Ltd, 1990, pp. 101.

[6] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits (Third Edition)*, McGraw-Hill International Editions, 2002, pp. 71-73.

[7] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits (Fourth Edition)*, John Wiley and Sons, New York, 2001, pp. 253-278.

[8] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'Temperature-Independent Direct Current Converter Technique', *IEE Electronic Letters*, Nov. 2005, Vol. 41, No. 23, pp. 1258-1259.

[9] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'PTAT Direct Current Converter for Bias Circuit Applications', *IEE Electronic Letters*, Apr. 2006, Vol. 42, No. 9, pp. 530-531.

[10] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'A Novel *mA* Level PTAT Current Generator Technique', *Proceedings of North East Workshop on Circuits And Systems (NEWCAS)*, Gatineau, Canada, June 2006, pp. 221-224.

[11] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'Direct Current Converter Circuit', *UK Patent Application GB051623.8*, 2005.

CHAPTER 6

Development of a Constant Gain LNA

6.1 A Constant Gain LNA Circuit

A LNA with novel constant gain bias circuit can now be developed. This is achieved by combination of the final LNA design of Chapter 2 and the 'Advanced RRV' PTAT CCCS of Chapter 5, as illustrated in Figure 6.1.

As discussed previously in Section 2.2.1, the collector current of the LNA input transistor Q_{22} should equal 1.5mA (I_{COPT}) in order to allow optimum noise performance. Now, neglecting base currents, $I_{C22} = I_L$. In this case, R_{PTAT} is adjusted so that $I_X = 50\mu A$ at 27°C. Therefore, the required current gain to be provided by the CCCS is defined as $A_I = \frac{I_L}{I_X} = \frac{1.5mA}{50\mu A} = 30$.

In order to ensure that $ROPT = 50\Omega$, and thus, facilitate simultaneous noise and impedance matching as defined in Chapter 2, N must equal 1. R_N and R_X are then chosen as $1.1K\Omega$ and 100Ω, respectively, in order to satisfy (5.17) so that $A_I = 30$.

I_X, I_1, I_2, I_W and I_L are measured at 27°C ($V_{CC} = 5V$) in order to test DC performance. These results are tabulated in Table 6.1.

$I_X (\mu A)$	$I_1 (\mu A)$	$I_2 (\mu A)$	$I_L (mA)$	A_I
50	53.180	53.587	1.624	32.484

Table 6.1 – DC current Values and Gain at 27°C ($V_{CC} = 5V$)

From Table 6.1, it is clear that the simulated current gain is greater than the desired value of 30. This is because (5.17), from which the desired value is obtained, assumes that $I_X = I_1 = I_2$. However, if I_2 (the current which exhibits greatest deviation from I_X) is substituted for I_X in (5.17) the current gain becomes:

$$AI = \frac{I_L}{I_2} = N\left(\frac{3RN}{RX} - 1\right) \qquad (6.1)$$

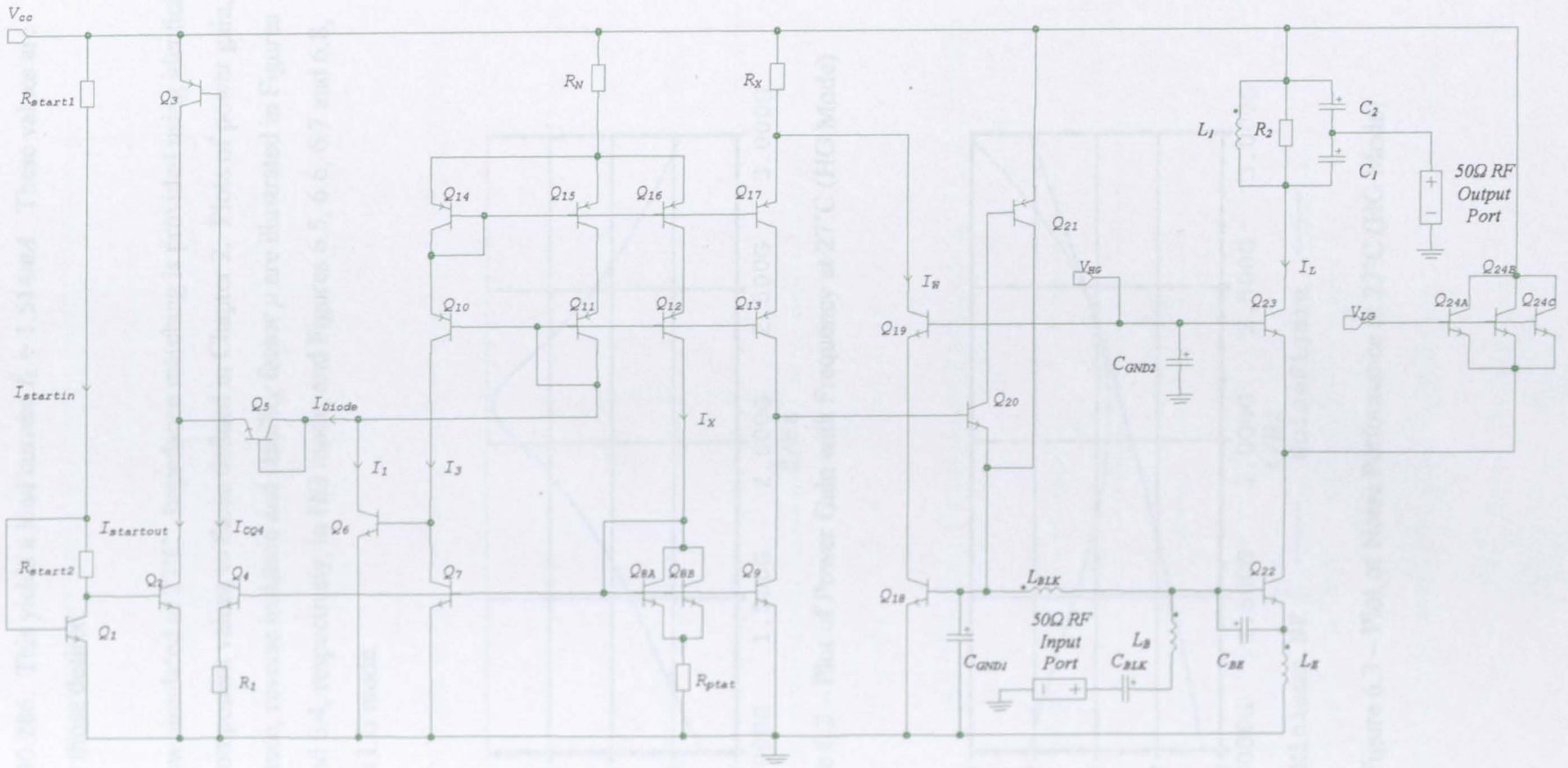

Figure 6.1 – Schematic of Final LNA with Novel CCCS Bias Circuit.

R_{PTAT} is now re-adjusted so that $I_2 = 50\mu A$ at 27°C and the measured current gain becomes $A_I = 30.286$. This yields a load current $I_L = 1.514mA$. These values are much closer to those desired.

The LNA is now simulated at 27°C. Impedance matching is provided using identical methods and component values to those defined in Chapter 2. Plots of power gain, noise performance, reverse isolation and stability factor μ are illustrated in Figures 6.2, 6.3, 6.4 and 6.4, respectively, in HG mode, and Figures 6.5, 6.6, 6.7 and 6.8, respectively, in LG mode.

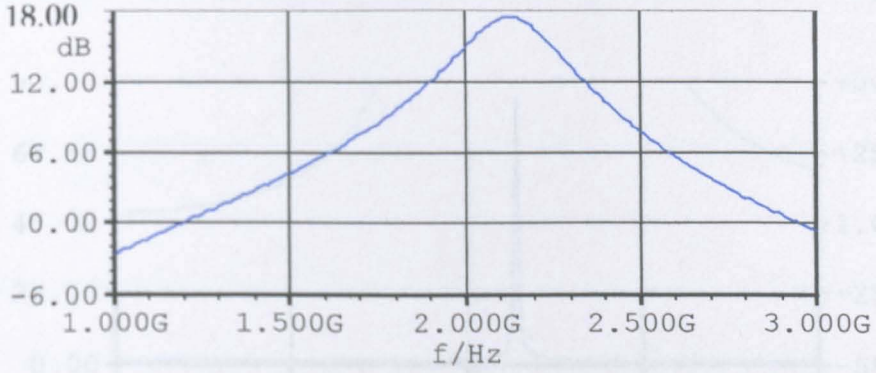

Figure 6.2 – Plot of Power Gain with Frequency at 27°C (HG Mode)

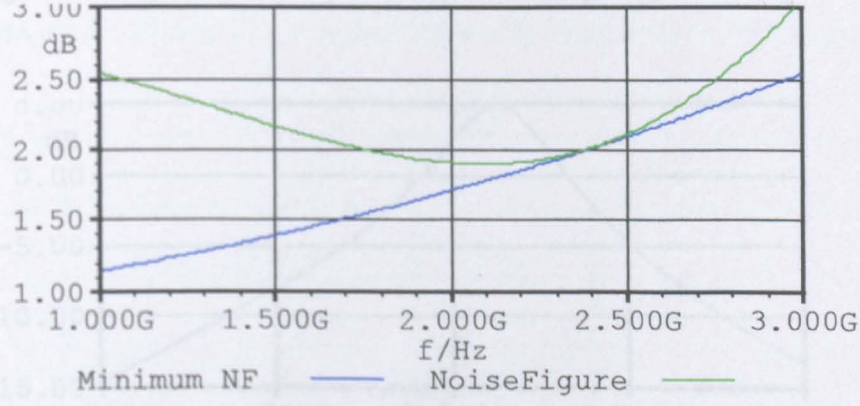

Figure 6.3 – Plot of Noise Performance at 27°C (HG Mode)

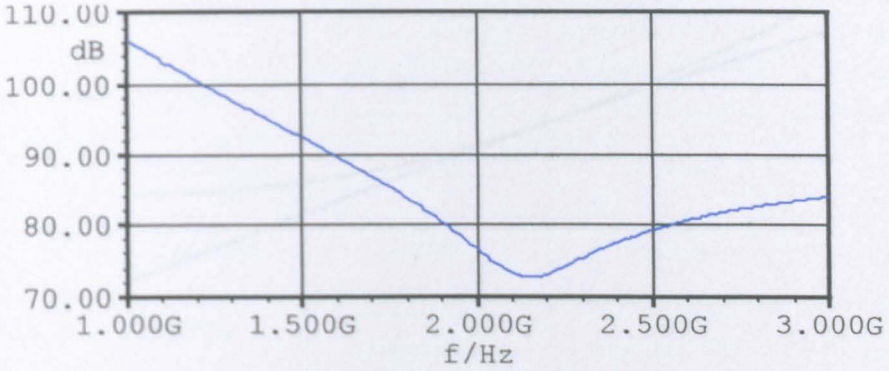

Figure 6.4 – Plot of Reverse Isolation with Frequency at 27°C (HG Mode)

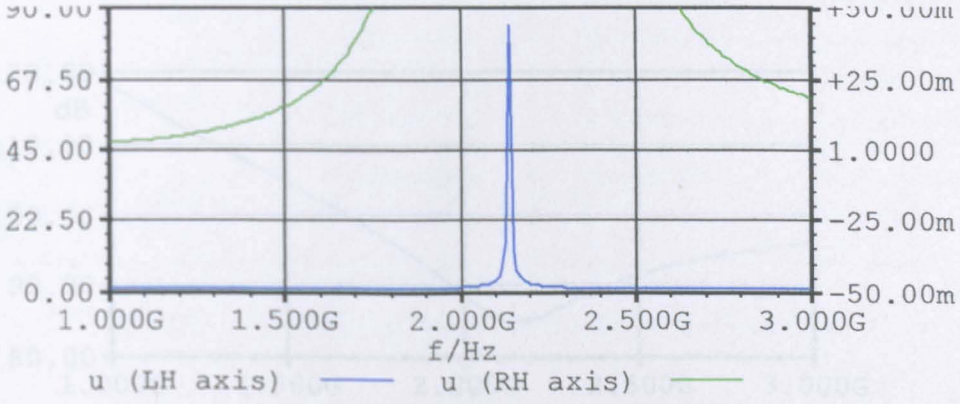

Figure 6.5 – Plot of Stability Factor μ with Frequency at 27°C (HG Mode)

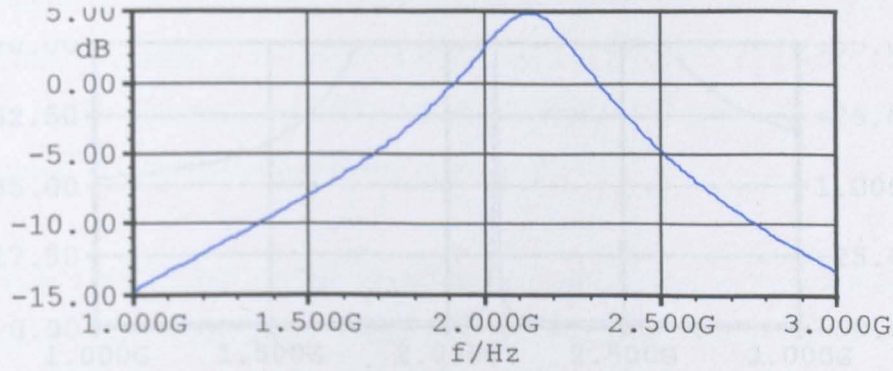

Figure 6.6 – Plot of Power Gain with Frequency at 27°C (LG Mode)

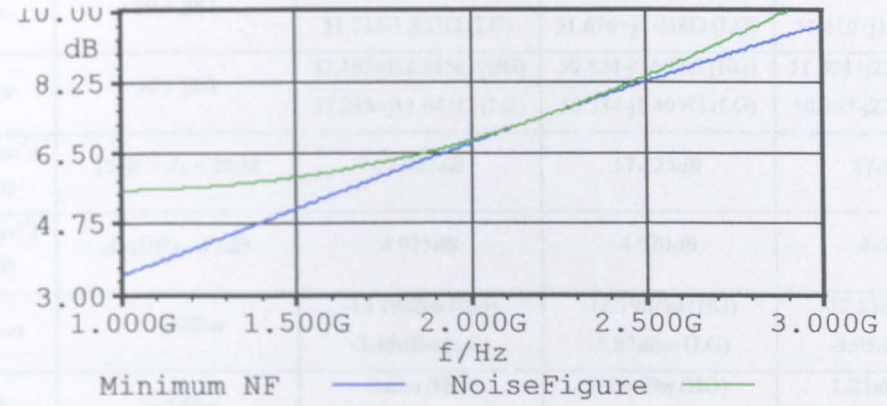

Figure 6.7 – Plot of Noise Performance with Frequency at 27°C (LG Mode)

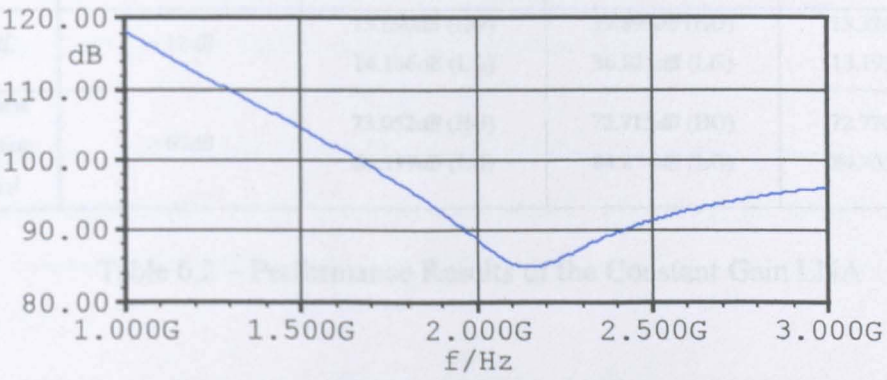

Figure 6.8 – Plot of Noise Performance with Frequency at 27°C (LG Mode)

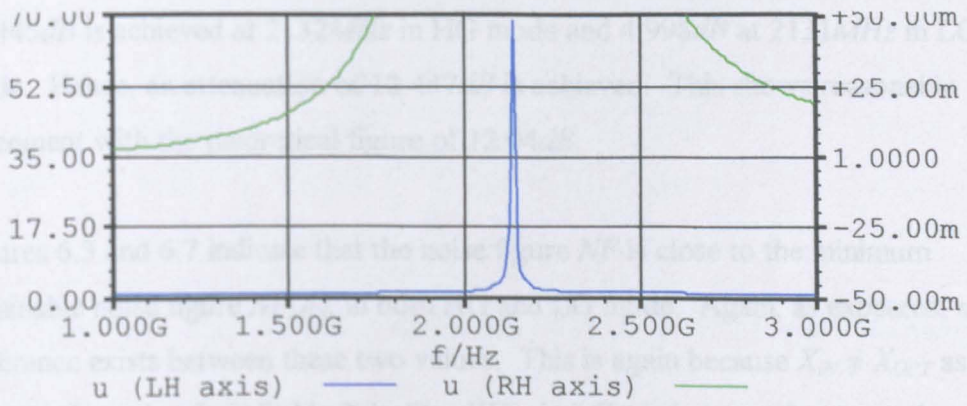

Figure 6. 9 – Plot of Stability Factor μ with Frequency at 27°C (LG Mode)

LNA Parameters	Targeted Values (2110*MHz* - 2170*MHz*)	Simulated Results (27°C)		
		2110*MHz*	2140*MHz*	2170*MHz*
Z_{IN}	50 + j0Ω	50.668-j1.593Ω (HG) 51.743-1.853Ω (LG)	50.595+j0.327Ω (HG) 51.676+j0.038Ω (LG)	50.538+j2.218Ω (HG) 51.610+j1.903Ω (LG)
Z_{OUT}	50 + j0Ω	37.165+j12.315Ω (HG) 37.288+j11.641Ω (LG)	50.824-j0.603Ω (HG) 50.334-j1.407Ω (LG)	51.304+j22.348Ω (HG) 50.363-j22.518Ω (LG)
$A_P(\lvert S_{21}\rvert^2)$ (HG)	15*dB* > A_P < 20*dB*	17.357*dB*	17.423*dB*	17.102*dB*
$A_P(\lvert S_{21}\rvert^2)$ (LG)	A_P(HG) - 12*dB*	4.925*dB*	4.970*dB*	4.633*dB*
ICP_{-1dB}	> -15*dBm*	-12.19*dBm* (HG) -3.45*dBm* (LG)	-12.79*dBm* (HG) -3.87*dBm* (LG)	-12.81*dBm* (HG) -3.95*dBm* (LG)
IIP_3	> -5*dBm*	0*dBm* (HG) -1.78*dBm* (LG)	0.04*dBm* (HG) -1.07*dBm* (LG)	1.23*dBm* (HG) -1.77*dBm* (LG)
NF	< 2*dB* (HG) <5*dB* (LG)	1.801*dB* (HG) 7.106*dB* (LG)	1.803*dB* (HG) 7.185*dB* (LG)	1.808*dB* (HG) 7.278*dB* (LG)
IRL	> 12*dB*	35.311*dB* (HG) 32.041*dB* (LG)	43.419*dB* (HG) 35.659*dB* (LG)	32.880*dB* (HG) 32.206*dB* (LG)
ORL	> 12*dB*	13.890*dB* (HG) 14.166*dB* (LG)	39.899*dB* (HG) 36.825*dB* (LG)	13.320*dB* (HG) 13.193*dB* (LG)
Reverse Isolation ($-S_{12}$)	> 60*dB*	73.052*dB* (HG) 85.199*dB* (LG)	72.715*dB* (HG) 84.874*dB* (LG)	72.770*dB* (HG) 84.935*dB* (LG)

Table 6.2 – Performance Results of the Constant Gain LNA

From Figures 6.2, 6.5, 6.6 and 6.9, it is clear that the LNA is unconditionally stable, in both HG and LG modes, at all frequencies at which the LNA provides gain (i.e. $A_P > 1$). Therefore, the LNA is free of any undesired oscillations. A peak power gain of 17.445*dB* is achieved at 2132*MHz* in HG mode and 4.998*dB* at 2131*MHz* in LG mode. Hence, an attenuation of 12.447*dB* is achieved. This shows reasonable agreement with the theoretical figure of 12.04*dB*.

Figures 6.3 and 6.7 indicate that the noise figure *NF* is close to the minimum obtainable noise figure NF_{MIN}, in both HG and LG mode. Again, as expected, a small difference exists between these two values. This is again because $X_{IN} \neq X_{OPT}$ as illustrated previously in Table 2.4. The *NF* is in LG mode is much greater than that of the LNA designs in Chapter 2. The reason for this is as yet unclear, however, since the only discernable difference between them is the addition of the 'Advanced RRV'

CCCS circuit, then, the cause is likely to stem from this. Figures 6.4 and 6.8 show that the reverse isolation is very good (>74*dB*) at all frequencies.

From Table 6.2 it is clear that the complete LNA meets the target specification, across the 2110*MHz* to 2170*MHz* frequency range at 27°C in HG mode. This is also true in LG mode with the exception of NF. However, this is not such a disaster as it might first appear since the purpose of the LG mode is to extend the dynamic range of the LNA. In this case the dynamic range is extended by the difference between the 1*dB* compression points in HG and LG mode minus the difference between the NFs in HG and LG modes (i.e. $(ICP_{-1dB(LG)} - ICP_{-1dB(HG)}) - (NF_{(LG)} - NF_{(HG)})$). Thus, the dynamic range is increased by 3.435dB, 3.538dB and 3.390dB at 2110MHz, 2140MHz and 2170MHz, respectively, in LG mode. However, further noise analysis, in order to determine the cause of and ultimately reduce the *NF* in LG mode, would be beneficial in the future in order to further extend the dynamic range.

The final key aspect of the LNA is that it should also provide constant power gain across the entire –40°C to 85°C temperature range. Therefore, the circuit of Figure 6.1 is re-simulated at –40°C and 85°C. These corresponding gain values are shown in Table 6.3.

Mode	Frequency (*MHz*)	A_P @ -40°C (*dB*)	A_P @ 27°C (*dB*)	A_P @ 85°C (*dB*)	Total A_P Variation (*dB*)
HG	2110	17.456	17.357	17.256	0.200
	2140	17.537	17.423	17.318	0.219
	2170	17.229	17.102	16.992	0.237
LG	2110	5.038	4.925	4.813	0.225
	2140	5.097	4.970	4.855	0.242
	2170	4.773	4.633	4.515	0.258

Table 6.3 – Gain Variation Across the –40°C to 85°C Temperature Range

From Table 6.3, a total gain variation of between 0.2*dB* and 0.258*dB* is seen at 2110*MHz*, 2140*MHz* and 2170*MHz*. Therefore, this circuit offers dramatic improvement, in terms of gain variation, over the LNA design with standard current

mirror type bias circuit (Figure 2.25) presented in Chapter 2. The total gain variation improvement is quantified in Table 6.4.

Mode	Frequency (*MHz*)	Total A_P Variation (Figure 2.25) (*dB*)	Total A_P Variation (Figure 6.1) (*dB*)	Total Improvement in A_P Variation (*dB*)
HG	2110	1.488	0.200	1.288
	2140	1.500	0.219	1.281
	2170	1.514	0.237	1.277
LG	2110	1.675	0.225	1.450
	2140	1.682	0.242	1.440
	2170	1.692	0.258	1.434

Table 6.4 – Total Gain Variation Improvement with 'Advanced RRV' Bias Circuit Over Standard Current Mirror Type Circuit

6.2 Summary

A constant gain LNA, formed by combination of the novel 'Advanced RRV' CCCS of Chapter 5 and the LNA design of Chapter 2, has been presented. This circuit has met the target specification of Chapter 1 with the exception of *NF* in LG mode. However, a dynamic range extension of between 3.390*dB* and 3.538*dB* in LG mode was provided across the 2110*MHz* to 2170*MHz* bandwidth. Furthermore, the LNA reduced the gain variation, across the same bandwidth, to between 0.2*dB* and 0.237*dB*, in HG mode, and 0.225*dB* and 0.258*dB*, in LG mode, across the entire -40°C to 85°C industrial temperature range.

CHAPTER 7

Conclusion and Future Work

7.1 Conclusion

In recent years the introduction of numerous telecommunication products and systems has created enormous growth in the telecommunications industry. Increased complexity of these products has led to the need for LNAs that will meet an ever-demanding specification; this is especially true of circuits intended for use with 3G mobile networks. Thus, LNA design is an active area of interest in the research community. However, in the author's view, the incidences of novel bias circuit design techniques in the technical literature, which are suitable for use in LNA design, are few and far between.

Most bias circuits seen in the technical literature rely on the use of practically identical current mirror schemes. Therefore, the major motivation behind and main focus of this thesis was to improve on traditional bias circuit design for LNA applications. Particularly, with regards to, providing temperature-independent DC current amplification of a much smaller temperature-dependent reference current (i.e. a Bandgap or PTAT current). The amplified output current can then be used to ensure that the LNA will maintain either constant voltage gain or DC power consumption across a wide temperature range.

Chapter 1 identified and explained key parameters that are important to LNA design. A performance specification, to which the final LNA subsequent designs were targeted, was also described.

In Chapter 2 a LNA design procedure was outlined for use with unilateral designs in order to obtain a minimum noise figure with maximum power transfer using well-established techniques. A LNA design with both High Gain and Low Gain modes was presented, which met the specification of Chapter 1 at 27°C. However, the uncompensated bias scheme produced large variations in gain with temperature. Thus, highlighting the need for a bias scheme that compensates for variations in temperature.

In order to achieve constant gain collector current of a bipolar LNA should be made proportional to absolute temperature (PTAT). The most common form of PTAT current generator technique, known as bootstrap biasing, was discussed in Chapter 3. Numerous combinations of current source and current mirror were analysed and compared. However, it was found that the bootstrap scheme inherently suffers from power supply sensitivity, thus, reducing the output current accuracy. A Start-Up circuit was also presented.

Chapter 4 introduced an alternative form of PTAT current generator circuit first proposed by Nauta and Nordholt in 1985 [1]. This offered improvements over the bootstrap bias technique since it is less sensitive to power supply variations, thus, resulting in an improved output current accuracy. However, those authors had not taken into account the impact of Early voltage mismatches present in these circuits. The author addressed this with extensive analysis in Section 4.1.2.2. It was found that provided the mismatch is kept below 3.4%, then, the measured sensitivity, of the Nauta and Nordholt circuit, to variations in power supply exceeds that of the best 'bootstrap bias' type circuit (i.e. the BWCS+VFCM) topology with zero Early voltage mismatch.

Neither of the techniques discussed in Chapters 3 and 4 are suitable for directly producing large *mA* level output currents, which are required for LNA biasing in order to maintain sufficient linearity. Therefore, a need exists for some form of current amplifier / converter that can scale up a small PTAT reference current or convert a PTAT voltage in to a *mA* level output current, accurately, without introducing any additional temperature coefficient. Traditional techniques VCCS and CCCS approaches were investigated in Chapter 5. However, these relied on the use of OAs or CCs; often resulting in an over elaborate circuit with a relatively high component count. The author proposed an alternative and novel form of CCCS used to scale up a PTAT reference current. This work has led to a patent application [2] and technical publications [3-5].

Chapter 6 culminated in the presentation of a constant gain LNA formed by combination of the novel 'Advanced RRV' CCCS of Chapter 5 and the LNA design

of Chapter 2. This circuit has met the target specification of Chapter 1 with the exception of *NF* in LG mode. However, a dynamic range extension of between 3.390*dB* and 3.538*dB* in LG mode was provided across the 2110*MHz* to 2170*MHz* bandwidth. Furthermore, the LNA reduced the gain variation, across the same bandwidth, to between 0.2*dB* and 0.237*dB*, in HG mode, and 0.225*dB* and 0.258*dB*, in LG mode, across the entire -40°C to 85°C industrial temperature range.

7.2 Future Work

Building on the results of this thesis, the author suggests that the next step would be to fabricate the LNA in order to compare the actual measured performance with the simulated results presented in this thesis.

However, the main outcome of this thesis is the development of a novel form of CCCS. Although the CCCS has been developed to provide DC current amplification in amplifier bias circuits, its use may not be limited to this application. In order to define other useful applications, it would be particularly worthwhile to evaluate the AC performance of this topology and define its limitations. The author is currently undertaking this work.

The reduced resistor version is a particularly attractive CCCS topology for further development as only two resistors define its current gain, thus reducing the required chip area and, hence, resulting in a circuit that provides a high quality alternative to more traditional OA or CC based CCCS designs. Indeed, it may be particularly beneficial to develop a reduced resistor type novel CCCS for use with a modern deep sub-micron CMOS process. This would allow the passive 'gain control' resistors to be replaced with active resistors formed from CMOS devices. This approach allows a higher level of integration, thus, dramatically reducing chip area. The use of CMOS devices will also enable operation at very low power supply voltages (i.e. <1.5V) and would significantly reduce power consumption.

Although not presented here, the author has begun preliminary design work of a novel CCCS in a 0.18um CMOS process. Initial simulation results are promising. A detailed investigation of AC performance will be undertaken in order to optimise frequency response and these findings will be presented future technical literature. The author intends to fabricate a CMOS CCCS demonstrator IC in order to provide proof of concept and verify simulation results.

Finally, it is hoped that the CCCS techniques presented in this thesis may become a standard circuit block in the analogue circuit designer's toolkit, offering a viable alternative to traditional OA and CC based designs.

7.3 References

[1] H. C. Nauta and E. H. Nordholt, 'A New Class of High-Performance PTAT Current Generators', *Electronic Letters*, Vol. 21, No. 9, Apr. 1985, pp. 384-386.

[2] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'Direct Current Converter Circuit', *UK Patent Application GB0516231.8*, 2005.

[3] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'Temperature-Independent Direct Current Converter Technique', *IEE Electronic Letters*, Nov. 2005, Vol. 41, No. 23, pp. 1258-1259.

[4] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'PTAT Direct Current Converter for Bias Circuit Applications', *IEE Electronic Letters*, Apr. 2006, Vol. 42, No. 9, pp. 530-531.

[5] M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey, 'A Novel *mA* Level PTAT Current Generator Technique', *Proceedings of North East Workshop on Circuits And Systems (NEWCAS)*, Gatineau, Canada, June 2006, pp. 221-224.

APPENDIX A

A.1 Defining the Output Current of a Basic Widlar Current Source

A.2 Defining the Output Current of a Buffered Widlar Current Source

A.3 Defining the Output Current of a Wilson Current Source

A.4 Defining the Sensitivity of the Output Current of a Wilson Current Source to Changes in Power Supply Voltage

A.5 Method Used to Determine the Forward Emission Coefficient (n) of a NPN Transistor

A.1 Defining the Output Current of a Basic Widlar Current Source

Applying KVL around the base emitter loop gives:

$$V_{be1} - V_{be2} - \frac{\beta_2 + 1}{\beta_2} I_{out} R_1 = 0 \qquad \text{(A.1)}$$

Where:

$$V_{be1} = V_T \ln \frac{I_{C1}}{I_{S1}} - \frac{V_T V_{ce1}}{V_A} \qquad \text{(A.2)}$$

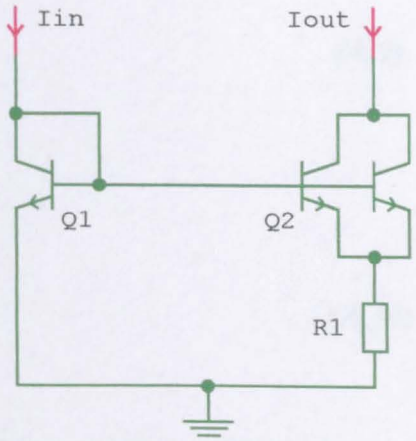

Figure A.1 – A Widlar Current Source

And:

$$V_{be2} = V_T \ln \frac{I_{out}}{I_{S2}} - \frac{V_T V_{ce2}}{V_A} \qquad \text{(A.3)}$$

Therefore:

$$\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{out}}{I_{S2}} = \left[\frac{\beta_2 + 1}{\beta_2} I_{out} R_1 + V_T \frac{V_{ce1} - V_{ce2}}{V_A} \right] \frac{1}{V_T} \qquad \text{(A.4)}$$

$$\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{out}}{I_{S2}} = \frac{\beta_2 + 1}{\beta_2} \frac{I_{out} R_1}{V_T} + \frac{V_{ce1} - V_{ce2}}{V_A} \qquad \text{(A.5)}$$

$$\ln \left(\frac{I_{C1}}{I_{out}} \frac{I_{S1}}{I_{S2}} \right) = \frac{\beta_2 + 1}{\beta_2} \frac{I_{out} R_1}{V_T} + \frac{V_{ce1} - V_{ce2}}{V_A} \qquad \text{(A.6)}$$

$$\ln \left(\frac{I_{C1}}{I_{out}} \frac{I_{S1}}{I_{S2}} \right) + \frac{V_{ce2} - V_{ce1}}{V_A} = \frac{\beta_2 + 1}{\beta_2} \frac{I_{out} R_1}{V_T} \qquad \text{(A.7)}$$

$$I_{out} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\left[\ln\left(\frac{I_{C1}}{I_{out}}\frac{I_{S1}}{I_{S2}}\right)+\frac{V_{ce2}-V_{ce1}}{V_A}\right] \tag{A.8}$$

By definition:

$$I_{in} = I_{C1}+\frac{I_{C1}}{\beta_1}+\frac{I_{out}}{\beta_2} \tag{A.9}$$

Therefore:

$$I_{C1} = \frac{\beta_1}{\beta_1+1}\left(I_{in}-\frac{I_{out}}{\beta_2}\right) \tag{A.10}$$

Finally, by substituting (A.10) back into (A.8), the output current is defined as:

$$I_{out} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\left[\ln\left(\frac{\frac{\beta_1}{\beta_1+1}\left(I_{in}-\frac{I_{out}}{\beta_2}\right)}{I_{out}}\frac{I_{S1}}{I_{S2}}\right)+\frac{V_{ce2}-V_{ce1}}{V_A}\right] \tag{A.11}$$

If β_1 and β_2 are both >>1 then (A.10) simplifies to:

$$I_{out} = \frac{V_T}{R_1}\left[\ln\left(\frac{I_{in}}{I_{out}}\frac{I_{S2}}{I_{S1}}\right)+\frac{V_{ce2}-V_{ce1}}{V_A}\right] \tag{A.12}$$

If $V_A >> \Delta V_{ce}$ then this result can be further simplified to give the well known equation:

$$I_{out} = \frac{V_T}{R_1}\ln\left(\frac{I_{in}}{I_{out}}\frac{I_{S2}}{I_{S1}}\right) \tag{A.13}$$

A.2 Defining the Output Current of a Buffered Widlar Current Source

Applying KVL around the base emitter loop gives:

$$V_{be1} - V_{be2} - \frac{\beta_2 + 1}{\beta_2} I_{out} R_1 = 0 \qquad (A.14)$$

Where:

$$V_{be1} = V_T \ln \frac{I_{C1}}{I_{S1}} - \frac{V_T V_{ce1}}{V_A} \qquad (A.15)$$

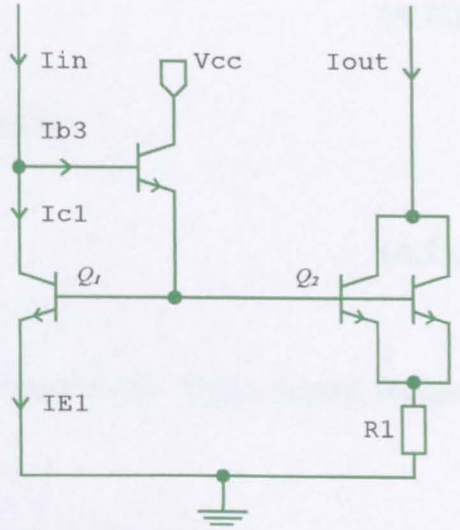

Figure A.2 – A Buffered Widlar Current Source

And:

$$V_{be2} = V_T \ln \frac{I_{out}}{I_{S2}} - \frac{V_T V_{ce2}}{V_A} \qquad (A.16)$$

Therefore:

$$\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{out}}{I_{S2}} = \left[\frac{\beta_2 + 1}{\beta_2} I_{out} R_1 + V_T \frac{V_{ce1} - V_{ce2}}{V_A} \right] \frac{1}{V_T} \qquad (A.17)$$

$$\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{out}}{I_{S2}} = \frac{\beta_2 + 1}{\beta_2} \frac{I_{out} R_1}{V_T} + \frac{V_{ce1} - V_{ce2}}{V_A} \qquad (A.18)$$

$$\ln \left(\frac{I_{C1}}{I_{out}} \frac{I_{S1}}{I_{S2}} \right) = \frac{\beta_2 + 1}{\beta_2} \frac{I_{out} R_1}{V_T} + \frac{V_{ce1} - V_{ce2}}{V_A} \qquad (A.19)$$

$$\ln \left(\frac{I_{C1}}{I_{out}} \frac{I_{S1}}{I_{S2}} \right) + \frac{V_{ce2} - V_{ce1}}{V_A} = \frac{\beta_2 + 1}{\beta_2} \frac{I_{out} R_1}{V_T} \qquad (A.20)$$

$$I_{out} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\left[\ln\left(\frac{I_{C1}}{I_{out}}\frac{I_{S1}}{I_{S2}}\right)+\frac{V_{ce2}-V_{ce1}}{V_A}\right] \quad \text{(A.21)}$$

By definition:

$$I_{C1} = I_{in} - I_{B3} \quad \text{(A.22)}$$

I_{B3} is the base current of Q_3, which in turn is given by:

$$I_{B3} = \frac{(\beta_1+1)I_{E2}+(\beta_2+1)I_{E1}}{(\beta_1+1)(\beta_2+1)(\beta_3+1)} \quad \text{(A.23)}$$

I_{E1} and I_{E2} are the emitter currents of Q_1 and Q_2 respectively. These, in turn, are given by:

$$I_{E1} = \frac{\beta_1+1}{\beta_1}I_{C1} \quad \text{(A.24)}$$

$$I_{E2} = \frac{\beta_2+1}{\beta_2}I_{out} \quad \text{(A.25)}$$

By combining (A.23), (A.24) and (A.25) an expression for I_{B3} can be defined as:

$$I_{B3} = \frac{\beta_1 I_{out}+\beta_2 I_{C1}}{\beta_1\beta_2(\beta_3+1)} \quad \text{(A.26)}$$

$$I_{B3} = \frac{I_{out}}{\beta_2(\beta_3+1)}+\frac{I_{C1}}{\beta_1(\beta_3+1)} \quad \text{(A.27)}$$

By substituting (A.27) into (A.21) we obtain:

$$I_{in} = I_{C1}+\frac{I_{out}}{\beta_2(\beta_3+1)}+\frac{I_{C1}}{\beta_1(\beta_3+1)} \quad \text{(A.26)}$$

$$I_{in} = I_{C1}\left(1+\frac{1}{\beta_1(\beta_3+1)}\right)+\frac{I_{out}}{\beta_2(\beta_3+1)} \tag{A.27}$$

Therefore:

$$I_{C1} = \frac{I_{in}}{1+\left[1/\beta_1(\beta_3+1)\right]} - \frac{I_{out}}{\beta_2\left[(\beta_3+1)+1/\beta_1\right]} \tag{A.28}$$

Finally, by substituting (A.29) back into (A.22), the output current is defined as:

$$I_{out} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\left[\ln\left(\frac{\left(\frac{I_{in}}{1+\left[1/\beta_1(\beta_3+1)\right]} - \frac{I_{out}}{\beta_2\left[(\beta_3+1)+1/\beta_1\right]}\right)}{I_{out}}\frac{I_{S1}}{I_{S2}}\right)+\frac{V_{ce2}-V_{ce1}}{V_A}\right] \tag{A.29}$$

If β_1 and β_2 are both >>1 then (A.29) simplifies to:

$$I_{out} = \frac{V_T}{R_1}\left[\ln\left(\frac{I_{in}}{I_{out}}\frac{I_{S2}}{I_{S1}}\right)+\frac{V_{ce2}-V_{ce1}}{V_A}\right] \tag{A.30}$$

If $V_A >> \Delta V_{ce}$ then this result can be further simplified to give the well known equation:

$$I_{out} = \frac{V_T}{R_1}\ln\left(\frac{I_{in}}{I_{out}}\frac{I_{S2}}{I_{S1}}\right) \tag{A.31}$$

A4.3 Defining the Output Current of a Wilson Current Source

Applying KVL around the base emitter loop gives:

$$V_{be1} - V_{be2} - \frac{\beta_2 + 1}{\beta_2} I_{C2} R_1 = 0 \qquad \text{(A.32)}$$

Where:

$$V_{be1} = V_T \ln \frac{I_{C1}}{I_{S1}} - \frac{V_T V_{ce1}}{V_A} \qquad \text{(A.33)}$$

And:

$$V_{be2} = V_T \ln \frac{I_{C2}}{I_{S2}} - \frac{V_T V_{ce2}}{V_A} \qquad \text{(A.34)}$$

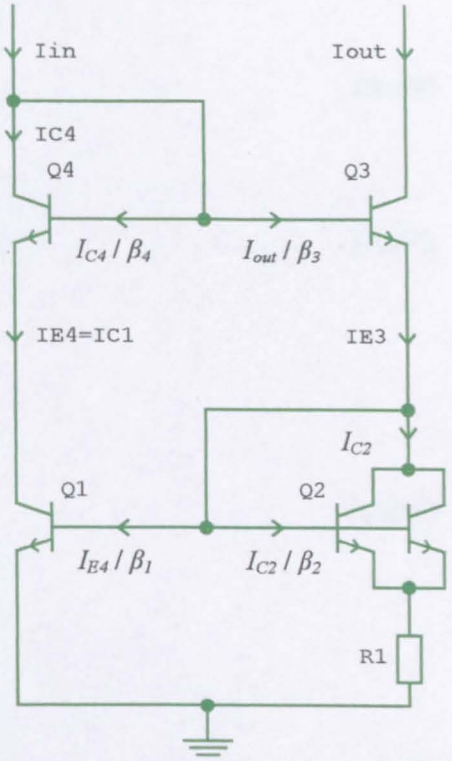

Figure A.3 – A Wilson Current Source

Therefore:

$$\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{C2}}{I_{S2}} = \left[\frac{\beta_2 + 1}{\beta_2} I_{C2} R_1 + V_T \frac{V_{ce1} - V_{ce2}}{V_A} \right] \frac{1}{V_T} \qquad \text{(A.35)}$$

$$\ln \frac{I_{C1}}{I_{S1}} - \ln \frac{I_{C2}}{I_{S2}} = \frac{\beta_2 + 1}{\beta_2} \frac{I_{C2} R_1}{V_T} + \frac{V_{ce1} - V_{ce2}}{V_A} \qquad \text{(A.36)}$$

$$\ln \left(\frac{I_{C1}}{IC2} \frac{I_{S1}}{I_{S2}} \right) = \frac{\beta_2 + 1}{\beta_2} \frac{I_{C2} R_1}{V_T} + \frac{V_{ce1} - V_{ce2}}{V_A} \qquad \text{(A.37)}$$

$$\ln \left(\frac{I_{C1}}{I_{C2}} \frac{I_{S1}}{I_{S2}} \right) + \frac{V_{ce2} - V_{ce1}}{V_A} = \frac{\beta_2 + 1}{\beta_2} \frac{I_{C2} R_1}{V_T} \qquad \text{(A.38)}$$

By careful examination of Figure A.3 it is noted that the diode connected transistor Q_4 acts as a level shift that forces V_{BE1} and V_{BE2} to be equal. Thus it holds that $V_{CE1} \approx V_{CE2}$. Therefore, (A.38) can be rewritten as:

$$\ln\left(\frac{I_{C1}}{I_{C2}}\frac{I_{S1}}{I_{S2}}\right) = \frac{\beta_2+1}{\beta_2}\frac{I_{C2}R_1}{V_T} \tag{A.39}$$

$$I_{C2} = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\ln\left(\frac{I_{C1}}{I_{C2}}\frac{I_{S1}}{I_{S2}}\right) \tag{A.40}$$

By definition:

$$I_{C2} = \frac{\beta_2}{\beta_2+1}\left(I_{E3} - \frac{I_{E4}}{\beta_1}\right) \tag{A.41}$$

And:

$$I_{E3} = \frac{\beta_3+1}{\beta_3} I_{out} \tag{A.42}$$

$$I_{E4} = I_{C1} = \frac{\beta_4+1}{\beta_4} I_{C4} \tag{A.43}$$

$$I_{C4} = \frac{\beta_4}{\beta_4+1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right) \tag{A.44}$$

Therefore, by substituting (A.44) into (A.43) we obtain:

$$I_{C1} = I_{in} - \frac{I_{out}}{\beta_3} \tag{A.45}$$

Also, by substituting (A.42) and (A.43) into (A.41) we obtain:

$$I_{C2} = \frac{\beta_2}{\beta_2+1}\left(\frac{\beta_3+1}{\beta_3} I_{out} - \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)\right) \tag{A.46}$$

Now, (A.45) and (A.46) are substituted back into (A.40) to give:

$$\frac{\beta_2}{\beta_2+1}\left(\frac{\beta_3+1}{\beta_3} I_{out} - \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)\right) = \frac{\beta_2}{\beta_2+1}\frac{V_T}{R_1}\ln\left(\frac{\left(I_{in} - \frac{I_{out}}{\beta_3}\right)}{\frac{\beta_2}{\beta_2+1}\left(\frac{\beta_3+1}{\beta_3} I_{out} - \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)\right)}\frac{I_{S1}}{I_{S2}}\right) \tag{A.47}$$

$$\frac{\beta_3+1}{\beta_3} I_{out} = \frac{V_T}{R_1}\ln\left(\frac{\left(I_{in} - \frac{I_{out}}{\beta_3}\right)}{\frac{\beta_2}{\beta_2+1}\left(\frac{\beta_3+1}{\beta_3} I_{out} - \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)\right)}\frac{I_{S1}}{I_{S2}}\right) + \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right) \tag{A.48}$$

$$I_{out} = \frac{\beta_3}{\beta_3+1}\left[\frac{V_T}{R_1}\ln\left(\frac{\left(I_{in} - \frac{I_{out}}{\beta_3}\right)}{\frac{\beta_2}{\beta_2+1}\left(\frac{\beta_3+1}{\beta_3} I_{out} - \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)\right)}\frac{I_{S1}}{I_{S2}}\right) + \frac{1}{\beta_1}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)\right] \tag{A.49}$$

This result can be rewritten as:

$$I_{out} = \frac{\beta_3}{\beta_3+1}\frac{V_T}{R_1}\ln\left[\left(\frac{I_{in} - \frac{I_{out}}{\beta_3}}{\frac{\beta_2(\beta_3+1)}{\beta_3(\beta_2+1)} I_{out} - \frac{\beta_2}{\beta_1(\beta_2+1)}\left(I_{in} - \frac{I_{out}}{\beta_3}\right)}\right)\frac{I_{S2}}{I_{S1}}\right] + \frac{\beta_3}{\beta_1(\beta_3+1)}\left(I_{in} - \frac{I_{out}}{\beta_3}\right) \tag{A.50}$$

If $\beta_1 = \beta_2 = \beta_3 = \beta_N$ then the output current is defined as:

$$I_{out} = \frac{\beta_N}{\beta_N+1}\frac{V_T}{R_1}\ln\left[\left(\frac{I_{in} - \frac{I_{out}}{\beta_N}}{I_{out} - \frac{1}{(\beta_N+1)}\left(I_{in} - \frac{I_{out}}{\beta_N}\right)}\right)\frac{I_{S2}}{I_{S1}}\right] + \frac{1}{(\beta_N+1)}\left(I_{in} - \frac{I_{out}}{\beta_N}\right) \tag{A.51}$$

If $\beta_N >> 1$ then this result can be further simplified to give the well known equation:

$$I_{out} = \frac{V_T}{R_1} \ln\left(\frac{I_{in}}{I_{out}} \frac{I_{S2}}{I_{S1}}\right) \tag{A.51}$$

A.4 Defining the Sensitivity of the Output Current of a Wilson Current Source to Changes in Power Supply Voltage

For simplicity, the output current of a Wilson Current Source that is 'Bootstrap Biased' with a generic current mirror can be written as:

$$I_{out} = I_X = \frac{V_T}{R_1} \ln \lambda m \qquad \text{(A.52)}$$

If V_{CC} changes then so does I_{out} because of corresponding changes in λ and m. Using (A.52), a further equation can be derived to give the sensitivity (S), to changes in V_{CC}, of the output current for a PTAT current generator circuit comprising of a Wilson current source and a generic current mirror. By definition:

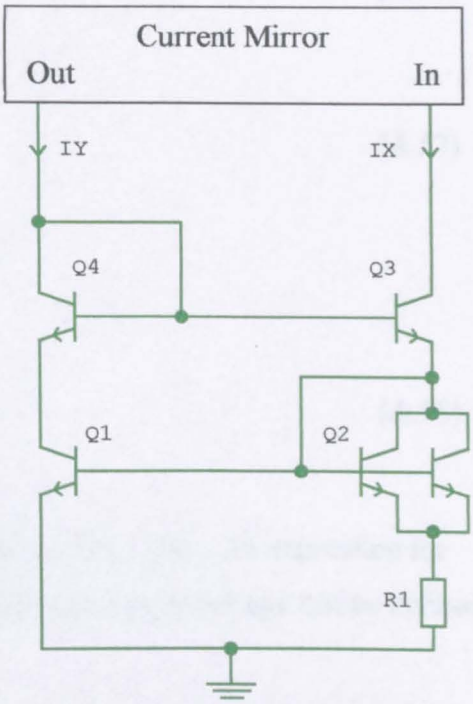

Figure A.4 –PTAT Current Generator using a Wilson Current Source with a 1:m Emitter Area Ratio

$$S = \frac{1}{\partial I_{out}} \frac{\partial I_{out}}{\partial V_{CC}} = \frac{\partial \ln I_{out}}{\partial V_{CC}} \qquad \text{(A.53)}$$

Now, from rearrangement of (A.52) we obtain:

$$R_1 I_{out} = V_T (\ln \lambda + \ln m) \qquad \text{(A.54)}$$

Noting that R_1 is a constant the above result is differentiated with respect to V_{CC} to give:

$$R_1 \frac{\partial I_{out}}{\partial Vcc} = Vr\left(\frac{\partial}{\partial Vcc}(\ln\lambda) + \frac{\partial}{\partial Vcc}(\ln m)\right) \tag{A.55}$$

However m does not change with V_{CC}. Therefore:

$$R_1 \frac{\partial I_{out}}{\partial Vcc} = Vr\left(\frac{\partial}{\partial \lambda}(\ln\lambda)\frac{\partial \lambda}{\partial Vcc}\right) \tag{A.56}$$

$$R_1 \frac{\partial I_{out}}{\partial Vcc} = Vr\left(\frac{1}{\lambda}\frac{\partial \lambda}{\partial Vcc}\right) \tag{A.57}$$

Now if (A.57) is divided by (A.54), we obtain:

$$\frac{1}{I_{out}}\frac{\partial I_{out}}{\partial Vcc} = \frac{1}{\ln(\lambda m)}\left(\frac{1}{\lambda}\frac{\partial \lambda}{\partial Vcc}\right) \tag{A.58}$$

The above result can now be substituted back into (A.53). Thus. An expression for the sensitivity of the output current to changes in power supply voltage can be defined as:

$$S = \frac{1}{\ln(\lambda m)}\left(\frac{1}{\lambda}\frac{\partial \lambda}{\partial Vcc}\right) \tag{A.59}$$

A.5 Method Used to Determine the Forward Emission Coefficient (n) of a NPN Transistor

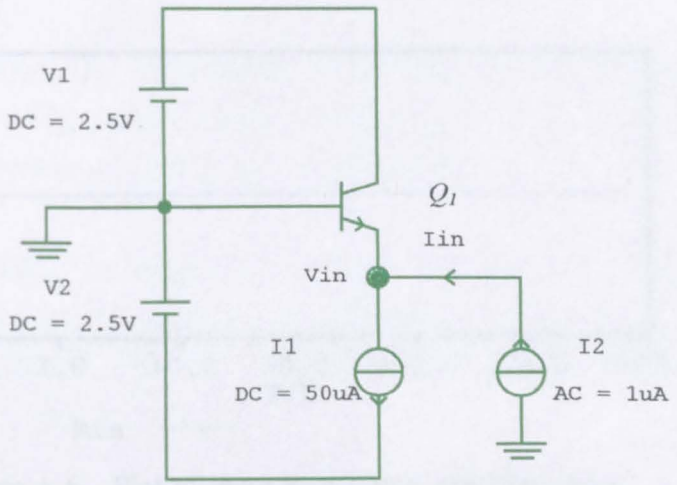

Figure A.5 – Circuit Used to Determine the Forward Emission Coefficient (n) of Q_1

Figure A.5 illustrates the circuit schematic used to determine the forward emission coefficient (n) of Q_1. The base and collector currents, I_B and I_C respectively, of Q_1 were measured when V_{CE}= 5V at 27°C:

$$I_B = 279.06\text{nA} \tag{A.60}$$

$$I_C = 49.721\mu\text{A} \tag{A.61}$$

By definition, the current gain, β, of Q_1 is given by:

$$\beta = \frac{I_C}{I_B} = \frac{49.721\mu A}{279.06nA} = 178.17 \tag{A.62}$$

Now, the input resistance, R_{in}, is swept across an arbitrary range of low frequencies (1Hz-1KHz) where:

$$R_{in} = \frac{V_{in}}{I_{in}} \tag{A.63}$$

The resulting plot is shown in Figure A4.6. From this plot it is easily determined that $R_{in} = 562.67\Omega$ at 1Hz (i.e. very close to DC).

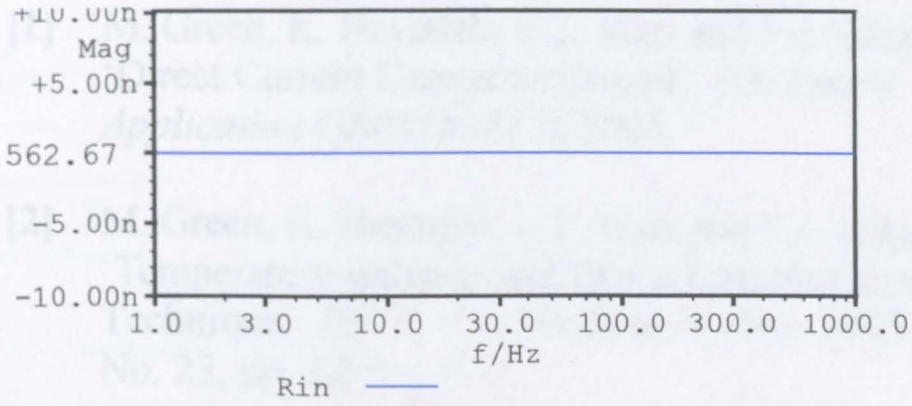

Figure A.6 – Plot of Input Resistance with Frequency

By definition the input resistance is also given by:

$$R_{in} = \frac{\beta}{\beta+1}\left(\frac{nV_T}{I_E}\right) \tag{A.64}$$

Therefore, the forward emission coefficient is given by:

$$n = \left(1+\frac{1}{\beta}\right)\frac{I_E R_{in}}{V_T} \tag{A.65}$$

$$n = \left(1+\frac{1}{178.17}\right)\frac{50E-6\times 562.67}{25.86E-3} = 1.094 \tag{A.66}$$

(12) UK Patent Application (19) GB (11) 2 428 918 (13) A

(43) Date of A Publication 07.02.2007

(21) Application No: 0516231.8

(22) Date of Filing: 05.08.2005

(71) Applicant(s):
Oxford Brookes University
(Incorporated in the United Kingdom)
Gipsy Lane Campus, Headington,
OXFORD, OX3 0BP, United Kingdom

(72) Inventor(s):
John Lidgey
Khaled Hayatleh
Bryan Hart
Matthew Green

(74) Agent and/or Address for Service:
Withers & Rogers LLP
Goldings House, 2 Hays Lane, LONDON,
SE1 2HW, United Kingdom

(51) INT CL:
H03F 3/347 (2006.01) ***G05F 3/26*** (2006.01)
H03F 1/30 (2006.01)

(52) UK CL (Edition X):
H3W WAM WUV
H3T T2B8 T2T2X T2T3B T2T3F T3J T3N T4D T4E1N T6PX T6V

(56) Documents Cited:
US 4574233 A **US 4347531 A**
US 4317082 A **US 20030214279 A1**

(58) Field of Search:
INT CL[7] **G05F, H03F**
Other: **TXTE**

(54) Abstract Title: **A DC current scaler using current mirrors**

(57) An integrated DC current amplifier/attenuator is based on current mirror techniques and operates at low voltages with low temperature sensitivity and without operational amplifiers. Identical input currents from unit A are fed to a first mirror Q1-Q2 having different emitter resistors R1, R2. The first stage output current taken from the emitter of Q2 is proportional to the input currents and is linearly dependent on the ratio of resistors R1, R2. The first stage output current is fed to a scaled second mirror Q5,Q6 which produces an output current IL for supply to a load, which may be a differential amplifier Q10,Q11. Unit A may produce a current proportional to absolute temperature (PTAT) so that the gain of the differential amplifier remains constant as temperature changes. A microampere PTAT generator can supply a milliampere bias current by scaling in the current mirrors. The mirror circuits may use FETs.

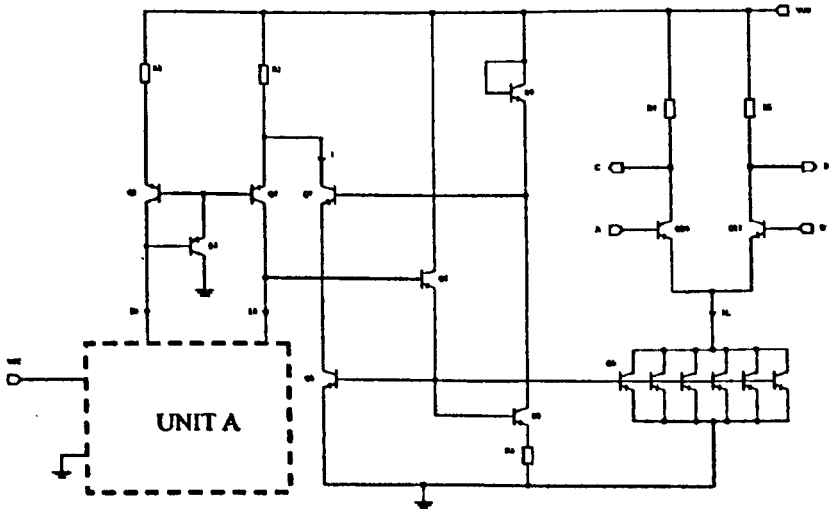

Figure 2

GB 2 428 918 A

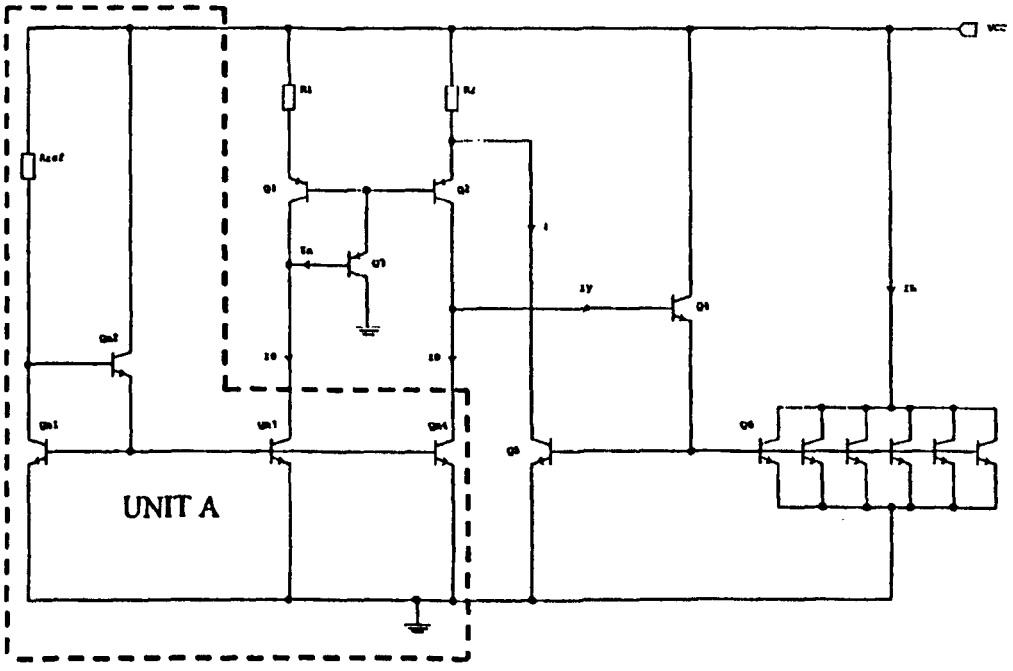

Figure 1

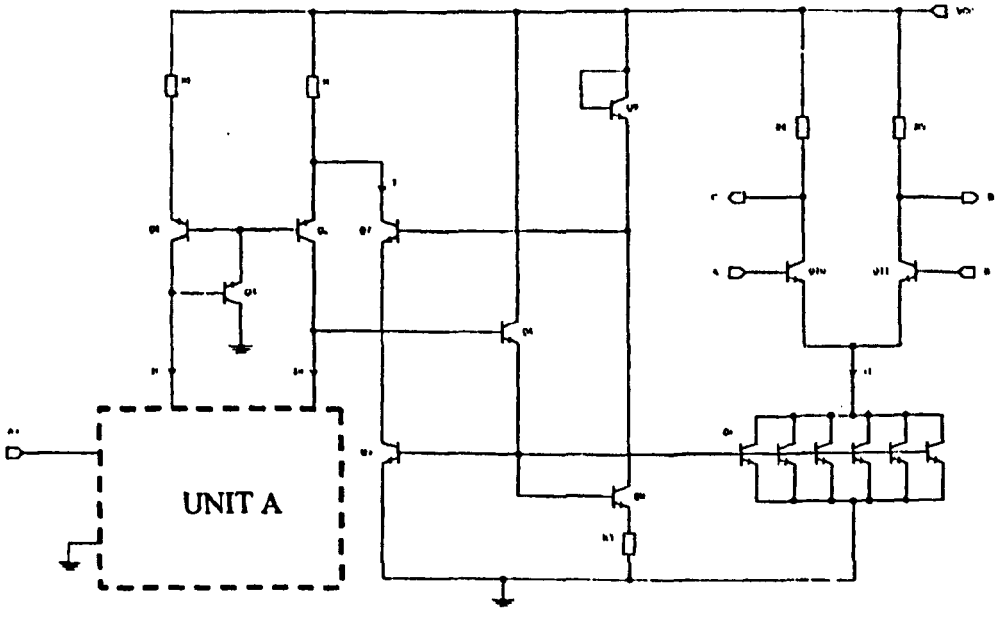

Figure 2

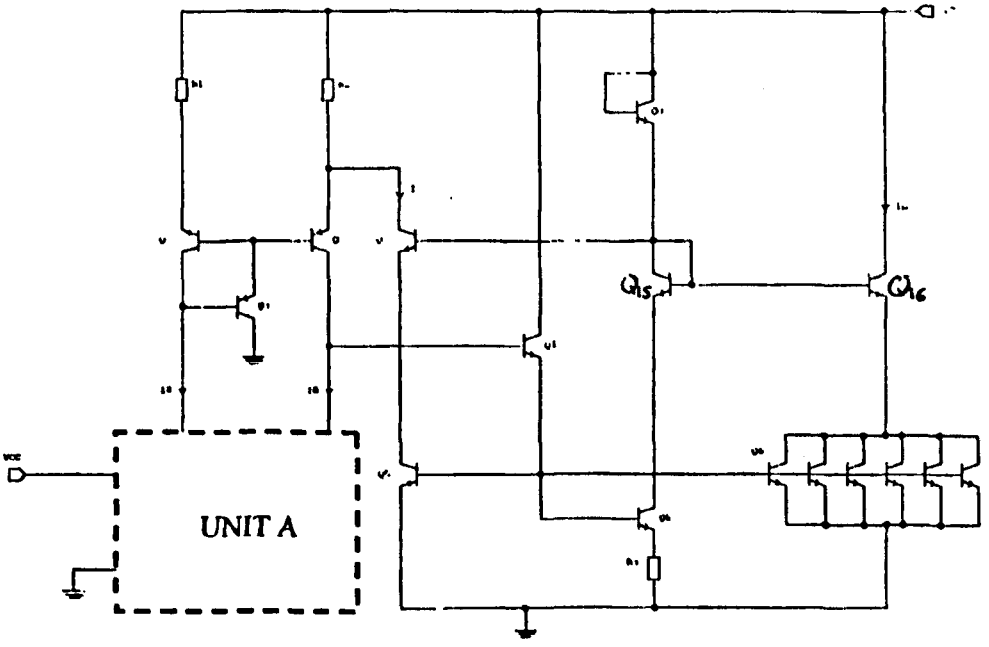

Figure 3

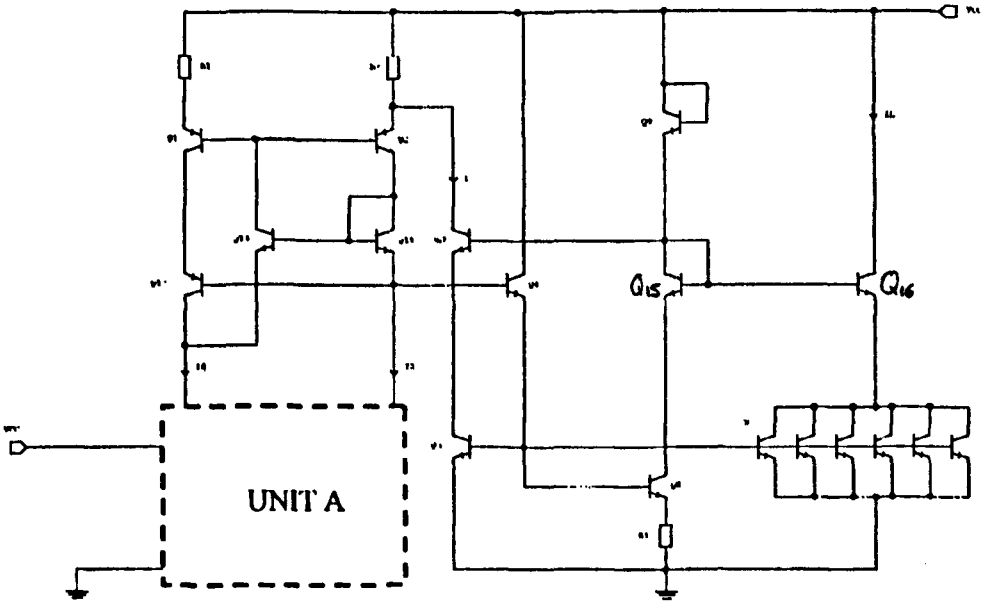

Figure 4

DIRECT CURRENT CONVERTER CIRCUIT

There are many applications in which an output current of an electronic system is designed to be dependent on the input current, the relationship between the input and output currents being temperature independent and preferably linear in scaling. Examples of such applications include ambient temperature dependent current sources, light intensity conversion circuits and precision current dividers. Designs for accurate analogue current converters are known but, to achieve the desired current gain, they tend to revert to the use of an operational amplifier (Op Amp). However, the use of Op Amp involves the use of a comparatively large number of components and a circuit that typically is not able to operate at low (less than 3.3V) power supply voltages.

It is therefore an aim of embodiments of the present invention to provide an analogue direct current converter (i.e. amplification or attenuation) circuit that provides an improvement on those known from the prior art.

According to a first embodiment of the present invention there is provided a direct current converter circuit comprising a first current mirror having two parallel circuit arms, each arm comprising a resistive element in series with a transistor coupled between a reference voltage and an input terminal arranged to receive an input current, the first current mirror further comprising an intermediate output node arranged to provide an intermediate current, the direct current converter circuit further comprising a second current mirror having a first transistor circuit having a current path terminal arranged to receive the intermediate current and a second transistor circuit having a current path terminal arranged to provide an output current, wherein the ratio of the output current to the input current is proportional to the ratio of the resistance of the resistive element in each arm of the first current mirror and is temperature independent.

The current converter according to embodiments of the present invention demonstrates a number of advantages over the prior art. When implemented in a monolithic integrated circuit, a chip area saving is achieved due to the use of fewer components compared to current converters using an Op Amp. Dependent on the transistors used, the current converter of the present invention is capable of operating with a supply rail voltage

significantly lower than 3.3V. Since the current gain is set by the ratio of just two resistors, the circuit design provides simplicity together with accurate and predictable current gain. The same circuit topology can be utilised to produce accurate current ratios greater than or less than unity. Furthermore, the circuit design exhibits inherently low temperature dependents.

Embodiments of the present invention will now be described, by way of illustrative example only, with reference to the accompanying figures, of which:

Figure 1 is a schematic illustration of a temperature independent current converter circuit in accordance with embodiments of the present invention, with an enhanced beta current mirror input;

Figure 2 schematically illustrates a temperature independent differential amplifier incorporating the current converter circuit according to a further embodiment of the present invention;

Figure 3 schematically illustrates a temperature independent current converter according to an embodiment of the present invention with high output resistance; and

Figure 4 schematically illustrates a high precision embodiment of the temperature independent current converter of the present invention.

A basic embodiment of a circuit according to the present invention is shown in Figure 1. The input current to be amplified or attenuated is provided, in this embodiment, by a beta enhanced dual output current mirror. The two outputs of the current mirror are each connected to respective input terminals of the current converter circuit. Each input terminal is connected to a current flow terminal of a transistor, in the example shown in Figure 1 a pnp bi-polar transistor Q_1, with the collector terminal being connected to the input terminal. Connected between the second current flow terminal of Q_1, which in this case is the emitter terminal, is a first resistor R_1, which is in turn connected to a supply voltage Vcc. In a similar manner, the second input terminal of the current converter circuit is connected to the collector of a second pnp bi-polar resistor Q_2, with the emitter terminal

of Q_2 being connected to a second resistor R_2, which in turn is also connected to the supply voltage Vcc. The base terminals (control terminals) of the first and second transistors Q_1 and Q_2 are connected to one another. To provide the necessary bias the emitter of a third pnp bi-polar transistor Q_3 is connected to the base terminals of the first and second transistors Q_1 and Q_2, with the collector of the bias transistor Q_3 being connected to ground. The base terminal of the bias transistor Q_3 is connected to the collector terminal of one of Q_1 or Q_2, that is it is connected to one of the two input terminals of the current converter circuit. The first and second transistors Q_1 and Q_2 therefore form a first current mirror, with resistors R_1 and R_2 provided as either degeneration resistors. Connected to the emitter of the second transistor Q_2 is the connector terminal of a further bi-polar transistor Q_5, in this case an npn transistor. The emitter of the further transistor Q_5 is connected to a common ground. The further transistor Q_5 forms the first transistor in a second current mirror. The second transistor of the second current mirror is provided by a further npn transistor Q_6. The base terminals of the first and second transistors in the second current mirror are connected to one another. In the embodiment shown in Figure 1 Q_6 actually comprises a plurality N of individual transistors, each with their base terminal connected to the base terminal of the first transistor Q_5 of the second current mirror. Each of the N transistors comprising Q_6 has an emitter area equal to the emitter area of Q_5. The emitter terminals of each of the transistors comprising Q_6 are connected to the common ground, whilst their collector terminals are connected to an output terminal of the current converter circuit, which in use will be connected to a terminal of a load L. A second bias transistor Q_4, again also an npn bi-polar transistor, is provided with its collector terminal connected to the supply voltage Vcc and its emitter terminal connected to the base terminals of Q_5 and Q_6 of the second current mirror. The base terminal of the second bias transistor Q_4 is connected to the input terminal of the converter circuit that is not connected to the bias terminal of the first bias transistor Q_3. It will be appreciated that the second transistor Q_6 of the second current mirror rather than comprising a plurality N individual transistors could be a single transistor of similar construction to that of the first transistor Q_5 of the second current mirror, but having an emitter area N times larger. In either case, the output current I_L sunk by the second transistor Q_6 of the second current mirror is N times the current sunk by the first transistor Q_5 of the second current mirror.

The operation of the current converter circuit shown in Figure 1 is as follows. The base current I_x of the first bias transistor Q_3 of the first current mirror is typically much smaller than the input current I_O flowing through that arm of the circuit. Similarly, the base current, I_Y of the second bias transistor Q_4 of the second current mirror, which is only supplying the base currents of the parallcled transistors Q_5 and Q_6 in the second current mirror, is also very small compared to the output current I_O that also flows through the second arm of the first current mirror. The input currents I_O through the two current arms are also the collector currents through the first and second transistors Q_1 and Q_2. Since the collector currents of Q_1 and Q_2 are substantially equal, the emitter-base voltages, V_{EB1} and V_{EB2} respectively, are also equal, as are their emitter currents, which have a value of I_O/α_P, where α_P is the common base direct current gain of both Q_1 and Q_2 Since the bases of Q_1 and Q_2 have a common potential, it follows that the potential difference across the resistors R_1 is equal to the potential difference cross resistor R_2.

The potential difference across R_1 is:

$$V_1 = I_O R_1/\alpha_P \qquad (1)$$

While the potential difference across R_2 is:

$$V_2 = [(I_O/\alpha_P) + I]R_2 \qquad (2)$$

Where I is the collector current drawn by the first transistor Q_5 of the second current mirror. Equating equations 1 and 2 gives the relationship between I and I_O, namely:

$$I = (I_O/\alpha_P)[(R_1/R_2) - 1] \qquad (3)$$

As stated above the collector current I_L of the second transistor Q_6 of the second current mirror is N times the collector current of the first transistor of Q_5 of the second mirror, which is I. Therefore:

$$I_L = N(I_O/\alpha_P)[(R_1/R_2) - 1] \qquad (4)$$

This may also be expressed in terms of the current scaling, or current gain, A_I, which is given by:

$$A_I = I_L/I_O = N(1/\alpha_P)[(R_1/R_2) - 1] \quad (5)$$

The common base direct current gain α_P of the transistors Q_1 and Q_2, is virtually temperature independent, as is also the ratio of the resistors R_1/R_2. This means that the current gain A_I of the current converter circuit as a whole is also virtually temperature independent. Consequently, accurate current gain or attenuation of I_O can be simply achieved by manipulating the values of R_1/R_2 and/or N accordingly.

As described above, the action of the first current mirror Q_1, Q_2 forces an equal voltage to be applied across both resistors R_1, R_2. Consequently, by arranging for resistor R_2 to have a value less than, say, resistor R_1 a greater current must be drawn through R_2 than R_1. However, by the action of the current mirror the collector currents through Q_1 and Q_2 must be the same, so the 'extra' current drawn through resistor R_2 is sunk by the first transistor Q_5 of the second current mirror Q_5 Q_6. Any variation in the emitter current (and hence collector current) of transistor Q_2 with respect to transistor Q_1 is seen at the base of transistor Q_4 (the collector current of transistor Q_{n4} of unit A being independently set) varying the emitter-collector current of Q_4 and therefore the base current of the first transistor Q_5 of the second current mirror. The variation in the base of Q_5 causes Q_5 to vary the current I being sunk by an amount corresponding to the original variation in the emitter current of Q_2 by transistors Q_4 and Q_5 that enforces the equal emitter currents in the transistors Q_1 and Q_2 of the first current mirror.

Although it is more straightforward to achieve current attenuation by adjusting the values of R_1 and R_2 accordingly, it will be appreciated that current attenuation may also be achieved by selecting the transistors Q_5 and Q_6 of the second current mirror such that the emitter area of the first transistor Q_5 is N times as large as the emitter area of the second transistor Q_6, such that $I_L = I/N$. Alternatively, the N number of transistors comprising the second transistor Q_6 of the second mirror may be connected in the known manner such that $I_L = I/N$.

Although the basic embodiment of the current invention shown in Figure 1 is illustrated in combination with a simple beta enhanced dual output current mirror, referenced as unit A in Figure 1, it will be appreciated that unit A could be any form of dual output reference current generator or any other circuit that provides an output current I_O that is desired to be amplified or attenuated. The output current I_O could also be a variable value current.

As also noted above, transistor Q_3 is provided solely to provide the base current for current mirror transistors Q_1 and Q_2, whilst transistor Q_4 is provided solely to provide the base current for current mirror transistors Q_5 and Q_6. The base currents could be provided by replacing Q_3 with a simple connection between the collector and base of Q_1, whilst Q_4 could be replaced by a direct connection between the collector of Q_2 and the bases of Q_5 and Q_6. However, the result will be significantly less accurate compared with that described previously.

It is known to those skilled in the art that "proportional to absolute temperature" (PTAT) bias currents are desired for bi-polar junction transistor amplifiers, so that the overall gain of the amplifier circuit becomes constant with temperature. Conventional PTAT current designs are known in which PTAT currents are provided in the microampere range, but due to resistor tolerances, for example, it is difficult to directly generate accurate PTAT currents in milliampere range using known PTAT circuit designs. The provision of accurate PTAT currents in the milliampere range is desirable for applications such as low noise bi-polar junction transistor amplifiers for linear radio frequency applications. Therefore, a particularly useful application of the current converter of the present invention is to amplify the output current amplitude of a conventional PTAT current source circuit. Post amplifying the output current using, for example, the circuit shown in Figure 1 forms the basis of a millampere output current range PTAT. In this application the unit A of Figure 1 is provided by a conventional low output current level PTAT. As stated above, the output currents of the PTAT current generator are proportional to absolute temperature. Since the output currents of the conventional PTAT generator comprise the input currents I_O of the current converter of the present invention, the output current of the converter circuit I_L is also proportional to absolute temperature.

A further application of the current converter according to embodiments of the present invention is in the provision of a temperature independent differential amplifier. The embodiment shown in Figure 2 is an emitter coupled differential amplifier biased with an enhanced PTAT current sink, which produces an overall amplifier with differential gain that is independent of temperature. The PTAT current sink will be of conventional design known in the art providing a current in the microampere range.

The emitter coupled differential amplifier comprises a first resistor R_4 connected at one terminal to the supply voltage Vcc and at the second terminal to the collector of a bi-polar npn transistor Q_{10}, the emitter terminal of which is connected to the collector terminal of the second transistor Q_6 of the second current mirror stage of the current converter circuit described with reference to Figure 1. The differential amplifier also comprises a second resistor R_5 which in turn has a first terminal connected to the supply voltage Vcc and a second terminal connected to the collector terminal of a second transistor Q_{11}, which is a matched npn bi-polar transistor matched to Q_{10}. The emitter terminal of Q_{11} is also connected to the input terminal, or collector terminal, of the second transistor Q_6 of the current converter second current mirror. The base terminals of the two transistors Q_{10} and Q_{11} of the differential amplifier provide first and second input terminals to the amplifier, whilst first and second output terminals are connected between the transistor and resistor of each arm of the differential amplifier. In contrast to the circuit illustrated in Figure 1, in the circuit of Figure 2 an additional transistor Q_7 of the npn type has been connected between the emitter of the second transistor Q_2 of the first current mirror and the collector terminal of the first transistor Q_5 of the second current mirror, with the emitter terminal of the additional transistor Q_7 being connected to the collector of the first transistor Q_5 of the second current mirror. The base bias voltage for the additional transistor Q_7 is provided by a diode strapped transistor Q_9, comprising an npn transistor having its collector and base connected to the supply voltage Vcc, with its emitter connected to the base of the further transistor Q_7. The bias current for the diode strapped transistor Q_9 is provided by a further transistor Q_8 having a collector terminal connected to the emitter terminal of Q_9, and therefore also the base terminal of Q_7, and its emitter terminal connected to the common ground, preferably via a further resistor R_3. The resistor R_3 is preferably provided, but not necessarily, in order to reduce the collector current of the transistor Q_8, as a power saving measure below the value of $I/\alpha n$ that would have been the case if R_3 were omitted. The

base of transistor Q_8 is connected to the common basis of the first and second transistors Q_5, Q_6 of the second current mirror.

Although a PTAT current could also be provided utilising the circuit shown in Figure 1 in conjunction with a PTAT current sink, i.e. by omitting transistors Q_7, Q_8, Q_9 and R_3, the output current would be less accurately defined due to V_{ce} variations in transistors Q_5 and Q_6. It should be noted that for the circuit of figure 2 there is no change in the circuit function if R_3, Q_8, Q_9 are removed and the voltage bias for the base of Q_7 is provided by other circuitry of which the design is known from the prior art. R_4, R_5, Q_{10} and Q_{11}can be replaced with other analogous circuitry of which the design is known from the prior art.

The small signal differential voltage gain, A_{BD}, of the differential amplifier stage is the product of the mutual conductance, g_m, of the long tailed pair formed by Q10 and Q11 and R_4, that is $A_{VD} = g_m x R_4$. The mutual conductance, g_m, is a temperature invariant because the collector currents of the two transistors of the differential amplifier stage Q_{10} and Q_{11} are PTAT, since the collector currents are provided by the output of the current converter circuit which in turn is driven by the PTAT current sunk by the PTAT current sink unit A. It therefore follows that the differential voltage gain of the differential amplifier stage is also temperature invariant, provided that the resistor R_4 has a zero temperature coefficient of resistance. (Any variation of the load impedance of the amplifier with temperature will alter the gain. It is therefore preferable that if using a resistor as the load it should have a zero Temperature Coefficient. In the case of RF design the load would use reactive components in the place of R4 and there would be no problem.)

A further, enhanced, embodiment of the current converter circuit illustrated in Figure 2 is shown in the circuit of Figure 3 and may be used as a current sink with a high output resistance. In addition to the circuit arrangement as shown in Figure 1, additional transistors Q_7, Q_8 and Q_9, together with optional resistor R_3, are provided as in Figure 2 and perform the same function as described with reference to Figure 2. Additionally, a further npn bi-polar transistor Q_{15} is provided with its collector terminal connected to the emitter terminal of diode strapped transistor Q_9 and its emitter terminal connected to the collector terminal of transistor Q_8. The base terminal of additional transistor Q_{15} is connected to its collector terminal and is also connected to the base terminal of a cascode transistor Q_{16}, the

collector of which is connected to the supply voltage Vcc and the emitter to the collector terminal of the second transistor Q_6 of the second current mirror of the current converter circuit. The additional transistor Q_{15} is provided to apply a suitable bias to the cascoded transistor Q_{16}. Cascoding transistor Q_6 by transistor Q_{16} increases the incremental output resistance above that possible with the circuit of Figure 1. The output resistance is now greater because Q_{16} is in the common base configuration. This has a higher output resistance than a transistor such as Q6 in the common emitter configuration. The enhanced circuit of Figure 3 may additionally be used in conjunction with the differential gain stage illustrated in Figure 2 to produce an improved differential gain amplifier with high resultant common-mode rejection due to the high incremental output resistance provided by the circuit of Figure 3. In this example, the cascaded transistor Q_{11} would be connected between the second transistor Q_6 of the second current mirror of the current converter and the two transistors Q_{10} and Q_{11} of the differential amplifier stage. As previously noted with respect to Figure 2, R_3, Q_8, Q_9 and Q_{10} of Figure 3 may be replaced with other known circuitry to provide the desired bias currents.

A further embodiment of the current converter circuit according to the present invention is illustrated in Figure 4. The circuit of Figure 4 is the same as that shown in Figure 3, but with the bias transistor 3 used to provide the bias current to the first and second transistors Q_1 and Q_2 of the first current mirror being replaced with additional transistors Q_{12}, Q_{13} and Q_{14}. Additional transistor Q_{12}, which comprises a further pnp bi-polar transistor has its emitter connected to the collector of the first transistor Q_1 of the first current mirror and its collector connected to the output of the current sink unit A. A second further transistor Q_{14}, which comprises a npn bi-polar transistor, has its collector connected to the connector of the second transistor Q_2 of the and its emitter connected to the second current input of the current sink unit A, whilst additionally having its emitter connected to the base of the first additional transistor Q_{12}. The third additional transistor Q_{13}, also an npn bi-polar transistor, has its collector connected to the common base of the first and second transistors Q_1 and Q_2 of the first current mirror and its emitter connected to the collector terminal of the first additional transistor Q_{12}. The base terminals of the second and third additional transistors Q_{13}, Q_{14} are connected to one another and also to the collector terminal of the second further transistor Q_{14}. The additional transistors Q_{12}, Q_{13} and Q_{14} fix the collector-base voltage V_{CB} of the first and second transistors Q_1 and Q_2 of the first current mirror of

the current converter, so that the collector-base voltages are virtually equal in value and independent of power supply voltage Vcc variations. Therefore, the current converter circuit as a whole exhibits an improved power supply rejection ratio. The circuit illustrated in Figure 4 achieves improved accuracy over a wider range of input currents and power supply values.

All of the embodiments of the present invention described above with reference to Figures 1 to 4 have been described with reference to bi-polar junction transistors. However, it will be appreciated by those skilled in the art that the current converter circuits described may additionally be implemented using field effect transistors, and their derivatives.

CLAIMS

1. A direct current converter circuit comprising a first current mirror having two parallel circuit arms, each arm comprising a resistive element in series with a transistor coupled between a reference voltage and an input terminal arranged to receive an input current, the first current mirror further comprising an intermediate output node arranged to provide an intermediate current, the direct current converter circuit further comprising a second current mirror having a first transistor circuit having a current path terminal arranged to receive the intermediate current and a second transistor circuit having a current path terminal arranged to provide an output current, wherein the ratio of the output current to the input current is proportional to the ratio of the resistance of the resistive element in each arm of the first current mirror and is temperature independent.

2. A direct current converter circuit according to claim 1, wherein each arm of the first current mirror further comprises a transistor having a first current path terminal connected to the respective resistive element, a second current path terminal connected to the input terminal and a control terminal, the control terminal of each transistor being connected to one another, whereby in use the current flow through the first current path terminal in each circuit arm is substantially equal.

3. A direct current converter circuit according to claim 2, wherein the intermediate output node of the first current mirror is located at a point of connection between the resistive element and first current path terminal of the transistor in one of the circuit arms.

4. A direct current converter circuit according to any preceding claim, wherein the ratio of the intermediate current to the input current is proportional to the ratio of the resistance of the resistive elements in each arm of the first current mirror.

5. A direct current converter circuit according to any preceding claim, wherein the first transistor circuit of the second current mirror comprises a single transistor and the second transistor circuit of the second current mirror comprises N transistors,

where N is an integer value, whereby the ratio of the output current to the intermediate current is N.

6. A direct current converter circuit according to any one of claims 1 to 4, wherein the first transistor circuit of the second current mirror comprises a first transistor having a current flow terminal having a first area A_1 and the second transistor circuit of the second current mirror comprises a second transistor having a current flow terminal having a second area A_2, wherein the ratio of the first terminal area to the second terminal area is N.

7. A direct current converter circuit according to any preceding claim further comprising:

a first further transistor having a current flow path connected between the intermediate output node of the first current mirror and the first transistor of the second current mirror and having a control terminal;

a second further transistor having a first current flow terminal coupled to a first common potential node and a second current flow terminal coupled to the control terminal of the first further transistor; and

a diode element having a current flow path connected in series with the current flow path of the second further transistor.

8. A direct current converter circuit according to claim 7, wherein the diode element comprises a diode strapped transistor.

9. A direct current converter circuit according to claim 7 or 8, wherein a first further resistive element is connected between first current flow terminal of the second further transistor and the first common potential node.

10. A direct current converter circuit according to any one of claims 7 to 9 further comprising:

a third further transistor having a current flow path connected between the second current flow terminal of the second further transistor and the control terminal of the first further transistor and having a control terminal; and

a fourth further transistor having a current flow path connected to the output current terminal of the second current mirror and having a control terminal, the control terminals of the third and fourth further transistors being connected to each other.

11. A direct current converter circuit according to claim 10 further comprising:

fifth and sixth further transistors each having a current flow path connected between the transistor of the respective circuit arms of the first current mirror and the respective input terminal, fifth further transistor having a control terminal connected to the input terminal of the circuit arm of the first current mirror in which the sixth further transistor is connected; and

a seventh further transistor having a current flow path connected between the input terminal of the circuit arm of the first current mirror in which the first current mirror transistors and having a control terminal connected to a control terminal of the sixth further transistor.

12. A direct current converter circuit according to any preceding claim, wherein said transistors comprise bi-polar transistors.

13. A direct current converter circuit according to any one of claims 1 to 11, wherein said transistors comprise field effect junction resistors.

14. A direct current converter circuit according to any preceding claim in combination with a differential amplifier stage, the differential amplifier stage being coupled to the output of the second current mirror.

15. A direct current converter circuit according to any preceding claim in combination with a PTAT current source, the PTAT current source being connected to the input terminals of the first current mirror.

Temperature-independent direct current converter technique

M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey

A novel temperature-independent direct current converter, the subject of a patent application number GB051623.8, is presented. Conversion ratios from less than unity to in excess of 50 are possible. Simulation measurements show an output temperature coefficient as low as 16 ppm/°C over the temperature range −40 to +85°C.

Introduction: There are many applications [1, 2] in which the output current of an electronic circuit or system is designed to be dependent on the input or a reference current, the ratio output-current/input-current being temperature-independent and linear. Designs for accurate IC current converters are known but, to achieve the desired current gain, they tend to employ an operational amplifier (op-amp). The approach described here is novel in that it permits operation at rail voltages lower than those at which op-amps normally work, although similar results can be obtained using a first-generation current conveyor (CCI) [3] combined with a few additional transistors as well as two resistors, the ratio of which gives an accurate and predictable current gain.

Circuit operation: Fig. 1 shows one example of the proposed current converter technique. The input current to be amplified (or, in principle, attenuated) is fed into a standard beta-enhanced dual-output current-mirror [4] formed by Q_{n1}, Q_{n2}, Q_{n3} and Q_{n4}. The two output currents, I_{01} and I_{02}, of the current-mirror are each connected to the respective terminals of a voltage following current mirror (VFCM) [5] formed by Q_{p1}, Q_{p2}, Q_{p3}, Q_{n5} and Q_{n6}. This configuration was chosen for its low sensitivity to power supply variations. Resistors R_1 and R_2 set the current gain/attenuation. The feedback loop from the collector of Q_{n4} to the emitter of Q_{p3} ensures that the emitter currents of Q_{p2} and Q_{p3} are equal (i.e. if $I_{01} = I_{02} = I_0$ as here). The buffering action of the compound emitter-follower formed by Q_{n9} and Q_{p4} makes I_B negligible compared with I_0.

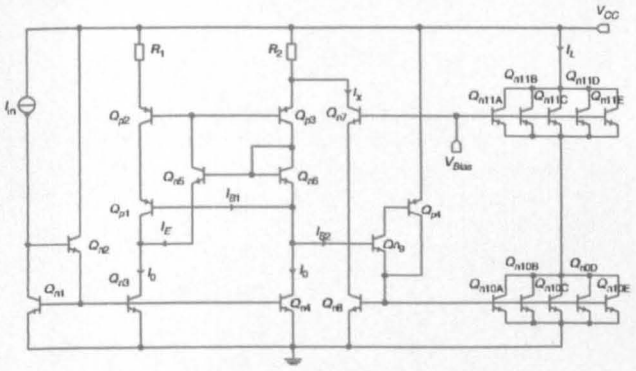

Fig. 1 *Simplified schematic of current converter*

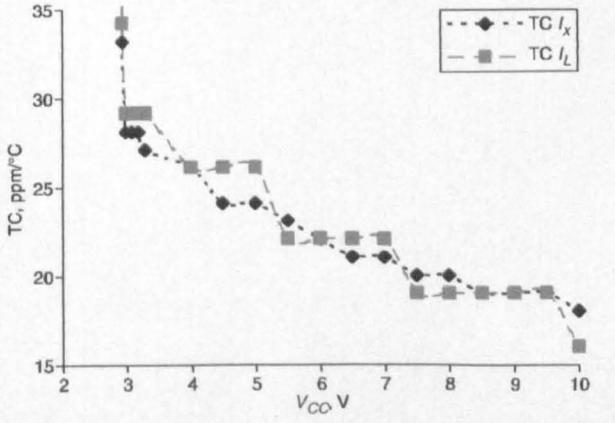

Fig. 2 *Temperature coefficient against power supply voltage ($I_{in} = 50$ μA)*

Since the bases of Q_{p2} and Q_{p3} have a common potential, it follows that the potential difference across the resistor R_1 is equal to the potential difference across resistor R_2. The potential difference across R_1 is:

$$V_1 = I_o R_1 \tag{1}$$

The potential difference, V_2, across R_2 is:

$$V_2 = (I_o + I_X)R_2 \tag{2}$$

where I_X is the collector current of Q_{n7}. It should be noted that (2) and all subsequent equations described below are only valid for $I_X > 0$. Hence, the condition $R_1 > R_2$ must be met. Equating (1) and (2) gives the relationship between I_X and I_o, namely:

$$I_X = I_o\left[\left(\frac{R_1}{R_2}\right) - 1\right] \simeq I_{in}\left[\left(\frac{R_1}{R_2}\right) - 1\right] \tag{3}$$

Transistors Q_{n10} and Q_{n11}, whose bases are driven, like those of Q_{n8} and Q_{n7}, respectively, supply the output current I_L. The bias voltage, V_{Bias}, for the cascode transistors Q_{n7} and Q_{n11} is two emitter–base voltage drops above earth, and provided by routine circuitry, not shown. Q_{n10} and Q_{n11} represent N transistors in parallel, each identical to Q_{n8} and Q_{n7}. However, they could be single transistors of similar construction to Q_{n8} and Q_{n7}, respectively, but having an emitter area N times as large. In either case $I_L = NI_X$. Thus:

$$I_L = NI_o\left[\left(\frac{R_1}{R_2}\right) - 1\right] \simeq NI_{in}\left[\left(\frac{R_1}{R_2}\right) - 1\right] \tag{4}$$

This may also be expressed in terms of the current scaling factor, or current gain, A_I, which is given by:

$$A_I = \frac{I_L}{I_{in}} = N\left[\left(\frac{R_1}{R_2}\right) - 1\right] \tag{5}$$

It is to be noted that A_I, being defined by a resistor ratio, is substantially temperature independent. Clearly, it is possible to achieve current attenuation as well as gain by choice of R_1, R_2 and/or N. This work is ongoing and currently the subject of a patent application.

Results and discussion: Zarlink Semiconductor supplied the device models used for its HJB bipolar process. Simulation tests were made using the software package APLAC to determine how accurately (5) predicted the value of A_I for the following arbitrary, but convenient, specification: $A_I = 50$ at 27°C, $N = 5$ and $I_{in} = 50$ μA with a TC of 0 ppm/°C. The adopted choice of $R_1 = 2.2$ kΩ, $R_2 = 200$ Ω satisfies (5).

Fig. 2 and Table 1 shows the simulated results for A_I and its TC. Rail supply sensitivity is conveniently expressed in Table 2 by the parameter S_v. S_v is defined as the mean percentage change in I_L per volt change in V_{CC}, over the V_{CC} range specified. The significance of the results is that (5) can be relied on as a useful design equation because the departure of A_I from the predicted value is much less than the uncertainty that would arise in practice through the tolerances on N and R_1/R_2. Thus, if the tolerances in these were both ±2% the overall accuracy would be of the order of 4%.

Table 1: Simulated current gain

V_{cc} (V)	A_I (−40°C)	A_I (27°C)	A_I (85°C)	TC of A_I (ppm/°C)
3.2	49.900	50.000	50.016	29
5	50.100	50.180	50.260	26
10	50.480	50.540	50.580	16

Table 2: Rail supply sensitivity

Temperature	S_v I_L (3–5 V)	S_v I_L (3–10 V)
−40°C	0.22%	0.17%
+27°C	0.20%	0.16%
+85°C	0.20%	0.15%

Acknowledgment: The authors thank Zarlink Semiconductor, Swindon, UK, for the device models used in this work.

22 August 2005
Electronics Letters online no: 20053035
doi: 10.1049/el:20053035

M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey (*School of Technology, Oxford Brookes University, Gypsy Lane Campus, Headington, Oxford, OX3 0BP, United Kingdom*)

E-mail: khayatleh@brookes.ac.uk

References

1 Toumazou, C., Lidgey, F.J., and Haigh, D.G.: 'Analogue IC design: the current mode approach' (IEE Circuits and Systems Series 2, Peter Peregrinus Ltd, UK, 1990)
2 Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G.: 'Analysis and design of analog integrated circuits' (Wiley, New York, 2001, 4th edn.), pp. 317–326
3 Smith, K.C., and Sedra, A.: 'The current conveyor: a new circuit building block', *Proc. IEEE*, 1968, **56**, pp. 1368–1369
4 Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G.: 'Analysis and design of analog integrated circuits' (Wiley, New York, 2001, 4th edn.), pp. 260–263
5 Hart, B.L., and Barker, R.W.J.: 'Modified current mirror with a "voltage following" capability', *Electron. Lett.*, 1982, **18**, pp. 970–972

PTAT direct current converter for bias circuit applications

M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey

A novel proportional to absolute temperature (PTAT) current converter is presented. Output current gain ratios in excess of 50 are possible without the use of an operational amplifier. Simulation measurements show an output temperature coefficient within 15 ppm/°C of the reference current over the temperature range of −40 to +85°C.

Introduction: It is particularly desirable to bias bipolar amplifiers with a proportional to absolute temperature (PTAT) collector current in order to eliminate any variations in voltage gain, that would normally arise, with changes in temperature. Traditional PTAT current generators [1, 2] can only accurately produce reference currents in the μA range because of the difficulty in fabricating close tolerance resistors of low ohmic value (<100 Ω). However, useful bias currents for bipolar amplifiers are often required to have a value of several mA in order to maintain sufficient linearity. Therefore, there is a need for some form of current converter that can scale up a reference current accurately and without introducing significant additional temperature coefficient (TC). Designs for accurate IC current converters are known but, to achieve the desired current gain, they tend to employ an operational amplifier (OA) although similar results can be obtained using a current conveyor (CC). The novel approach described here permits operation at rail voltages lower than those at which OAs and CCs normally work. Accurate and predictable current gains are achieved by choice of a resistor ratio.

Circuit operation: Fig. 1 shows an example of the proposed PTAT current converter technique. The PTAT reference current to be amplified, or attenuated, is developed using a modification of a technique described in [3]. Q_{N4}, forms part of a simple loop amplifier that forces equal currents, namely I_1, I_{REF} and I_2, through Q_{N1}, Q_{N2} and Q_{N6} by sensing any difference in these currents and feeding it back to the current sources Q_{P1}, Q_{P3} and Q_{P4}. This, in conjunction with the difference in V_{BE} of Q_{N1} and Q_{N2}, creates the necessary condition for the reference current, I_{REF}, to be PTAT. I_{REF} is given by:

$$I_{REF} = \left(\frac{V_T}{R_{REF}}\right) \ln x \tag{1}$$

where V_T is the 'thermal voltage' and x is the emitter area ratio of Q_{N2} to Q_{N1}. Additional start-up circuitry, based on a variation of a scheme described in [4], is provided. However, for simplicity it is not shown here.

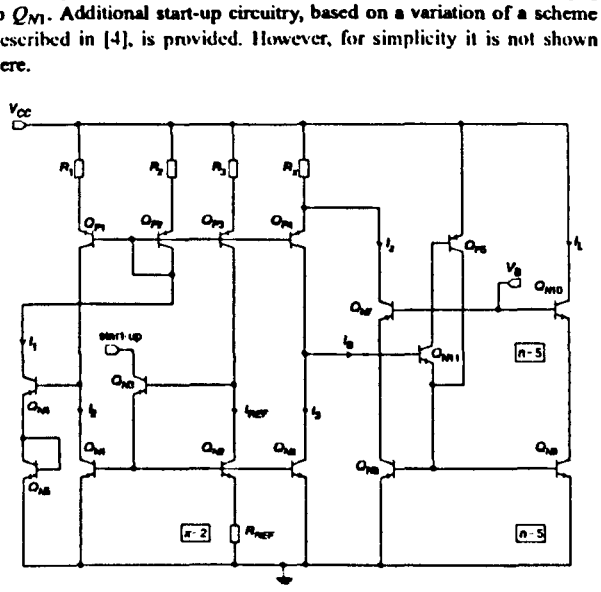

Fig. 1 *Simplified schematic of proposed PTAT current converter*

Resistors R_1, R_2, R_3 and R_X set the current gain/attenuation. A feedback loop from the collector of Q_{N7} to the emitter of Q_{P6} ensures that the emitter currents of Q_{P1}, Q_{P2}, Q_{P3} and Q_{P4} are equal (i.e. if $I_{REF} = I_1 = I_2 = I_3$ as here). The buffering action of the compound emitter-follower formed by Q_{N11} and Q_{P5} ensures that I_B is negligible compared with I_3.

Since the bases of Q_{P1}, Q_{P2}, Q_{P3} and Q_{P4} have a common potential, it follows that the potential difference across the resistors R_1, R_2 and R_3 is equal to the potential difference across resistor R_X. It should be noted that $R_1 = R_2 = R_3$. The potential difference across R_1 is:

$$V_1 = I_{REF} \cdot R_1 \tag{2}$$

while the potential difference, V_X, across R_X is:

$$V_X = (I_{REF} + I_Z) \cdot R_X \tag{3}$$

where I_Z is the collector current of Q_{N7}. Equating (2) and (3) gives the relationship between I_X and I_{REF}, namely:

$$I_Z = I_{REF}\left[\left(\frac{R_1}{R_X}\right) - 1\right] \tag{4}$$

Transistors Q_{N9} and Q_{N10}, the bases of which are driven, like those of Q_{N8} and Q_{N7}, respectively, supply the output current I_L. The bias voltage, V_B, for the cascode transistors Q_{N7} and Q_{N10} is two base-emitter voltage drops above earth, and provided by routine circuitry, not shown. Q_{N9} and Q_{N10} represent n transistors in parallel, each identical to Q_{N8} and Q_{N7}. However, they could be single transistors of similar construction to Q_{N8} and Q_{N7}, respectively, but having an emitter area n times as large. In either case $I_L = n.I_Z$. Thus:

$$I_L = I_{REF \cdot n} \cdot \left[\left(\frac{R_1}{R_X}\right) - 1\right] \tag{5}$$

This may also be expressed in terms of the current scaling factor, or current gain, A_I, which is given by:

$$A_I = \frac{I_L}{I_{REF}} = n \cdot \left[\left(\frac{R_1}{R_X}\right) - 1\right] \tag{6}$$

It is to be noted that A_I, being defined by a resistor ratio, is substantially temperature independent. Clearly, it is possible to achieve current attenuation as well as gain by choice of resistor ratio and/or n. This work is currently subject of a UK patent application number [5].

Results and discussion: Zarlink Semiconductor supplied the device models used for their HJB bipolar process. Simulation tests were made using the software package APLAC to determine how accurately (6) predicted the value of A_I for the following arbitrary, but convenient, specification: $A_I = 50$, $n = 5$, $x = 2$ and $I_{REF} = 50$ μA at 27°C. The adopted choice $R_1 = 2.2$ KΩ, $R_X = 200$ Ω satisfies (6) so that $I_L = 2.5$ mA. Table 1 shows the simulated results for A_I and its TC. Rail supply sensitivity is conveniently expressed in Table 2 by the parameter S_V. S_V is defined as the mean percentage change in I_L per volt change in V_{CC}, over the voltage range specified.

Table 1: Simulated current gain of improved circuit (A_I *target* = 50)

V_{CC} (V)	A_I (−40°C)	A_I (27°C)	A_I (85°C)	TC of A_I (ppm/°C)
3	51.039	50.995	50.945	−15
5	50.932	50.879	50.856	−12
10	50.725	50.715	50.686	−6

Table 2: Rail supply sensitivity

Temperature (°C)	$S_V A_I$ (3–5 V) (%)	$S_V A_I$ (3–10 V) (%)
−40	0.11	0.08
+27	0.11	0.08
+85	0.09	0.07

The significance of the results is that (6) can be relied upon as a useful design equation. This is because the simulated measurements of A_I are very close (within less than 2%) of the predicted value across the entire −40 to +85°C temperature and 3 to 10 V voltage ranges. In addition, the PTAT current converter only introduces an additional TC magnitude, to the output current, of less than 15 ppm/°C across the 3 to 10 V entire voltage range. Finally, this circuit exhibits very low

sensitivity to changes in power supply voltage. A_I differs by no more than 0.08% per volt across the entire 3 to 10 V voltage range and -40 to $+85$°C temperature range. It also offers the advantage of a low component count. To summarise, this work has presented a novel technique for producing accurate PTAT currents at milliampere levels without the use of an op-amp.

Acknowledgments: Thanks are due to Zarlink Semiconductor, Swindon, UK for the device models used in this work.

3 January 2006
Electronics Letters online no: 20064385
doi: 10.1049/el:20064385

M. Green, K. Hayatleh, B.L. Hart and F.J. Lidgey (*School of Technology, Oxford Brookes University, Gypsy Lane Campus, Headington, Oxford OX3 0BP, United Kingdom*)

E-mail: Khayatleh@brookes.ac.uk

References

1 Toumazou, C., Lidgey, F.J., and Haigh, D.G.: 'Analogue IC design: the current mode approach' (IEE Circuits and Systems Series 2, Peter Peregrinus Ltd, 1990), pp. 74–77
2 Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G.: 'Analysis and design of analog integrated circuits' (Wiley, New York, 2001, 4th edn.), pp. 314–317
3 Nauta, H.C., and Nordholt, E.H.: 'New class of high-performance PTAT current sources', *Electron. Lett.*, 1985, **21**, (9), pp. 384–386
4 Hart, B.L., and Barker, R.W.J.: 'Automatic start-up technique for complementary PTAT current generators', *Electron. Lett.*, 1982, **18**, pp. 776–777
5 Green, M., Hayatleh, K., Hart, B.L., and Lidgey, F.J.: 'Direct current converter circuit', UK Patent Application GB051623.8, 2005

A Novel mA Level PTAT Current Generator Technique

M. Green, K. Hayatleh, B.L Hart and F.J. Lidgey

School of Technology, Oxford Brookes University,
Oxford, United Kingdom
Khayatleh@brookes.ac.uk

Abstract—**An accurate PTAT current of mA level is often required for biasing bipolar amplifiers in order to achieve gain flatness over a specific temperature range. However, this is often difficult to achieve without the use of an Operational Amplifier (Op-Amp). This work presents two 2.5mA Proportional To Absolute Temperature (PTAT) current generator circuits, based on a technique that is the subject of a patent application. Simulation measurements show an output Temperature Coefficient (TC) within 15ppm/°C of the reference current over the temperature range of -40°C to +85°C, and a rail supply sensitivity of less than 0.32%. This is achieved without the use of an operational amplifier.**

I. INTRODUCTION

It is desirable to bias bipolar transistor long-tailed pair differential amplifiers with a tail current that is PTAT in order to minimise variation in voltage gain, that would normally arise, with change in temperature. Well established PTAT current generators [1-2] can only accurately produce reference currents in the microampere range. However, bias currents for long-tailed pair bipolar amplifiers are often required to have a value of several milliamperes in order to produce significant voltage gain and maintain sufficient linearity. Therefore, there is a need for some form of current converter that can scale-up a reference current, accurately, and without introducing any significant additional TC. Designs for accurate IC PTAT generators capable of producing currents in the milliampere range are known but they tend to employ an Operational Amplifier (Op-Amp). The novel approach described here permits operation at rail voltages lower than those at which Op-Amps normally work. Accurate and predictable current gains are achieved by choice of a resistor ratio.

II. CIRCUIT OPERATION

A. Basic Circuit

Figure 1 shows one example of the proposed PTAT current generator circuit technique. The PTAT reference current to be amplified, or attenuated, is developed using a modification of a technique described in [3]. The high performance PTAT current generator is formed by Q_{N1}, Q_{N2}, Q_{N3}, Q_{N4}, Q_{N5}, Q_{P1}, Q_{P2}, Q_{P3} and R_{REF}. The reference current, I_{REF}, is given by the well known equation shown below:

$$I_{REF} = \left(\frac{V_T}{R_{REF}}\right) \ln x \tag{1}$$

Where, V_T is the 'thermal voltage' and x is the emitter area ratio of Q_{N2} to Q_{N1}. Additional start-up circuitry based on a variation of a scheme described in [4] is provided. However, for simplicity is not shown here.

I_{REF} is mirrored via Q_{N6} and Q_{N7}, by a magnification factor y, to form two virtually identical output currents, I_{01} and I_{02}. Thus:

$$I_{01} = I_{02} = I_0 = I_{REF}.y \tag{2}$$

I_{01} and I_{02} are each connected to the respective terminals of a Voltage Following Current Mirror (VFCM) [5] formed by Q_{P4}, Q_{P5}, Q_{P6}, Q_{N8} and Q_{N9}. This configuration and that of the PTAT current generator were both chosen for their low sensitivity to power supply variations. Resistors R_1 and R_X set the current gain/attenuation. The feedback loop from the collector of Q_{N7} to the emitter of Q_{P6} ensures that the emitter currents of Q_{P5} and Q_{P6} are equal (i.e., if $I_{01} = I_{02} = I_0$, as here); the buffering action of the compound emitter-follower formed by Q_{N14} and Q_{P7} makes I_B negligible compared with I_0.

Since the bases of Q_{P5} and Q_{P6} have a common potential, it follows that the potential difference across the resistors R_1 is equal to the potential difference across resistor R_X. The potential difference across R_1 is:

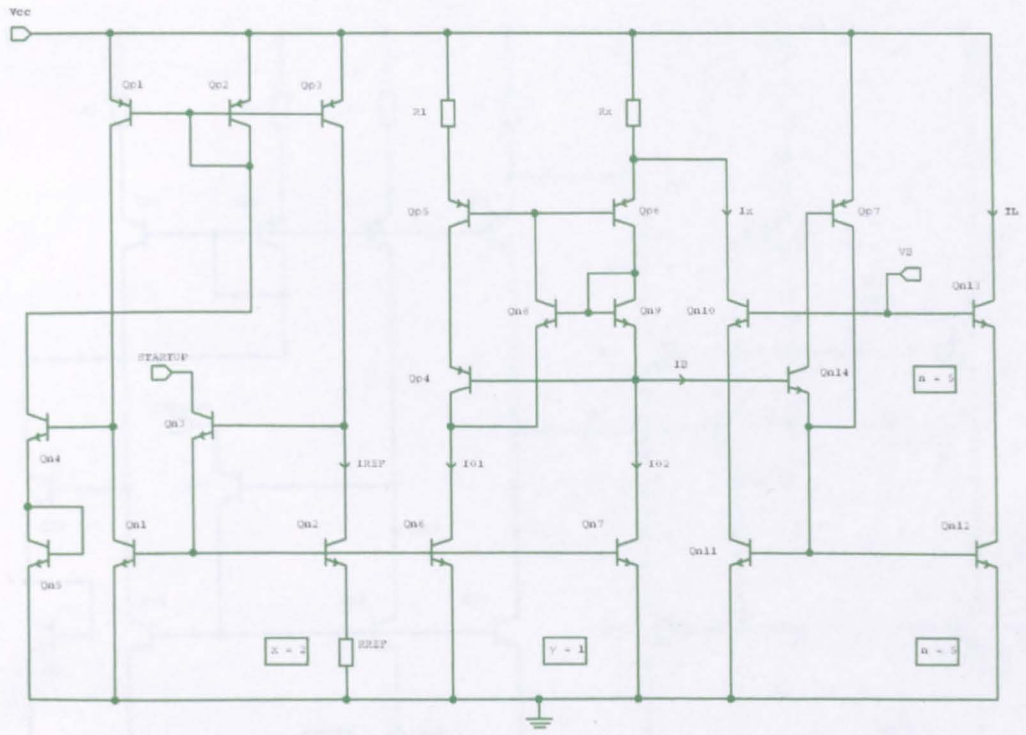

Fig. 1 - Simplified Schematic of Basic 2.5mA PTAT Current Generator

$$V_1 = I_o \cdot R_1 \tag{3}$$

Denoting the collector current of Q_{N10} by I_X, the potential difference across R_X is:

$$V_X = (I_o + I_X) \cdot R_X \tag{4}$$

Equations 2, 3 and 4, when combined, give the relationship between I_X and I_{REF}, namely:

$$I_X = I_o \left[\left(\frac{R_1}{R_X}\right) - 1\right] = I_{REF}.y.\left[\left(\frac{R_1}{R_X}\right) - 1\right] \tag{5}$$

Transistors Q_{N12} and Q_{N13}, whose bases are driven, like those of Q_{N11} and Q_{N10}, respectively, supply the output current I_L. The bias voltage, V_B, for the cascode transistors Q_{N10} and Q_{N13} is two emitter-base voltage drops above earth, and provided by routine circuitry, not shown. Q_{N12} and Q_{N13} represent n transistors in parallel, each identical to Q_{N10} and Q_{N11}. However, they could be single transistors of similar construction to Q_{N10} and Q_{N11} respectively, but having an emitter area n times as large. In either case, $I_L = n.I_X$. Thus:

$$I_L = n.I_o.\left[\left(\frac{R_1}{R_X}\right) - 1\right] = I_{REF}.y.n.\left[\left(\frac{R_1}{R_X}\right) - 1\right] \tag{6}$$

This may also be expressed in terms of the current scaling factor, or current gain, A_I, which is given by:

$$A_I = \frac{I_L}{I_{REF}} = n.y.\left[\left(\frac{R_1}{R_X}\right) - 1\right] \tag{7}$$

It is to be noted that A_I, being defined by a resistor ratio, is substantially temperature independent. Clearly, it is possible to achieve current attenuation as well as gain by choice of R_1, R_X and/or n and y.

B. *Improved Circuit*

Figure 2 shows an alternative configuration of the proposed PTAT current generator circuit technique. The high performance PTAT current generator is still formed by Q_{N1}, Q_{N2}, Q_{N3}, Q_{N4}, Q_{N5}, Q_{P1}, Q_{P2}, Q_{P3} and R_{REF} but with the addition of Q_{N6}, Q_{P4}, R_1, R_2, R_3 and R_X. These additions provide an extra PTAT current, I_1, that is identical to the reference current, I_{REF}. I_1 is given by:

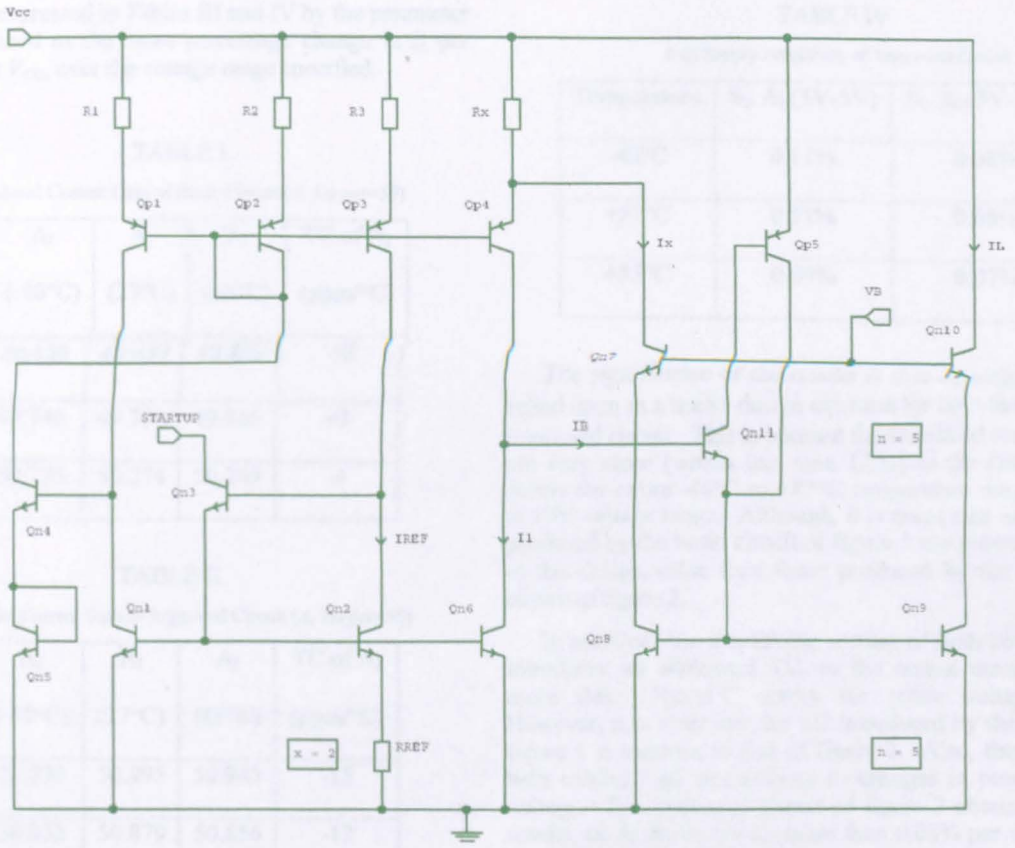

Fig. 2 - Simplified Schematic of Improved 2.5mA PTAT Current Generator

$$I_1 = I_{REF} = \left(\frac{V_T}{R_{REF}}\right).\ln x \tag{8}$$

The start-up circuitry based on that shown in [4] remains unchanged (not shown for simplicity). This configuration differs in that I_X is tapped directly from the PTAT generator and, thus, the need for a VFCM stage or equivalent is negated whilst also reducing the overall circuit power consumption.

In this case, R_1, R_2, R_3 and R_x provide the current gain/attenuation. It should be noted that R_1, R_2 and R_3 are identical. The operation of both the feedback loop and output current stage are identical to that shown in figure 1. Hence, using previous derivations it can be shown that:

$$I_X = I_1.\left[\left(\frac{R_1}{R_X}\right)-1\right] \approx I_{REF}.\left[\left(\frac{R_1}{R_X}\right)-1\right] \tag{9}$$

$$I_L = n.I_1.\left[\left(\frac{R_1}{R_X}\right)-1\right] \approx I_{REF}.n.\left[\left(\frac{R_1}{R_X}\right)-1\right] \tag{10}$$

Similarly, the current scaling factor, or current gain, A_I, which is given by:

$$A_I = \frac{I_L}{I_{REF}} = n.\left[\left(\frac{R_1}{R_X}\right)-1\right] \tag{11}$$

Clearly (7) and (11) are identical if the magnification factor y is unity.

III. RESULTS AND DISCUSSION

Zarlink Semiconductor supplied the device models used for their HJB bipolar process. Simulation tests were made using the software package APLAC to determine how accurately equations 7 and 11 predicted the value of A_I for both circuits using the following arbitrary, but convenient, specification:

$A_I = 50$, $y = 1$, $n = 5$ and $I_{REF} = 50\mu A$ at 27°C. The adopted choice $R_1 = 2.2K\Omega$, $R_2 = 200\Omega$, satisfies equation 7 so that $I_L = 2.5mA$.

Tables I and II show the simulated results, for A_I and its TC, regarding the basic and improved circuits respectively. Rail supply sensitivity for the basic and improved circuits is

conveniently expressed in Tables III and IV by the parameter S_V. S_V is defined as the mean percentage change in I_L per volt change in V_{CC}, over the voltage range specified.

TABLE I.

Simulated Current Gain of Basic Circuit (A_I *Target=50*)

V_{CC} (V)	A_I (-40°C)	A_I (27°C)	A_I (85°C)	TC of A_I (ppm/°C)
3	49.429	49.447	49.487	+9
5	49.746	49.753	49.765	+3
10	50.275	50.274	50.249	-4

TABLE II.

Simulated Current Gain of Improved Circuit (A_I *Target=50*)

V_{CC} (V)	A_I (-40°C)	A_I (27°C)	A_I (85°C)	TC of A_I (ppm/°C)
3	51.039	50.995	50.945	-15
5	50.932	50.879	50.856	-12
10	50.725	50.715	50.686	-6

TABLE III.

Rail Supply Sensitivity of Basic Circuit

Temperature	S_V A_I (3V-5V)	S_V A_I (3V-10V)
-40°C	0.32%	0.24%
+27°C	0.31%	0.24%
+85°C	0.28%	0.22%

The significance of the results is that equation 7 can be relied upon as a useful design equation for both the basic and improved circuit. This is because the simulated results for A_I are very close (within less than 1.2%) to the design value across the entire -40°C to +85°C temperature range and 3V to 10V voltage range. Although, it is noted that values of A_I produced by the basic circuit of figure 1 are generally closer to the design value than those produced by the improved circuit of figure 2.

TABLE IV.

Rail Supply Sensitivity of Improved Circuit

Temperature	S_V A_I (3V-5V)	S_V A_I (3V-10V)
-40°C	0.11%	0.08%
+27°C	0.11%	0.08%
+85°C	0.09%	0.07%

The significance of the results is that equation 7 can be relied upon as a useful design equation for both the basic and improved circuit. This is because the simulated results for A_I are very close (within less than 1.2%) to the design value across the entire -40°C to +85°C temperature range and 3V to 10V voltage range. Although, it is noted that values of A_I produced by the basic circuit of figure 1 are generally closer to the design value than those produced by the improved circuit of figure 2.

In addition, the amplifying section of both circuits only introduces an additional TC, to the output current, of no more than 15ppm/°C across the entire voltage range. However, it is clear that the TC introduced by the circuit of figure 1 is superior to that of figure 2. Also, these circuits both exhibit high insensitivity to changes in power supply voltage. The improved circuit of figure 2 obtains the best results, as A_I differs by no more than 0.08% per volt across the entire 3V to 10V voltage range and -40°C to +85°C temperature range. It also offers the advantages of reduced component count and current consumption. In summary, this work has presented a novel technique for producing accurate PTAT currents of milliampere level without the use of an Op-Amp.

ACKNOWLEDGMENT

Thanks are due to Zarlink Semiconductor, Swindon, UK for the device models used in this work.

REFERENCES

[1] C. Toumazou, F.J. Lidgey and D.G. Haigh, *Analogue IC Design: the current mode approach*, IEE Circuits and Systems Series 2, Peter Peregrinus Ltd, 1990, pp. 74-77.

[2] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits (fourth edition)*. Wiley, New York, 2001, pp314-317.

[3] H.C. Nauta and E.H. Nordholt, 'New Class of High-Performance PTAT Current Sources', Electronics Letters, April 1985, Vol. 21, No.9, pp. 384-386.

[4] B.L. Hart 'Automatic start-up technique fo complementary PTAT current generators', Electronic Letters, 1982, 18, pp 776-777.

[5] B.L. Hart and R.W.J. Barker, 'Modified current mirror with a "voltage following" capability', Electronics Letters, 1982, 18, pp. 970-972.