A 0.6V pure MOS voltage Reference for Bio-medical applications with 40ppm/°C temperature drift

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This paper exploits the well-known MOS beta multiplier circuit to synthesise a voltage reference, which is well suited for low voltage and ultra-low power bio-medical applications. The present technique uses only MOS transistors to generate PTAT and CTAT currents. Self-biasing technique has been used to minimize the temperature and power supply dependency. A prototype in 65nm CMOS has been developed, at room temperature it is generating 40μmV reference voltage with 2.6mV drift over wide temperature range (from -40 to 125°C). This has been designed to operate with a power supply down to 0.6V and consumes 1.4μA current from the supply. The simulated temperature coefficient is 40ppm/°C. Circuit occupies 0.039mm² area.

Introduction: A low voltage bandgap reference, specifically one that can operate on low voltage is always challenging. There is a growing requirement that operates in wide range applications including filters, memory, data converters, bio-medical applications [1]. Portable and wearable bio-medical devices are capable of detecting signals in areas such as electrocardiography (ECG) and electroencephalography (EEG), sensitive to these sensitive signals require high precision ADC (~12 bit) which requires highly accurate and low power voltage reference circuit.

The fundamental operating principle of a reference circuit is to generate scaled combination PTAT and CTAT current/voltage to generate temperature independent voltage. There have been several attempts to build this concept. A typical low voltage bandgap [2] uses BJTs to generate PTAT current and to fabricate in the standard CMOS process parasitic vertical PNP Bipolar Junction Transistor (BJT) has been used. This has three problems, one of these transistors is having poor current gain (β) and sensitive to process variation which could lead to temperature drift of the reference voltage. The second problem is the power supply voltage requirement, Vbe of the BJT (~0.7V) doesn’t scale with the process and limits the supply voltage. The third problem is BJT bias current is significantly high compared to the counterpart (MOSFET), which is a big problem for the bio-medical and wearable application. Hence there is a clear motivation for pure MOS transistor based designs.

Peak current source has been modified as bandgap reference by exploiting the difference between Vgs of two transistors [3], but this requires cascading of transistors hence not suitable for low voltage and poor power supply rejection, which demands a Voltage Regulator. Another method is to generate reference based on extrapolated M3, M4 threshold voltage (Vth) at very low temperature to realize low voltage operation [4], but this has unacceptable process variation which requires calibration. [5,6] are based on mutual cancellation of mobility and threshold voltage, but it is difficult to track both variations and often very sensitive to the transistor models very strongly, which might create yield problem while going for mass production. Most of the designs use op-amps in the core circuit to achieve high performance such as temperature independence, power supply insensitivity, but they come at the expense of power and area [7]. These designs require voltage headroom’s also, which makes them not suitable for low voltage applications. This paper explores standard beta multiplier circuit to generate PTAT and CTAT currents and finally bandgap reference voltage generation. Some of the key metrics differentiate our work from the state of art is low power, low voltage, and less complexity. The rest of the paper is organized as follows. Section 2 introduces the beta multiplier circuit and qualitative treatment of its PTAT and CTAT nature, Section 3 describes proposed reference circuit and implementation details. Finally, section 4 summarizes the simulation results and layout of the prototype.

2. Beta Multiplier: Fig.1 shows the beta multiplier (constant g_m) conventional circuit [8]. The fundamental principle of working is to create a voltage drop equal to the difference between the Vgs of two transistors carrying same current but different sizes (W/L). Transistor M1, M2 connected in a such a way that Vgs-1-Vgs-2 defines current through Rs. The current mirror formed by M2, M1 will force the same current through Transistors M3, M4. Though this is a very common circuit, feedback mechanism in this circuit is very subtle. Fig.2 shows the I-V characteristics of M3, M4. From the figure, circuit settles at the intersecting point of the two curves. During the circuit converging to the desired operating, it can be either side of the intersecting point. If the current lesser than the desired one means I1>I2 and vice versa. If I1-I2>0, then circuit current must increase. Current can be increased by increasing voltage of the node A. So feedback should work in such a way that somehow node A has to increase if circuit detects I1-I2>0 and vice versa. Since M1, M2 connected in series, node A can detect the current difference and it increases according to i1-i2 polarity hence by connecting Node A to gate of the M1, circuit acts as negative feedback circuit. M1 aspect ratio (W/L) must be higher than M4, because Vgs has to be lesser than Vn+Vt. To save power this circuit has been designed in the deep sub-threshold region by increasing the devices sizes and controlling resistor Rs.

Drain current of the NMOS operating in the sub-threshold region can be expressed as follows.

\[ I_D = \frac{W}{L} I_0 \exp \left( \frac{V_{gs} - V_{th}}{\eta V_T} \right) \left( 1 - \exp \left( \frac{-V_{th}}{V_T} \right) \right) \]  

(1)

Where \( I_0 = \mu_n C_{ox} (\eta = 1) W/2 \), and W is the width is the length, \( \mu_n \) is electron mobility, \( C_{ox} \) is gate oxide capacitance, \( \eta \) is sub-threshold slope factor, \( V_T \) is thermal voltage, \( V_{th} \) is threshold voltage. For Vds=4V (−100mV at room temperature), Vds term in (1) is very less and Ids is almost independent of Vds, it is expressed as

\[ I_D = \frac{W}{L} I_0 \exp \left( \frac{V_{gs} - V_{th}}{\eta V_T} \right) \]  

(2)

\[ V_{gs} = V_{th} + \eta V_T \ln \left( \frac{I_D}{I_0} \right) \]  

(3)

Fig. 1 Beta Multiplier circuit

Fig. 2 V-I characteristics of the beta multiplier

The circuit configuration as shown in fig:1(a) constrains the difference between vgs of M3, M4 in a relation given as follows.
\[ V_{gs3} - V_{gs4} = I_1 R_4 \]  

(4)

Substituting (3) into (4) results the transistor current as follows.

\[ I_1 R_4 = \eta V_T \ln \left( \frac{T}{T_0} \right) \]

(5)

If the aspect ratio of \( M_6 \) is \( \beta \) times higher than \( M_5 \), then current can be expressed as

\[ I_1 = \frac{\eta V_T \ln(\beta)}{R_S} \]

(6)

From (6), the voltage drop across \( R_5 \) is PTAT, because thermal voltage (K\( T \)) increases with temperature. A PTAT current carrying Transistor gate to source voltage (\( V_{gs} \)) and threshold voltage (\( V_{th} \)) decreases with temperature [12], because increasing temperature will increase electrons thermal energy and requires less voltage to invert the channel in the MOSFET and it can be approximated as a first order polynomial with a negative slope as follows.

\[ V_{gs}(T) - V_{gs}(T_0) + K_{th}(T - T_0) \]

(7)

Where \( K_{th} \) is temperature coefficient of \( V_{gs} \). Fig. 3 shows the simulated gate to source voltage of the transistor wrt temperature. It has been showing CTAT nature with -0.3mV/0C temp coefficient.

\[ \frac{\partial V_{ref}}{\partial T} = 0 \] at a known temperature. Hence by differentiating (8) we can deduce the following condition.

\[ \alpha_1 \frac{R_1}{R_S} \frac{\partial V_{gs}}{\partial T} + \alpha_2 \frac{V_{gs3}}{R_2} = 0 \]  

(9)

At room temperature \( \frac{\partial V_{gs}}{\partial T} = 0.087mV/0C \) and from previous section \( \frac{\partial V_{gs}}{\partial T} = -0.3mV/0C \). We have chosen \( \alpha_1 = \frac{1}{\beta} \), \( \alpha_2 = 1 \) for the design flexibility and \( \beta = 24 \) for the layout matching between \( M_5 \) and \( M_6 \). Substituting these values into (9) we can show that \( \frac{R_1}{R_S} = 3.255 \) to keep a perfect balance between CTAT, PTAT current and hence minimum temperature drift.

**Fig. 3 Gate to source voltage wrt temperature**

3. **Proposed Bandgap reference circuit:** As explained in the introduction, the idea of bandgap reference is scaled summation of PTAT and CTAT current’s and convert into voltage. From the section 2, Beta multiplier bias current is having PTAT nature. Unfortunately, CTAT current is not available in beta multiplier, but \( Vgs3 \) will have CTAT nature, using a conventional voltage to current converter formed by \( OP2, M5, R1 \) will create CTAT current through \( M5 \). Fig. 2 shows the proposed full schematic of the bandgap reference. It contains Beta multiplier, \( V \) to \( I \) converter and current summation network. \( M_p \) carries PTAT current and \( M_c \) carries CTAT and hence the voltage across \( R2 \) is temperature independent voltage. To have a flexible design and minimize the resistor values, used scaling factors \( \alpha_1 \) and \( \alpha_2 \) in the current mirrors \( M_1, M_p \) and \( M_2, M_c \), respectively.

Current through \( M_5 \) is given by \( \alpha_1 \frac{V_{gs3}}{R_1} \)

Voltage across \( R2 \) is given by the following expression

\[ V_{ref} = \left( \alpha_1 \frac{\partial V_T}{\partial T} + \alpha_2 \frac{V_{gs3}}{R_2} \right) \frac{R_1}{R_S} \]

(8)

\[ \frac{\alpha_1}{\alpha_2} \eta V_T \ln(\beta) + \frac{\alpha_2}{\alpha_1} \frac{V_{gs3}}{R_2} \]

\[ \frac{\partial V_T}{\partial T} = \frac{m_V}{T} \]

\[ \frac{\partial V_{gs3}}{\partial T} = \frac{1}{\beta} \]

\[ \frac{\partial V_{gs}}{\partial T} = -0.3mV/0C \] and from previous section \( \frac{\partial V_{gs}}{\partial T} = -0.3mV/0C \) at a known temperature. Hence by differentiating (8) we can deduce the following condition.

\[ \alpha_1 \frac{R_1}{R_S} \frac{\partial V_{gs}}{\partial T} + \alpha_2 \frac{V_{gs3}}{R_2} = 0 \]  

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**Fig. 4 Proposed bandgap Reference**

**Fig. 5 Self-bias CTAT generator**

CTAT circuit is a voltage to current converter with \( Vgs \) as input. As shown in Fig. 4, \( OP1 \) adjusts the current through \( M5 \) until the voltage drop across \( R1 \) equals to the \( Vgs \) of the \( M3 \). The bottle neck here is any offset in the opamp will also convert as current, which will create an error in the desired CTAT current, hence opamp needs to design with ultra-low offset. Increasing device sizes in the opamp will decrease the offset, but due to inverse square law relation between offset and device area [10], this method occupies a lot of silicon area. Very-efficient and well known way of minimizing the offset will be chopper stabilization method but this needs a clock generator and ripple filter [11]. Self-bias is one way of biasing analog circuits which will have minimal offset, less temperature drift, so we have chosen self-bias scheme [9] and Fig. 5 shows the detailed implementation of the circuit. \( M_1, M_2, M_3, M_4, M_t \) forms the opamp and \( M_5, R_1 \) forms the current converter. \( M_2, M_c \) transistors produce bias voltage required for the \( M_t \) by sensing the output of the opamp. Unfortunately, self-biasing needs start up circuit to kick the circuit from undesired zero current operating point, for simplicity start-up circuit hasn’t shown in fig. 5.
Fig. 6 Self-bias CTAT open-loop response

Fig. 6 shows the open loop frequency response of the CTAT current generator, which has been designed with 80dB dc gain to minimize the systematic offset and 50° phase margin for a well-behaved transient response. To assess the efficiency of the self-bias strategy, opamp offset variation with temperature has been simulated and compared with a fixed bias (means Mt bias has been derived from a diode connected transistor carrying fixed current). Fig. 7 shows the offset of the opamp, which shows 3x improvement with self-bias scheme.

Fig. 7 Simulated Offset of the self-bias opamp

4. Bandgap reference simulation results:
Proposed circuit has been implemented in 65nm 1-poly 8-metal CMOS technology, Table-1 shows the parameters of the transistors and resistors used in the proposed voltage reference circuit.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Bandgap Reference</th>
<th>Self-Bias Opamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Name</td>
<td>W/L (um/um)</td>
<td>Component Name</td>
</tr>
<tr>
<td>M1</td>
<td>42/3.2</td>
<td>M1</td>
</tr>
<tr>
<td>M2</td>
<td>42/3.2</td>
<td>M2</td>
</tr>
<tr>
<td>M3</td>
<td>48/3</td>
<td>M3</td>
</tr>
<tr>
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<tr>
<td>M6</td>
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<tr>
<td>M7</td>
<td>14/3.2</td>
<td>M7</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Resistors</th>
<th>Component Name</th>
<th>Resistance (KΩ)</th>
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</thead>
<tbody>
<tr>
<td>Rr</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>Rs</td>
<td>227.85</td>
<td></td>
</tr>
<tr>
<td>Rs</td>
<td>312</td>
<td></td>
</tr>
</tbody>
</table>

Simulations have been performed on layout extracted netlist and results as follows. Fig: 8 shows the CTAT and PTAT, scaled summation of these currents produces reference voltage according to the equation (9).

Fig. 8 CTAT and PTAT currents

Fig:9 shows the bandgap reference voltage (voltage across Rs) variation from -40°C to 125°C. At room temperature reference voltage is 404mV, the maximum deviation of the voltage over full temperature range is 2.64mV means 0.65% accuracy and this design achieves 40ppm/°C while powered from 0.6V supply. The circuit starts working properly when power supply voltage greater than or equal to 0.6V. Minimum working power supply voltage 0.6V limited by CTAT generator opamp. In the supply voltage range from 0.6 to 1V, reference voltage changes by 2.3mV means the supply or line sensitivity is 1.8%/V. Yield is the main parameter for volume semiconductor products, hence Monte Carlo variation is critical results for any sensitive circuits like the present one. Fig:11 depicts the histogram of the reference voltage, showing 2.166mV standard deviation with a mean of 404mV.

Fig. 9 Bandgap reference voltage wrt temperature

Fig.12 shows the simulated power spectral density (PSD) of the reference voltage. From the noise analysis of the circuit, flicker noise of transistor M3,M4 and channel thermal noise of the CTAT generator...
opamp (OA1) are the dominate noise contributors. The summary of the performance listed in table II.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Supply Voltage</td>
<td>0.6</td>
<td>V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>1.4</td>
<td>µA</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>404 mV</td>
<td>µV</td>
</tr>
<tr>
<td>Temperature range</td>
<td>-40 to 125°C</td>
<td></td>
</tr>
<tr>
<td>Temperature Coefficient</td>
<td>40</td>
<td>ppm/°C</td>
</tr>
</tbody>
</table>

Integrated Noise (.1-10KHz) | 41 uV |
Technology                  | 65 nm |
Area                        | 3975 um²|

Conclusion: A low voltage bandgap reference circuit has been proposed and demonstrated 40ppm/°C temperature coefficient. With the help of Sub-threshold MOSFET current equation, closed form for the output voltage has been derived and it is closely matching with the simulation results. A transistor level Demonstration with the layout shown and all results have been explained in the last section.

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References