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doi: 10.1016/j.aeue.2014.04.022

This version is available: https://radar.brookes.ac.uk/radar/items/5ad32a31-939d-4983-98df-66b0d86ec9ec/1/

Available on RADAR: July 2016
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CMRR-Bandwidth Extension Technique for CMOS Differential Amplifiers

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Abstract

An exemplary design demonstrates how to extend the common-mode rejection ratio (CMRR) bandwidth of a CMOS differential amplifier. The design presented uses MOSFETs with a channel length of 180nm. A novel circuit technique is employed that partially compensates for the output capacitance of the tail current sink, thereby more than quadrupling the CMRR bandwidth in the example considered.

Keywords: (MOSFET differential amplifier, Common-mode-rejection-ratio, Bandwidth)

1. Introduction

The primary function of a differential amplifier is to produce an output signal that is a linearly amplified version of the normally small difference between two input signals, while rejecting the larger part of the two input signals that are common to both of them. The extent to which it is able to do this successfully is quantified by the ‘Common-Mode-Rejection-Ratio’ (CMRR), an important parameter in differential amplifiers for many applications, particularly in medical instrumentation [1]. The most commonly encountered common-mode voltage is line or mains interference, at 50Hz or 60Hz. However, with increasing use of switched-mode power supplies and other higher frequency generators, good CMRR at higher frequencies is becoming more important to reduce the amplitude of high frequency common-mode signals in precision instrumentation applications. There have been many improvements to the classical differential pair amplifier [2-4] that improve the CMRR. However, almost all increasing the low frequency CMRR by reducing the common-mode gain, but little has been published to date to address the need for higher CMRR bandwidth performance. This paper outlines a circuit technique that specifically addresses this issue by reducing the tail sink-current capacitance significantly, resulting in a substantial increase in the CMRR bandwidth. Simulation results for an exemplary MOSFET source-coupled differential design, illustrate the advantage of the technique. It produces a four-fold CMRR bandwidth improvement.

2. Normal Circuit Operation

The amplifier shown in Fig.1 is a standard type of MOSFET directly-coupled differential amplifier, appropriately labelled for the discussion that follows. It is well-known that such a source-coupled differential pair amplifier provides good performance provided $M_1$ and $M_2$ are well-matched. That is achievable with good IC design techniques, such as the use of common-centroid layout methodology.

Fig. 1. Typical CMOS differential amplifier circuit $R_T$, $C_T$, $C_{gd3}$, $C_s$ and $C_{db}$ are defined in the text
M1 is in the common-gate connection with its gate connected to DC voltage $V_{GG}$, where $V_{DD} > V_{GG} > V_{SS}$. The drain current $I_T$ is supplied by the Tail Current Generator (TCG) connected to its source. TCG can be merely a resistor but is often a current generator in order to increase the incremental input resistance, $R_T$, seen looking into the drain of M1. This needs to be a high value for a low common-mode gain and hence a high CMRR at low frequencies. TCG will have an unavoidable nodal capacitance, $C_T$, associated with it. This needs to be low to maximize the CMRR bandwidth.

The amplifier inputs $v_1$ and $v_2$ and, in this particular case, the single output $v_0$ can each be considered to comprise two components, (i) a differential-mode component, $v_d$, and (ii) a common-mode component, $v_c$.

Thus,

$$v_1 = v_c + \frac{1}{2}v_d$$

(1)

$$v_2 = v_c - \frac{1}{2}v_d$$

(2)

and,

$$v_0 = A_d v_d + A_c v_c$$

(3)

The differential-mode voltage gain, $A_d$, and the common-mode voltage gain, $A_c$, are defined as follows,

$$A_d = \left| \frac{v_o}{v_d} \right| \text{ With } v_c = 0$$

(4)

and,

$$A_c = \left| \frac{v_o}{v_i} \right| \text{ With } v_d = 0$$

(5)

The CMRR, denoted here by the symbol $\varrho$, is defined as,

$$CMRR = \varrho = \frac{A_d}{A_c}$$

(6)

$A_d$ and $A_c$ are frequency-dependent, hence so too is $\varrho$. For the determination of $A_d$ the differential-drive considered, the long-tailed pair, formed by M1, M2 and its common-source tail current $I_T$, is imagined to be reconfigured as two common-source half circuits. By inspection, $A_d$ has a DC and very-low-frequency gain of magnitude $g_m R'_L / 2$, where $g_m$ is the transconductance of each of M1, M2 at a DC operating current $I_T$ and $R'_L = R_L \parallel r_{ds} \ (r_{ds} \text{ being the drain-source incremental resistance of each of the MOSFETs}).$ Based on the work of [5], with appropriately modified notation, $A_d$ exhibits a dominant pole at a radian frequency $\omega_{pc}$.

$$\omega_{pc} = \frac{1}{R'_L C_L}$$

(7a)

$$\omega_{zc} = \frac{1}{R_T C_T}$$

(7b)

In this equation, $C_{gs}$ and $C_{gd}$ have their usual MOSFET significance and $C_L$ is the load capacitance existing at the drain of each of M1, and of M2.

For the determination of $A_c$, the circuit is regarded as two separate stages, each having a source load $2Z_T$, where, $Z_T = R_T / C_T$ and the drain load $Z_L = R'_L / C_L$.

Hence, in terms of the complex frequency variable $s$, $A_c(s) = \frac{Z_L}{2Z_T} = \frac{R'_L}{2R_T} \frac{(1 + s R'_T C_T)}{\left(1 + s R'_L C_L\right)}$

(8)

Thus, $A_c$ exhibits a DC and very low-frequency gain of magnitude $-R'_L / 2R_T$, and a pole at a radian frequency $\omega_{pc}$ and zero at $\omega_{zc}$.

$\omega_{pc} = \frac{1}{R'_L C_L}$

(9a)

$\omega_{zc} = \frac{1}{R_T C_T}$

(9b)

$C_T$ comprises three capacitances, $C_{gd}$, and $C_{gb}$, respectively the drain-gate and drain-substrate capacitance of M1, together with $C_T$ the stray capacitance at its drain, thus,

$$C_T = C_S + C_{db} + C_{gb}$$

(10)

The zero at $\omega_{zc}$ on the plot of $A_c$ versus $\omega$ now appears as a pole on the CMRR-frequency plot in addition to the pole at $\omega_{pc}$, and the pole of $\omega_{pc}$ on the $A_c$ plot appears as a zero on the CMRR plot. The nature of existing circuit designs is such that $\omega_{pc} > \omega_{zc}$, because $R_T >> R'_L$, $R_S$. Furthermore, $\omega_{pc} > \omega_{zc}$ because, even if $(C_T + C_{pd}) = 10 C_T$, $R_T >> R'_L$, $R_S$ (e.g., $R_T >> 100 R'_L$).

Consequently, $\omega_{zc}$ is the dominant pole on the CMRR-frequency plot, and effectively determines the CMRR -3dB bandwidth because of the relationship of $\omega_{zc}$ to $\omega_{pd}$ and $\omega_{pc}$.

Thus, on a Bode plot of $\varrho$ versus $\omega$, $\varrho$ is constant at a value $\varrho_o = g_m R_T$ only up to a frequency $\omega_{zc}$. From the above discussion,

$$\varrho_o \omega_{zc} = g_m R_T$$

(11)

So, for a specified and practically achievable $\varrho_o$, $\omega_{zc}$ is maximized by minimizing $C_T$. This can be done, as described below, by using a MOSFET variant of an elegant bipolar technique outlined by Baxandall and Swallow [6], but seemingly neglected in the literature until investigated in detail in recent years by Terzopoulos [7].

In passing, it is worth noting that the constancy of the product $\varrho_o \omega_{zc}$ with variation in $R_T$ is analogous to the constancy of the gain-bandwidth product in resistively loaded common-source (and common-emitter) voltage amplifier stages.
3. Improved CMRR Circuit

The circuit shown in Fig.2 is a modified version of Fig.1, in that an additional common-gate connected P-MOS transistor, M4, is now incorporated into the circuit to compensate for C<sub>dg3</sub>, and M4 operates with its gate connected to a DC supply, V<sub>NN</sub>, where, V<sub>DD</sub>=V<sub>NN</sub>=V<sub>SS</sub>, and its source is connected to the gate of M3. It is supplied with a DC bias current, I<sub>k</sub>, and its drain is connected to the source of M3. A change in the drain voltage of M3 gives rise to a change i<sub>j</sub> in the gate-drain capacitance, C<sub>gd3</sub>.

A part, i<sub>k</sub>, of i<sub>j</sub> is returned to the source circuit of M3. Hence, at the drain terminal of M3, C<sub>gd3</sub> appears to be a substantially smaller capacitance C<sub>gd3</sub>.

\[
C_{gd3} \approx C_{gd3} \left[ 1 - \frac{i_k}{i_j} \right]
\]  (12)

The nodal capacitance at the drain of M3, which was designated C<sub>j</sub> in Fig.1, now becomes C<sub>T</sub>

\[
C_T = C_S + C_{dh3} + C_{gd3} \left[ 1 - \frac{i_k}{i_j} \right]
\]  (13)

The condition \[ \frac{i_k}{i_j} = 1 \] is not possible because of current lost in the gate-source capacitance, C<sub>gs4</sub>, and source-substrate capacitance, C<sub>shb</sub>, of M4.

However, the ratio \[ \frac{i_k}{i_j} \] can be made to approach unity by suitably proportioning the gate width of M4 relative to that of M3, and by choice of the ratio \[ \frac{I_k}{I_f} \], for a given value of I<sub>f</sub>.

4. Results and Discussion

To demonstrate the proposed bandwidth extension technique, Fig.2 was simulated for an illustrative, but not necessarily optimised, design using CADENCE/ VIRTUOSO, with process tsme18rf technology. The channel length for all the transistors was 180nm, and the gate widths of corresponding transistor number subscript, were: \( w_f = w_f = 1\mu m; \ w_f = 10\mu m; \) \( w_f = 20\mu m. \) Test conditions were: \( R_S = 0; \ V_{DD} = 5V; \ V_{NN} = -2.5V; \ V_{SS} = -5V; \ V_{GG} = 1V; \ I_f = 0.1mA; \ I_f = 1mA. \) I<sub>f</sub> was the output of a PMOS 1:1 current mirror with a cascode output stage. TCG was an NMOS 1:1 current mirror with a double-cascode output stage added to give increased incremental output resistance.

In the test mode, Fig.2 was used throughout. In the first series of tests the CMRR-frequency performance of Fig.1 was simulated. To achieve this the drain terminal of M4 was disconnected from the source of M1, and connected instead to V<sub>SS</sub>. The output of the TCG was set to 1mA. Graph (A) in Fig.3 shows the resulting CMRR performance.

In a second series of tests, intended to show the improvement in CMRR bandwidth, the circuit shown in Fig.2 was used with the output of the TCG set to 1.1mA. Thus, M3 operated under the same DC conditions for both tests. The CMRR performance is shown by Graph (B) in Fig.3.
bandwidth, $\omega_{zc}$ as determined from the phase-shift corresponding to the -3dB points, is more than quadrupled.

In a third series of tests to see what happens when the design of Fig.1 was operated with same total current as the proposed design of Fig.2, $I_f$ in Fig.1 was 1.1mA, the current used for Fig.2. The resulting CMRR-frequency plot is curve C, which shows a lower cut-off frequency than curves A and B. Curves A, B and C all have slightly different values of $g_o$. This is because the different DC bias currents in the tests leads to differing values of the small signal parameters $g_m$ and $r_d$ of the MOSFETs (and hence differing values for $R_T$). Curves A and C are for the same $C_T$, but the effective $R_T$ of $C_T$ is greater than that of A. In accordance with the discussion in section 2, above, this means a lower $\omega_{zc}$ but that the curves are coincident well above their cut-off frequencies.

It should be noted that the load resistors ($R_L$) have been used to simplify the discussion and analysis. The resistive loads gave a low frequency value of $A_d$ in the region of 60dB. In practice it is most likely that P-MOS transistors configured as active load current sources would be used instead to provide a considerably higher $A_d$. However, the method of increasing bandwidth of CMRR which has been presented here is still maintained with active loads in the drains of $M_1$ and $M_2$.

In this paper a MOSFET differential amplifier has been considered because of the growing importance of CMOS in analogue circuit design. However, depending on the application, bipolar transistors maybe employed, instead of MOSFETs, with $M_1$, $M_2$, $M_3$, $M_4$ being replaced by bipolar transistors $Q_1$, $Q_2$, $Q_3$, $Q_4$ respectively. Then the presence of $Q_4$ not only partially compensates of the collector-base capacitance of $Q_3$, but, as shown in [7], it also increases the incremental output resistance seen looking into its collector.

5. Conclusions

The addition of only one transistor, plus associated bias circuitry, into a conventional source-coupled differential amplifier has been shown to extend the CMRR bandwidth substantially. This performance improvement is a result of local feedback reducing the source-coupled nodal capacitance of the differential pair. This technique is primarily applicable to an integrated circuit realization of the source-coupled differential amplifier because closely matched transistors operating at the same temperature are essential for satisfactory operation.

References


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In 1991 he was joint winner of the IEE’s Rayleigh Best Book Prize for his contribution to, ‘Analog Signal Processing: the Current-Mode Approach’, published by Peter Peregrinus Limited. Also, he has a long term interest in using computers in education and in recent years has focused on the development of computer-based-learning for teaching undergraduate electronics.