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Improved Designs for Current Feedback Op-Amps

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ABSTRACT

The input stage design in CFOAs is primarily responsible for determining the performance of the amplifier, including CMRR [1], [2]. This paper presents the designs of two new CFOAs, one employing a cascoding technique, the other a bootstrapping technique, that provide both a high CMRR (common-mode rejection ratio) and a reduced d.c. offset voltage. Moreover, the new CFOAs design exhibits an extended high frequency bandwidth, and improved gain accuracy, enabling them to be used in applications requiring variable closed-loop gains with constant bandwidth.

Keywords: voltage-mode operational amplifier; Analogue signal processing; Current-feedback op-amp; Current mode technique; Common-mode rejection ratio; Slew-rate; Bandwidth.

1. Introduction

The term operational amplifier or “op-amp” refers to class of high gain DC coupled amplifier with two inputs, inverting and non-inverting, and a single output [3], [4]. The op-amp is used extensively in almost every electronic system, as it is the backbone, and the core of all fields of electronic signal processing [5], [6].

In electronic circuit design, there are many occasions where a general-purpose voltage-mode operational amplifier (VOA) is useful. If the application calls for differential inputs, high input impedance, low output impedance, high common-mode rejection ratio (CMRR), and low input referred offset voltage, the (VOA) provides a basic topology for achieving these requirements. Unfortunately, it has inherent limitations in both the gain-bandwidth trade-off and slew-rate (SR) [7], [8]. Typically, the gain-bandwidth product is a constant and the slew-rate is limited to a maximum value determined by input stage bias current [9]. The slew-rate limitations of the VOA are overcome in the alternative architecture op-amp, referred to as the current-feedback op-amp (CFOA) [10], [11]. CFOAs have been around approximately 35 years, but their popularity increased in only the last 15 years. CFOAs have greater slew rate than VOAs, thus, CFOAs are receiving increasing attention as basic building blocks in analog circuit design, and are now recognized for their excellent performance in analog signal processing [12]. CFOAs can therefore be better at solving high frequency problems than their VOA counterparts [13], [14].

Despite exhibiting excellent high frequency and high speed performance, current-feedback operational amplifiers (CFOAs) generally exhibit poor 10.1080/21681724.2015.1023366In the new designs presented here, a cascoding technique is employed in the input stage. The simulation results presented below show significant improvements in performance of CMRR, power supply rejection ratio (PSRR), and bandwidth, as well as a desirable reduction in input referred offset voltage.

2. AN ESTABLISHED INPUT ARCHITECTURE

For comparison purposes, the schematic circuit of an established CFOA architecture is shown in Fig. 1. [20].

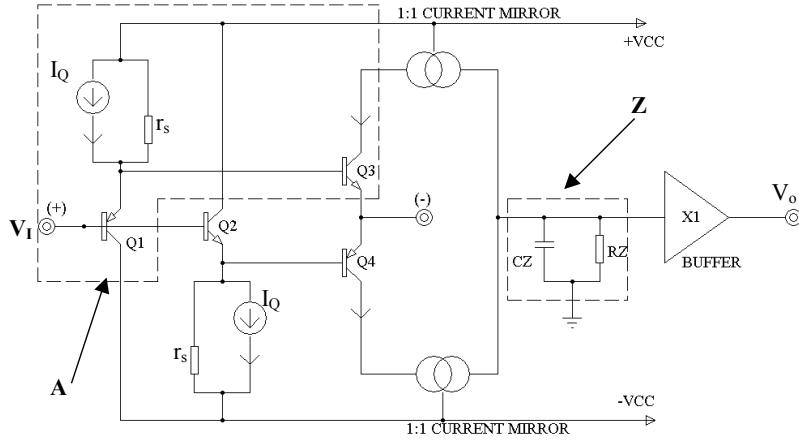


Figure 1. Schematic of an established CFOA architecture

For simplicity in a first-order analysis, the NPN and PNP transistors are assumed to have identical characteristics. Within the contour A, Q_1 together with its emitter load (bias current source I_Q with output resistance r_s) and Q_3 comprise an input ‘half-circuit’ and it is this half-circuit concept that is explored further in this paper. The other half-circuit, comprising Q_2 and its emitter load and Q_3 , behaves in an identical, complementary, manner. Consider, first, the CMRR, ρ . Fig. 2, in which diode D_1 represents the base-emitter junction of Q_1 , shows an equivalent circuit for A when a common-mode input signal, v_{cm} , is applied. As far as the change, i , in the collector current of Q_3 is concerned, the circuit behaves like a 1:1 current mirror in which the effective rail supply is decreased in amount by v_{cm} , so, i comprises two components, viz, $-(v_{cm}/r_s)$ due to the current change in D_1 and $-(v_{cm}/r_o)$ due to the change in collector emitter voltage across the common-emitter collector output resistance, r_o , of Q_3 . Thus:

$$i = -v_{cm} \left(\frac{1}{r_s} + \frac{1}{r_o} \right) \quad (1)$$

This neglects the current change in the collector-base resistance, r_μ , of Q_3 , but since $r_\mu \gg r_o$ [21], this is negligible. The common-mode current, i_{cm} , flowing in load impedance Z , in Fig. 1, after being transmitted via the 1:1 current mirrors CM1, CM2 is double that given in equation 1, because of the complementary action of Q_2 , Q_4 . Hence,

$$g_{Tc} = \left| \frac{i_{cm}}{v_{cm}} \right| = 2 \left(\frac{1}{r_s} + \frac{1}{r_o} \right) \quad (2)$$

Fig. 3 shows the equivalent circuit for A when a differential-mode signal, v_{dm} , is applied. Again, i has two major components, one due to change in base-emitter voltage ($\equiv v_{dm}$), and the other due to change in collector-emitter voltage of Q_3

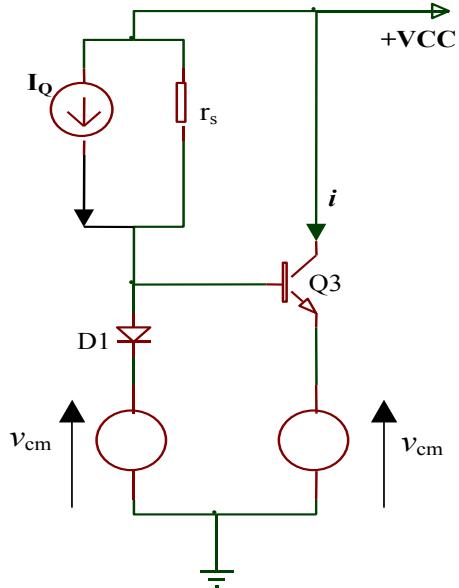


Figure 2. Representation of section A, for common mode signal v_{cm}

$$i \approx v_{dm} \left(g_m + \frac{1}{r_o} \right) \quad (3)$$

In this equation g_m (the transconductance of Q_3) = I_Q/V_T , with V_T ($=KT/q$) being the ‘thermal voltage’ ($\approx 25\text{mV}$ at room temperature). As with i_{cm} , i_{dm} is double that given by equation 3. Given that i_{dm} is the differential-mode current.

$$g_{Td} = \left| \frac{i_{dm}}{v_{dm}} \right| \approx 2 \left(g_m + \frac{1}{r_o} \right) \approx 2g_m \quad (4)$$

The approximation is valid as $g_m \gg 1/r_o$ where, $r_o = V_A/I_Q$, V_A ($\gg V_T$) being the Early voltage. From equations 2 and 4;

$$\rho = \frac{g_{Td}}{g_{Tc}} \approx \frac{g_m}{\left(\frac{1}{r_s} + \frac{1}{r_o} \right)} \quad (5)$$

For the special case $r_s = r_o$,

$$\rho \approx \frac{V_A}{2V_T} \quad (6)$$

This equation is applicable when I_Q is the output of a simple current mirror, as is meant to be the case for Fig. 1. Table 1 shows summaries of the variations of CMRR, A_{dm} and A_{cm} with changing values of r_{ce1} , r_{ce2} , r_{e1} , and r_{e2} .

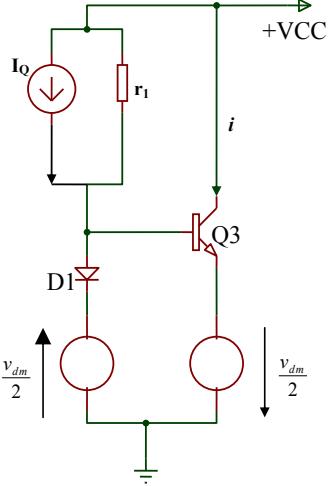


Figure 3. Representation of section A, for differential-mode signal v_{dm}

To test this theoretical result, the full transistor level CFOA shown in Fig. 4 was simulated using SPICE. This was undertaken using Analog Devices XFCB device parameters. The variations of CMRR, A_{dm} and A_{cm} with changing values of r_{ce1} , r_{ce2} , r_{e1} and r_{e2} are listed in Table 1. The obtained frequency responses of A_{dm} , A_{cm} and CMRR are shown in Fig. 5. The values of the Early voltages V_{AP} of the PNP devices Q_7 and Q_4 , and V_{AN} of the NPN device Q_5 and Q_3 were then doubled and the simulation repeated.

Increase parameter	CMRR	A_{dm}	A_{cm}
r_{ce1} , and r_{ce2}	Increases	No change	Decreases
r_{e1} , and r_{e2}	Decreases	Decreases	No change

Table 1

These results are shown in Fig. 6. The results presented in Fig. 7 correspond to Early voltages of the input transistors four times greater than the actual AD-XFCB parameters. Although changing the values of V_A in practice is virtually impossible, as a simulation exercise since $r_{ce} \approx V_A/I_{CQ}$, comparison of the results does confirm the anticipated significance of r_{ce} in determining the CMRR of the CFOA.

In moving from Fig. 5 through to Fig. 7, the values of A_{cm} decreased as expected by 6dB, the values of A_{dm} remained almost unchanged, and the CMRR increased by 6dB for each step in doubling of V_A . Consider, next, the offset voltage, V_{os} . This is the voltage at the emitter of Q_3 when Fig. 1 is connected as a unity-gain follower (V_o connected to the inverting input), and V_1 is set to zero. Ideally, $V_{os} = 0$, but in reality V_{os} is finite (a few mV) because of mismatch in the V_{BES} of Q_1 , Q_3 . Finally, consider the SR. This, like V_{os} , is measured in the unity-gain configuration with a resistance (typically between 750Ω and $2k\Omega$ for 15V rail supplies) [22] connected between V_o and the inverting input, when a positive step voltage is applied at the non-

inverting input. Transistors Q₁ and Q₄ (Fig. 1) tend to switch off and the SR is limited by the current, I_Q available at the base of Q₃.

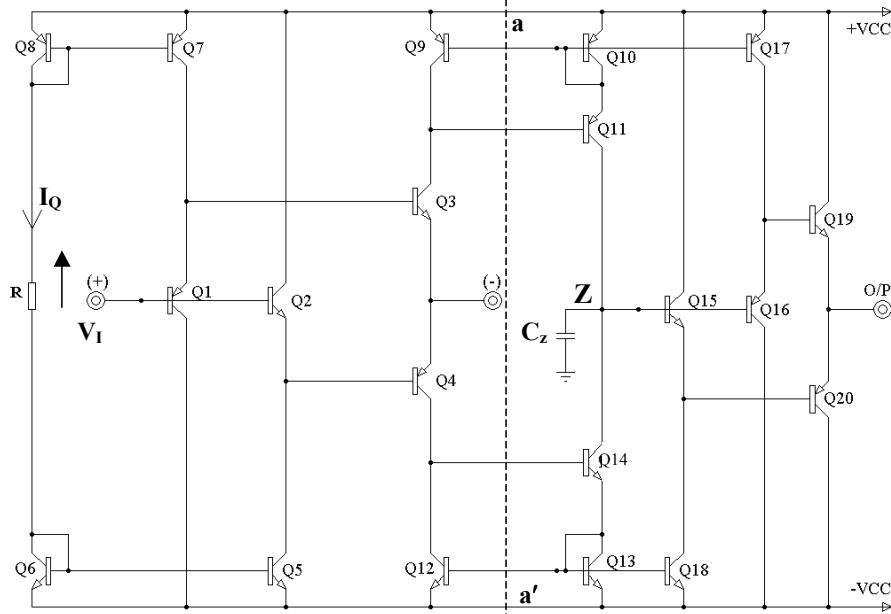


Figure 4. Circuit diagram of a basic CFOA

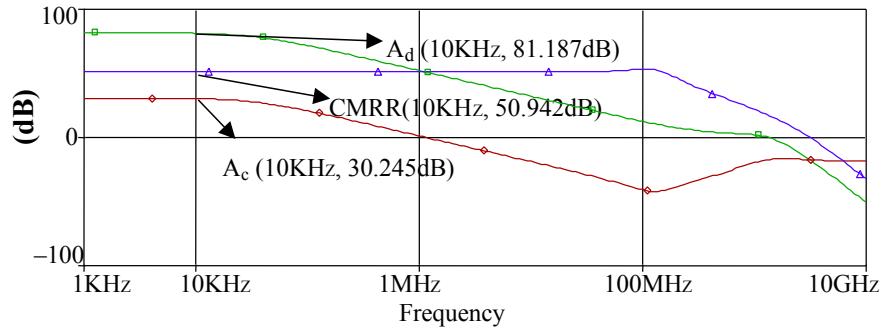


Figure 5. SPICE results for A_{dm}, A_{cm} and CMRR versus frequency for Fig. 4 using AD-XCFB process parameters.

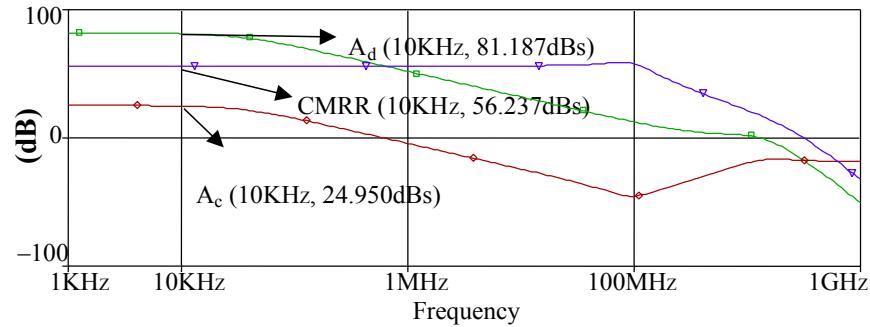


Figure 6. A_{dm}, A_{cm} and CMRR versus frequency, as in Fig. 5, except that V_A has been doubled for the input stage devices.

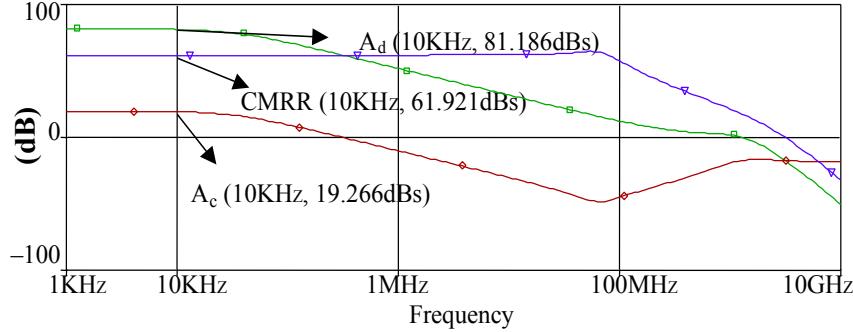


Figure 7. A_{dm} , A_{cm} and CMRR versus frequency, as in Fig. 6 except that V_A has been quadrupled for the input stage devices.

3. Quiescent power dissipation

The quiescent power dissipation for any amplifier circuit is a characteristic, which designers usually try to minimize. It is apparent from Fig.4 that there are eight conduction paths, from $+V_{CC}$ power supply to the $-V_{CC}$ power supply, each passing a quiescent current I_Q , defined by R , $+V_{CC}$, $-V_{CC}$.

The quiescent power dissipation P_Q is thus given by

$$P_Q = 2V_{CC} \times 8I_Q = 16V_{CC}I_Q \quad (7)$$

where,

$$I_Q = \left(\frac{2V_{CC} - 2|V_{BE}|}{R} \right) \quad (8)$$

Alternatively, we can write,

$$P_Q = 16V_{CC} \left(\frac{2V_{CC} - 2V_D}{R} \right) \quad (9)$$

4. CFOA with cascoding

Fig. 8 shows the proposed Cascode CFOA design. The box, A, encloses a cascode current mirror which is replicated three times, in NPN form, in the input stage. A similar PNP cascode current mirror also replicated three times in the design. The output stage of the CFOA is a class-AB complementary pair. The mirror-symmetry of the input stage about an imaginary horizontal line joining the '+', and '-' inputs guarantees a low offset voltage. The cascode transistors Q_{15} , Q_{16} increase the effective collector output resistances of Q_3 , Q_4 , respectively.

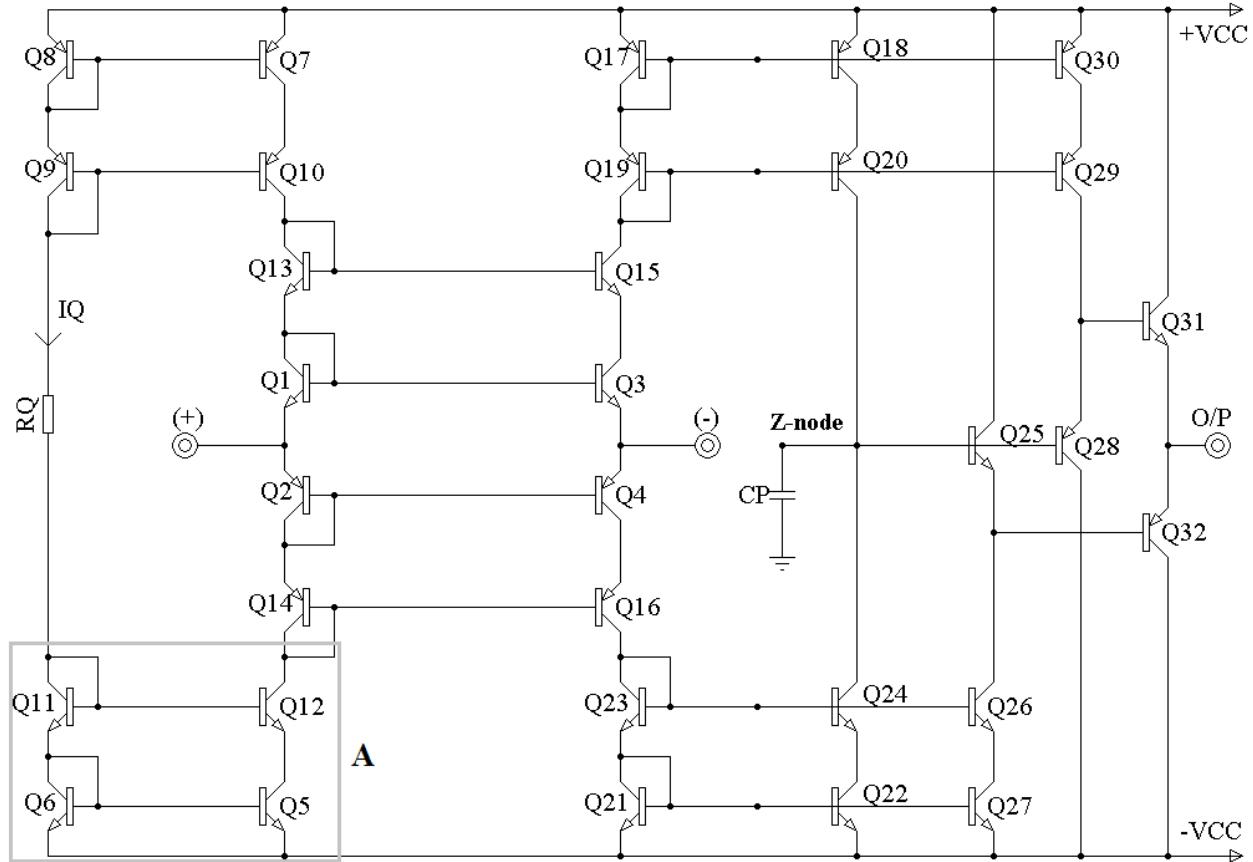


Figure 8. A CFOA with Cascoding

5. CFOA with forward and reverse-bootstrapping

A bipolar-transistor CFOA based on an alternative cascode scheme is shown in Fig.9, and should be compared with the Cascode CFOA shown in Fig.8. Fig. 9 shows an improved CFOA with a novel input stage that utilises both forward and reverse boot-strapping to achieve the desired effect of increasing significantly the CMRR.

In Fig. 9, the Cascode Current-mirrors [21], $(Q_7+Q_8+Q_{13}+Q_{14}+Q_{26}+Q_{35})$ and $(Q_5+Q_6+Q_{15}+Q_{16}+Q_{25}+Q_{36})$ are supplied with a common input current, I_Q , via the resistor R_Q . Since the action of the two buffered-mirrors is the same, only one is considered here, $(Q_7+Q_8+Q_{13}+Q_{14}+Q_{26}+Q_{35})$. Q_{17} , with its base bias provided by the diode-connected transistors Q_{19} , Q_{21} and Q_{23} , increases the output resistance of the Q_{14} cascode current source, and in the same way Q_{18} cascodes Q_{16} and increases the output resistance of Q_{16} . The input transistors Q_1 and Q_2 are cascoded by Q_9 and Q_{11} respectively.

This novel input circuit topology gives higher CMRR, and lower DC offset voltage because the use of both casoding and boot-strapping results in a significant decrease in the common-mode currents within the input stage.

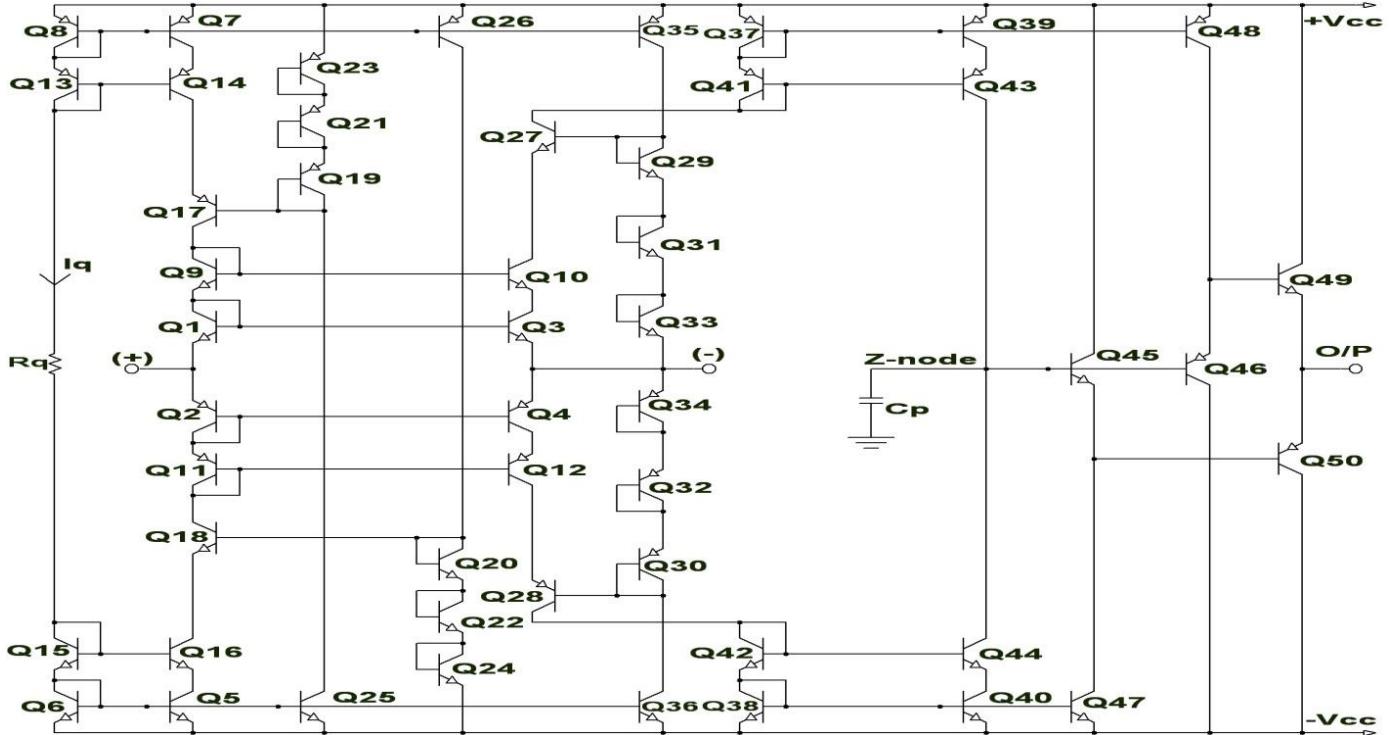


Figure 9. Circuit diagram of a CFOA using Forward and Reverse-Bootstrapping

6. Simulation results

OrCAD PSpice was used to verify the operation and performance of the circuits. The technology used in the simulation was the complementary bipolar XFCB process of Analog Devices, Santa Clara, California (**see Acknowledgements**).

The power supply voltages were set to $\pm 4.5V$. For comparative assessment three CFOAs were simulated, namely, (i) a conventional CFOA [23] (ii) the Cascode CFOA shown in Fig.8, and (iii) the Forward and Reverse Bootstrapping CFOA shown in Fig.9. All three were simulated with the same technology parameters, and were set to operate at a bias current, I_Q , equal to 0.50mA . A list of the simulated characteristics of both improved CFOAs, and conventional CFOA is given Table .2. The CMRR in both the Cascode CFOA, and the Forward and Reverse Bootstrapping CFOA have been increased, to about 80.1dB , and 90.5dB respectively, whilst in the conventional CFOA it remains at about 50.4dB . Fig .10 gives the PSpice simulation of the CMRR vs. frequency characteristic for the three CFOAs. A substantial improvement in the CMRR has thus been achieved.

Fig. 11 shows that the overall AC gain accuracy for the Cascode CFOA is given as $800\mu\text{V}$, compared to 5.9mV for the conventional CFOA and 6.2mV for the Forward and Reverse-Bootstrapping CFOA. For the Forward and Reverse Bootstrapping CFOA the bandwidth was 69MHz , and for the Cascode CFOA and the conventional CFOA was 65.6MHz , and 52.3MHz respectively as shown in Fig 12. The transient results for the three CFOAs, driving a $10\text{K}\Omega$ load resistance, are shown in Fig 13, and Table 2. The non-inverting impedances of the three CFOAs were determined, and the results are in line with the expected values for a differential signal, Fig

14, and Table 2. Fig 15 shows the inverting input impedance response versus the frequency for the three CFOAs. Table 2 shows that the DC offset voltage was reduced dramatically in both the Cascode CFOA, and the Forward and Reverse-Bootstrapping CFOA to $\pm 166\text{mV}$, and $\pm 5.1\text{mV}$, respectively; compared with the much larger $\pm 12.5\text{mV}$ of the conventional CFOA.

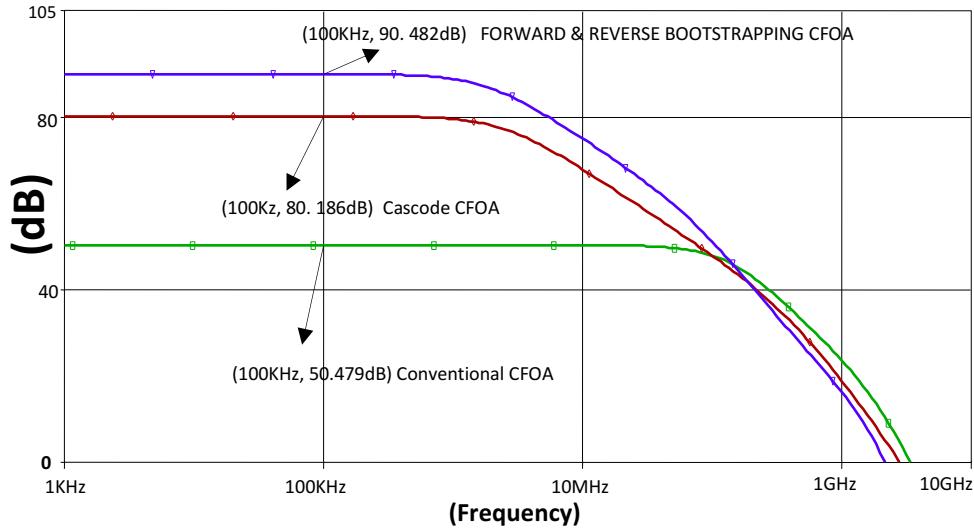


Figure 10. CMRR~Frequency, comparisons

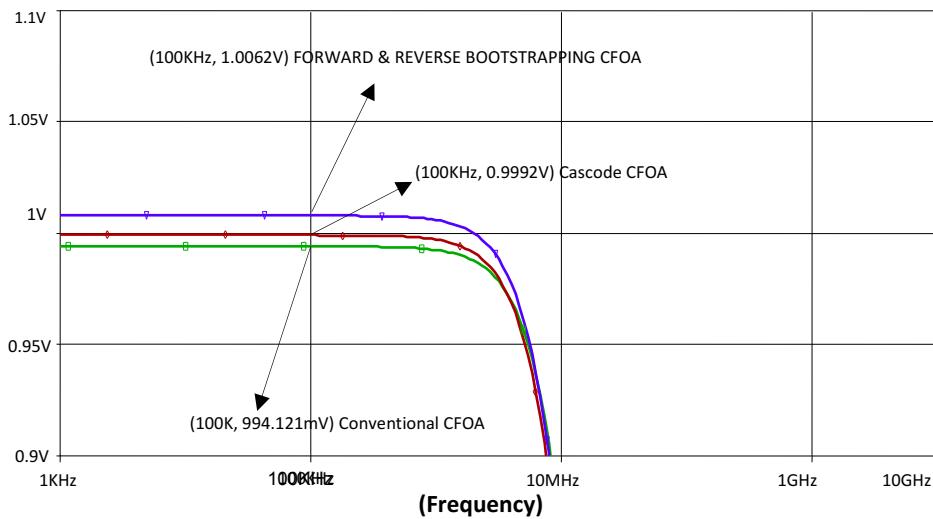


Figure 11. AC gain accuracy ~ Frequency, comparisons

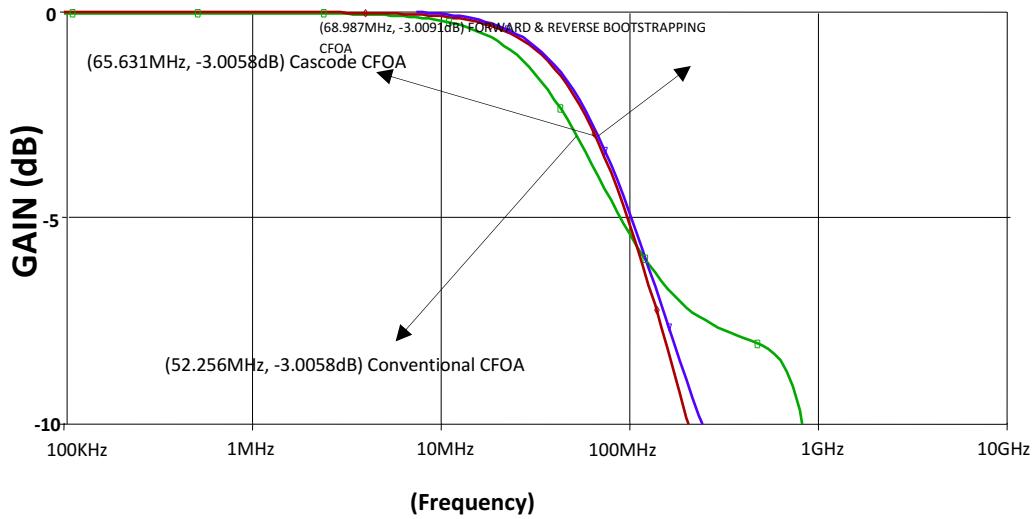


Figure 12. Frequency responses for unity closed-loop gain comparisons

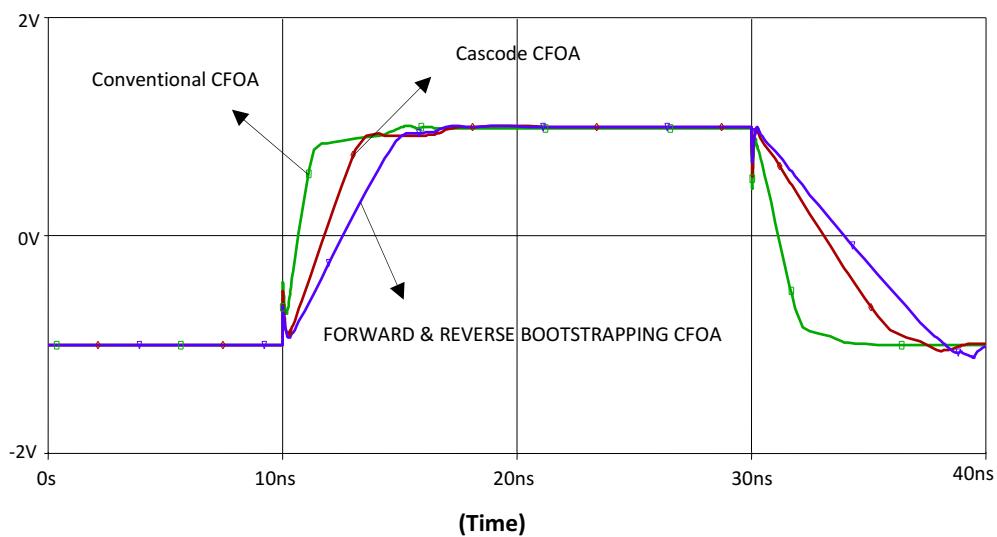


Figure 13. Slew Rate comparisons

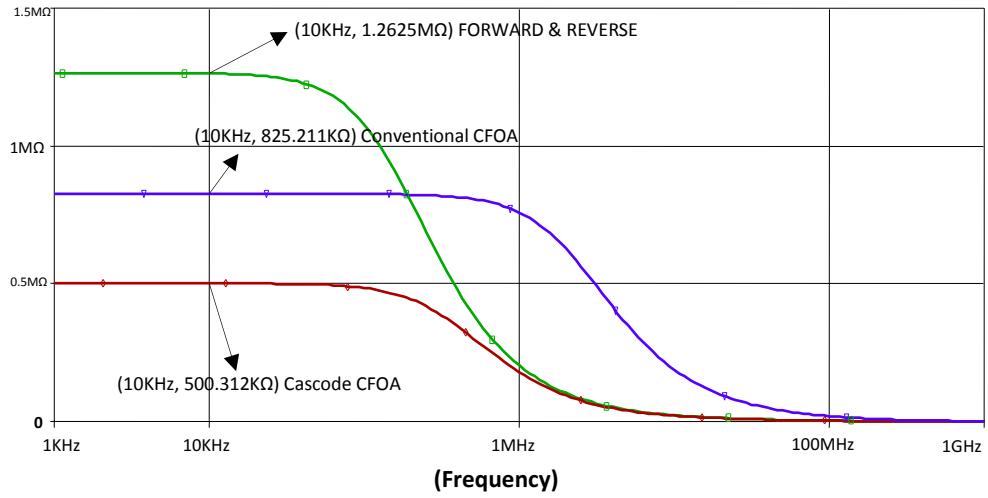


Figure 14. Input impedance~frequency, comparisons for the CFOAs, each configured as a non-inverting unity gain amplifier

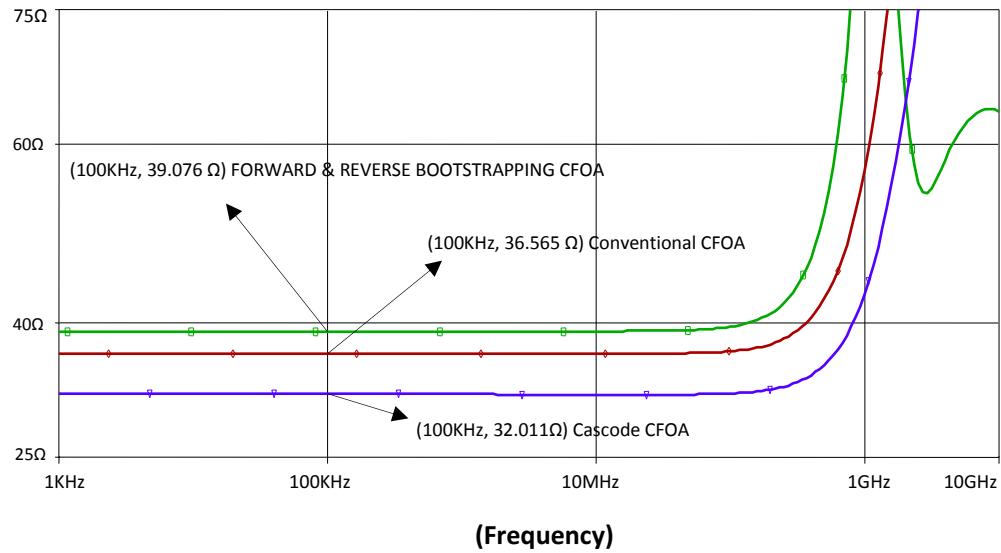


Figure 15. Input Resistances (inverting) ~Frequency comparisons

	CONVENTIONAL CFOA (Fig .4)	CASCODE CFOA (Fig .8)	FORWARD & REVERSE BOOTSTRAPPING CFOA (Fig 9)
CMRR	50.5dB	80.2dB	90.5dB
Bandwidth	52.3MHz	65.6MHz	69MHz
Inverting input resistance (at 0V d.c. input)	36.6Ω	32Ω	39.1Ω
Non-inverting buffer input resistance (at 0V d.c. input)	825.2K Ω	500.3KΩ	1.3MΩ
AC gain error (Unity gain, Vin = 1V pp)	5.9mV	800μV	6.2mV
Input offset voltage (at 0V d.c. input)	±12.3mV	±166μV	±5.1mV
Slew rates	SR+ =1351V/μs SR- =965.6V/μs	SR+ =650.1V/μs SR- =360.3V/μs	SR+ =460.4V/μs SR- =290.2V/μs

Table 2

7. Conclusions and future work

Analysis of the conventional CFOA has provided a deeper understanding of the internal operation of the circuit, and this work revealed that the shortcomings in CMRR, input referred offset voltage and gain accuracy of the CFOA are in the design of the input stage. This part of the amplifier is responsible for the poor CMRR performance compared with that of a voltage-mode op-amp. Using the initial analysis of the conventional CFOA as a benchmark, two new CFOAs with improved performances have been designed and developed. Both of these new CFOAs have a high CMRR with an acceptably high SR. The benefits of greater accuracy, reduced DC offset voltage, together with an architecture that has a high CMRR, and acceptable bandwidth (of about 69MHz) make these CFOAs a welcome and useful addition to the analogue designer's tool kit.

However, the price paid for these improvements is a reduced output voltage swing for given rail voltages, because of vertical transistor stacking. Clearly, the new CFOAs do use more transistors but the performance advantages particularly in terms of CMRR improvement justify the increased complexity when this parameter is of paramount interest. The primary disadvantage are the moderately high power supply voltages required. The authors are currently modifying the design to reduce the power supply voltage requirements by replacing the conventional cascode circuits with folded-cascodes.

Bipolar technology CFOA offer high-speed, high-bandwidth, high-slewing amplifier with low-frequency noise performance at low quiescent currents. Moreover, bipolar transistors inherently offer better matching, resulting in lower offset voltages than CMOS for any given architecture. However, if the op amp interfaces with a high-impedance sensor, such as a thermocouple with some passive filtering, then keeping bias currents to a minimum will be important and CMOS is a better technology to choose.

This work is on-going, and the authors anticipate being able to report new CFOAs using CMOS technologies and BiCMOS hybrid technology, the latter taking the best from both worlds and providing superior performance at a price point that is becoming more competitive.

Acknowledgements

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