

A 20-MHz 0.323-mW 23.9-dBm-IIP3 4th-order Current-Reuse Lowpass Filter

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Abstract—A source follower lowpass filter which has a capability of bulk-attenuation cancellation in higher order is presented. Under strong inversion bias arrangement for high frequency application, this fourth-order-filter is simulated in a 0.18 μm standard CMOS process and exhibits a 20 MHz bandwidth with total power consumption of 0.323 mW from 1.8 V supply. Third order intermodulation distortion verification with 1.9 and 2.1 MHz signal archives 23.9 dBm IIP3 with 75.5 dB dynamic range. By using figure-of-merit as a benchmark indicator, the proposed filter is one of the top in its class with the lowest power consumption.

Index Terms—Source Follower Filter, Low Power

I. INTRODUCTION

One of an important block which functions as a signal conditioning and extensively utilizes in telecommunication and sensor system is a filter. The requirement for filter design emphasizes low power consumption, high dynamic range (wide linear range with low noise) and small chip area. Source follower (SF) is one of an analog filter scheme which provides the aforementioned specifications from its compact structure, especially SF with high frequency (HF) application [1]–[5]

In this paper, a source follower with bulk neutralization (SFB) filter with body effect cancellation [6] which targeted for biomedical application is redesigned for high frequency signal filtering. The structure of this paper is organized as follows. In section II, the transfer function and other relevant design parameter of the filter is described. The pseudo-differential scheme of the proposed filter which benefits from wider linear range and common-mode feedback circuit exclusion is presented in section III. The simulation results in section IV reveal a high linearity (IIP3 = 23.9 dBm) and low power (0.323 mW).

II. PROPOSED HF BIQUAD FILTER

The second-order current-reuse filter from [6] which targets for high frequency application is shown in Fig. 1. For higher order filter implementation, the N-input biquad (Fig. 1(a)) and the P-input biquad (Fig. 1(b)) can be cascaded.

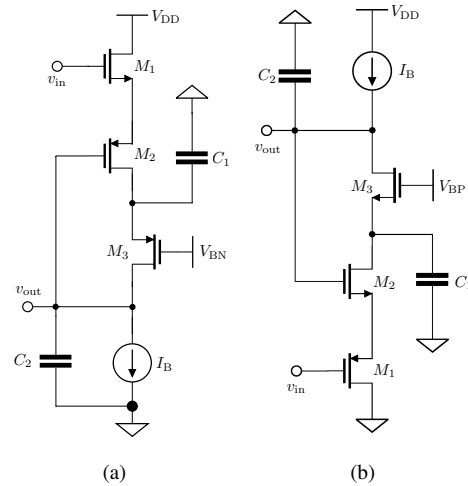


Fig. 1. (a) N-input and (b) P-input biquad filter.

The transfer function of these biquads is derived as in eq. (1) where g_{mi} is the gate-only-transconductance and g_{mti} is the gate-and-bulk-transconductance of each transistor. Under standard n-well CMOS process, $g_{mt1} = g_{m1} + g_{mb1}$ and $g_{mt2} = g_{m2}$ for the N-input biquad while $g_{mt1} = g_{m1}$ and $g_{mt2} = g_{m2} + g_{mb2}$ for P-input biquad where g_{mbi} is the bulk transconductance.

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m1}g_{m2}}{g_{m2}g_{m1}} \cdot \frac{\frac{g_{m1}g_{m2}g_{m3}}{(g_{m1}+g_{m2})C_1C_2}}{\left(s^2 + s\left(\frac{g_{m3}}{C_1}\right) + \frac{g_{m1}g_{m2}g_{m3}}{(g_{m1}+g_{m2})C_1C_2}\right)} \quad (1)$$

TABLE I
RELEVANT FILTER DESIGN PARAMETERS.

	N-input	P-input
K	$\frac{g_{m1}}{g_{m1}}$	$\frac{g_{m2}}{g_{m2}}$
ω_o	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2(g_{m1}+g_{m2})}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2(g_{m1}+g_{m2})}}$
Q	$\sqrt{\frac{C_1g_{m1}g_{m2}}{C_2(g_{m1}+g_{m2})g_{m3}}}$	$\sqrt{\frac{C_1g_{m1}g_{m2}}{C_2(g_{m1}+g_{m2})g_{m3}}}$

The filter parameters for examples: pass-band gain (K), natural frequency (ω_o) and quality factor (Q) can be extracted from eq.(1). Summary of these parameters is shown in Table I which reveals that the N-input biquad has gain attenuation due to bulk effect of the NMOS. Unexpectedly, the pass-band gain of the P-input biquad cancel out the gain loss from the N-input when these two biquads are cascaded.

III. FOURTH-ORDER DIFFERENTIAL FILTER IMPLEMENTATION

A fourth-order filter with pseudo-differential configuration is realized as shown in Fig. 2. The advantages of this arrangement is not only input linear range extension (even harmonics cancellation) but also capacitor area reduction by half (targeting at the same bandwidth as the single-ended scheme). The price to pay for this enhancement is higher power consumption and noise.

To minimize the input referred noise (IRN), the PMOS input biquad filter which provides higher pass-band gain is chosen as the first stage. With design target for HF application, this pseudo differential filter is biased with $I_B = 30 \mu A$ to obtain 20 MHz bandwidth. The transconductance of each transistor and the quality factor of each stage are shown in Table II.

TABLE II
4th-ORDER DESIGN PARAMETERS.

Parameter	N-input	P-input
g_{m1} (mA/V)	0.493	0.504
g_{mb1} (mA/V)	0.097	0
g_{m2} (mA/V)	0.339	0.61
g_{mb2} (mA/V)	0	0.012
g_{m3} (mA/V)	0.368	0
g_{mb3} (mA/V)	0.56	0.01
Q	0.618	1.62

IV. SIMULATION RESULTS

This proposed fourth-order lowpass filter is simulated in a 0.18 μm standard CMOS process. The input DC common mode of the P-input stage is set as 300 mV. The total power consumption from the core filter and

the bias current is 323 μW under 1.8 V supply voltage. The frequency response of this proposed filter is shown in Fig. 3 which indicates 20 MHz bandwidth with 0-dB pass-band gain.

To determine the dynamic range (DR) of this proposed filter, the input linear range and input-referred noise (IRN) are calculated from Fig. 4 and 5, respectively. With 400 mV_P - 2 MHz sinusoidal signal, the output harmonic of this filter indicates a -40.89 dBc third harmonic distortion (HD3) as shown in Fig. 4. The output noise power spectral density (PSD) of this proposed filter as shown in Fig. 5 reveals 68.4 μV_{rms} IRN (integrating from 100 kHz to 20 MHz). As a result, the DR with 1% THD of this filter is 75.5 dB.

The input third-order intercept point (IIP3) is demonstrated by applying a two-tone sinusoidal signal (1.9 and 2.1 MHz) with -6.478 dBm (0.15 V_P) amplitude to this proposed filter. A -62.66 dBc third-harmonic intermodulation (IM3) is figured out as shown in Fig. 6. The relationship between IIP3 and IM3 [7] is

$$IIP3 = P_{in,dB} - (0.5 \times IM3_{dB}), \quad (2)$$

where $P_{in,dB}$ is the input signal power. Subsequently, IIP3 of 24.85 dBm is calculated from eq. (2). To verify this calculation, IIP3 test under quasi-periodic steady state (QPSS) analysis is simulated with -20 dBm input power which concedes 23.95 dBm IIP3 as shown in Fig. 7.

The performance comparison with other state-of-the-art filters is summarized in Table III. This proposed passband gain compensation filter has the lowest power per pole among the recent works while a comparable high IIP3 as in [5] is achieved. To characterize the power, noise and linearity performance of a filter, a figure of merit is determined in two different aspects.

$$FoM = \frac{P_{DUT}/N}{f_{BW} \cdot SFDR \cdot N^{4/3}} \quad (3)$$

$$FoM_{DR} = DR + 10 \cdot \log_{10} \left(\frac{f_{BW}}{P_{DUT}/N} \right) \quad (4)$$

The first figure of merit (FoM) in eq. (3) [8] is emphasized on a spurious free dynamic range where P_{DUT} is the power consumption of the filter core circuit, N is the filter order, f_{BW} is the filter -3dB bandwidth and $SFDR = (IIP3/P_N)^{2/3}$ (P_N is the input-referred noise power). The other figure of merit (FoM_{DR}) [1] which highlighted on the DR at 1 % THD is depicted in eq. (4). The FoM and FoM_{DR} of this proposed filter are determined as shown in Table III. On benchmarking with other recent filter design, this filter has the best FoM and FoM_{DR} (as shown in Fig. 8 and 9, respectively) while consuming power as half of [5].

V. CONCLUSION

A source follower filter with 0-dB pass-band gain designed for HF application is verified in a standard CMOS process. Under pseudo differential configuration, this fourth-order LPF has a 20 MHz bandwidth under

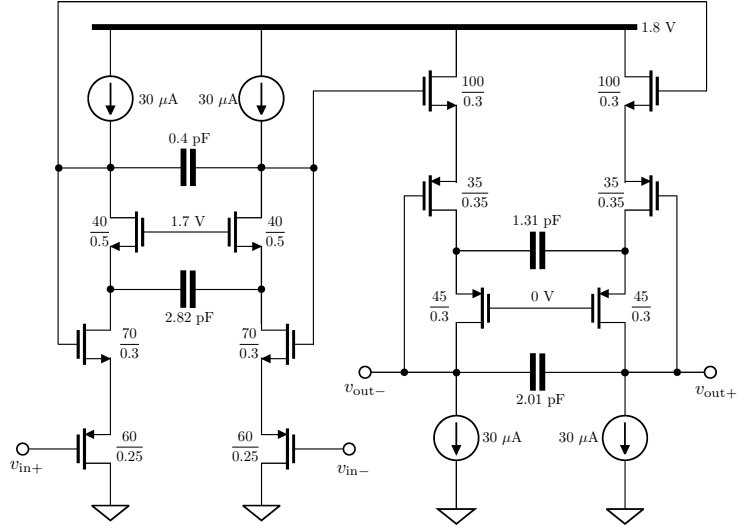


Fig. 2. The proposed 4th-order pseudo-differential filter with 30 μA bias current for HF application.

TABLE III
SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART FILTERS

	This work	JSSC'20 [5]	JSSC'15 [2]	ESSCIRC'18 [3]	TCAS'18 [4]
Technology	0.18 μm	0.18 μm	0.18 μm	28 nm	0.18 μm
Architecture	SFB	SF	SSF	FSF	SC
V_{DD} (V)	1.8	1.3	1.8	1	1.8
Filter order	4	5	4	4	4
Bandwidth (MHz)	20	20	33	100	0.49-13.3
Power (mW)	0.323	0.65	1.38	0.97	4.3
Power per pole	0.08075	0.13	0.345	0.2425	1.075
DC Gain (dB)	0	0	-5	-2.6	17.6
$V_{inTHD@-40dBc}$ (V _p)	0.4	0.675	0.225	0.16	0.1
IIP3 (dBm)	23.98	24.5	18	12.5	11.1
IRN (nV _{rms} /√Hz)	15.1	15.3	7.8	9.8	6.5
DR @ THD -40 dBc (dB)	75.5	76.9	70	61	74.9
FoM ($\times 10^{-18} \cdot \text{J}$)	0.32	0.36	1.2	1.9	16.9
FoM _{DR} (dB)	189.4	188.7	179.8	177.5	170.4

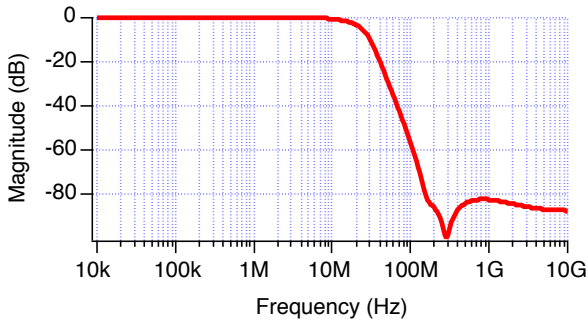


Fig. 3. Frequency response of the proposed LPF when $I_B = 30 \mu\text{A}$.

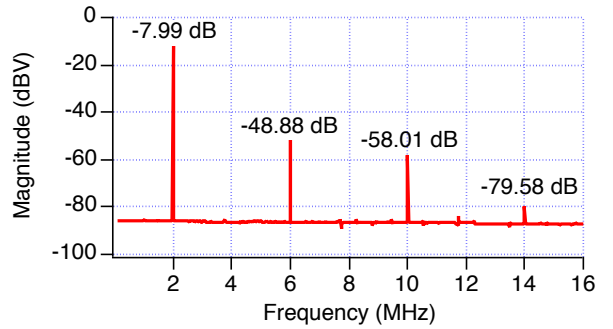


Fig. 4. The harmonic component of this proposed filter when the 2 MHz - 400 mV_p sinusoidal input is applied.

1.8 V supply and total current consumption of the filter core at 180 μA . The dynamic range of this filter

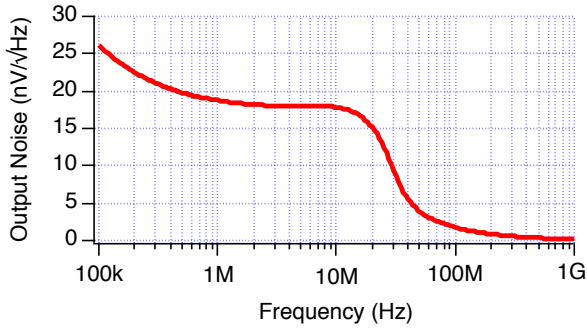


Fig. 5. The output noise characteristic of this proposed filter

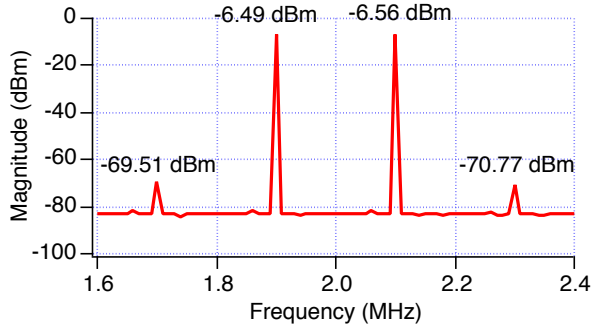


Fig. 6. Inter Modulation Distortion (IMD) verification of this proposed filter when two tone input signal of 1.9 and 2.1 MHz is applied.

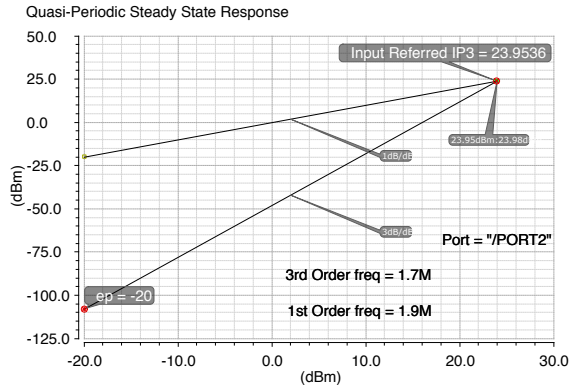


Fig. 7. A quasi-periodic steady state (QPSS) simulation of this proposed filter under -20 dBm input power.

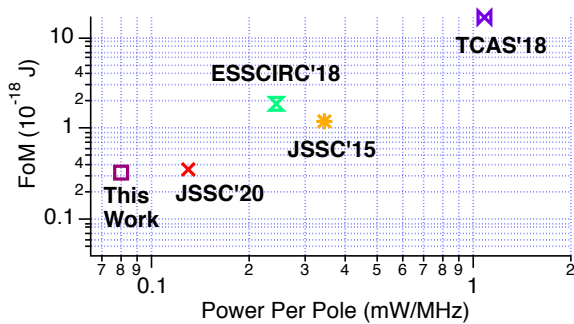


Fig. 8. FoM plot vs. the power per pole of the filter.

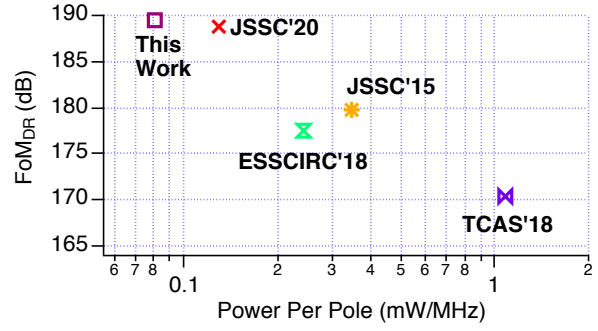


Fig. 9. FoM_{DR} plot vs. the power per pole of the filter

is examined with 400 mV_P-2 MHz sinusoidal signal which exhibits -40 dBc THD and 68.4 μ V_{rms} IRN. Two-tone test with input signal of 1.9 and 2.1 MHz signal indicates 23.98 dBm IIP3.

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