LOW POWER AND HIGH SIGNAL TO NOISE RATIO BIO-MEDICAL AFE DESIGN TECHNIQUES

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Low Power and high Signal to Noise Ratio Bio-medical AFE Design Techniques

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Abstract

The research work described in this thesis was focused on finding novel techniques to implement a low-power and noise Bio-Medical Analog Front End (BMEF) circuit technique to enable high-quality Electrocardiography (ECG) sensing. Usually, an ECG signal and several bio-medical signals are sensed from the human body through a pair of electrodes. The electrical characteristics of the very small amplitude (1u-10mV) signals are corrupted by random noise and have a significant dc offset. 50/60Hz power supply coupling noise is one of the biggest cross-talk signals compared to the thermally generated random noise. These signals are even AFE composed of an Instrumentation Amplifier (IA), which will have a better Common Mode rejection ratio (CMRR). The main function of the AFE is to convert–the weak electrical Signal into large signals whose amplitude is large enough for an Analog Digital Converter (ADC) to detect without having any errors. A Variable Gain Amplifier (VGA) is sometimes required to adjust signal amplitude to maintain the dynamic range of the ADC. Also, the Bio-medical transceiver needs an accurate and temperature-independent reference voltage and current for the ADC, commonly known as Bandgap Reference Circuit (BGR). These circuits need to consume as low power as possible to enable these circuits to be powered from the battery.

The work started with analysing the existing circuit techniques for the circuits mentioned above and finding the key important improvements required to reach the target specifications. Previously proposed IA is generated based on voltage mode signal processing. To improve the CMRR (119dB), we proposed a current mode-based IA with an embedded DC cancellation technique. State-of-the-art VGA circuits were built based on the degeneration principle of the differential pair, which will enable the variable gain purpose, but none of these techniques discussed linearity improvement, which is very important in modern CMOS technologies. This work enhances the total Harmonic distortion (THD) by 21dB in the worst case by exploiting the feedback techniques around the differential pair. Also, this work proposes a low power curvature compensated bandgap with 2ppm/^{0}C temperature sensitivity while consuming 12.5uW power from a 1.2V dc power supply. All circuits were built in 45nm TSMC-CMOS technology and simulated with all the performance metrics with Cadence (spectre) simulator. The circuit layout was carried out to study post-layout parasitic effect sensitivity.

List of principal terms and abbreviations

Transceiver	It is a system that includes a transmitter, receiver and antenna.
Active electrodes	Electric leads that are equipped with an amplifier and are attached to patients to simulate or record any potential
Amplifiers	An electrical device is used to increase the amplitude of an electrical signal.
Artefacts	Minor blurring to significant distortion of the output signals may affect the interpretation of the medical interpretation (diagnosis).
Cadence	It is a System Design Enablement provider delivering tools and software to help in building circuits and simulating them.
Spectrum	Frequency domain representation of the signal
Common-Mode	The average value of a differential mode signals
ECG (Electrocardiography)	A test is used to detect and monitor the heart's electrical activity.
Filtering	Removing specific frequency-band from a signal.
Instrumentation amplifier (IA)	It is an amplifier that has been developed with input buffer amplifiers that are specifically used to reject common signals at the input, and hence it is suitable for use in measurement and test equipment.
Variable gain Amplifier (VGA)	Amplifier with a programmable gain option, which is mainly to amplify/attenuate the signal.

PVT CORNERS	In a chip, several transistors behave differently. Hence foundries will specify the Process corners.
DIGITAL SIGNAL PROCESSING (DSP)	It is a digital system which can process the signal with high linearity and no PVT variation.
Noise	The electric noise in the Signal is being read from a patient. This kind of noise will blur the true Signal and make it inaccurate.
Opamp	Operational amplifier. It is a high-gain electronic voltage amplifier with a differential input and a single-ended output.
FIELD PROGRAMMABLE GATE ARRAY (FPGA)	A digital circuit with all possible digital components like all logic gates and flip-flops, hence any functionality can be implemented in the field.
ANALOG TO DIGITAL CONVERTER (ADC)	A device that will convert fast-varying analog signals into digital bits.
BANDGAP REFERENCE	It is a circuit whose output voltage is independent of temperature.
DYNAMIC RANGE	Maximum input signal range of an amplifier.
INL (Integral non-linearity)	The error between the ADC actual output and ideal output
DNL (Differential non-linearity)	The error between the ADC/DAC step size and the actual step size.
LSB	Least Significant Bit (of an ADC/DAC)
Filter Order	The number of independent energy storage elements in a circuit or the power of the denominator transfer function.
CMRR	Common mode rejection ratio of the differential pair while processing the differential signal.

PSRR	Power supply rejection ratio of a reference voltage/current circuit.
Pole	The frequency at which an amplifier's transfer function gains would become infinite.
Zero	The frequency at which an amplifier's transfer function gains would become zero.
Phase Margin	Closed transfer function's phase at the frequency where the gain of the amplifier becomes unity (unity gain frequency).
Gain Margin	Closed-loop transfer function's gain at which the phase of the amplifier becomes -180^0
Overshoot	The difference between the maximum value of the step response and the actual value.
Steady-state error	The step response output error from the actual value reaches the final state without ringing.
UGB	The frequency corresponds to the unity gain of a closed-loop amplifier.
Type of the system	Several integrators in the closed-loop amplifier or the number of zeros at the origin.
SFDR	Spurious Free dynamic range of an ADC while digitizing the signal.
SNR	Signal-to-Noise Ratio (of ADC/DAC while ignoring any spurs in the spectrum).
FFE	Feed-Forward Equalizer to reduce the ADC gain non-linearity
THD	Total Harmonic Distortion of the amplifier when it is characterized in the frequency domain.
ENOB	The effective number of the bits of ADC

Class-AB	This is a kind of amplifier whose output current is unlimited by the quiescent current used in the output stage.
PPM	Parts per million
Flicker Noise	It is a random noise with -10dB/dec roll of frequency response.
Nyquist Plot	It is a polar plot drawn in the complex plane to assess the stability
Sub-Threshold Region	
EOS	Electrical Over Stress
Decimation Filter	Under-samples a signal and does averaging to minimize the high-frequency noise content.
PPM	Parts per million-mainly used to define the very small variation of a larger quantity

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Chapter 1: INTRODUCTION

1.1 Bio-medical Signal Monitoring

Most medical equipment using electrodes attached to patients requires an analog front end (AFE) with high-precision, low-power amplifiers (HPLPAs). Without a high level of precision, the captured signals could become distorted, leading to misinterpretation and even misdiagnosis. Another important consideration is power consumption. With a growing need for continuous monitoring and hence 'wearable technologies, it is very important to minimise power consumption to maximise battery life [1].

Figure 1.1 shows a typical biomedical system where an HPLPA is needed. This system consists of an instrumentation amplifier (IA), a variable gain amplifier (VGA) and an analog digital converter (ADC). The IA amplifies the small input signal without adding a significant amount of noise. The VGA amplifies the IA output such that the ADC will experience a constant amplitude signal. Hence VGA maximizes the dynamic range of ADC, so efficient use of ADC bits. The VGA output is fed to an ADC [2] so that the output of the system is in a digital format. This is necessary to convert the processed biomedical signals (always in the analog domain and can be any value between a maximum and minimum) to the digital domain (they can be just one of two levels – on or off). Hence, this allows processing and storage by a digital device, such as a computer [3].

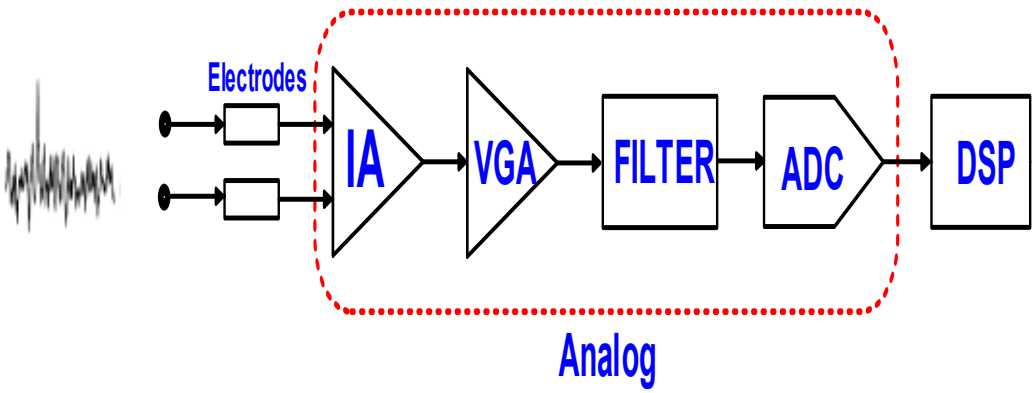

Figure 1.1 Block diagram of a Biomedical monitor system

Typically, biomedical signal monitors are mainly large and powered through the mains; hence power consumption is not an issue. The high power and large available space provide opportunities for the simultaneous monitoring of other biomedical signals (e.g., temperature and respiration) and allow for alarms to be set when the parameters fall outside of a certain value [4]. The population of many countries where there is good healthcare is ageing. That is, a growing proportion of the population is elderly [5]. This brings challenges: particularly in the field of healthcare. More and more people need their health condition monitored, sometimes on a long-term basis, and increasingly the typical hospital-type appliance is becoming less viable due to increased strain and demand for health services [4]. As mentioned above, there is a growing need for portable devices to allow for continuous (and often remote) monitoring, and this is where the HPLPA proposed here could be a great enabler. Of course, the cost is also an issue. The Health Services of even the most prosperous of countries could not afford to provide a 'typical' biomedical monitor to everyone who needs it [6]. The cost would be highly prohibitive. This is even more of a consideration in less economically developed countries. The research proposed here could allow for devices to be made that are significantly cheaper than existing hospital-type appliances, in addition to being equally important, as it can enable the operation of these new devices by 'non-experts', with the collected data stored in memory for later interpretation by a medical practitioner [7]. It could also enable continuous wireless/internet data transmission to medical practitioners. This would be of huge benefit to both rich and developing countries. The benefits this brings to the medical field have high potential, as any anomalies in 'normal' biological signals could be picked up immediately.

Harrison et al. (2007) Present a typical HPLPA with low power consumption and low noise performance [8]. Unfortunately, this implementation has a poor common-mode rejection ratio (CMRR) of 90dB, mainly limited by the output voltage swing of the IA [9].

Nagulapalli et al. (2017) [10] propose a current mode IA demonstrating a CMRR of 115dB. The main contribution of this paper is to convert the input voltage signal into a current signal and use a trans-impedance amplifier to convert this back into a differential voltage. In this way, the CMRR is insensitive to variations in component parameters [10]. However, this technique has unacceptable noise performance and poor sensitivity because of the use of multiple stages. The paper [10] also proposes a chopper-based input referred offset correction technique. In this implementation, a low-frequency clock has been used to swap the differential pair devices in the IA so that the offset voltage will be converted to a high frequency, which can then be filtered by a low pass passive filter [10] requiring a resistor of comparatively large physical size and a capacitor. Hence, this leads to the disadvantage that the filter occupies almost 60% of the design area. The input impedance of the IA is 500Mohm, such a high value is due to the MOS high input impedance nature.

1.2 Electrical characteristics of the Biomedical Signals

Most bio-medical instruments sense signals through electrodes. Biological signals can be classified into mainly three types: Action potentials (AP), local field potentials (LFP), and Electrocorticography (ECG) signals. Out of these three, the first two can be obtained from a single-unit recording. ECG signals can be measured using electrodes at the cortex surface, which is relatively difficult to record. Typical AP signals have a bandwidth of 100Hz-7KHz with amplitude ranges from 10uV-500uV, while LPF occupies the frequency spectrum up to 100Hz with an amplitude as max as 5mV. ECG signals bandwidth lies between 0.5Hz-200Hz with amplitude up to 100uV. Electrically, ECG signals are difficult to process because of their tiny amplitude and limited bandwidth [6]. Processing them involves a lot of circuit techniques and computations. Table 1.1 shows the electrical characteristics in a straightforward way for different biomedical signals [8].

Table 1.1 Electrical characteristics for different biomedical signals

Parameters	Bandwidth	Amplitude	Spatial Resolution	Invasiveness
Single-Unit	0.1-7KHz	<500uV	0.2mm	invasive
LFP (Local Field Potential)	<200Hz	<5mV	1mm	Moderately invasive
ECG (Electrocorticography)	0.5-200Hz	<100uV	0.5cm	Moderately invasive
EEG (Electroencephalography)	<100Hz	10-20uV	3cm	Non- invasive

Figure 1.2 shows the bio-medical signal processing concept in a nutshell [12]. Biological signals within the human body will be extracted with the electrodes. Due to the tissue and skin interaction, electrodes will sense the weak signals with a huge DC offset voltage. Also, the electrode output will have been distorted by the common-mode noise through the power supply coupling (50/60Hz). The output of the electrodes will be fed to the AFE to process the signal. This means amplifying the signals by removing the offset

and noise. Due to the weak nature of the electrical signal and large common-mode noise, the AFE needs to amplify the signal by a significant amount without having any coupling from the noise and 60Hz noise [4]. Hence the AFE should have high CMRR under high mismatch electrical component conditions, simulated through a Monte Carlo method. The output of the AFE will be fed to a low-power, high-resolution ADC (usually 10-15bit) to convert the analog signal into the digital domain; hence a Field Programmable Gate Array (FPGA) or Digital Signal processor (DSP) can do further processing [4].

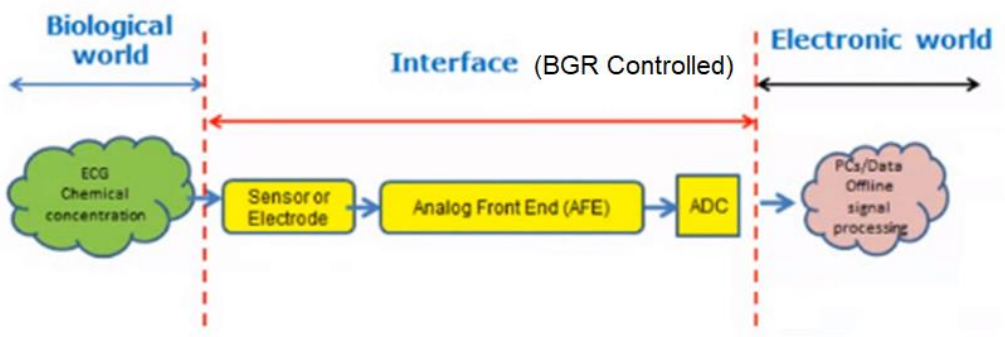

Figure 1.2 Bio-medical sensing concept

A Bandgap Reference (BGR) would be a key analog building block in biomedical systems that would maintain high accuracy and sensitivity [3]. This block can be added as a control system to a typical bio-medical system, as shown in Figure 1.2 and explained in chapter 4. The transistors in the AFE and ADC need accurate bias current and voltage to keep them in the saturation region. BGR produces a temperature-independent voltage by summing the scaled versions of Proportional to Absolute Temperature (PTAT) and Complimentary to Absolute Temperature (CTAT) voltages. Another critical block in the AFE is the Variable Gain Amplifier (VGA), which acts as a linear amplifier whose gain can be programmed either as an analog control voltage or digital control bus (usually 8-bit). VGA will ensure the amplitude or the signal power at the ADC input is constant to maximise the Signal to Noise ratio (SNR). Hence VGA improves the sensitivity of the

circuit. Every analog circuit is sensitive to transistor properties like transconductance (g_m) and output conductance (g_{ds}). Unfortunately, g_m, and g_{ds} are very sensitive to the process, voltage, and temperature (PVT) corners [3]. Hence analog circuits must be designed so that they meet all the required specifications for independent PVT corners. This requires a careful bias selection of transistors such that they have enough headroom for every corner of the PVT variation. The VGA output signal will be fed to the ADC, which will convert the analog input signal into a 12-bit digital signal (12-bit ADC will have 73.6dB SNR). This 12-bit digital bus will drive a Digital Signal Processor to perform further digital computation [7].

1.3 Hypothesis and Research Questions

This research tests the following hypothesis:

The bio-logical signal sensed through the electrodes can be detected and digitised using electrical circuits without significant distortion while consuming minimal power from the battery.

Answering the following research questions will help in testing the hypothesis:

1. What are the main problems with the existing bandgap circuits, and how can they be improved from the PowerPoint of view?
2. What is the lowest power limit of a bio-medical transceiver for a given SNR, and what are the difficulties in achieving the same in real-time implementation?
3. How to implement a high CMRR front-end Instrumentation Amplifier?
4. What are the limitations of the present VGA circuit architectures, especially from the PVT spread point of view?
5. How to implement the low-power ADC as a last stage of the AFE before the bio-medical signal handing over to the DSP?
6. How can you test the system?
7. How can the results be evaluated?

n Aim and Objectives

The research aims to develop a novel low-noise bio-medical front-end circuit design for ECG signal sensing.

The objectives of the research are:

- Investigate and analyse the existing literature, mainly on Instrumentation amplifiers (IA), Variable gain Amplifiers (VGA), Filters, Bandgap reference (BGR) and ADC architectures.
- Propose new circuit techniques to improve the following:
    I. Enhancement of CMRR of an IA while consuming low power and lower power supply voltage.
    II. Linearity enhancement of VGA.
    III. Low-power ADC design.
    IV. Compact bandgap reference, which will save area.
- Simulate and refine the proposed design using software such as Cadence/LT-spice to prove the validity of the proposed design.
- Develop the layout of the proposed design in Taiwan Semiconductor Manufacturing Company (TSMC) 45nm technology and back annotate the parasitic resistance and capacitance of the critical nodes.

1.5 Original Contribution

The original Contribution of this research was to develop a low-power and highly sensitive Analog Front End (AFE) that senses low-amplitude ECG signals and produces the digital output. The developed system consists of a current Instrumentation Amplifier (IA), gain insensitive VGA, a switch capacitor-based Analog to Digital Converter (ADC) and a small form factor Bandgap reference. The IA has been implemented as a feedback amplifier with a proposed current reusing amplifier. This design achieved 1.26 NEF and 1.6% THD. A servo loop-based VGA was proposed to minimize the gain sensitivity to the PVT corners. Through simulations, it was proven that there was a 9.5dB improvement in the gain. A 60dB switch capacitor-based ADC based on a passive switch capacitor-based integrator avoids the use of power-hungry complex opamp designs like telescopic or folded cascode opamps. This ADC relies on a counter-based decimation filter so that out-of-band noise will be rejected up to a higher degree without requiring any continuous time analog filters. Overall, the ADC demonstrates an energy efficiency of $1.2\,\frac{\mathrm{pJ}}{\mathrm{bit}}$ while sampling at 10 KS/s.

A new bandgap architecture has been developed, which uses one BJT instead of 25 in a traditional circuit. This bandgap exploits a novel self-bias opamp which reduces the systematic offset by 45% compared to the existing one, and the overall bandgap archives a 12.5ppm/^{0}C temperature coefficient over the industrial temperature range of -40 to 125^{0}C. Also, this bandgap works from a lower power supply voltage of 750mV, which is 25% lower than the state-of-the-art.

A prototype has been implemented in CMOS 45nm technology and demonstrated the successful sensing of an ECG signal. The chip was simulated with an input signal whose amplitude is 100uV (pk-pk differential) and a bandwidth of 10KHz. The results demonstrated a 58 dB Signal Noise Ratio (S while consuming 109µW power from a 1.2V supply. The overall noise of the circuit is 0.674uV (integrated over the full frequency band).

The research work presented in this thesis has resulted in 8 peer-reviewed publications.

1.6 Structure of The Thesis

The thesis includes eight chapters explaining the procedures to achieve the research objectives. Following this introductory chapter, the other chapters' compromise of:

Chapter 2 is the literature study of the state of bio-medical transceiver components and their specification for a target application. It starts with the Instrumentation Amplifier (IA) study and its main parameters to consider, like CMRR, PSRR, Gain and input-referred noise concerning its published work. The next block is VGA, which will amplify the signal processed from the IA and feed the signal to ADC. The next and essential block is the bandgap reference, which will generally reference voltage/current for every block in the chip. The main problem with the existing state-of-the-art design is that it occupies a large area and consumes high power. This has been studied extensively in chapter 2 and proposes design targets for state-of-the-art improvement.

Chapter 3 is the product design specification specifying the system's overall design. This includes the block's specifications budget to divide the gain between the IA and VGA is discussed. In addition, how the noise will be shared among all the blocks in the chain is also discussed. Several Quantitative/Qualitative metrics were derived from the transceiver sensitivity point of view. It also derives the ADC specifications, adding significant quantisation noise while sampling.

Chapter 4 introduces the bandgap reference (BGR) design techniques and proposes a single BJT-based circuit, which occupies a compact area and archives better minimal temperature drift across PVT corners. Post-layout results were presented along with the layout.

Chapter 5 explains IA and VGA design techniques and proposes a novel VGA that minimises the gain variation, which is sensitive to PVT variation. This will also compare the state-of-the-art design and shows a 17% improvement in the gain spread.

Chapter 6 proposes a 12-bit 10ks/s low power time-domain ADC, saving significant power than Sigma delta ADC's existing continuous time. Also, this chapter shows the STF and NTF of the design.

Chapter 7 discusses the implementation of the system, which means IA, VGA, ADC and Bandgap will be put together and demonstrates the overall results as a unit rather than individual blocks. Also, it shows the final layout of the chip in 45nm CMOS technology.

Chapter 8, the final chapter of this thesis, concludes the work done and proposes future work. The reference list follows this chapter. Appended to the end of the thesis are conference and journal papers.

1.7 Summary

This chapter presented an introduction to the thesis and then continued to set out the hypothesis and research questions of the research. It then covered the aim and the objectives needed to achieve this aim. It also stated the original contribution of the approaches that will be followed to get to the final solution. Finally, the thesis structure was outlined.

The literature review is explored in the following chapter. It discusses modern approaches and technologies in this research area and provides a full critical evaluation of these technologies.

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Chapter 2:
LITERATURE REVIEW

2.1 Introduction

ECG signals are very important biological signals that can be sensed through electrodes. Electrical signals from the electrodes are fed to the analog front end (AFE) for signal processing. A good understanding of the electrical properties of the ECG signals is necessary to design the optimal AFE characteristics like gain and noise without consuming a lot of power [12]. Due to the interaction between the tissue and electrodes, there will be up to 10mV DC offset at the output, which can saturate the front-end instrumentation amplifier (IA), the first block in figure 1.1 [12]. A review of the existing IA architectures and important parameters to be considered for this application will be investigated. Also, identifying the problems with the existing proposals with respect to the CMRR, Noise, Power consumption and supporting qualitative analysis has been given. The next block (in figure 1.1 [12]) is the Variable Gain Amplifier (VGA), which will amplify/attenuate the differential output voltage of the IA to maintain the constant amplitude signal at the input of the ADC. Before feeding the VGA signal to the ADC, anti-aliasing filtering is necessary to avoid the under-sampling of aliased signals folding back into the signal bandwidth. A brief review of these blocks of figure 1.1 [12] will be given, and recent state-of-the-art publications have been discussed. Most electronics systems need a stable reference voltage and current to provide the required biasing for the opamps and threshold voltage for the ADC. An architectural description of bandgap reference will be discussed in terms of important parameters like temperature coefficient, Power supply rejection ratio (PSRR) and accuracy.

2.2 Electrical properties of Electrocardiograph (ECG) sensing

Figure 2.1 [12] shows the electrodes' electrical properties when interacting with the human body. The electrical study of the interface is essential to understand the noise requirements of the AFE. Figure 2.1 [12] also shows the membrane capacitance (C_m), resistance (R_m) and active intercellular potential (V_m). The I_S represents the ionic diffusion current, which flows into the gap between the cell membrane and the adhesion media and flows into the seal resistance (R_S) to form the extracellular potential V_E. The electrode contact area is exceedingly small. Hence its series impedance is very high (R_{CT}) and thermal noise [12]. This higher resistance causes several electrical issues since noise generation at the input will compromise the system's dynamic range, but it must be very tiny from a safety point of view. The electrode interface generates an unacceptable dc offset due to the interaction of the tissues, the offset is typically 10mV, and the integrated RMS thermal nose in the interested signal band is 1-2μV [12].

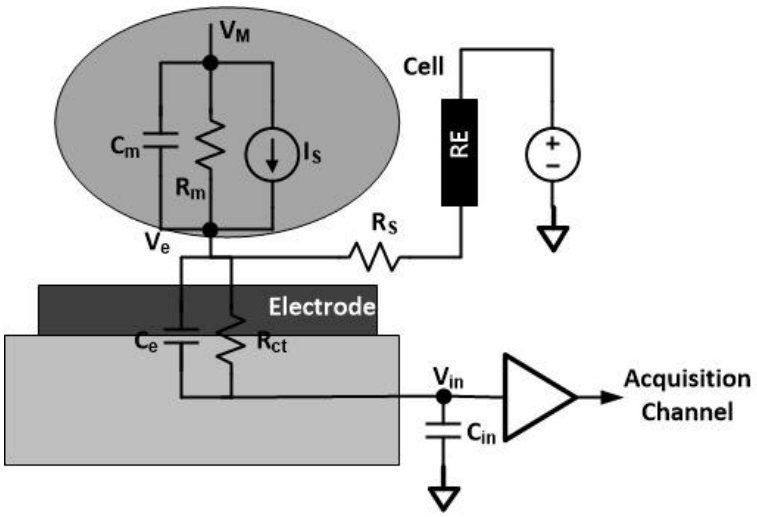


Figure 2.1 Electrical equivalent model of Electrode [12]

The electrode noise spectral density due to the R_{CT} and R_S at the acquisition channel input can be expressed as Equation 2.1:

$$V_{n,in} = \sqrt{4KTR_S.\Delta f + \frac{KT}{C_E}} \tag{2.1}$$

Where Δf is the ECG signal bandwidth, the first term in (2.1) represents noise due to R_S, which is flat in the frequency domain, and the second term is due to the R_{CT}, which is low pass in nature. Typical interface parameters are R_{CT}=6.8MΩ, C_E=3.2nF, and R_S=1MΩ. Figure 2.2 [13] shows the simulated power spectral density (PSD), which depicts $4*10^{-7}$ at a very low frequency and its roll-off start at 10 Hz with $-20\frac{\mathrm{dB}}{\mathrm{dec}}$ slope, eventually it reaches the noise floor of $1.2 \times 10^{-2}\frac{\mathrm{V}}{\sqrt{Hz}}$. The small input amplitude, narrow bandwidth, small size, and low power requirements make the AFE design process challenging [13].

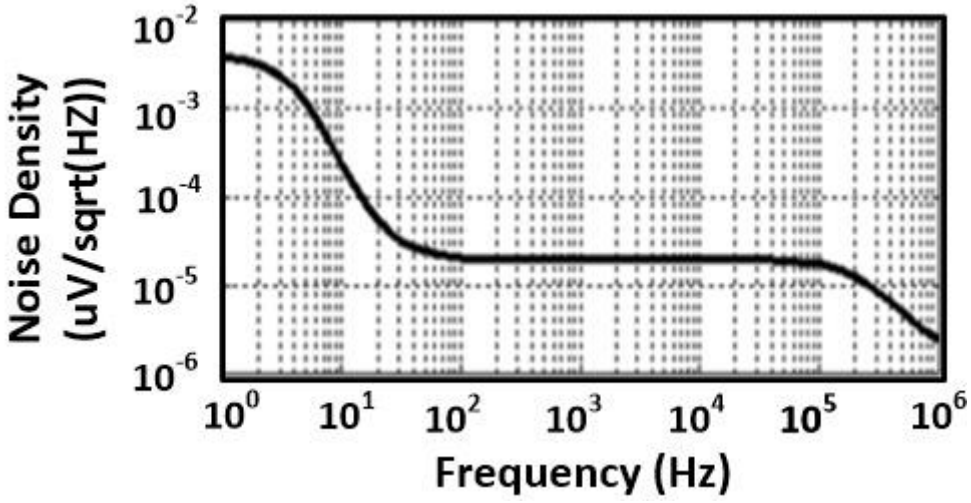


Figure 2.2 Electrode interaction noise [13]

Figure 2.3 [13] depicts the transistor implementation of IA (presented as LNA), VGA (presented as PGA) and sigma-delta ADC. The IA (LNA) has been implemented as a capacitor feedback amplifier whose gains are defined as the ratio of feedback and input capacitor. The PGA design is based on switch capacitor principles with a large pseudo resistance in the feedback to define the DC operating point of the PGA.

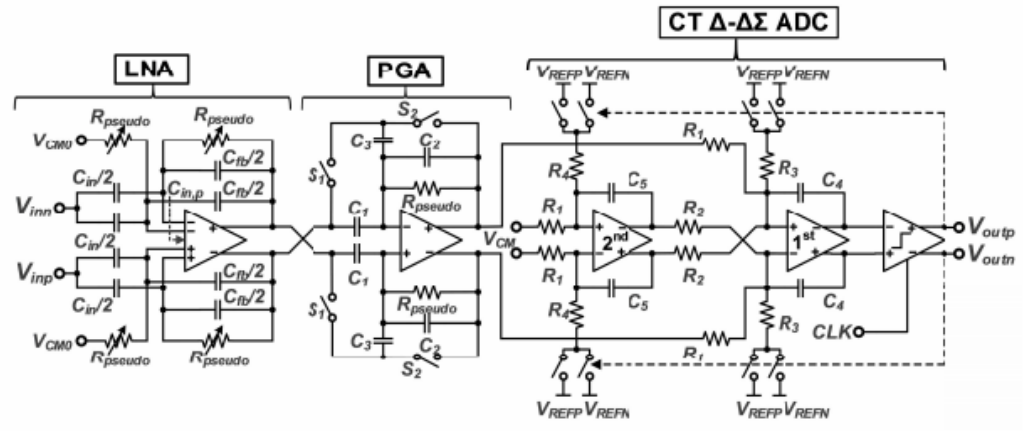


Figure 2.3 Circuit implementation of the AFE block diagram [13]

2.3 Literature Survey of the Analog Front End (AFE)

2.3.1 Instrumentation Amplifier (IA)

The IA will be the first stage in the AFE to amplify the differential signal with very high CMRR so that common-mode noise in the signal will be rejected. The common-mode noise could be electrode-generated interface noise, power supply noise (50/60Hz) and device-generated thermal noise/flicker noise. There are fundamentally two different ways that IA architectures have been explored.

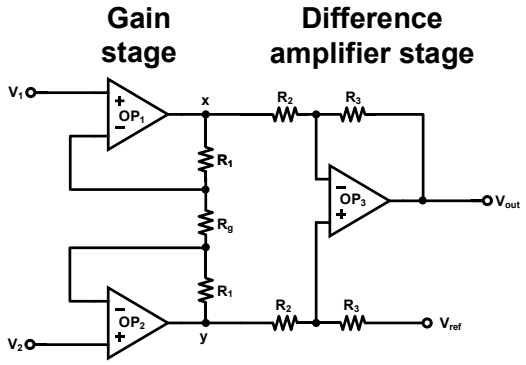


Figure 2.4 Three-Opamp high CMRR IA schematic [14].

The most popular way is the voltage mode signal processing technique, involving a 3-opamp-based structure, as shown in figure 2.5 [14]. The first gain stage of figure 2.5 [14] consists of two opamps, op1, op2 and common mode resistors R_1, R_2, and R_3, which aims to amplify the differential signal (V_1-V_2) while keeping the common-mode gain close to unity. If any common-mode disturbance presents at the input, that will directly appear across R_g and the same voltage at nodes X and Y (assuming the opamp offset is less than the signal swing). The main purpose of R_G is to improve the CMRR. The second stage acts as a differential to the single-ended converter. It presents a negative gain for the signal at node x and a non-inverting amplifier for the signal at node Y.

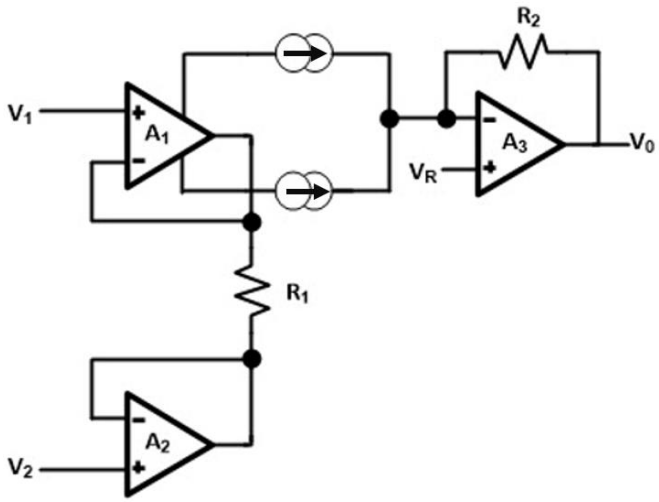


Figure 2.5 The proposed schematic in [15].

The three-Opamp high CMRR IA is well-known and widely used due to several advantages and implementation difficulties. Both of these are summarised in Table 2.1 below. The overall gain of the three-Opamp high CMRR IA [14], shown in figure 2.4, can be expressed in equation (2.2).

$$Overall\ gain = \frac{R_3}{R_2}\left(1 + \frac{2R_1}{R_g}\right) \tag{2.2}$$

Table 2.1 Summary of the Three-Opamp high CMRR IA [2, 3].

Advantage	Disadvantage
Input impedance is very high hence less loading on the electrode heads	With a modern CMOS process, where resistors are matched up to 1% in a 3-sigma lot, 70% of the circuit area is dominated by resistors, resistor area trades with CMRR.
Both inputs have symmetrical electrical loading, hence good high-frequency CMRR.	On-chip opamps are offset typically in the range of 1mV, which will affect the SNR at the output. Equation (2,3) depicts the impact of the opamp offset on the output voltage.
A programmable Rg can implement variable gain.	The resistors will generate a significant amount of noise since their value is very high.
	Given the supply voltage limitation in the CMOS technologies, the maximum signal swing in the second stage will be limited due to the first stage's high gain nature.

$$\boldsymbol{V_{out}} = \frac{\boldsymbol{R_4}}{\boldsymbol{R_3}}\left(\mathbf{1} + \frac{\mathbf{2}\boldsymbol{R_2}}{\boldsymbol{R_g}}\right)(\boldsymbol{V_{OSP1}} - \boldsymbol{V_{OSP2}}) + \left(\mathbf{1} + \frac{\boldsymbol{R_3}}{\boldsymbol{R_4}}\right)\boldsymbol{V_{OSP3}} \tag{2.3}$$

There have been multiple proposals to improve the performance of the IA. [15] proposes a modified 3-opamp IA, which will work on the lower supply voltage, which is compatible with the 45nm CMOS technology, but unfortunately, CMRR has not improved much [13]. Most of the proposed IA's are processing the signal in the voltage domain; hence the max signal amplitude is limited by the power supply. In order to improve the CMRR, [16] proposed a current mode-based IA, which will solve the current dynamic range issue of

the transceiver. The proposed design is depicted in figure 2.6[15]. The amplifiers A_1 and A_2 will act as voltage buffers and convert the input signal into the current. CM_1 and CM_2 current mirrors will extract the current from the output stage of the opamp A1, which means opamps and current mirrors acts as a voltage to the current converting stage. Opamp A_3 and resistor R_2 form a current-voltage converter (Trans-impedance amplifier). The output of the Opamp (A3) will represent the amplified version of the input signal with excellent CMRR at the cost of the additional current mirrors compared with existing techniques [4-6]. The CMRR can be improved by reducing the input referred offset of the opamps, either though proper layout or chopper stabilization techniques (requires external clock generator)

The main issue with this proposal, shown in figure 2.6, is the requirement of high bandwidth opamp to process a certain input signal bandwidth, and flicker noise will be more. In addition, because there is always DC flowing through any active component, it will raise the flicker noise floor and the corner frequency.

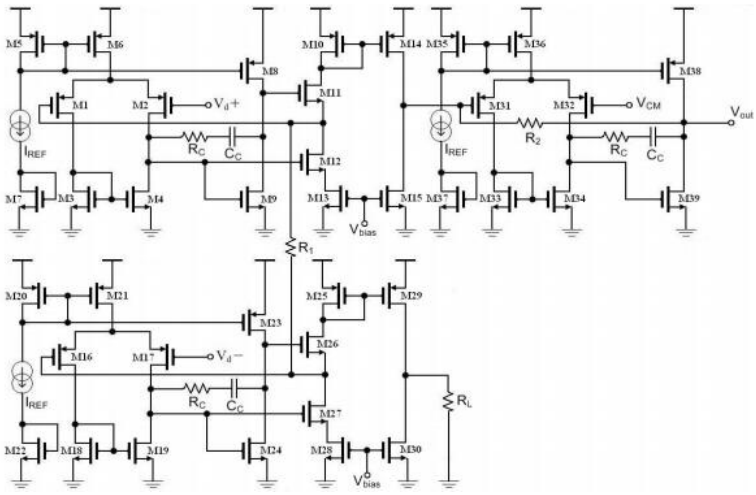


Figure 2.6 Transistorized implementation of Figure 4 [15]

Here Opamps A1 and A2 will carry continuous current, which will also raise the power consumption. Figure 2.6 shows the transistor implementation of the block diagram in [15], using folded cascade opamps for A_1, A_2 and a class-AB final output stage. Transistors M_1 and M2 act as a differential pair for a low voltage signal, and M3 and M4

act as a differential pair for high voltage signals. A simple common source stage followed by this differential pair acts as a second-stage amplifier, which will improve the signal swing capability of the voltage-to-current converter. Figure 2.7 shows the CMRR versus differential input signal, which depicts 112dB, which is good enough for sensing applications. Because the actual sensing signal will be around 1mV in the worst case, the common-mode disturbance would be in the order of 100mV. Hence a CMRR of more than 100dB would be sufficient for the present application. It is one of the most accurate IA in the literature, with the following disadvantages. (i) Very high-power consumption. (ii) Frequency compensation of the negative feedback loops is quite challenging as DC flows from one opamp to another opamp.

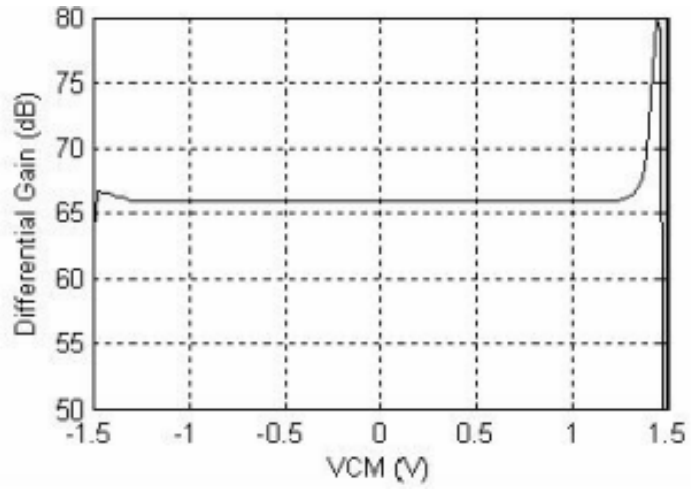


Figure 2.7 CMRR vs differential signal amplitude [15].

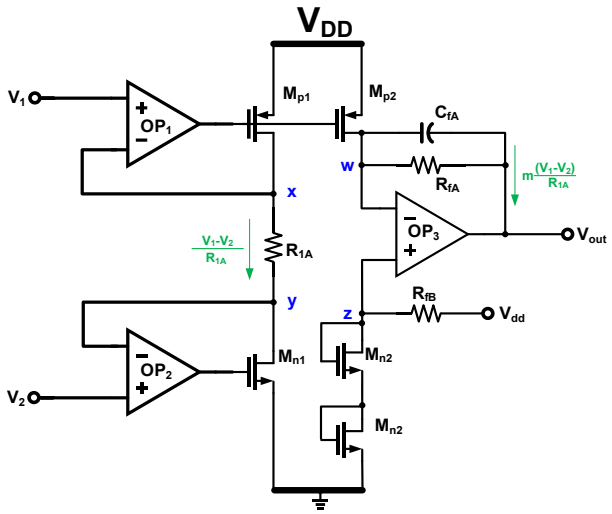


Figure 2.8 The current mode IA schematic is proposed in [18].

[18] illustrates a current mode IA without requiring any power-hungry Class-AB output stage. The schematic is shown in figure 2.8, which shows that the R_{1A} resistor will convert the input signal into a current signal, mirrored into a low noise TIA, formed by Op3 R_{1f}. Op3 input common mode was defined using a MOS-based potential divider formed by R_{FB}, MN_2 & MN_3. This work resulted in a high CMRR similar to [15] while consuming very low power. However, this will have a noise penalty. Hence there is a need to develop good noise performance IA while keeping good CMRR. Also, none of the proposed IA's has a DC cancellation loop, an important feature to offset with-stand resulting from the electrodes. The negative feedback loop formed by op_3, RF_A, M_{P2} can be unstable due to two dominate poles in the open-loop transfer function. So to improve the phase margin, a feedback capacitor C_{FA} has been introduced, which creates a zero in the loop gain function hence it will improve the phase margin.

2.3.2 Variable Gain Amplifier (VGA)

The variable gain amplifier (VGA) appears second, after the instrumentation amplifier (IA), to maintain a constant signal available to the ADC to maintain a constant dynamic range. The VGA is needed because The IA can only amplify the signal without attenuating. Hence this could be a distortion problem with a large signal at the input. The

IA can realise a high CMRR that rejects 50/60Hz common mode noise, limiting the power supply interference. To obtain a clean neural signal recording, the IA input-referred noise must be lower than the signal amplitude [16]. Practically the input-referred noise of the IA should be lower than the background noise of the recording site. However, for a thermal noise-limited amplifier with constant bandwidth and power supply voltage, the amplifier's power is proportional to $1/V_n^2$, where V_n is the input-referred noise of the amplifier.

VGA is a critical block in most analog front-end or signal-processing systems [18]. The important parameter of the VGA is defined as the Dynamic range, which is the ratio of the maximum possible signal at the input to the minimum required signal. The system's linearity limits the maximum signal, and the random noise of the system limits the minimum signal amplitude. For a given sensitivity (minimal detectable signal strength) of the AFE, the VGA needs to have a very well-defined gain range; otherwise, the final ADC dynamic range will be compromised [19]. Hence, the ADC cannot use a full number of bits for the conversion process. The VGA gain variation range should be large enough to amplify the min and max limits of the input signal. A lower than required gain would compromise the SNR (Signal to Noise ratio), and the higher gain would clip the signal at the minimum, and maximum value and linearity will be compromised. Existing VGA architectures are mainly based on the degenerated differential pair, whose gain is very sensitive to the PVT variations [20].

Figure 2.9 (a) shows the conventional differential pair, whose gain is the ratio of the load resistance (R_L) and degeneration resistance (R_s) as expressed in equation 2.4. Degeneration improves the linearity of the VGA by dropping most of the signal across the resistor rather than the transistor. Unfortunately, this technique creates a problem for the transistor's headroom voltages because of the DC drop across R_s. The DC gain is expressed as follows, which is approximately defined by R_L and R_s when $g_m R_s \gg 1$.

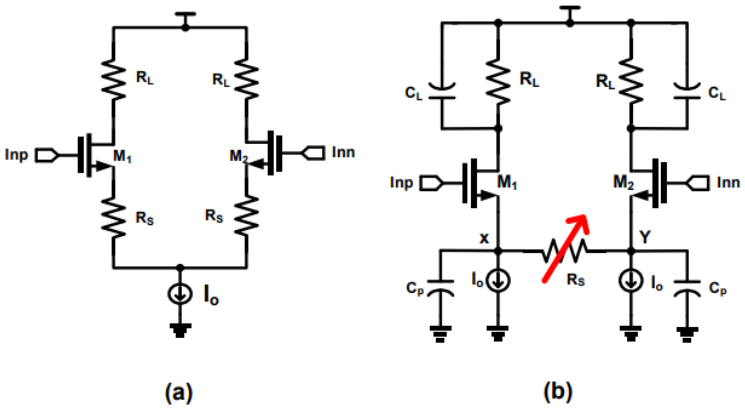


Figure 2.9 (a) Conventional VGA [19] (b) Split degenerated VGA [20]

$$A_{DC} = \frac{g_m}{1+g_m R_s} R_L \sim \frac{R_L}{R_S} \tag{2.4}$$

[20] proposed a modification technique by making the dc drop across Rs zero by adding two current sources while keeping the total current constant, as shown in figure 2.9 (b). The technique has several disadvantages as shown in figure 2.9 (b). The current noise will appear directly at the output because each current source (I_0) will see different impedance on both sides, one side is Rs, and another side is $1/g_m$. The output integrated noise is expressed in equation 2.5.

$$v_n^2 = 4KTg_{m1}\left[\frac{\frac{1}{g_m}-R_s}{\frac{1}{g_m}+R_s}\right]^2 R_L^2 \tag{2.5}$$

Second, the parasitic capacitance at the tail node of the degeneration resistance will create unacceptable peaking in the frequency response, which will create noise peaking at that frequency, and linearity will be compromised. Figure 2.10 shows the effect of parasitic capacitance on the frequency response. The major issue with the proposed techniques is that the gain is strongly dependent on the Process, Voltage, and Temperature (PVT) corners, and the integrated noise at the output is not acceptable [17]. Currently, no technique has been proposed to solve the peaking issue, but several references reported that minimising the parasitic capacitance helps eliminate this problem to a large extent. Alternatively, limiting the lower end of the gain variation will

solve the issue because C_p does not affect the higher gain. Hence designing a slightly higher gain range would fix this issue at the cost of harmonic distortion and power consumption.

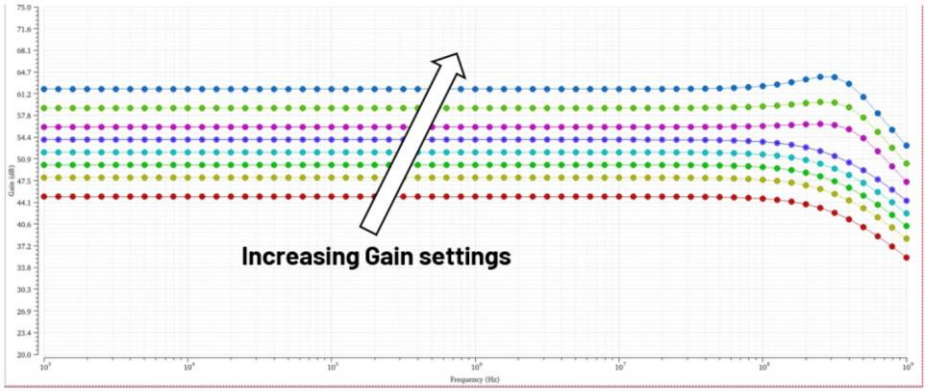


Figure 2.10 Frequency response showing the C_p effect [21].

Resistor degeneration will create noise and peaking problems, and non-degeneration will be prone to PVT variation. One way to avoid these problems is to use a non-degeneration method but providing the differential pair's bias current to stabilise the gain is the best method to fix the issue. [21] proposed a way to stabilise the gain by using a constant g_m bias, which will ensure the trans-conductance (g_m) of the transistor as a function of the resistance. The schematic shown in Figure 2.9 (a) has the best noise performance provided higher supply voltage available to bias the structure, where 2.9(b) has the best performance for the lower supply with moderate noise performance. Also frequency response of 2.9(a) is insensitive to the parasitic capacitance of the tail node.

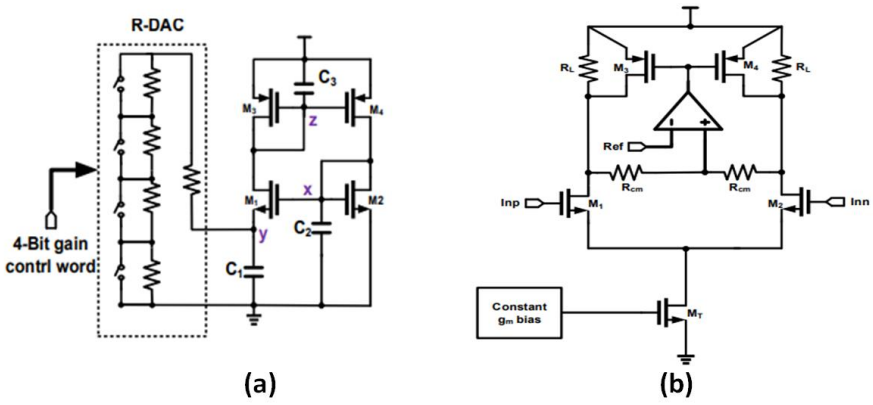


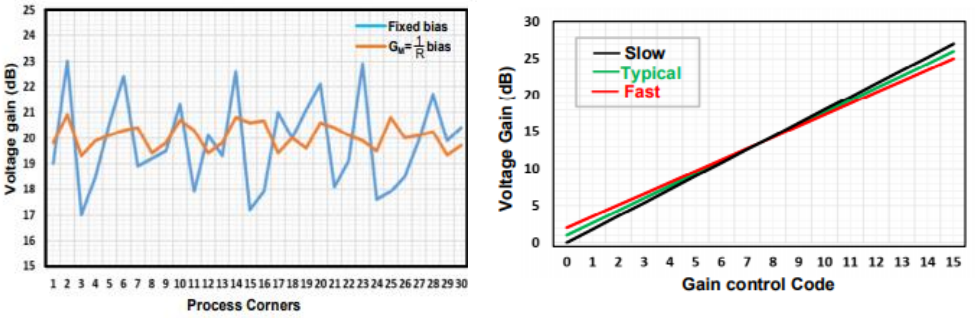
Figure 2.11 (a) Bias Circuit (b) VGA Schematic [21]

Figure 2.11(b) [21] shows the conventional differential pair with bias generation. Since the current varies with the PVT corners, the differential pair output common-mode voltage can compromise the linearity and distortion. Hence, a Common Mode Feedback Loop (CMFB) was added, which will sense the output common-mode voltage through R_{CM} resistors and corrects it through Opamp-1. Opamp-1 injects the common mode current into the load resistance through the PMOS transistors (M_3, M_4). Figure-2.11(a) shows the constant gm circuit. Transistor M_1 is degenerated by a programmable resistance (shown as R-DAC in the picture). The voltage across the resistance is the difference between V_{gs1} and V_{gs2}. Due to the four times the size of M_1, compared to M_2, v_{gs2} is two times smaller than V_{gs1}.

$$V_R = V_{GS1} - V_{GS2} = \frac{V_{ov}}{2} \tag{2.6}$$

From the transistor small-signal model, g_m can be expressed as (2.7). RP is the DAC's programmable resistance, V_{OV} is the overdrive voltage, and I_B is the bias current.

$$g_m = \frac{2I_B}{V_{ov}} = \frac{1}{R_P} \tag{2.7}$$



(a) **(b)**

Figure 2.12 (a) VGA Gain across PVT (b) Gain vs Control Code [21]

The bias current from the constant gm circuit shown in 2.11(a) will stabilise the gain. Figure 2.12(a) shows the gain of the VGA wrt to the PVT corners. Fixed bias results in voltage gain variation from 17 to 23dB (35% of the variation). The adaptive bias through the constant g_m circuit gain shown in figure:2.12(a) depicts the gain range of 20.5 to 19.6dB, which is 3.5%. Compared with the fixed bias, the adaptive bias has shown significant improvement in the gain, but this circuit has the following downsides (1) the performance is strongly depending on the square law current equation, which is not very true in modern CMOS technologies due to the several second-order effects [21]. (2) M_1 heavily degenerates, and its source terminal is not at ground potential, whereas the M_2 source is at ground potential. Hence there will be a body effect-induced threshold voltage (V_{th}) difference; therefore, there will be a gm error. (3) The supply sensitivity would also be a problem due to the output impedance degradation through channel length modulation. M_3 drain to source voltage (V_{DSM3}) depends on the V_{DD}, whereas M_4 drain voltage is independent of $V_{DD;}$ therefore, it will create current mismatch errors. These three effects described above will create tracking errors in the g_m, leading to VGA gain errors. Also, this circuit adds one extra opamp and bias circuitry, adding additional power consumption to the transceiver power budget.

2.3.3 Bandgap reference circuit (BGR):

Several analog circuits require a voltage reference whose output voltage is independent of the temperature. This reference voltage will be used for Low Drop-out regulators (LDO) and as a signal reference for Analog to Digital converters (ADCs) [20]. The accuracy of the reference voltage will determine the ADC static performance, such as Integral Non-Linearity (INL) and differential non-linearity (DNL). For instance, a 10-bit ADC works on a 1.2V power supply, with its Least Significant Bit (LSB) value around ~1.17mV. The maximum allowed error is 0.5*VLSB, which is 0.585mV. Which mandates the bandgap reference voltage drift over the industrial temperature range (-40 to 125^0C). The typical bandgap voltage would be around [13] [21] 600mV, so it should have 45.6ppm/^{0}C performance.

The bandgap reference works in the following principle. To maintain zero or minimum temperature drift, two voltages with opposite temperature drifts will be summed with the proportional scaling factors. The junction voltage of the diode will decrease with temperature with a slope of -2mV/^{0}C. Hence it is called Complimentary to Absolute Temperature (CTAT) voltage. The V_{BE} of the BJT can be expressed as (2.8), where V_T is the thermal voltage, I_s represents the reverse saturation current, and IC is the bias current.

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{2.8}$$

The difference in V_{BE} of the two diodes, whose current densities are different, can be used as positive temperature coefficient voltage (PTAT). For example, if two diodes carry the same current with an area ratio of n, their difference voltage can be expressed as shown in equation 2.9.

$$delta\_V_{BE} = V_T \ln n \tag{2.9}$$

To achieve the minimum temperature coefficient, the PTAT and CTAT voltage should have equal and opposite polarities. The PTAT slope is 17.3 times smaller than CTAT slope, hence PTAT voltage has to amplifier by 17.3 and then CTAT and PTAT will be added to achieve zero Temperature Coefficient. The Bandgap o/p voltage can be expressed as follows.

$$V_{BG} = V_{BE} + 17.2 * \ delta\_V_{BE} \tag{2.10}$$

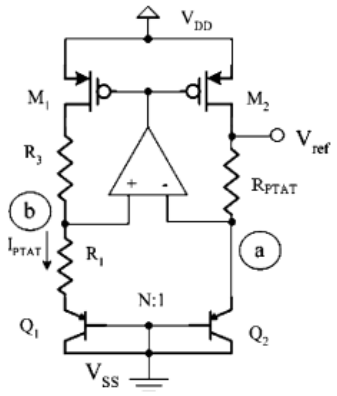


Figure 2.13 Voltage mode Bandgap Schematic [22]

The first popular implementation is proposed in [22] and is shown in figure:2.13. As explained in the introduction, the PTAT voltage will be formed across a PTAT resistance R1 node potential is CTAT. M_1 and M_2 current mirror forces the same current through both diodes, and the bandgap loop operating point will be a specific point where both voltages will be the same. The voltage at the M_2 drain will be the bandgap voltage (V_{ref}), expressed in equation 2.11. The temperature coefficient of the V_{BE} is -1.6mV/^{0}C. To get the minimum temp coefficient, Rptat/R_1 ratio should be around 7.2.

$$V_{ref} = V_{BE} + \frac{R_{ptat}}{R_1} V_T \ln n \tag{2.11}$$

This architecture works very well, but unfortunately, this technique requires a supply voltage greater than 1.3V, which may not be the case for modern CMOS processes like 130nm and smaller [22], and they often have a supply voltage of less than 1.2V. [23] proposed a technique to scale the supply voltage based on a current summation

technique rather than voltage summing as in previous architecture, as shown in figure:2.14. The simple modification is to add two parallel resistors (R_{2A}, R_{2B}) across the opamp. These resistors carry CTAT current, and R_1 will carry PTAT current. Hence, they can be summed in the proper ratio to get the zero temperature coefficient voltage in R3. The output voltage can be expressed as follows.

$$V_{ref} = \left(V_{BE} + \frac{R_{2A}}{R_1} V_T \ln n\right) \frac{R_3}{R_{2A}} \tag{2.12}$$

As it is clear from the expression, the output voltage can be scaled with the resistor ratio. Hence it works with the supply voltage being less than 1V. Though this is low voltage compatible, this occupies a large silicon area because of the large resistors. Also, it has multiple operating points because, in Figure 2.14, when there is less current during the start-up, the resistors will consume all the current until the BJTs are turned on. Hence, nodes a and b have the same potential; hence, there are multiple operating points. This is one reason why Power-On Reset (POR) based start-up monitor circuits are very popular.

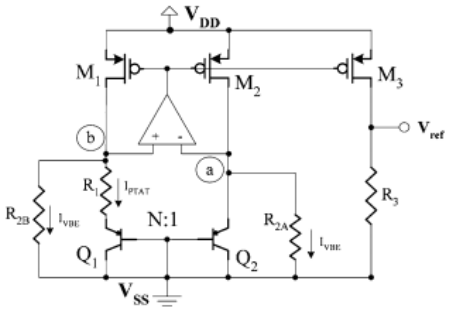


Figure 2.14 Current mode Bandgap reference (aka Bamba bandgap) [24]

[24] [25] proposed minor modifications to improve the accuracy or power consumption, but they all are very similar to [26]. Most of the proposals have several problems, as explained in the following. (1) These bandgaps use several BJT devices. They are costly in the CMOS process. Hence minimising/eliminating the devices will make them compatible with the CMOS process technologies. Also, the BJTs in the CMOS process will suffer from several non-idealities. They are vertically formed devices, where n-well

is the BJT base, which is wider and makes current gain (β) close to 1 or sometimes less than 1. Also, BJT reverse saturation current is very high compared to the actual BJT. The silicon area occupied by them is quite high because of the extensive use of resistors, and they are in the order of several megaohms. In any proposed bandgap so far, the resistors occupy >92% of the overall circuit area. (2) They all require a start-up circuit. Because of its balanced nature, any previous proposals will have a stuck point at zero current. Hence without a start-up ckt, the bandgap could have started the issue. Recently several researchers have proposed only MOS-based bandgap references to avoid BJT devices [26] [27] [28]. [27] described a microwatt bandgap reference, which will consume 12.3μW power, suitable for biomedical applications, as shown in Figure 2.15.

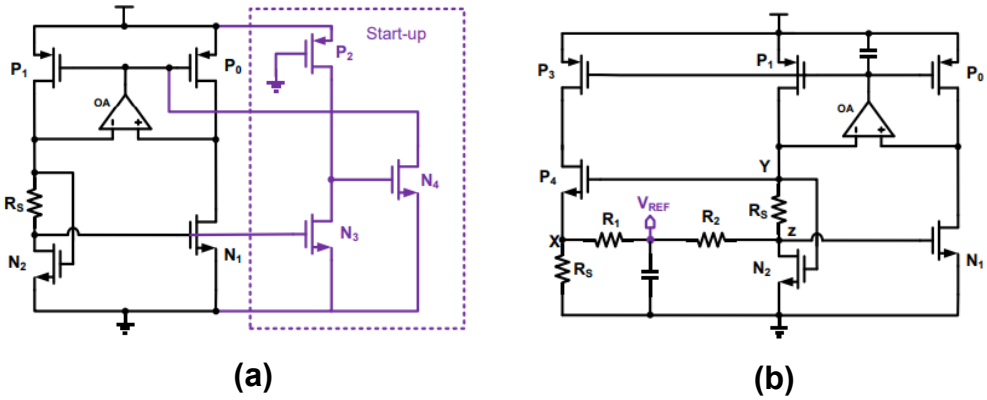


Figure 2.15 (a) Beta Multiplier used (b) microwatt bandgap core, the only use of MOS devices [27]

Figure 2.15(a) shows the beta multiplier exploited for the bandgap core design. Compared with the conventional beta multiplier, the degenerated resistance R_S used in the drain of N_2 is compared to the source of N_2 to avoid the body effect. Also, OA opamp has been used to equalise the drain voltages of the PMOS devices P_1 and P_0 such that channel length modulation would not affect the accuracy of the circuit. Here the N_2 aspect ratio (W/L) is four times higher than the N_2 aspect ratio, so the bias current has a PTAT nature. It has been derived as follows.

$$V_{rs} = V_{gs1} - V_{gs2} = \frac{2}{u_n c_{ox} \frac{W}{L}} \frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{2.13}$$

In equation (2.13), by substituting K=4, we can derive the gm of the $N_{2,}$ equal to $1/R_s$. Also, (2.13) reveals that the bias current is PTAT in nature because the mobility of the electrons will decrease with the temperature. The beta multiplier needs a start-up circuit because zero current in N_2 is being forced to the N_1 side, and the PMOS current mirror also forces the same. Hence the zero current will be the stable operating point. N_3, N_4, and P_2 form the start-up circuit, which works as follows. When there is no current in the core circuit, the N_3 drain potential will be very high and close to the V_{DD}. Hence the N_4 transistor will pull down the opamp output voltage, enabling the bias current. Once the circuit current reaches a required level (enough to turn on N_3), the N_3 drain will be at a very low potential, somewhere close to the ground potential; hence the start-up circuit will be in an off-state without disturbing the actual operation.

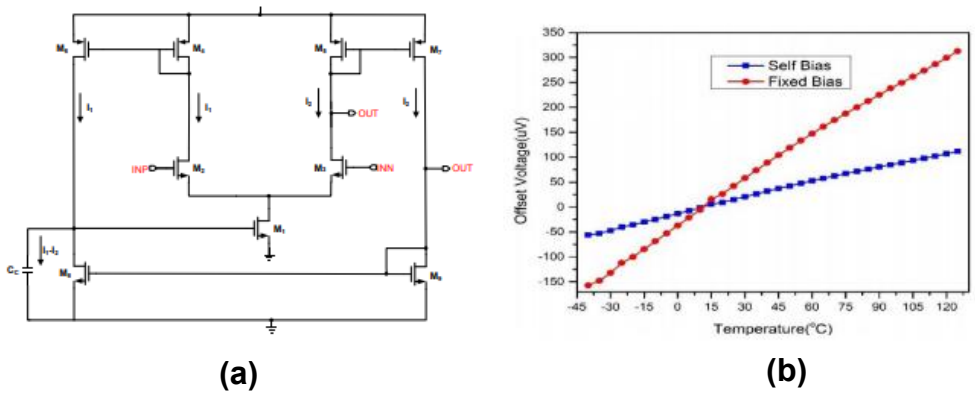


Figure 2.16 (a) Self-bias opamp (b) offset of the self-bias opamp[16]

Figure 2.15 (b) shows the bandgap core schematic, summing CTAT and PTAT voltages with a proper scaling factor to get the zero temperature coefficient. Here node Z potential has a CTAT nature because the threshold voltage (V_{th}) will decrease with temperature. On the other hand, node X potential has a PTAT nature because the beta multiplier core current is mirrored through a PMOS current mirror and pumped into the resistor R_s, as described in equations (2.14) & (2.15).

$$V_X = R_B \frac{2}{u_n c_{ox} \frac{W}{L} R_S^2} \left(1 - \frac{1}{\sqrt{k}}\right)^2 \tag{2.14}$$

$$V_Z = V_{th} + \sqrt{\frac{2I_B}{u_n c_{ox} \frac{W}{L}}} \quad (2.15)$$

To sum up these two voltages (V_x&V_z), a potential divider has been used, which is formed by R_1 and R_2. These two resistance values are much higher than those node impedances to minimise the loading. In this scheme, the scaling factors are the ratio R_1 over R_2 hence independent of PVT and can easily be tuneable. For typical CTAT and PTAT sensitive numbers, the PTAT scaling factor will be around 5.6, which is small compared to the BJT version. Hence less opamp offset the effect on the BGR output. The reference voltage can be expressed as follows.

$$V_{Ref} = \frac{V_x R_2 + V_y R_1}{R_1 + R_2} = \frac{1}{1+\beta}\left(V_{th} + \frac{\alpha}{u_n c_{ox} \frac{W}{L}}\right) \quad (2.16)$$

Where,

$$\alpha = \frac{1}{R_S}\left(1 - \frac{1}{\sqrt{K}}\right)\left(\frac{1}{2} + \beta\left(1 - \frac{1}{\sqrt{k}}\right)\right) \quad (2.17)$$

Figure 2.16(a) shows the opamp schematic that has been used in the beta multiplier core. Instead of the standard 2-stage conventional opamp, this has used a special class of opamp called the self-bias opamp to improve the systematic offset [28]. In this structure, M2, M3, M4, and M5 form the differential pair with low output impedance at the output. For the conventional amplifier, the tail current will be biased from a fixed current source, and the output branch will support the bandgap core current (which has a PTAT nature). The output is referenced to Vgs of M9, where the current density of M9 and bandgap core device will be referenced to PTAT Vgs; hence they don't match together. In [28], authors have biased the M8/M9 transistors with a self-bias nature, which means the bandgap current will bias the opamp. Hence the current density of the output device will match, and systematic offset will be minimised (max-25.4μV). Though systematic offset is very less, its temperature variation will affect the bandgap output's temperature drift over the scientific temperature range (-40^{0}C-125^{0}C). Figure 2.16(b) shows the simulation results comparing the standard/self-bias opamp offset in the typical

process corner versus the temperature. The offset generally increases with temperature because it is proportional to the g_m/I_d ratio of the input transistors. In the standard bias, the offset varies from -150 to 320μV, whereas in the self-bias, it has gone down from -50 to 87μV. Hence self-bias scheme improves the input-referred offset voltage by a factor of 2.3.

2.3.4 Anti-Aliasing filter:

The amplified signal will be fed to the ADC to digitise the analog input signal; so that it can be processed by a digital processor. However, the VGA output will have several image tones, which can be aliased back to the signal band, increasing the noise floor and distortion levels. For example, a low pass filter will pass the frequencies below its cut-off frequency and filters all the frequencies above the cut-off frequency. So in the present signal processing contest, a low pass filter designed to reject the aliases will be required, known as an anti-aliasing filter. The major electrical requirements of the filter can be tableted as follows.

Table 2.2 Electrical Specifications [31].

Parameter	Value
Type of the filter	4^{th} Order Low pass filter
In-band gain	32dB
3-dB Bandwidth	<8MHz
Passband Gain Ripple	<5%
Integrated Noise	20nV
Dynamic Range	>39.8dB
Filter Approximation	Butterworth Filter
Max acceptable input signal	<500mV

Several types of Anti-aliasing filters have been reviewed in the literature [31]. They are passive filters, active RC filters, and transconductance-capacitance(g_m-c). Passive filters are designed with pure RLC components, which are very bulky and difficult to integrate into an IC. However, they are the best from a power consumption and noise generation point of view. Active RC filters are designed with only R, C and opamps. Inductors are eliminated; hence, they are very compact, allowing easy integration within the modern CMOS technology-based chips. They are known for their excellent linearity. Unfortunately, the opamp consumes significant power and generates unacceptable noise [31]. Gm-c filters compromise the active RC and passive filters and are known for their speed because of their open-loop nature. Unfortunately, gm-c has very poor linearity due to the excess overdrive of the open-loop OTA designs existing so far. In the bio-medical instrumenting area, active-RC filters are more common in nature. [31] [32] [33] [34] have proposed several techniques in the literature with the best performance suitable for bio-medical transceivers. Figure 2.17 depicts all the verities of the filters.

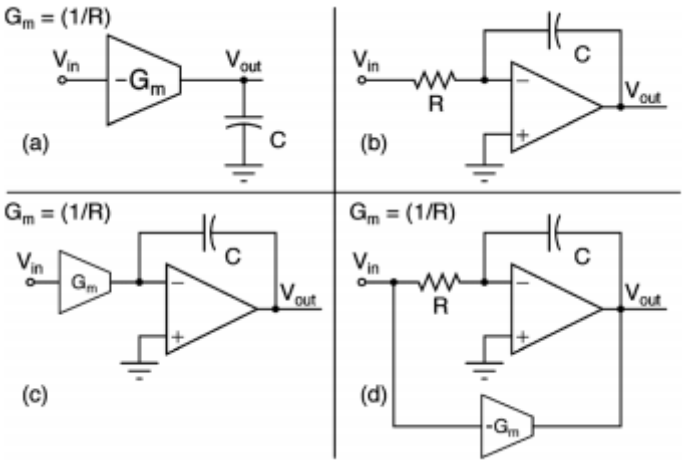


Figure 2.17 (a)gm-c filter (b)active RC filter (c)improve active RC filter (d)feedback based assisted RC filter[31]

2.4 Summary

In this chapter, how to sense a tiny and low-frequency bio-medical signal is described briefly and also explained the challenges involved in that. All the blocks involved in the sensing were described, and their specification was mentioned. Recent literature on IA, VGA, Filter, Bandgap Reference and ADC blocks studied and described the state-of-the-art specification metrics. The IA senses the signal and amplifies it without adding much noise. The VGA amplifies/attenuate the signal to keep the input amplitude at the ADC constant. The anti-aliasing filter reduces the image signals folding back to the signal bandwidth of the interest. The fundamental working principle is explained in such a way that it clarifies what has been done so far and what to do to improve Bio-medical sensing performance. Performance metrics of each block are described qualitatively to make the sensor noise budget more accurate and easy to analyse.

The next chapter discusses the performance trade-offs among the different blocks in the signal path and derives the target specifications of each block.

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Chapter 3: SYSTEM SPECIFICATIONS

3.1 Introduction

As discussed in chapter 2, to design a power-efficient and high-performance analog system/bio-medical sensor, it is important to come up with optimal system specifications from the results (could be sensitivity, input-referred noise and power dissipation). To develop the system specifications, it is essential to have a good understanding of the input signal frequency-domain characteristics. For example, if the signals have a steep roll of a certain frequency range (fraction of the overall Bandwidth), the amplifier should have a higher-order filter nature.

In this chapter, section 3.2 discusses the ECG signals' frequency domain characteristics. Then followed by section 3.3 briefly explains the ECG signal characteristics. Finally, the rest of section 3.4-3.6 explains the IA, VGA, Bandgap and ADC specifications, respectively.

3.2 Characteristics of the ECG signals.

The ECG wave is the accumulated total of action potentials of the cells in the body. The position and orientation of the Electrodes will decide the characteristics of the ECG wave [35]. For most signal processing applications, ECG waves can be treated as a vector. Each segment is represented in five segments P, Q, R, S, and T, as shown in figure:3.1, which is a picture corresponding to the electrodes' positions on the patient's left wrist. Each segment in the picture represents specific region functioning of the heart. In the atria, cells undergo depolarization, and the P-Wave occurs, as shown in figure:3.1. Always electrical impulse travels from left to right atria [36]. QRS wave occurs when the vertical cells undergo depolarization. Also, the picture shows the duration from each section, all possible sections and amplitude as well. Equation (3.1) describes the relationship between the QT and QTC waves [37]. The duration of P, QRS, P-R, and Q-TC wavers are -(0.08-0.1s), (0.06-0.10s), (0.12-0.2), (<=0.44s), respectively.

$$QT_C = \frac{QT}{\sqrt{RR}} \tag{3.1}$$

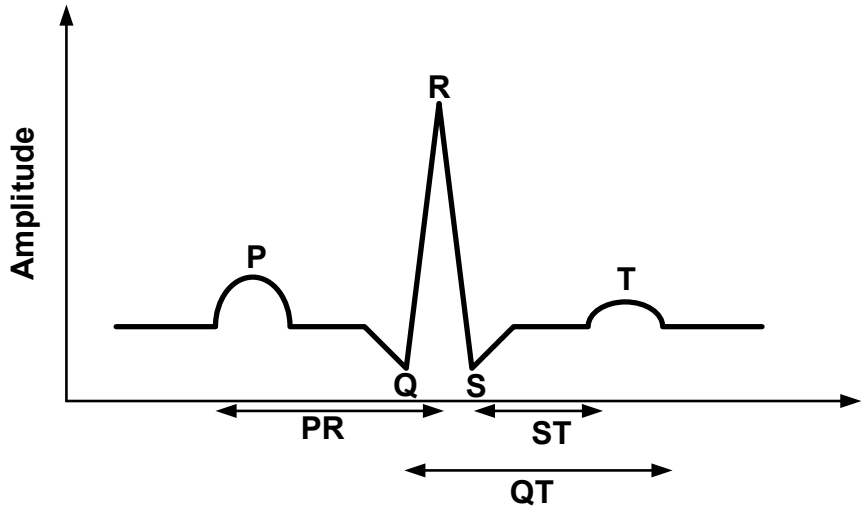

Figure 3.1 ECG signal time-domain Profile [37]

Figure 3.2 shows the frequency domain representation of the typical ECG signal shows the signal bandwidth of the signal ranging from 0.1-200Hz, and the amplitude is as low as 1mV-RMS. This is very useful information for the sensor design as this will decide the lower cut-off frequency of the front-end IA and the target input referred noise in order to meet the sensitivity specification and power consumption [37].

3.3 Electrical model of Skin-Electrode.

The ECG sensor input impedance plays a significant role in determining the distortion and input-referred noise. Hence understanding the electrical behaviour of the interface is essential before getting into the actual design. Ohm's law does not work at the non-linear junction interfaces due to multiple-layer involvement. In the skin/body, ions are electrical current creators, like electrons are carriers in the metals/semiconductors. Figure 3.3 [38] shows a simple passive first-order electrical model of the skin-electrode interface.

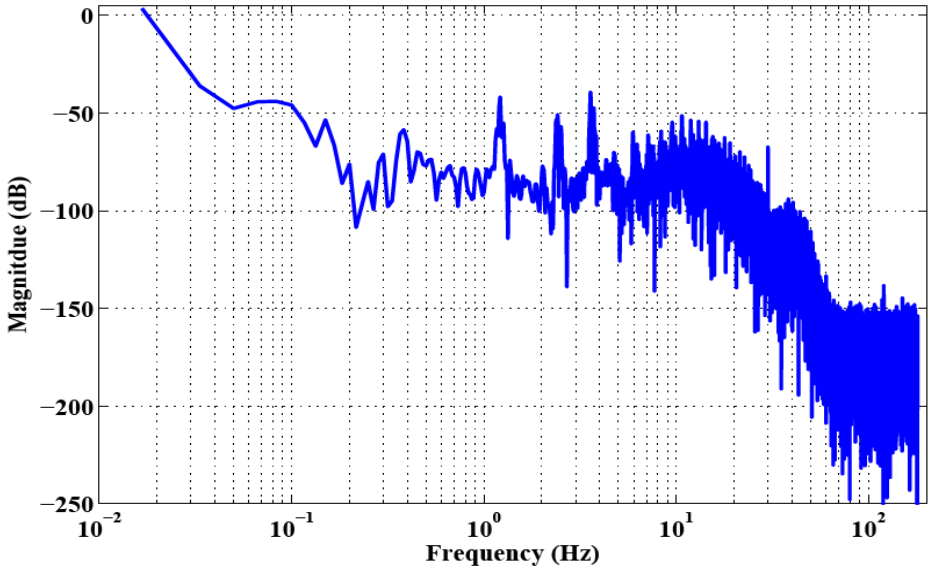

Figure 3.2 ECG signal time-domain profile [38].

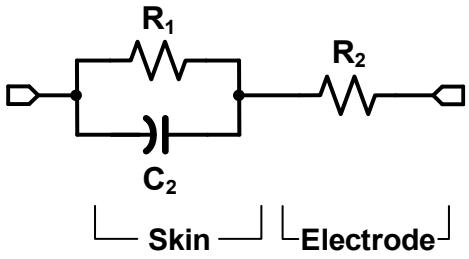

Figure 3.3 First order Skin and electrode model [38].

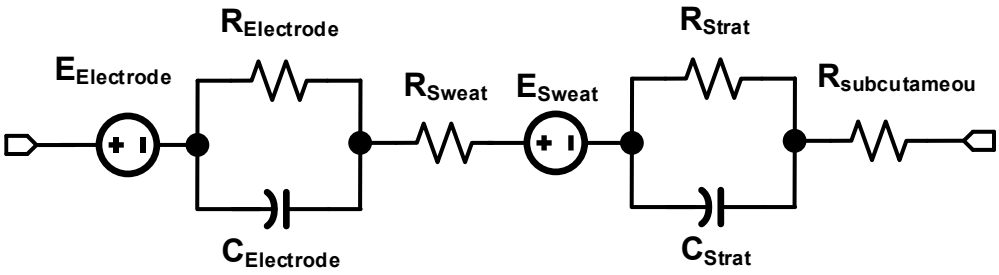

Figure 3.4 Second-order Skin and electrode model [38].

This model is easy and simple to construct with real-time values and works for a very limited range of the input signal bandwidth. Therefore, a second-order and more accurate electrical model has been given in [38], as shown in Figure 3.4. Compared with the first-order, this second-order model works for the full band of the frequency range. Unfortunately, this is complex to construct and most importantly, the parameters will vary from one type of skin to another [38].

3.4 System Requirements

Much work has been done in the literature for ECG signal sensing and week signal sensing like touch screen systems. However, most techniques were working around enhancing the CMRR of the Instrumentation Amplifier (IA) [38]. This is mainly because most of the sensitivity loss for the sensor is due to common-mode interference. Consequently, several techniques were developed to overcome interference and amplify the signal to boost the Signal Noise Ratio (SNR) [38][40]. However, no work has been done to realize handheld ECG sensors with extremely low power. Here is the list of major challenges that exist in the literature.

1: CMRR enhancement of IA in the high-frequency range where amplifier bandwidth cannot track the common-mode signal [38].

2: How to integrate large resistors or capacitors to bring the lower cut-off frequency of the feedback network. Unfortunately, large resistors occupy a lot of the impractical silicon area. Several people designed pseudo resistors to realize the area efficient MΩ range resistance but at the cost of linearity limitations. The resistance value is unpredictable with +/-40% PVT variation [39] because they have been exploiting the sub-threshold region-biased transistor. Also, mixed-signal implementation has been very popular these days. However, due to the digital nature, they have successfully got sub-Hz 3-dB bandwidths at the cost of the input sensitivity.

3: PVT variation of the Variable Gain Amplifier (VGA) gain is very high, hence, limiting the SNR of the signal sensed by the ADC. In the literature, 36% variation has been listed so far. Any reduction in this variation could lead to the optimal design of the ADC; therefore, there is no need to support the full range of input signal variation [40].

4: Most common preferable ADCs are either Successive Approximation (SAR) or Sigma-Delta ADC. They both are very power-consuming for above 10-b applications. In SAR,

the comparator occupies a significant area and consumes 35% of the full system power. Therefore, any reduction in the ADC power will significantly improve the state-of-the-art to a greater extent [41].

Table 3.1 shows the targeted system specifications for this thesis work. They were derived by considering the major challenges discussed above and taking into the effect of the power dissipation supported by the battery.

Table 3.1 System Level specification.

Parameter	Specifications
RMS input amplitude	1mV
Bandwidth (Programmable)	0.1-200Hz.
SNR	60dB
ENOB	>9.5bits
Distortion	<3%
Supply voltage	1.2V
Power consumption	<50μW
Input Impedance	>5MΩ
CMRR (Low Frequency)	>120dB
CMRR (High Frequency)	>65dB
Input referred Noise	6.5μV
Input Sensitivity (pk-pk)	3.2mV
Area	1mm*2mm
Technology	CMOS 45nm

3.5 IA Specifications

The purpose of the IA is to amplify the signal without adding significant noise while input is dominated by the common mode noise and dc offset resulting from the electrodes. Also, it must provide a high impedance to the electrodes. Otherwise, the signal will be dropped across the electrodes rather than at the IA input. Therefore, specifications were derived as follows. The minimum input signal at the IA is 1mV, and input-referred noise is 2. 9uV. So typical VGA gain would be in the range of 20dB in the worst corner, and ADC minimum acceptable signal would generally be 100mV [42].

$$IA_{gain} = \frac{Minimum\ Accetpable\ signal_{ADC}}{VGA_{gain}} * Input\ signal_{min} \tag{3.2}$$

From the above equation (3.2), we can deduce that the amplifier's closed-loop gain is 6 (15dB). Since the IA architectures are based on the feedback-based amplifier, the open-loop gain should maintain a minimum value to minimize the steady-state error in the step response. The feedback factor (β) to maintain the closed-loop gain of 6 would be 1/7. The steady-state error can be expressed as (3.3), where A_o It is the open-loop gain [43].

$$Error_{steadystate} = \frac{\frac{1}{\beta A_o}}{1+\frac{1}{\beta A_o}} \tag{3.3}$$

For 1% steady-state error, A_o It can be calculated as 76.4dB, which demands a two-stage opamp, with the first stage being a telescopic cascade opamp as the forward amplifier [43]. Noise Efficiency Factor (NEF) is one of the major merits of an IA, which compares the power consumption for a given thermal noise to a single BJT device without considering any flicker noise. NEF is defined as (3.4), where $S_{u,in}$ is the input-referred noise, and I_{bias} Is the bias current. As it indicates, lower bias current and input referred noise results in better (lower) NEF, means the IA/VGA design is power efficient for a given noise budget. Intuitively NEF compares the noise of a given design with single BJT noise. The state of art achieved number is ≈4.3 and the goal of the present research

work is improving this further down. Also NEF helps in comparing two different designs. Two different design can be compared with NEF number and can be quantified which has better noise without requiring all the characterization data. In this research work, NEF is planning to improve by decreasing the noise by exploring the new circuit design techniques without increasing the power. Table 3.2 shows the derived/target specification of the IA.

$$NEF = \sqrt{S_{u,in}\Delta f \frac{2I_{bias}}{\pi V_T.4KT.\Delta f}} \tag{3.4}$$

$$NEF = \sqrt{\frac{2}{V_T}\frac{I_{bias}}{g_m}} \tag{3.5}$$

Table 3.2 IA specification.

Parameter	Specifications
Closed-loop-Gain	15dB
Open-Loop-Gain	76.4dB
NEF	3.9
Bandwidth	0.1-250Hz
Input referred noise	2.9μVrms
Power dissipation	10μW

3.6 VGA Specifications

The main purpose of the VGA is to attenuate/amplify the IA output so that ADC input will experience constant input voltage [44]. Without VGA, if the input signal amplitude is very high, then ADC will saturate; hence VGA needs to attenuate the signal. On the other hand, if the input signal amplitude is very small, then ADC will experience low SNR; hence the VGA must amplify the signal. The targeted input signal range is 25mV to 200mV, and ADC input needs 100mV. Therefore, the required VGA gain range varies from -6dB to 12dB; hence the overall input-referred noise can be expressed as (3.6). Hence the second term of equation (3.6) shows that the IA gain will suppress the VGA noise; here IA gain is 6 (equation (3.2)). Hence the VGA noise will be reduced by 36 times, so we are not considering very hard specifications here. To keep the noise below the noise floor,10nV/sqrt (Hz) will be the maximum allowed noise.

$$v_n^2 = V_{n,IA}^2 + \frac{V_{n,VGA}^2}{A_{IA}^2} + \frac{V_{n,ADC}^2}{A_{IA}^2 A_{VGA}^2} \tag{3.6}$$

Table 3.3 VGA specification.

Parameter	Specifications
Gain Range	-6 to 12dB
Linearity (THD)	3.5%
Power dissipation	3.9μW
Bandwidth	0.1-300Hz
Input referred noise	2.9μVrms

The overall bandwidth of the sensor is approximately dependent on the low bandwidth block in the signal chain. To be precious, it is expressed as follows.

$$\frac{1}{BW^2} = \frac{1}{BW_{IA}^2} + \frac{1}{BW_{VGA}^2} + \frac{1}{BW_{ADC}^2} \tag{3.7}$$

In the above equation (3.7), the BW represents the equivalent small signal bandwidth of the sensor, whereas the rest of the terms represent the bandwidth of the individual

blocks, IA, VGA, and ADC, respectively. From this expression one can understand that overall BW of the systems approximately equals to the lower BW cell in the system, means if VGA is slower than IA, ADC then overall BW of system is equal to VGA BW, so optimization has to be done to improve the BW of the low speed block. Also other blocks BW should be higher than lower BW blocks.

The distortion performance of an amplifier is a critical parameter as it represents how efficiently an amplifier can produce the output without adding other frequency components apart from input. Linearity can be quantified by using THD parameter, which compares the power of the unwanted harmonic components to fundamental signal component power, hence lower THD means better the distortion performance. In this work, a target THD of <5% has been used for the 10-b ADC.

In this work, the IA bandwidth is small compared to other blocks (VGA, ADC); therefore, it can be assumed that this bandwidth dominates the overall system bandwidth; hence, $BW \approx IA_{BW}$. The VGA power consumption does not need to be very high as power dissipation always trades with the noise, and VGA is not a noise-limited block [44].

3.7 Bandgap Specifications.

The purpose of the bandgap reference (BGR) is to provide a temperature-stable reference voltage/current to the rest of the chip. This is very important, especially when there is an ADC. The ppm/^{0}C accuracy of the reference affects the ADC performance over the full sweep of the temperature. For example, 10-Bit ADC with a 1V reference supply requires 0.5LSB of 31μV over the industrial temperature range (-40 to 125^{0}C). If the error budget is split equally for the Quantization noise and temperature, then the required Temperature Coefficient (TC) of the reference generator would be around 0.89ppm/^{0}C. This requirement mandates an even better performance BGR. Also, as a side requirement, BGR will have to provide the current/voltage requirement of the chip (for example, to bias the opamps and current mirrors). The integrated thermal noise of the BGR dictates the output Signal to Noise Ratio (SNR). For 10-bit ADC, the SNR will be given by the following expression [45].

$$SNR = 6.02N + 1.76 \tag{3.8}$$

Equation (3.8) has been derived under the assumption of sinusoidal signal inputs and white Quantization noise (means frequency independent power Spectral Density). One can understand from this equation as follows. To improve the SNR of the ADC by 6dB, one has to redesign the ADC by one more bit (which will double to ADC power and area). Approximately in the present work most of the signals are high active sinusoidal signal so this equation will be very useful. Also in this work an overall SNR of 60dB has been targeted. The following table shows this work specification that would advance the state-of-the-art from the performance point of view.

Table 3.4 BGR specification.

Parameters	Specification
Supply Voltage	1V
Noise	1.2μV
Accuracy (Pre-Trimming)	1%
PVT variation	0.5%
Current consumption	11.2 μ
Temperature Coefficient	64ppm/^{0}C
PSRR (Low Frequency)	-80dB
PSRR (High Frequency)	-16dB
Area	0.0288mm^2

3.7.1 ADC Specifications

ADC senses the amplified signal from the VGA and digitizes it with the required resolution (10-b) without losing accuracy, which means that the digital output represents the continuous time input signal within the signal bandwidth. For the present bio-medical application, the 10b resolution would suffice as the required SNR is approximately 55dB. Therefore, a 10b ADC would ideally give 62dB SNR; hence 7dB is the margin for unaccounted errors like supply noise and thermally generated noise [46] [47]. Therefore, SNR will be expressed as the following equation. Where Δ is the Least Significant Bit (LSB) size, A is the signal amplitude, and C is the sampling capacitance.

$$\boldsymbol{SNR} = \frac{\frac{\boldsymbol{A^2}}{\boldsymbol{2}}}{\frac{\boldsymbol{\Delta^2}}{\boldsymbol{12}}+\frac{\boldsymbol{KT}}{\boldsymbol{C}}} \tag{3.9}$$

Except for flash ADC, every other architecture relay on the clocking as sampling the signal would be mandatory to avoid the aliasing of the under-sampled tones. One major challenge with the ADC is power dissipation and area [48]. Power dissipation dictates the conversion speed and accuracy. Fortunately, speed is very low here (max 10ks/s); hence, fewer architectures would meet the system specifications. Most of the silicon area will be occupied by the sampling capacitors due to the matching and noise requirements. For 1V supply, the LSB is ≈97.65μV, and the sampling capacitor should be greater than

13.4pF. The power consumed per conversion must be minimized to enhance the battery lifetime. Typically, 17.3fJ/conversion would be the best based on the state-of-the-art given so far[48]. Integral Non-Linearity (INL) is defined as the difference between the actual and ideal ADC characteristics as expressed in equation (3.10), where V_D represents the ADC output, V_{zero} is the minimum input voltage and $V_{lsb-ideal}$ Represents the ideal output difference for the two adjacent codes. For example, INL is pictorially represented in figure:3.5. Here, ideal characteristics can be constructed by either the endpoint method or best-fit curve.

$$INL = \left|\frac{V_D - V_{Zero}}{V_{lsb-ideal}} - D\right| \tag{3.10}$$

Where $0 < \mathrm{D} < 2^N - 1$. INL mainly decides the non-linear distortion introduced by the ADC, which means the higher the INL (let us say 2lsb's), the higher the harmonic content in the o/p digital representation. Therefore, in applications like Audio and Video, INL less than 0.5lsb's are typical target specification [50] [51]. However, for the Biomedical application, this is not a very strict specification as linearity, and non-linearity distortion are not a big concern. Hence we are specifying ±2.5LSB to minimize the silicon area.

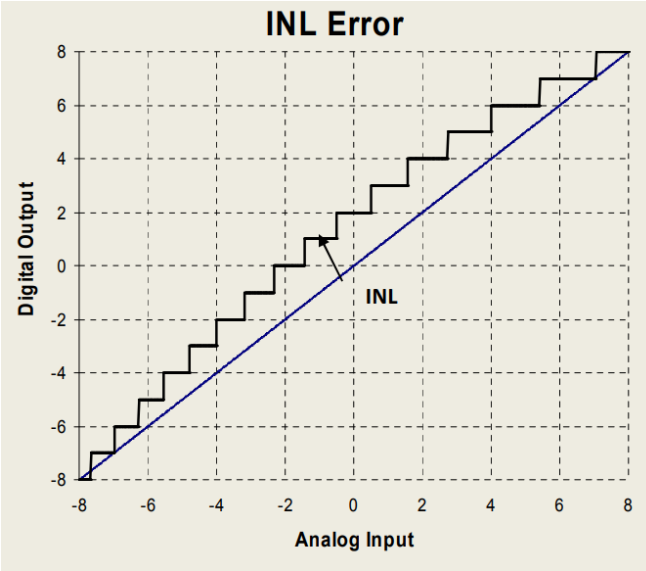

Figure 3.5 ADC INL representation [49]

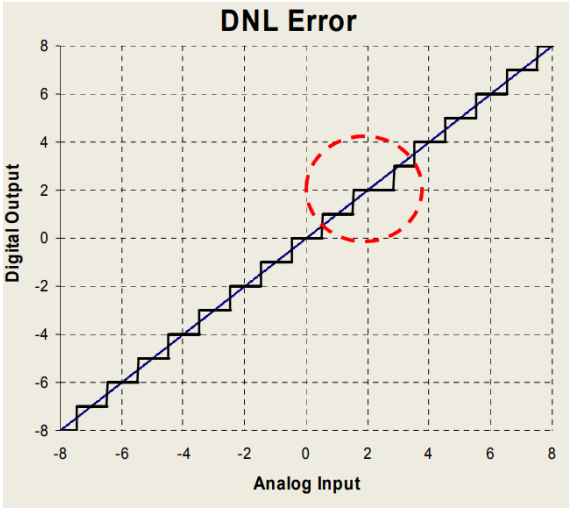

Figure 3.6 ADC DNL representation [49]

Differential Non-Linearity (DNL) is defined as the error between the actual step size and ideal LSB as shown in equation (3.11) and described in figure:3.6

$$DNL = \frac{V_o[N+1]-V_o[N]}{LSB} - 1 \tag{3.11}$$

DNL has to be less than 1LSB so that ADC characteristics are monotonic; hence any digital feedback loop around the sensor will work accurately without having any stability issues. Comparing the performance of the ADC, the Figure of Merit (FOM) has been proposed in [52], as given in equation 3.12. Table 3.5 depicts the specifications targeted in the present thesis work.

$$FOM = \frac{Power}{F_S 2^{ENOB}} \tag{3.12}$$

Table 3.5 ADC specification.

Parameters	Specification
Supply Voltage	1V
Resolution (bits)	10
Sampling Rate (ks/s)	10
SNDR (dB)	60
ENOB (bits)	9.5
DNL (LSB)	1.2
INL (LSB)	±2.5
Power Consumption (μW)	14.8
FOM (fJ/conv)	17.3

3.8 Summary

In this chapter, different important design specifications of the ECG sensor have been discussed and derived. The design aims to optimize the overall power consumption in the worst-case working condition (FF-Process corner and hot temperature) and less silicon area. This has been done by budgeting the power so that high-performance blocks like ADC and IA have been given high priority, and other blocks like VGA and Bandgap circuits have been biased at the lowest power. Apart from overall target specifications, each block's specifications were derived from several rules of thumb like SNR and Harmonic distortion.

The next chapter will discuss the proposed high accurate temperature-independent Bandgap reference.

3.9 References

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Chapter 4: Bandgap Reference design

4.1 Introduction

Bandgap reference is a key circuit in most analog systems because they all require stable reference voltage/current [53]. The temperature stability of the bandgap has a strong effect on the output performance of an ADC, a sensor, and a biomedical transceiver. In the literature, there has been much work done. However, most of the research work performed so far has been using BJT devices to generate the CTAT voltage, which occupies a significant silicon area and requires a special mask to fabricate them in a typical CMOS process. The generic CMOS process offers vertical parasitic BJT devices formed out of an n-well PMOS transistor [54]. These parasitic devices will have much less current gain (β) and unacceptable base resistance (R_b). In recent days pure CMOS-based circuits have been proposed [54][55]. They relied on the fact that the threshold voltage (V_{TH}) of an NMOS transistor has a negative temperature coefficient, and the difference between the V_{gs} of the two transistors has a PTAT nature, so combining these two will get the bandgap natured output. Unfortunately, they all underperform compared to the existing BJT-based proposals. The conclusion is that BJT-based circuits occupy very much silicon area, and MOS-based circuits occupy less silicon area and have poor performance. In this work, a mixed-mode circuit has been proposed that uses both BJT and MOS devices with acceptable performance (refer to table 3.5) while occupying a very small active silicon area.

4.2 Diode Characteristics

The diffusion current in a BJT is exponentially related to the applied voltage at the base-emitter junction, as expressed in equation 4.1. Thus, where I_D is the diode current, I_S is the reverse saturation current, V_{BE} is the base-emitter forward bias voltage, and V_T is the thermal voltage [54].

$$I_D = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right) \tag{4.1}$$

Also, equation (4.1) reveals that V_{BE} has a negative temperature coefficient, typically -2mV/^{0}C [55]. The temperature coefficient has a very weak dependency on the bias current and process variation. For a first-order approximation, it is negligible. Furthermore, it is independent of PVT variation due to the exponential V-I relation, whereas the MOS transistor will abide by the square law, which has much less slope. On the other hand, the reverse saturation current strongly depends on the temperature and is directly proportional to the area of the base region. As expressed in equation (4.2), where b is the proportionality factor, m is the temperature index of mobility, and E_G is the bandgap energy of the silicon [55].

$$I_S = bT^{4+m}exp^{\frac{-E_g}{KT}} \tag{4.2}$$

In this thesis work, the V_{BE} of BJT is used as the CTAT voltage with a single-finger transistor compared to a 48-finger device in the conventional circuit [55]. Figure 4.1 shows the voltage-current characteristics of the diode for different temperatures. The top trace corresponds to -40^{0}C, and the bottom curve corresponds to 125^{0}C. This shows that bandgap circuits require high voltage at low temperatures, or the minimum voltage of the circuit is limited by the minimum temperature of interest.

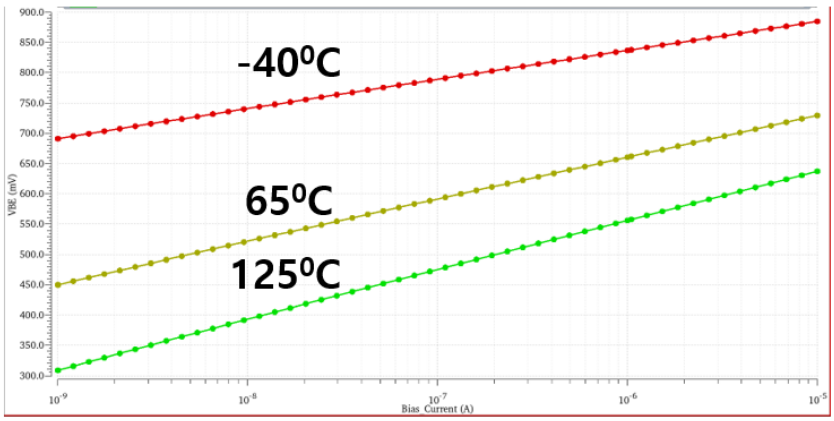

Figure 4.1 Diode Voltage-Current Characteristics

4.3 PTAT Generation

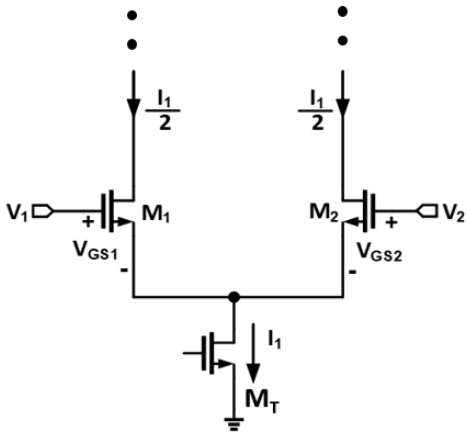

Figure 4.2 PTAT generation concept

Figure 4.2 shows the proposed PTAT generation technique. It is a differential pair with different transistor sizes for M_1 and M_2. Assume bias voltages V_1 and V_2 will be generated by a self-bias circuit, which will ensure minimum current through the tail current source (I_1). The V_{GS} of the MOS transistor and delta of the V_{gs} of M_1 and M_2 can be expressed in equations (4.3) & (4.4). Where η is the subthreshold slope factor, V_T is the thermal energy and I_0 is the sub-threshold current [55]. Both equations are valid only if the transistors are biased in a strong inversion region, meaning $V_{ds}>>4V_T$.

$$V_{GS} = V_{th} + \eta V_T \ln\left(\frac{I_d}{\frac{W}{L} I_0}\right) \tag{4.3}$$

$$V_{GS1} - V_{GS2} = \eta V_T \ln\left[\left(\frac{W}{L}\right)_1 / \left(\frac{W}{L}\right)_2\right] \tag{4.4}$$

Equation (4.3) describes a first-order approximation, whereas equation (4.4) shows that delta V_{GS} will increase with temperature; hence it can be exploited as a PTAT voltage, provided the subthreshold factor is not changing with the temperature. Equation (4.4) is very similar to a PTAT voltage generated by BJT without using an expensive process [56]. Furthermore, the BJT version has several errors related to the current gain, whereas MOS-based circuits have fewer errors [56]. In the proposed circuit shown in fig:4.2, the challenge is the need to generate the input voltage of the differential pair with a known

offset. Any PVT variation in the input voltage will directly affect the BGR o/p voltage accuracy. Figure 4.3 shows the simulated PTAT voltage, which is 42mV at -40^{0}C and 74mV at 125^{0}C. The slope is approximately +193µV/^{0}C, and the slope is independent of the temperature. This is another major advantage of the proposed PTAT method because its slope is almost six times higher than the conventional BJT version; hence less gain is required for the final output generation [57]. Due to the lower BGR gain, the opamp non-idealities like offset and noise will be amplified with a small conversion factor. The next section will describe how the PTAT and CTAT voltage was summed up to get the BGR voltage.

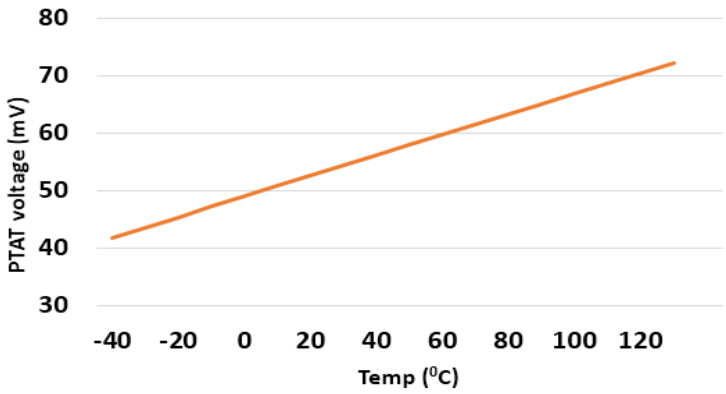

Figure 4.3 Simulated PTAT voltage wrt Temperature

4.4 Proposed Method

The following circuit synthesis methodology will help us to come up with the final proposed circuit. To generate the zero-temperature coefficient output of the bandgap, one needs to generate the PTAT and CTAT voltages, and there must be a way to add both in a controllable scaled summation independent of the PVT corners and circuit non-idealities. In the previous section, the PTAT generation was explained in a detailed manner. The V_{BE} of the BJT can be used as the CTAT voltage [58]. Now the question is how to add them, one option is in the form of the differential pair, and another is a simple diode-connected PMOS device. Figure 4.4 shows the proposed mixed-mode circuit bandgap reference. Transistors M_1, M_2, M_3, M_4, and M_5 form the PTAT generation loop, and the potential difference between nodes x and y represents the PTAT voltage. The biasing transistor M_7 and the potential divider R_1 and R_2 convert the PTAT voltage into the current. M_3, M_4 currents are same due to the differential amplifier nature and M_7 current also same as M_3 because it is driven by differential pair output. The current mirror formed by $M_{5\text{-}7}$ will inject current into M_6 so that they will have same current. $M_{6\text{-}T}$ forms a current mirror so the current in all branches are same, this is called self-bias nature as every transistor current has been forced to same and insensitive to mismatch. The same PTAT current has been used to bias the Q_3 PNP device such that node z potential has a CTAT nature [59]. One important point to note here is that BJT current can be anything, not necessarily PTAT, but the curvature nature of the V_{BE} will have a minimal deviation from the ideal curve for PAT nature. Therefore, the value of m in equation (4.2) will be 1 for this kind of circuit configuration. Resistor R_3 senses the PTAT voltage at node X and CTAT voltage at node Z, and it generates current proportional to V_{BE3}.

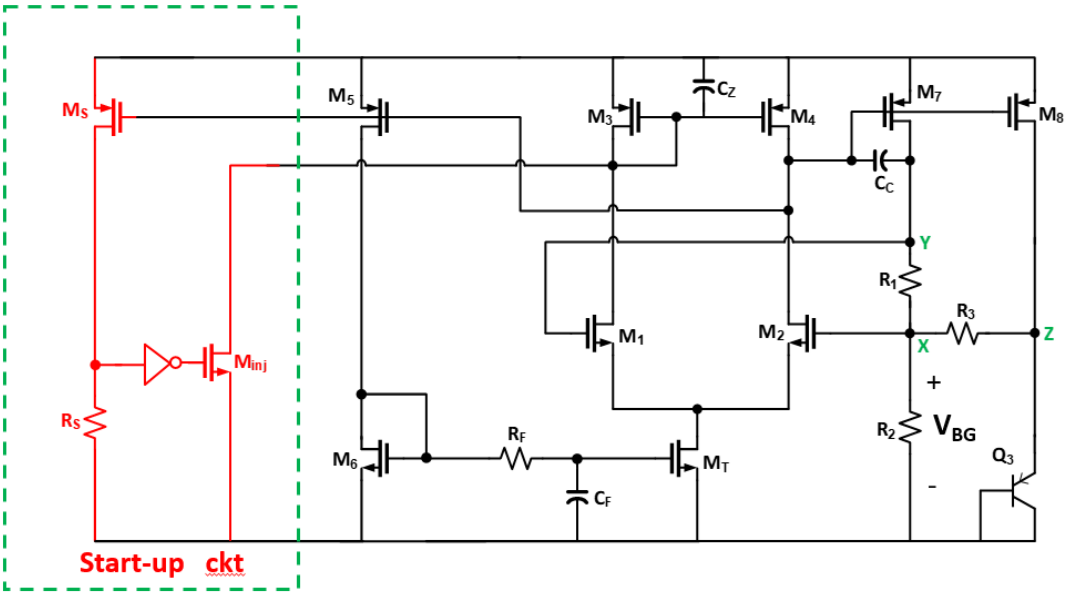

Figure 4.4 A proposed bandgap reference schematic

The output voltage of the BGR at node z can be expressed as follows (4.5 and 4.6).

$$V_{BG} = V_{BE}\frac{R_2}{R_1+R_2} + \frac{V_{PTAT}}{R_1}\frac{R_2R_3}{R_2+R_3} \tag{4.5}$$

$$V_{BG} = V_{BE}\frac{R_2}{R_1+R_2} + \frac{\eta V_T \ln\beta}{R_1}\frac{R_2R_3}{R_2+R_3} \tag{4.6}$$

Where β is the aspect ratio of M_1 to M_2, from the simulation, the temperature coefficient of CTAT (V_{BE}) is -1.6mV/^{0}C, and PTAT is 0.087mV/^{0}C. So to find the relation for getting a minimum temp coefficient for the o/p voltage, its derivative wrt to temperature should be zero.

$$\frac{\partial V_{BG}}{\partial T} = \frac{\partial V_{BE}}{\partial T}\frac{R_2}{R_3+R_2} + \frac{\partial V_T}{\partial T}\frac{\eta \ln\beta}{R_1}\frac{R_2R_3}{R_2+R_3} = 0 \tag{4.7}$$

Let us assume R_3=2R_2 for simplicity and $\beta = 8$ for the matching comfort in the layout. Equation (4.7) can be simplified as follows.

$$\frac{\partial V_{BG}}{\partial T} = \frac{\partial V_{BE}}{\partial T}\frac{1}{3} + \frac{\partial V_T}{\partial T}\frac{2\ln\beta}{3}\frac{R_2}{R_1} = 0 \tag{4.8}$$

For the minimal temperature coefficient, the R_2/R_1 ratio can be calculated as 4.59. Therefore, this circuit can result in the sub-1V, like the Bamba bandgap reference [55]. Equation (4.6) shows that any voltage can be obtained by varying the R_3/R_1 ratio without

restricting it to 1.2V, like in conventional architecture. This work targeted 525mV nominal voltage with a 2.5% variation budget for the Process and voltage corners and 0.5% for the temperature. These will be explained clearly in the simulation results section. The main advantage of the proposed circuit is that it does not have non-idealities resulting from the BJT parasitic effects like base width modulation and kirk effect [55]. Also, this circuit of Figure 4.4 has fewer bias current branches, hence less thermal noise and lower power consumption, which enables its applications in the Internet of Things (IoT) and biomedical circuits.

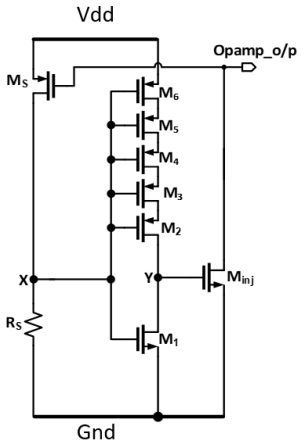

Figure 4.5 Start-up circuit used in the bandgap reference.

Like any self-bias circuit, the proposed circuit also needs a start-up circuit, which will provide the kick-pulse to the opamp output when the circuit is stuck at zero current – an unwanted operating point. Figure 4.5 shows the start-up circuit that replaces the start-up section of Figure 4.4. This start-up circuit of Figure 4.5 is used in this thesis work. Transistor M_S senses the bandgap current and pumps it into the large resistance R_s. Hence, if the current is zero in the main bandgap, the voltage across R_S will be zero. M_1 to M_5 transistors form the skewed inverter, which senses the zero input voltage at node-x and injects start-up current into the opamp o/p through the M_{inj} NMOS transistor. So resistor (R_S) main role is to sense zero current mode of the circuit and activate the BGR start-up circuit. Without RS, there is no guarantee of the BGR functionality and results in

circuit failure in the real time operation. When the bandgap output reaches the expected voltage, the inverter should switch off the M_{inj} transistor; hence it will not disrupt the actual bandgap operation. In some extreme PVT corners, several undesired operating points may exist, so the number of operating points needs to be found in every design, and the start-up circuit must be able to recover from any such point, and one must make sure the bandgap output voltage will recover to the desired target voltage [60]. A unique simulation methodology has been used in this, which will be discussed in the design methodology section.

4.5 Design Methodology

In this section, the design techniques used for the proposed circuit will be described, mainly how to design the circuit so that the optimal operating point will be achieved and how to minimize the temperature coefficient.

4.5.1 Operating point design.

The design of the bandgap starts with how to select PTAT voltage. From equation (4.3), the ratio of M_1 and M_2 will decide the PTAT voltage. For the layout simplicity, the ratio chosen was 8, which resulted in 54.7mV PTAT voltage at 65^0C. The temperature coefficient of the PTAT can be calculated as 250μV/^{0}C. The CTAT temperature coefficient can be calculated from the diode VI characteristics, which are approximately estimated as 1.94mV/^{0}C. In the entire design, the g_m/I ratio of the transistors is adjusted as15 when the offset voltage is critical. For example, in the differential pairs and voltage sensing section (M_1, M_2 in this design), seven have been used for the current mirror sections to minimise the noise and mismatch-induced current error (M_5, M_6, M_7 in this design). The closed-loop bandgap-gain or scaling factor is ≈ 7.98. The offset of the main differential pair is amplified with 7.98 gain and appears in the final output; hence M_1 and M_2 sizes were optimised to minimise its random offset.

Table 4.1 Component values [63].

Component name	Value	Component name	Value
M_1/M_2	8.4u/0.32u	R_1	12.78KΩ
M_3/M_4	6.8u/0.32u	R_2	42.34KΩ
M_6/M_T	9.6u/0.32u	R_3	19.23KΩ
M_5/M_7	19.2u/0.32u	R_5	37.98KΩ
M_8	16.8u/0.32u	C_5	32.5pF
M_S	4.2u/0.32u	C_Z	54.3pF
M_{INJ}	2.1u/0.32u	C_C	26.3pF

The random offset parameters of the transistors were given by the following pilgrim's equations [59] 4.7a and 4.7b. Where W and L represent the width and length of the differential pair devices and A_β, A_{VT} are statistical Monte-Carlo parameters from the foundry.

$$\frac{^{\delta}\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}} \tag{4.7a}$$

$$^{\delta}{}_{VT} = \frac{A_{VT}}{\sqrt{WL}} \tag{4.7b}$$

The target output voltage will be around 525mV, with the bias filter formed R_F, C_F will reduce the noise resulting from the self-bias loop. Its 3-dB bandwidth is 15KHz. From the design equations and available area point of view, all other component values were calculated and given in table 4.1.

4.5.2 Frequency Compensation.

Every feedback loop needs to compensate for a better-closed loop step response. For optimal performance, loop dynamics like pole-zero locations and unity-gain bandwidth needs to be evaluated accurately. In the proposed circuit, the two dominant poles correspond to nodes Y and Z. Also, there is a high-frequency pole-zero doublet due to the C_Z parasitic capacitance. For the system to be stable, it should have 20dB/dec roll-off at unity gain bandwidth, meaning the second dominant pole must be shifted to a higher frequency using lag compensation or miller compensation. Lag compensation achieves unconditional stability while decreasing the closed-loop bandwidth, whereas the miller technique improves the bandwidth with a small compensation capacitor at the cost of poor PSRR at the output. Miller compensation has been adopted to achieve a small form factor [61]. The loop-gain and pole-zero locations can be expressed as equations (4.8 to 4.10).

$$Loopgain = \frac{g_{m1}}{g_{ds1}+g_{ds4}} g_{m7} \left(R_1 + \frac{R_2 R_3}{R_2+R_3}\right) \tag{4.8}$$

$$Dominate\ Pole = \frac{g_{m1}}{C_1+C_c\left(1+\frac{g_{m7}}{g_{ds1}+g_1+g_2}\right)} \tag{4.9}$$

$$non-Dominate\ Pole = \frac{g_{m7}+g_2+g_1}{C_L+\frac{C_c C_1}{C_c+C_1}} \tag{4.10}$$

Figure 4.6 depicts the simulated Gain-Margin (GM) and Phase-Margin (PM) through cadence stability analysis [62]. First, the frequency response was plotted, and these two parameters were derived from that. From the plot, PM is always above $60^{0,}$ and GM is always 12dB.

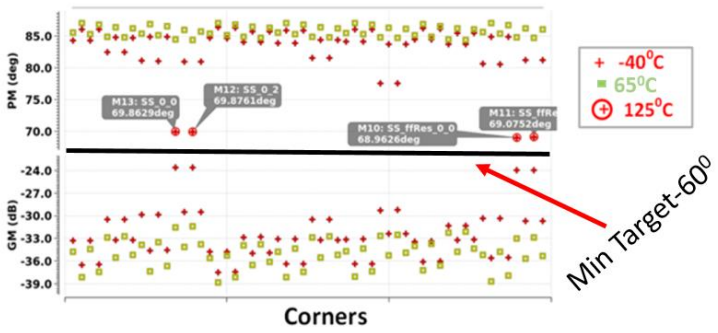

Figure 4.6 Phase and Gain margin across PVT corners.

4.5.3 Power Supply Rejection Ratio (PSRR).

Supply noise finds its way to the output of the single-ended circuit due to the limited bandwidth. Therefore, the impact of the supply can be defined as PSRR, which is expressed in equation (4.11).

$$PSRR = \frac{Output\ voltage}{Supply\ Noise} * \frac{1}{Amplifier\ gain} \tag{4.11}$$

Accuracy-intensive circuits do require a proper PSRR across the frequency band of interest. At very low frequencies, all the feedback loops will have a higher gain (50dB). Hence the low-frequency PSRR is usually not a concern. However, due to the limited bandwidth of the circuit, beyond the 3-dB bandwidth frequency, the PSRR starts to degrade. This can be viewed as the zero in the transfer function. The transfer function of the PSRR can be expressed as (4.12), where g_m and g_{ds} are related to the transistor small-signal parameters and Z, P_1, and P_2 are the zero and dominant poles of the proposed BGR [63]. Figure 4.7 shows the frequency response of the equation (4.12). This can be understood as follows:

$$PSRR = \frac{1}{\frac{g_{m1}}{g_{ds1}+g_{ds4}} g_{m7}\left(R_1+\frac{R_2R_3}{R_2+R_3}\right)} \frac{\left(1+\frac{S}{Z}\right)}{\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_2}\right)} \tag{4.12}$$

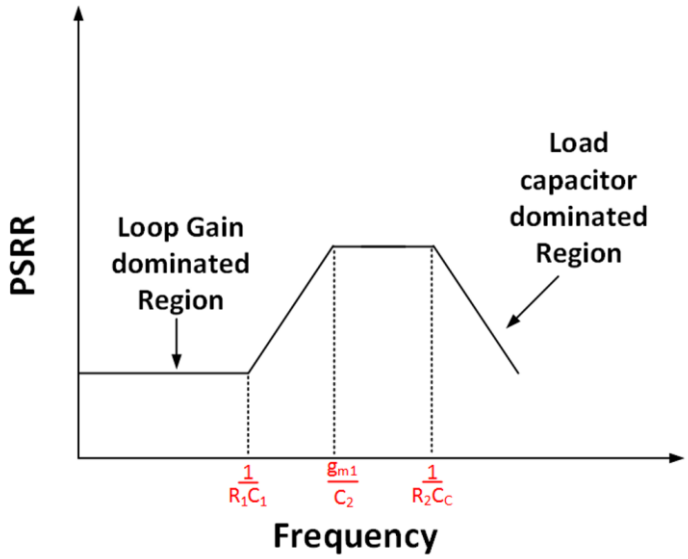

Figure 4.7 PSRR plot from the small-signal model.

A superior PSRR can be achieved at a very low frequency because of the loop gain and lower loop dynamics. However, as soon as the frequency is higher than the first dominant pole, the PSRR degrades because op-amps cannot track the power supply, and it will not replicate the supply noise at the gate of all PMOS current sources. Near the unity gain frequency (g_{m1}/C_2), the PSRR reaches the minimum value and is limited by the o/p impedance of the current sources. This minimum value is the major concern in all the highly sensitive designs, as this can be as low as -10dB and means 33% of the supply noise at this frequency will corrupt the output. Several techniques have been proposed in the literature [56] [60] to improve this value [64]. One popular technique injects a small amount of the supply noise through a high-pass filter, improving results by 6-7dB. Unfortunately, poor device modelling and supply distribution network will limit the improvements in the results. For the present work, I achieved 15.6dB without exploiting any of these techniques apart from increasing the bandwidth and self-biasing the opamp. Beyond this frequency, the load capacitance will further decrease the output impedance and improve the PSRR. The above plot is a model plot, but accurate simulation results have been given across PVT in the simulation results section.

4.5.4 Start-up circuit simulation.

The bandgap start-up circuit must be evaluated carefully to find all hidden zero-current operating points. [63][64] Several people exploited using voltage ramp slope techniques or relying on the leakage current to avoid the little current consumption, but these are proven unsafe for the high-yield silicon production industry. The wish list of a successful start-up circuit is as follows.

1. It must draw a negligible current when the BGR has reached the desired output and pumps more current when it is stuck to zero.

2. It should start on its own at a very cold temperature (-400C).

3. The circuit should not consider the leakage current as the actual current. Hence the bias current should be much greater than the worst-case leakage current at high temperature (125^0C). It is important to note that the leakage current exponentially increases with the temperature.

4. Start-up circuit operation should be independent of any transient glitches happening on the low impedance nodes like supply voltage or reference voltages.

5. The final point is that it should switch off quickly when the bandgap reaches its final operating point. Any residue leakage current will impact the bandgap temperature sensitivity.

In this work, I used a static start-up circuit in [55]. Even though designing these circuits is not very challenging, verification would be very challenging. The main issue is that it is difficult to rely on the transient simulation due to the accuracy limitations. Therefore, I uniquely simulated the start-up in this work, which will catch all the undesired operating points in the DC sweep simulation. I introduced a voltage source at the output of the op-amp (M_4 transistor gate terminal in the schematic), and it has been swept from zero to the maximum voltage (V_{DD}). For a given circuit condition, this circuit will have a specific

output voltage at this node, and if the voltage happens to be that exact voltage, then the voltage source will supply zero current. This is a unique way to find the operating point. For all the other battery voltages, it will supply/sync a high amount of current since the battery and opamp will fight to force that node voltage. Hence, if the current through the voltage source has one zero ampere cross point, it means it has only one operation, which is a sign of a successful and reliable start-up circuit. Figure 4.8 shows the simulation results corresponding to the Fast process corner, high temperature, and Monte-Carlo mismatch condition. This shows the current through the voltage source, which swept its value from 0 to 1V [65].

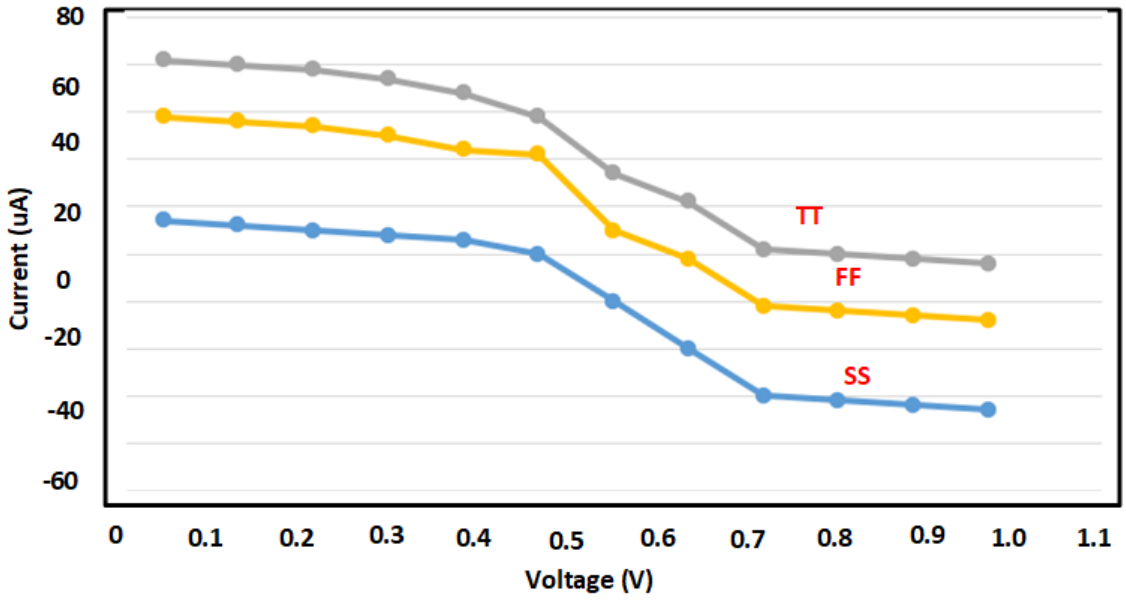

Figure 4.8 The operating point of the bandgap reference circuit.

It clearly shows that around 0.5V, the voltage source current crosses zero, and this has only one unique crossing point. Beyond 0.5V, either current is the +ve or –ve current; hence, the voltage source and battery are trying to force that node. Near the zero crossings, the plot was zoomed in and shown in an inset. The total current consumption of the start-up circuit is 600pA in the worst corner. Sometimes it is good practice to add a digital control to kick start or switch off this circuit if this does not work, but this is SPI control. Hence I have not considered adding this to the present work.

4.5.5 Layout Design techniques.

Layout/Mask design defines the analog circuit's fabrication guidelines and how accurately the devices will be fabricated. The layout of the transistor indicates the clear top view, and several layers were included. Figure 4.9(a) shows the layout of a single-finger transistor. The vertical blue line indicates the polysilicon gate (aka POLY) to form the channel and enables the charge flow from drain to source. The green rectangles on both sides of the poly show the diffusion regions of the transistors (aka OD). These are used to form the drain and source regions of the transistor. The width and length of the transistor can be defined as shown in Figure 4.9(a). The other transistor parameters, like oxide thickness and diffusion width, cannot be shown in the layout. Hence it cannot be a design parameter [66].

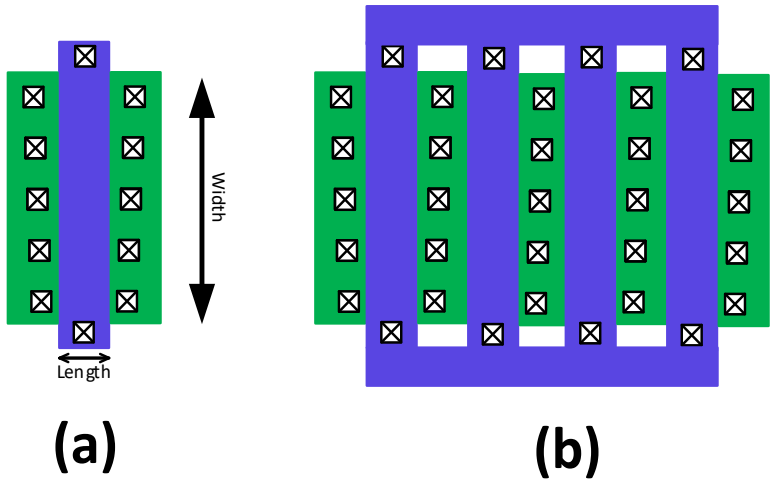

Figure 4.9 MOS transistor layout (a) Single finger (b) Multi-finger [58]

Beyond these two layers, there will be metal to connect the transistor with another component. They are several metal stacks. In this CMOS technology, 13 metals were defined as M_1 to M_{13}. The connection between the several metals can be made with VIA. For example, M_1 and M_2 can be joined by VIA-1. Transistor POLY and OD are connected to M_1 metal through contacts (shown as a rectangular cross in the above picture). Often multi-finger transistors are required, especially while carrying higher current and to minimize the capacitance at the drain and source and to minimize the area. Instead of

connecting two single-finger devices, a multi-finger was used mainly with shared drain and sources, as shown in Figure 4.9(b), where all poly gate terminals have been connected. Here the gate can be connected only on one or on both sides. On both sides, the connection will decrease the gate resistance hence less thermal noise due to the gate, but this adds significant coupling capacitance due to the additional connection. A good analog layout is required to minimize the random offset resulting from the circuit. Here are the common practices for the bandgap reference.

1. All matched transistors should have identical surroundings. So, for example, if one transistor has metal on the left side, then I need to keep explicitly similar kinds of metal in the right direction to protect the symmetry.

2. All matched transistors should have identical current directions.

3. Current mirror devices should match very accurately. A special technique called inter-digitization is popular, as shown in figure:4.10. If two transistors, M1 and M2, are intended to match in aspects, they must be arranged in the patterns like M_1, M_2, M_2, M_1, M_1, M_2, M_2, M_1 such that the linear process mismatch gradient will cancel for the first order. Unfortunately, this style will not cancel any other profile mismatches. This can be exploited mainly for the current mirrors and degenerated transistors.

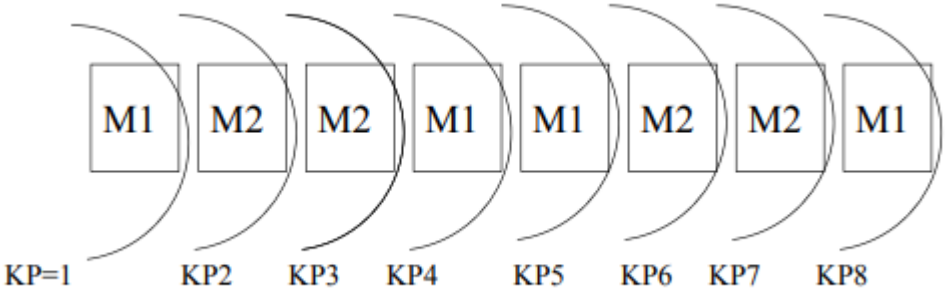

Figure 4.10 Inter-digitization Layout model for current mirrors.

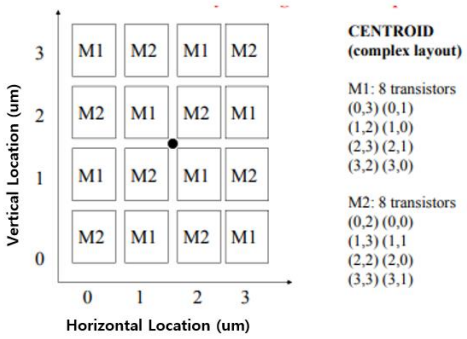

Figure 4.11 Common-Centroid Layout model for differential pairs.

4. For differential pairs, the common-centroid-based layout style is popular to cancel the offset resulting from both transistors. Figure 4.11 depicts the model picture for this style. The centroid of both devices should be at the same point; hence higher-order mismatch profiles can be cancelled. In this picture, the M_1 centroid is at (2,2). Also, the orientation of M_2 is adjusted such that it also has a centroid at (2,2). In this fashion, both devices' multipliers should be an integer multiple of 4; otherwise, it is impossible to have proper cancellation. Unfortunately, this technique will add a significant amount of capacitance at the input of the differential pair terminals due to the complicated routing network, which will also add significant couplings to the nearby high-frequency clocks and sensitive nets. Fortunately, in this work, the added capacitance is not a performance issue because the targeted bandwidths are far from the intrinsic bandwidth of the technology [67]. With this style of layout, multi-dimensional mismatch profile can also be cancelled and offset of the differential pair can be minimized.

5. In recent technologies (less than 90nm), the LOD effect has come into the picture. While fabricating the devices, Darin and source diffusion regions experience different mechanical pressures. The direction and magnitude of the pressure affect the mobility of the majority of charge carriers in the transistor. Hence, current also is a function of the stress as given in equation 4.13. Where μ_n represents the carrier

mobility, C_{ox} Represents the oxide capacitance per unit area, and Vth represents the threshold voltage of the Transistor.

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 (1 + \alpha V_{DS}) \quad (4.13)$$

To match two transistors against the LOD effect, each device should not have shared diffusion regions; hence in this work, I have used explicitly unshared devices for all the opamps input devices. Due to this effect, the BSIM models added extra parameters in the current equation (4.13), called S_A, S_B, and S_C, which mainly capture the length of each diffusion from the gate edge[68].

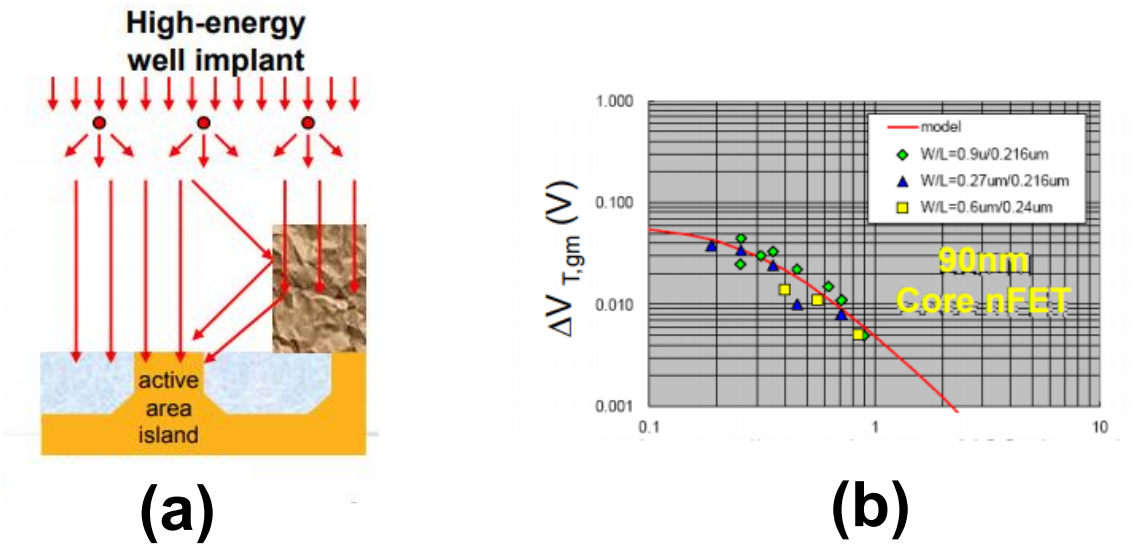

Figure 4.12 (a) Well proximity effect (b) Delta Vth versus distance between the devices and n-well edge.

6. Deep N-well nearby any critical NMOS need to be avoided because during implanting the N-well (to minimize the resistance), high energy particles will be bombarded from the implanting gun, which can scatter a lot and find their way into the nearby NMOS transistor. Figure 4.12(a) shows how energy particles impact the NMOS. Extra implants in the NMOS channel will affect its threshold voltage, and sometimes transconductance will be degraded. Figure 4.12(b) shows the effect of the N-well distance on the Vth, which shows that increasing

the distance will decrease the threshold voltage deviation from the actual value. The best way to avoid this effect is to maintain a constant distance between the nmos and N-well (1.6um in this work); hence all nmos devices Vth will affect in the same manner. For many applications, we are not concerned about the deviation of the V_{TH} as long they all have a similar mismatch.

7. The proposed bandgap reference schematic's layout was designed with all the above guidelines, as shown in Figure 4.13.

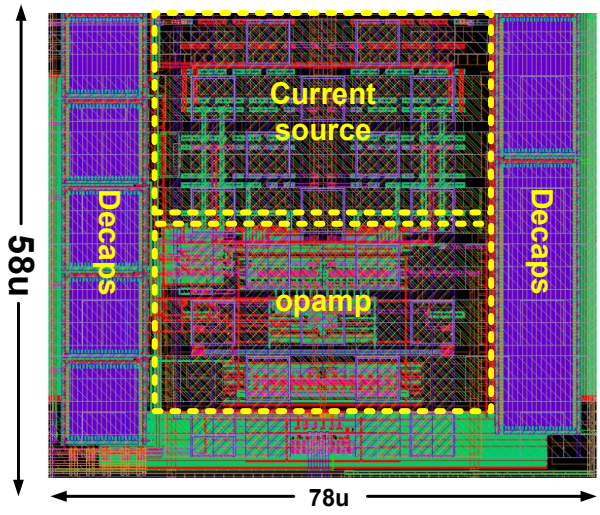

Figure 4.13 The layout of the proposed circuit

4.6 Simulation Results

The targeted bandgap reference was designed in 45nm CMOS technology, consisting of 11 metals, including the Redistribution Layer (RDL) and Metal Insulator Metal (MIM) capacitors. In this process, silicide resistors with a sheet resistance value of 800Ω are available, especially for the BGR kind of circuit. There is a strong need for high-density resistors as they will decide the overall area and performance of the circuit.

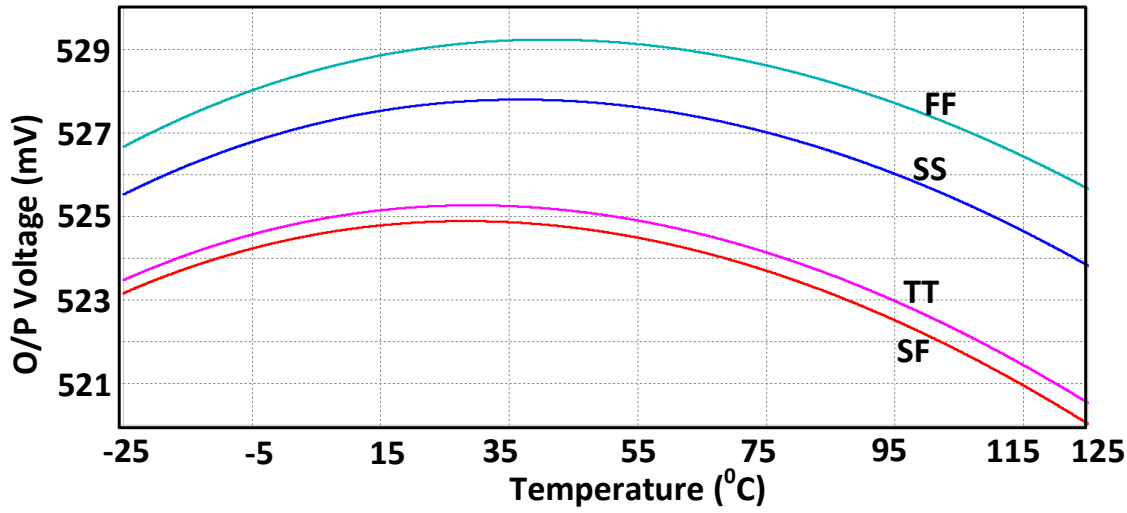

Figure 4.14 Output voltage versus Temperature.

Figure 4.14 depicts the DC performance of the BGR while the temperature is swept over the industrial temperature range of -40-125^{0}C. The targeted output voltage is 525mV in typical process and room temperature conditions [63]. The plot shows that the output voltage varies by 8.1mV across different process corners. In the SF corner, the output has been degraded to 520.8mV at high temperatures. This is because the opamp offset has been increased to 3.4mV compared to the 1.8mV in the typical process. Several design techniques have been used to minimise the opamp offset drift, like self-bias opamp to track its bias current nature similar to the BGR core current and increasing the opamp input device sizes to reach the higher gm/id ratio of value 16. As a result, the Parts per million performance parameter can be expressed as follows in equation (4.14) [69].

$$PPM_{output} = 2\frac{V_{0,max}-V_{0,min}}{V_{0,max}+V_{0,min}}\frac{10^6}{165} \quad (4.14)$$

The calculated PPM is 12.4 ppm/^{0}C, which is far better than the state-of-the-art. The noise of the BGR is another important specification, as it will dictate the SNR of the output ADC. Typically, the integrated noise performance should be less than half of the LSB of the ADC so that SNR will be limited by the ADC rather than the BGR. Figure 4.15 shows the simulated noise PSD, with -150dB at 100Hz and mostly dominated by the MOS current sources' opamp flicker noise and thermal noise. The integrated noise over the interested frequency band is 89.45μV.

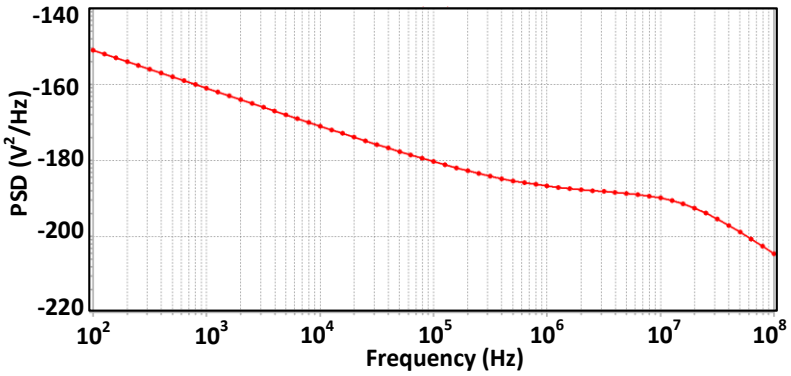

Figure 4.15 Simulated noise spectral density.

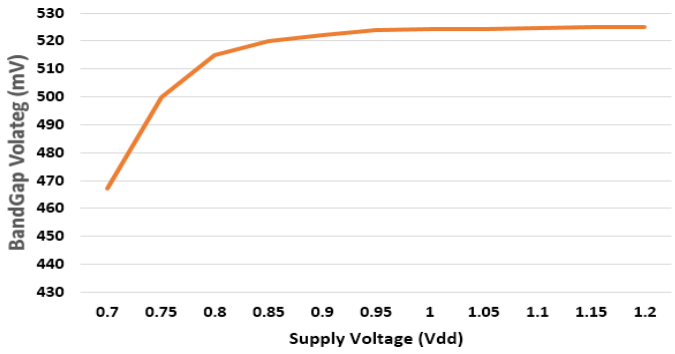

Figure 4.16 Simulated output supply sensitivity.

The BGR output should be ideally independent of the supply voltage so that any minor variation in the battery would create less disturbance to the overall system. Figure 4.16 shows a simulated supply sensitivity of the output means how much variation in the output for a given supply drift. It reveals that from 1.2V to 0.8V supply change, only

7.9mV change in the overall output; hence it has 19mV sensitivity per volt of the supply voltage. Any supply voltage less than 850mV, the circuit shows significant output deviation because the opamp has limited headroom [55]. Hence this circuit does not work below this supply. BGR has negative feedback, so stability is crucial for a healthy time domain response. The metrics to assess the stability are phase margin (PM) and Gain margin (GM). Having PM>60^0 and GM>12dB is a good sign of stability without ringing. Figure 4.17 shows the simulated bode plot of the open-loop response of the BGR with the help of the cadence STB simulation method. It reveals that the DC gain of the loop varies from 57-73.5dB and the phase margin is 69.2^0 in the worst-case PVT corner. The unity-gain bandwidth of the loop varies from 21-29.6MHz. The best way to assess the stability is a time domain step response, though the frequency domain is easy to design [70]. There could be some non-linear effects, making the frequency domain a function of time rather than constant with time. Figure 4.18 shows the step response at the three different temperatures. A positive step is applied at 5us, as shown in the picture, it has created a disturbance in the output, but it has been settled down to an initial value with a healthy exponential settling behaviour without having any ringing; this says that BGR has very good stability across PVT corners.

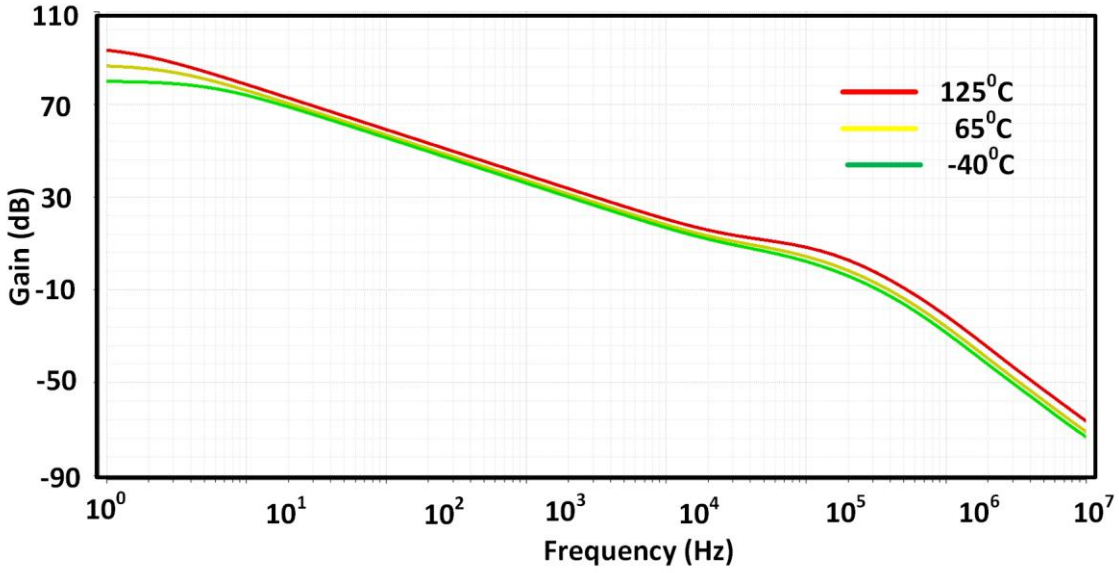

Figure 4.17 Simulated frequency domain stability results.

Furthermore, a negative step was applied at 15us. Finally, the output settles to an initial value, with a settling time of 1.2us. The worst-case stability corner is FS, Cold, 1V supply. The loop gain is very high in this corner, and stability is poor but good enough for the present applications.

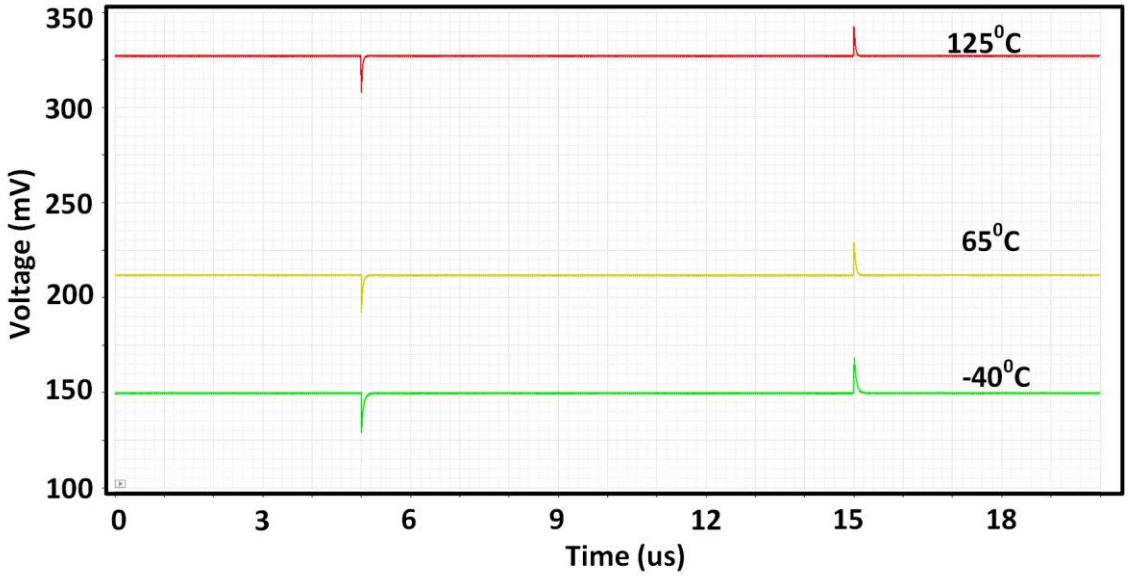

Figure 4.18 Simulated step response for different temperature conditions.

4.7 Summary

A single BJT-based BGR has been proposed, which enables a small area and low-voltage solution. Previously proposed circuits relay on two BJTs with a large emitter area ratio, which requires a large silicon area and accurate device fabrication. A self-bias technique has been explored in the present proposal to achieve less temperature drift. Hence a temperature coefficient performance of 10.2ppm/^{0}c has been achieved. Also, the minimal usable supply voltage is 850mV without requiring any native devices. The proposed circuit was published in [63]

The next chapter describes how to design a Bio-medical Analog front End (AFE) and Variable Gain Amplifier (VGA) for high-sensitivity and low-power applications.

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Chapter 5: AFE Design

5.1 Introduction

Most of the high-accuracy sensors' overall noise and power dissipation are dominated by the front-end amplifier combination like the IA and VGA. Therefore, a low noise and high linearity IA is required to amplify the weak input signal without significant addition of the noise (typical noise factor=3dB). Unfortunately, the sensor/transceiver's required gain is much higher than the maximum possible gain of the IA while maintaining low noise. Hence there would be a strong need to use a VGA followed by the IA, which will shift the frequency characteristics of the entire input spectrum. On the other hand, the noise of the VGA is not stringent as the noise will be attenuated by IA gain. This chapter explains the proposed IA and VGA design procedure and summarizes the simulation results with the help of the post-layout extraction.

5.2 IA Architectural Design

5.2.1 Introduction

There are mainly two types of Instrumentation Amplifier (IA) architectures. One is a popular three-opamp architecture, which many found useful in discrete, device-based implementation for integrated chip solutions [71]. However, it is not ideal due to the large number of resistors needed. In addition, there is no mechanism to adjust its gain, and it has thermal noise generation. The second architecture, the most suitable for the chip design solution, is a feedback-based IA, as shown in Figure 5.1, proposed in [71]. The feedback-based IA targeted ECG signal sensing in 90nm CMOS, where the input signal is extracted from the human body through electrodes. These are connected at the V_{in} input port, as shown in Figure 5.1. The input is AC coupled because any DC offset resulting from the electrodes will compromise the circuit's dynamic range. Hence AC coupling would be the first preference. This is an inverting configuration where the ratio of capacitors defines the gain. Unfortunately, due to the lack of negative DC feedback, the circuit output will be saturated with the power supply voltage when there is any disturbance.

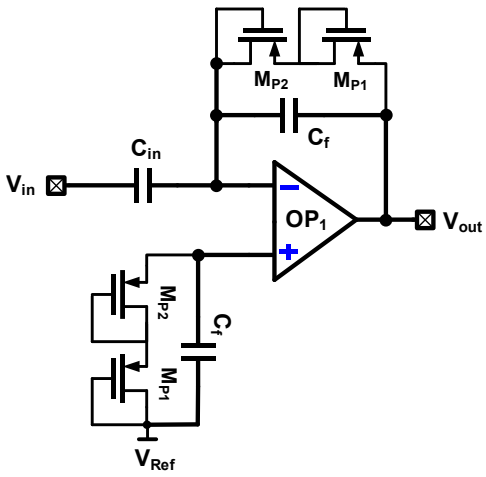

Figure 5.1 Feedback based closed-loop IA

In order to avoid this latch-up issue, several methods have been proposed [72][76]. One simple and less noisy technique is to add a large resistor across the feedback capacitor,

which will decrease the low-frequency gain. For the frequency range of interest, less than 100Hz, this resistor value would be close to 0.5GΩ, occupying a large silicon area. [73] proposed a nmos transistor-based resistor designed to operate in the sub-threshold region and will present a very high resistance, as shown in fig:5.1, where M_{P2} and M_{P1} form the feedback pseudo-resistor. The IA architecture shown above will exhibit a bandpass frequency response. The RC feedback network determines the lower cut-off frequency, while the amplifier unity-gain bandwidth (UGB) determines the upper cut-off frequency. The non-inverting terminal of the OTA has been configured with the same feedback resistor/capacitance to obtain a symmetrical configuration, thus increasing the CMRR and minimizing the offset [76]. Given that C_p is the main OTAs input parasitic capacitance, gm is the OTAs trans-conductance, and Ro is the OTAs output impedance. The amplifier feedback factor (β) can be written as $\frac{C_f}{C_f+C_P+C_{in}}$. The loop-gain can be expressed as follows:

$$\mathrm{LG(s)}=\frac{\beta G_m R_o}{1+SR_oC_{Leff}} \tag{5.1}$$

Where,

$$\mathrm{C_L}=\frac{\mathrm{C_f(C_P+C_{IN})}}{\mathrm{C_f+C_P+C_{IN}}} \tag{5.2}$$

$$closed-\text{loop gain}\ =-\frac{C_{in}}{C_f}\frac{1}{1+\frac{SC_{Leff}}{\beta G_m}}\frac{SR_bC_f}{1+SR_bC_f} \tag{5.3}$$

Equation (5.3) reveals that the closed-loop gain has zero at the origin, whose frequency is decided by the feedback elements and two poles, which are decided by the opamp UGB. Due to the operational amplifier virtual ground, the parasitic capacitance at the inverting amplifier does not affect the closed-loop gain. The ratio $\frac{C_{in}}{C_f}$ can be used to calculate the mid-band gain using equation (3). Due to the OTAs virtual ground, the parasitic input capacitance, Cp, is independent, while the loop-gain is dependent [77]. The lower cut-off frequency is $\frac{1}{R_bC_f}$ and the upper cut-off frequency is $\frac{\beta G_m}{C_{Leff}}$. The electrode

resistance (Rs) has been neglected in the above analysis because it is very small in comparison with the feedback resistor (R_b) and generates a high-frequency zero $\frac{1}{R_S C_{in}}$ Which is normally much higher than that of the amplifier bandwidth. The pseudo resistor and OTA are noise contributors in the amplifiers. However, because of the very low bandwidth, the R_b contribution is much lower; therefore, the OTA noise can be considered separately. The input-referred noise can be expressed as follows

$$\overline{V_{n,AMP}^2} = \overline{V_{n,OTA}^2} \frac{(C_{in}+C_f+C_P)^2}{C_{in}^2} \tag{5.4}$$

$\overline{V_{n,AMP}^2}$ is the input-referred noise of the IA and $V_{n,OTA}^2$ is OTA input-referred noise. OTA noise is generally inversely proportional to the power dissipation because g_m will increase with the power dissipation. [78] defined a Noise Efficiency Factor (NEF), a common dimensionless figure of merit for comparing various designs for a given power budget expressed as (5.5). NEF lets someone compare the various IA architectures from a noise perspective.

$$NEF = V_{n,OTA}\sqrt{\frac{2I_{total}}{\Pi.V_T.4KT.BW}} \tag{5.5}$$

State-of-the-art designs exhibited a NEF of 1.67, with novel architectures like noise cancellation and cascaded current bias re-using-techniques [78].

5.2.2 Proposed opamp

OTA is crucial in the design of the BPA. Its noise performance determines the overall noise performance of the analog front end and, thus, sensitivity. In addition, the amplifier's open-loop gain determines the steady-state error in the step response. Figure 5.2 shows the traditional folded cascode, frequently used as an OTA for BPA applications [78]. Compared to other design architectures, such as telescopic or current mirror opamps, folded cascode OTAs will provide a better signal swing for a given supply voltage. However, the conventional architecture has a minor disadvantage in that the full

signal current from the M_1 does not reach the cascode device M_4. Because of the current division at nodes X and Y, one option is to increase the impedance looking into M_2 or decrease the impedance looking into M_4. The voltage gain can be expressed as:

$$Gain = g_{m1}\left[\frac{g_{m4}}{g_{m4}+g_{ds2}}\right]\frac{g_{m5}}{g_{ds5}g_{ds6}} \tag{5.6}$$

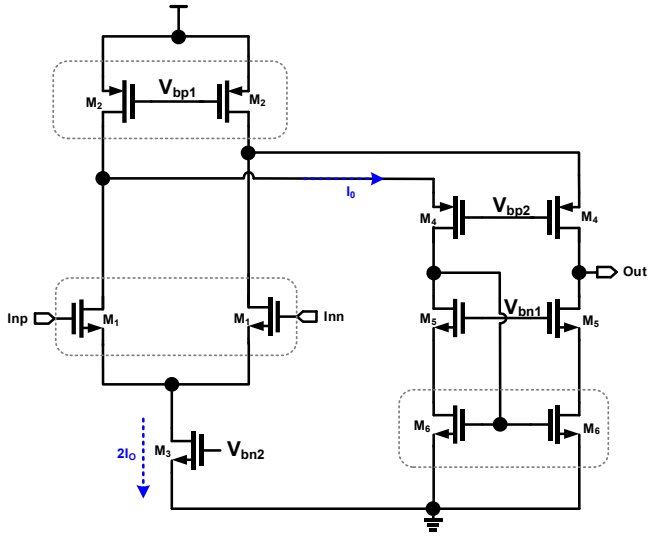

Figure 5.2 Folded-Cascode Op-amp

Transistor M_1 will be biased to gain maximum g_m, such that offset and noise will be minimized. The simple way to do this is by increasing its size until it reaches a point where gm/id is maximized. The PSD of noise is expressed as follows: (M_4 and M_5 contributions have been neglected) [75]. Where γ is the noise factor, 0.95 in this CMOS technology, and K and T are the Boltzmann constant and absolute temperature, respectively.

$$V_{n,thermal}^2 = 8KT\gamma\frac{1}{g_{m1}}\left(1+\frac{g_{m2}}{g_{m1}}+\frac{g_{m6}}{g_{m1}}\right) \tag{5.7}$$

Unfortunately, to maintain the current of M_1 and M_4, the folding transistor M_2 carries a large amount of current, resulting in a much larger g_m and a high noise contribution. Increasing the current flowing through the differential pair, g_{m1} can be increased while noise is reduced. However, this is a power-hungry approach, and the NEF will suffer significantly as a result. There has been a great deal of research into reducing input

noise. Reference [79] suggests adding a current steering branch to the cascode devices, but this would only reduce the cascode devices' contribution, and it has only been introduced for the telescopic cascode amplifier. [80] suggests a noise cancellation technique for a closed-loop amplifier, but this is not feasible in the current situation. One method to greatly reduce the noise is to increase the g_{m1} of the input differential pair so that each contribution decreases as it refers to the input. The method used to increase the g_{m1} without significantly increasing power consumption is to use the current reusing concept, which involves using the same bias current for both nmos and pmos input pairs.

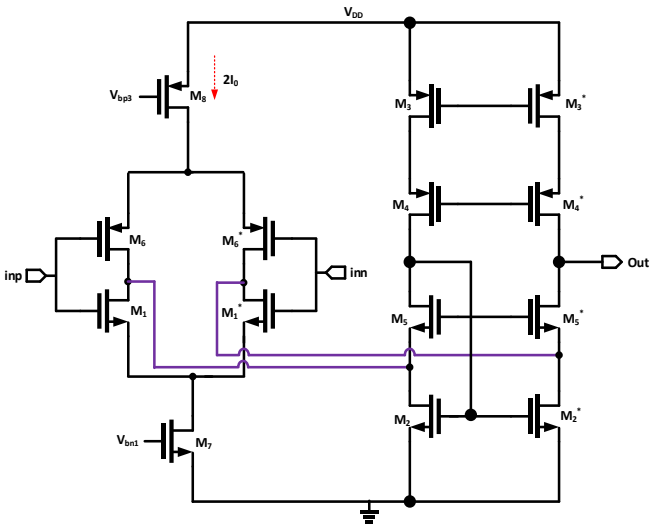

Figure 5.3 Proposed Current-Reusing Folded-Cascode Op-amp

The proposed concept in this work is shown in Figure 5.3, where the M1 and M6 pairs form the complementary differential pair. Both pairs will generate higher g_m for the same bias current. As the input voltage increases, the M_1 current increases, M_6 current decreases, and the differential pair's output current is doubled relative to a traditional nmos or pmos circuit. The standard amplifier is a class-A amplifier, which is very similar to class-AB amplifiers [81]. If g_{m1} and g_{m6} denote the transconductances of M_1 and M_6, the total small-signal current coming out of the composite differential pair is $Vi*(g_{m1}+g_{m6})$. The differential pair is connected to the cascode load devices at Y and Z while previously connected at nodes A and Z in conventional OTA. Due to the diode connection from the

M_5 drain to the M_2 gate in the proposed design, node Y has a very low impedance ($1/g_{m5}.g_{m2}.r_{02}$), while in the traditional design, it is $1/g_{m5}$. As a result, M_5 will receive a significant portion of the differential pair's signal current rather than M_2. The gain can be expressed in (5.8a), which has a higher voltage gain than the conventional OTA gain given by equation (5.8a). The proposed and conventional amplifiers are compared at an 8:1 ratio in equation (5.8b)

$$Gain = g_{m1}\frac{g_{m5}}{g_{ds5}g_{ds6}} \tag{5.8a}$$

$$\frac{Gain_{Proposed}}{Gain_{conventional}} = 1 + \frac{g_{ds2}}{g_{m4}} \tag{5.8b}$$

Current reusing mainly improves the effective g_m of the design without increasing the power consumption, this can be confirmed by equation 5.8(b). The input-referred noise decreases by the same ratio as the improved g_m. This takes place due to the improvement of g_m and the improvement in the noise approximately by 30%. The input-referred noise can be shown to be very low in equation (5.9), which is significantly lower than the conventional folded cascode OTA noise (refer to equation 5.7) [82].

$$V_{n\,thermal}^2 = 8KT\gamma\frac{1}{g_{m1}+g_{m6}}\left(1+\frac{g_{m2}}{g_{m1}+g_{m6}}+\frac{g_{m3}}{g_{m1}+g_{m6}}\right) \tag{5.9}$$

A conventional bias circuit is used to bias all of the cascode current sources in the proposed amplifier. M_4 and M_5 bias voltage noise are insignificant due to the cascode stage gain, which would suppress it, whereas M_7 and M_8 noise occurs as a common mode at the output and is therefore suppressed by the amplifier CMRR. However, with unity gain at the output, M_2 and M_3 current source noise will appear, so it must be optimized by lowering their g_m and using a bias filter [83].

5.2.3 Simulation Results

The proposed IA has been implemented in 45nm standard CMOS technology (1P11M). The capacitors Cin=20pF and Cf=100fF were used to achieve a target closed-loop gain of 46dB. The amplifier should be capable of processing all of the signals mentioned in

the introduction, ranging from 0.1Hz to 18KHz. A pseudo resistor is used to meet this strict bandwidth requirement, formed by sub-threshold PMOS transistors (M_{p1} and M_{p2} in Figure 5.3) to achieve the order's feedback resistance of the order of 10TΩ. The amplifier's closed-loop frequency response is shown in Figure 5.4, with the lower and upper cut-off 3-dB frequency points of 0.1Hz and 18KHz, respectively. To reduce the noise contribution of all differential pair devices, the W/L ratio of the input devices (M_1 and M_6) were increased to 420/0.24um to keep them in the deep-subthreshold region, resulting in a gm/id of approximately 23.1. According to equation (5.1), all cascode load devices must have a much lower g_m. As a result, these transistors were biased in the deep saturation region due to their smaller sizes; they all work with a g_m/i_d ratio of 8[73].

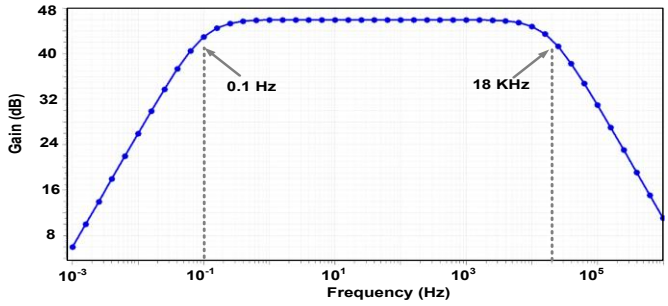

Figure 5.4 Simulated Frequency response of the IA

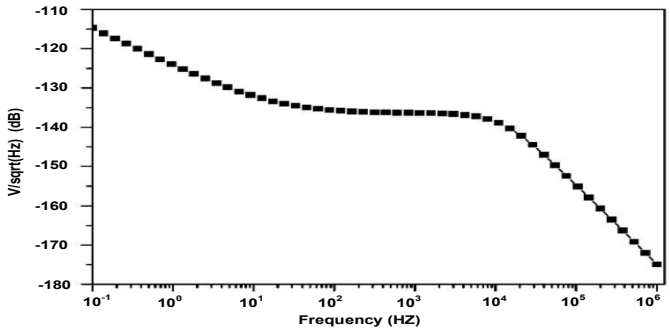

Figure 5.5 Simulated input-referred noise of the IA

The rms noise of the design can be calculated by integrating the PSD plot from 0.1Hz to 10MHZ frequency limits, hence the PSD shown in fig:5.5 has been integrated and the input referred RMS noise is 2.12μV. The assumption while integrating the PSD is noise is very small compared to the actual signal. Because of the small-signal noise simulation,

which ignores all nonlinearity-induced noise, a transient noise simulation with both flicker and thermal noise contributions are on [84] by referring back to the input voltage of approximately 2.23μV. Linearity is a must-have feature in any frontend amplifier for distortion-free recording [85][86], which means that irrespective of the signal frequency, the input and output waveforms should be matched exactly apart from linear amplification. Figure 5.6 shows the simulated linearity versus input signal amplitude. Typically, linearity would be very good at very low input amplitudes because the signal current is smaller than the bias current. As soon as the signal amplitude is comparable, the transistor small-signal parameters will deviate from the designed value; hence linearity or Total Harmonic Distortion (THD) will be degraded. The proposed amplifier works well up to 8mV pk-pk input signal without adding significant distortion (<1% THD). THD rises quickly after that due to the limited power supply voltage - apart from the above-explained reason. THD can be greatly improved by increasing the supply voltage to 2.5V, but most biological signal amplitudes are well within 5mV, so the proposed THD design is more than adequate [87] [88]. Another important specification for an IA is the CMRR, which indicates how much common-mode noise will be converted into a differential signal, considered increased noise, and SNR will be compromised. 60dB CMRR means there will be 10mV of common-mode noise. Since there is much common-mode interaction among the multi-electrode recording channels, a high Common Mode Rejection Ratio (CMRR) is an absolute requirement [79].

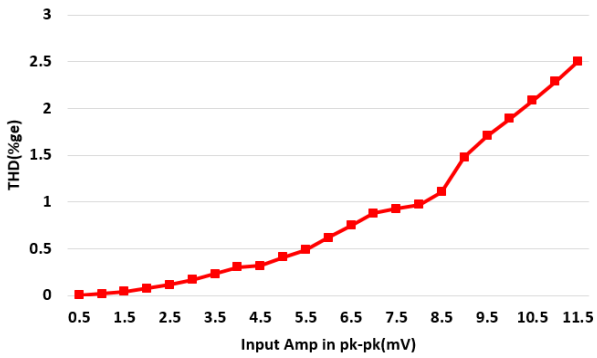

Figure 5.6 Simulated Linearity wrt to the input amplitude

Otherwise, common-mode crosstalk could appear as a differential signal at the output, corrupting the required signal. Also, CMRR needs to be verified at the worst process corner, where every transistor is different from the dimension point of view due to the mismatch. Usually, Monte Carlo simulations will capture this by assigning a random variable to every dimension of the transistor-like Width, Length, oxide thickness and junction depth (X_{jd}). Usually mean and standard deviation of these dimensions were measured and included in the device models. Hence a hyper cube-based Monte Carlo simulation could capture the performance variation due to the mismatch. Table 5.1 describes the performance summary of the designed IA, and it depicts a 24% improvement in the NEF while consuming a similar amount of power from the power supply.

Table 5.1 Performance Summary table I

Parameter	Reference [76]	Reference [77]	Reference [82]	The Proposed IA
V_{dd} (V)	2.8	2.8	1.8	1
Power (µW)	7.56	2.4	20.8	8.67
CMRR (dB)	66	65	88	75
Closed-Loop Gain (dB)	40	39.4	52.1	46
Bandwidth (Hz)	45-5.12K	0.36-1.3K	4-10K	0.1-18K
Input referred Noise (µV)	3.06	3.12	2.6	2.12
NEF	2.67	3.09	3.38	2.41
Area (mm^2)	0.16	0.13	0.058	0.0478
Technology (nm)	500	600	180	65

5.3 VGA Architectural Design

A Variable Gain Amplifier (VGA) is a highly linear amplifier whose gain can be increased/decreased in a controlled fashion. A VGA is mainly introduced before an ADC to improve the dynamic range, which means when the input signal is very low in amplitude, it should amplify the signal so that the thermal noise of the system will not limit SNR. On the other hand, it will attenuate the signal if the input has an amplitude such that SNR will not be limited by the distortion and linearity of the ADC. Usually, the gain will be programmed with the digital/analog control signal. Figure 5.7 shows the various bio-medical signals' input amplitude and spectral bandwidth. For the target SNR of 60dB, the VGA gain needs to be in the range of -12 to 28dB. Therefore, the wish list of the VGA can be described as follows. 1. Low input noise while consuming minimum power 2. In the present work, there is minimal capacitive loading to the proceeding bloc, for example, IA. 3. PVT independent gain range (means minimum and maximum gain limits should not vary with the process corners) [80].

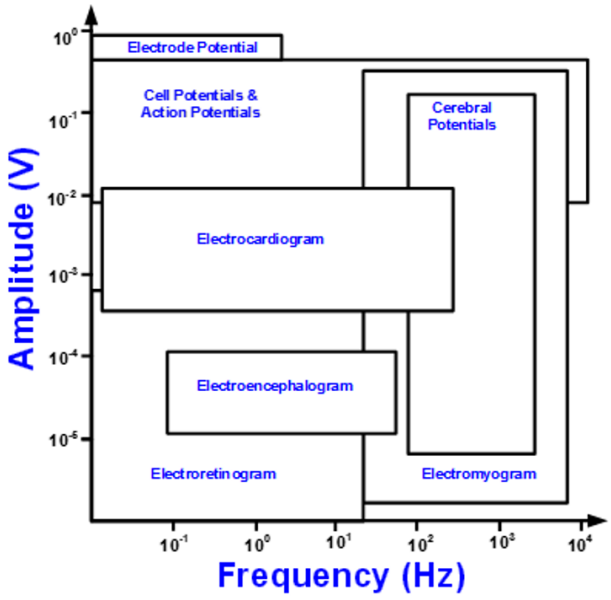

Figure 5.7 Pictorial representation of the biological signals

Practically the noise generated by the VGA should be much less than the IA input-referred noise. But the power consumed by the VGA is proportional to $1/V_n^2$ where V_n is

the input-referred noise of the amplifier. In order to design a low-noise VGA, the power must be higher, which is a difficult trade-off for a low-power VGA design [79].

5.3.2 Proposed Architecture

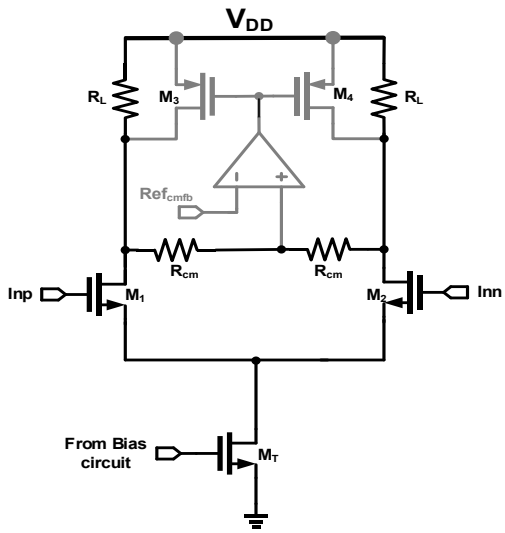

Figure 5.8 Proposed VGA core schematic.

In the present design, the VGA's main target specifications are to minimize the gain variation while generating much less thermal noise; linearity is also very important as the input signal could vary from 100uV to 25mV. Hence the large signal gain should be independent of the input signal. Figure 5.8 shows the proposed VGA core, where the tail current is generated from the M_T device, whose bias voltage is generated from an adaptive analog loop (which will be explained in the next section). The gain can be changed by adjusting the g_m of the transistor (by changing the bias current) or load resistance (R_L). Adjusting the R_L impacts the power spectral density (PSD) of the noise and 3-dB bandwidth. Hence, I decided to use gm as the variable in this work. However, unfortunately, this will alter the output common-mode voltage, which may push the differential pair devices (M_1 & M_2) into the linear region to compromise distortion [81]. Therefore, bleeder current sources $M_{3\text{-}4}$ was introduced at the output, which are driven by an opamp to adjust the current for a given target output common-mode voltage. R_{CM}, opamp and M_3, and M_4 form the CMFB loop. R_{CM} senses the o/p common mode voltage

and opamp forms negative feedback adjust the o/p common mode voltage. The potential divider formed by R_{CM} acted as a common mode sensor and generated a reference for the opamp. To adjust the VGA, gain low, the tail current will be decreased, and CMFB will increase the current to keep the output voltage as it is. The voltage can be expressed as follows.

$$\text{Gain} = \frac{g_m}{\frac{1}{R_L}+\frac{1}{R_{CM}}+\frac{1}{R_O}} \sim \; g_m R_L \qquad (5.10)$$

Where g_m is the input device transconductance, R_L is the load resistance, and R_0 is the output resistance. Here R_L is much smaller than R_{CM} and R_o. Hence approximately, the gain is only dependent on R_L. The above equation (5.10) shows the variable gain by varying the long-tail pair current [76]. The bias current can be set to generate a differential pair g_m that is inversely proportional to R_L. Therefore, the gain can achieve a PVT-insensitive nature. Equation (5.11) shows that the gain and transconductance (g_m) can be expressed as:

$$g_m = \frac{\alpha}{R_L} \text{and Gain} = \alpha \qquad (5.11)$$

The question here is how to generate bias voltage to keep the gain independent of PVT. It means the loop must adjust gm to keep track of resistance variation [82].

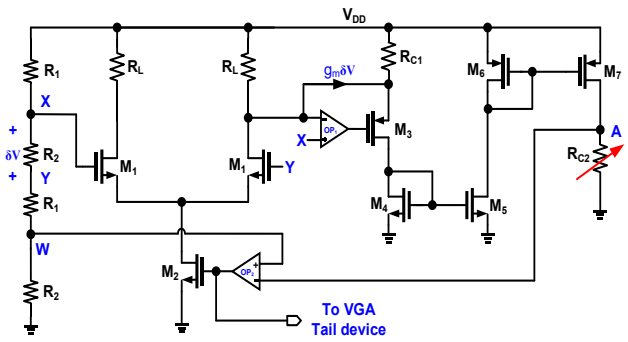

Figure 5.9 Proposed Bias circuit for VGA core.

This circuit applies a small voltage δV across the differential pair, which yields a differential pair signal current of g_m*δV that flows into the load resistance R_L, thus achieving a voltage drop equal to R_L*g_m*δV. Through the long-tail pair current

modulation, the negative feedback loop will control the voltage drop across the differential pair and across the resistor. Hence the transconductance (g_m) depends on the load resistor R_L.

$$\mathrm{RL} * \mathrm{gm} * \delta\mathrm{V} = \delta\mathrm{V} \quad \text{hence,} \quad \mathrm{RL} * \mathrm{gm} = 1 \tag{5.12}$$

This method is almost independent of the imperfections resulting from CMOS technology scalings, such as the hot carrier effect and velocity saturation [76]. The proposed servo bias loop shown in Figure 5.9 contains a potential divider formed by R_1 and R_2 (Figure 5.9), which yields a common-mode voltage for the differential pair formed by M_1 and M_2. Their value (85K) does not affect the circuit. Only the ratio of the resistors defines the input common-mode voltage range of the differential pair. The differential pair creates a signal current of g_m*δV, which will flow into the load resistance and the trans-impedance stage formed by the Op1, M_3, and $R_{c1.}$ The input impedance of this Trans-impedance amplifier (TIA) stage can be expressed as the following equation.

$$\mathrm{Gain} = \frac{1}{Ag_m} \tag{5.13}$$

The negative feedback topology provides a low-impedance path. Hence most of the signal current will flow through M_3 if transistor M_3 has a lower impedance than R_{c1} (approximately equal to 23.5KΩ). The signal current flowing in the current mirrors, comprising M_4, M_5, M_6 and M_7, creates a voltage drop of g_m*δV* R_{C2} across the compensation resistor R_{c2}. The opamp (op_3) adjusts the long-tail current source M_2 gate voltage until the voltage across R_{C1} is equal to node X voltage. Hence g_m of the differential pair only depends on the reference resistor (in our case, R_{c1}) irrespective of the process corners and power supply voltage [86], which means the g_m of M_2 tracks the resistance variations, and its gate bias voltage can be used to bias other devices to stabilize the g_m variation range. The output voltage of op-amp (op_3) will be used to reference the VGA long-tail current source bias. The Op-amp architectures (op_2 and op_3)

will have no impact on the functionality of the proposed circuit or PVT insensitivity advantage if the op-amps have enough gain to minimize the input-referred systematic and random offset [82]. In the new VGA design, both op-amps are single-stage amplifiers with a PMOS input stage for op_2 and an NMOS input stage for op_1.

5.3.3 Design and Simulation Results

The proposed VGA design and its bias circuit in Figure 5.8 and Figure 5.9 are implemented in 65nm standard CMOS technology to verify the operation and performance of the circuit. The power supply voltage was set to 1V for a nominal gain of 22dB at ±5dB gain tuning with the gain control signal. The VGA supports 400mV peak-to-peak differential output signal without becoming non-linear [87]. The circuit draws 56µA at room temperature. Figure 5.10 shows the frequency response simulation for the new VGA design for different closed-loop gain settings. The bandwidth for the new VGA design was 6MHz at the typical process corner and 65^0C temperatures. The gain sensitivity across PVT corners in the new VGA design was 1.3dB variation at (21.4dB nominal gain). In the conventional VGA (with the fixed bias current), the simulated gain sensitivity across PVT corners (TT-FF-SS-FS-SF MOS corners and -40^0C to 125^0C and min and max supply voltage) is high at 6.7dB as shown in Figure 5.11. Compared with an existing configuration, the gain sensitivity has been reduced by approximately 5.4dB.

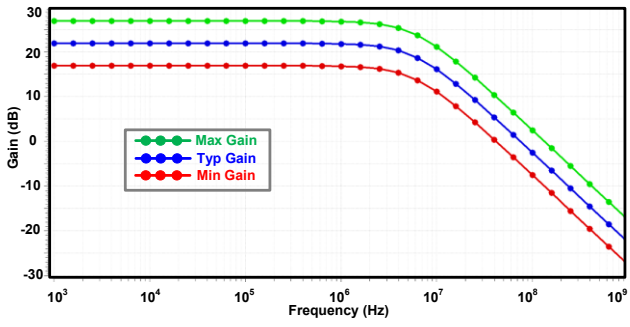

Figure 5.10 VGA frequency response.

Most of the new VGA design characteristics are significantly better than the conventional VGA, with the notable exception of the power consumption, which has increased by

around 17.5% compared with conventional VGAs [19]. However, the power consumption is still more than adequate for typical VGA application requirements. Higher temperature leads to a decrease in mobility. Hence the transconductance (g_m) decreases. This will result in a negative temperature coefficient for the VGA gain. In order to address the shortcomings of the new design, bias current (proportional to absolute temperature (PTAT)) is used to bias the amplifier [83]. The new design circuit produces a current that increases with temperature. Figure 5.12 gives the simulation of the gain variation vs the temperature characteristic (-40^{0}C to 125^{0}C) for both the conventional VGA and the new VGA design circuit. The conventional VGA remains at about 4.8dB variation over the temperature range, while the new VGA has been reduced to about 1.2dB sensitivity, showing a four-times improvement.

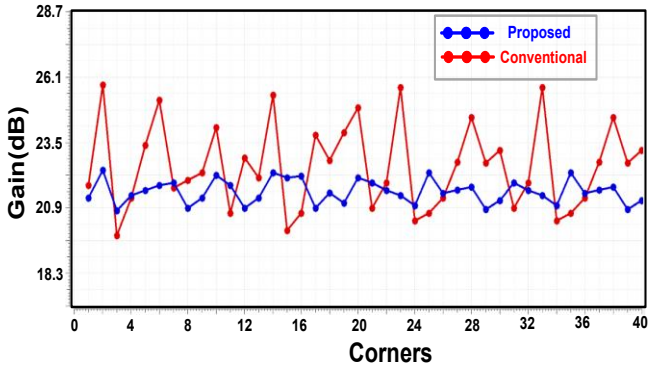

Figure 5.11 Gain vs PVT corners.

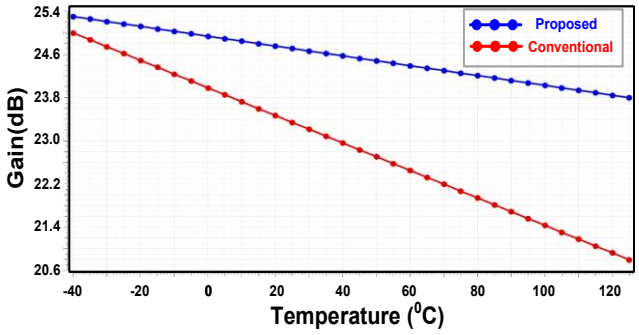

Figure 5.12 Gain variation wrt to temperature.

Since there is no degeneration resistance, the tail current source noise will not contribute to the overall input-referred noise [85]. Therefore, the new VGA design will have less

input referred noise than the conventional VGA. Figure 5.13 shows the simulated results of the input-referred noise spectral density ($V/\sqrt{Hz}$) of the proposed VGA, with the integrated noise over the entire frequency band, is approximately equal to 0.768μV. The noise exhibits a 10KHz flicker noise corner at a regular supply voltage and 125^0C temperature simulation condition. The dominant noise contributors are the input devices (M_1 pair) and the bleeder current source (M_3). Also, the main reason the noise is very low compared to the state of the art is to eliminate the degeneration resistance in the signal path. The following expression (5.14) shows the noise spectral density with the degeneration. With the degeneration, there is a need for two current sources, and there is a common mode to differential mode conversion, and finally, the current source noise appears at the output with a conversion factor as given in (5.14). Fortunately, the tail current source noise will appear at the output as a common mode without the degeneration resistance since it experiences the same impedance on both sides of the differential pair [84]. According to the authors, this is the biggest advantage of having no degeneration resistance.

$$O/p\ \text{noise} = 4KT\gamma g_{mt}\left[\frac{R_S+\frac{1}{g_{m1}}}{R_S+\frac{2}{g_{m1}}} - \frac{\frac{1}{g_{m1}}}{R_S+\frac{2}{g_{m1}}}\right] \qquad (5.14)$$

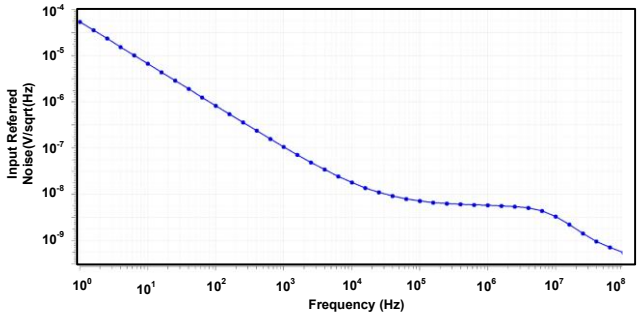

Figure 5.13 VGA output noise at 125^0 temperature.

Figure 5.14 shows the histogram of the voltage gain corresponding to a 500-points Monte Carlo simulation; it exhibits 22dB nominal gain and 0.2dB standard deviation. Typically mismatch is related to the area of the transistors for a given bias current; hence the

design used maximum W*L of the transistor while maintaining the same $\frac{W}{L}$ Ratio. The following design guidelines have been followed during the VGA design.

1. For current sources, the g_m of the transistor needs to be minimized; hence threshold voltage (V_{th}) mismatch will be converted into a current mismatch, which will be minimised. Also, transistor length (L) has been increased while maintaining the larger area rather than W. The current efficiency of the transistor (gm/id ratio) is adjusted around 8 [85].

2. Differential pairs were designed by increasing the W (contrary to the current source) to maximize the g_m/id ratio to minimize the mismatch impact on the input-referred offset. A gm/id ratio of 17-19 has been used over the opamps and VGA input pair [86].

3. There has not been much attention to resistors and capacitors because the typical resistor mismatch in this process is 0.3%, whereas the transistors mismatch is 4-5%; hence resistors are not near the significant contributor's list.

4. In addition to the design techniques, special consideration has been taken in the layout using techniques like common centroid for differential pairs and interdigitating for current mirrors in the layout [87]. Also, the surroundings around the differential pair devices are identical (including metals) to minimize the edge effects like the good proximity effect and the Shallow Trench Isolation effect (STI) [88].

For a typical Gaussian statistical random process, 99.97% of the fabricated chips will stay with ±3σ around the mean (μ). In the present case, 99.97% of VGA's gain will be between 21.4–22.6dB. Also, the simulated distribution is very close to the Gaussian distribution, which indicates that transistors were biased with a significant amount of overdrive voltage margin and saturation margins.

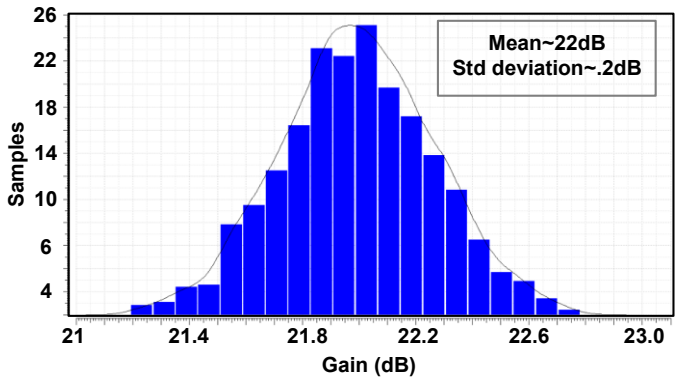

Figure 5.14 VGA small-signal gain histogram (500-point MC sim) under typical corner at 125^0 temperature.

5.3.4 Comparison with the state of the art

Table 5.2 Performance Summary table II

Parameter	[81]	[85]	This work	Unit
Output Voltage swing	67	112	25-400	mV
Power supply	3.3	1.8	1-1.8	V
Temperature range	-40 to 125	-40 to 125	-40 to 125	^{0}C
Gain Range	5-9	10-13	17-27	dB
Integrated Noise (10Hz-100MHz)	1200	1823	0.768	µV
Gain Standard deviation	0.64	0.39	0.2	dB
Gain PVT variation	Not given	Not given	6.04	%
3dB bandwidth	2.3	4.1	6	MHz
Power Consumption	340	129	56	µw
Technology	180	500	65	nm
Area	Not given	Not given	1716	µm^2

Table 5.2 shows the comparison of the present VGA concerning the published results. Compared to [81] and [85], the present work outperforms the noise and gain stabilization points of view while consuming 50% less power. Also, this is the first VGA design demonstrating the gain stabilization technique.

5.4 Summary

IA noise and THD decide the performance of the overall ECG sensor. Design techniques of an optimal IA have been discussed in a very detailed manner. The VGA plays a significant role in the analog frontend circuit for any ADC-based sensor or transceiver because it will maintain enough dynamic range; hence the ADC works within the limits of the noise and distortion limited input range, providing optimal SNR. In this work, a degeneration resistance-less VGA, with a negative feedback loop, to maintain the constant gain independent of the PVT corners by using the constant g_m circuitry has been developed.

The next chapter discusses the design of low-power over-sampled ADC with an analog decimation filter, which can support up to 10ks/s sampling rate.

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Chapter 6: ADC Design

6.1 Various ADC Architectures

The main purpose of an ADC in biomedical sensing is to digitize the VGA output so that a computer/ digital processor can process the medical signal. There have been several general-purpose architectures in the literature for meeting numerous application requirements, like speed, accuracy, and area. Table-6.1 describes details about various types of ADCs wrt to their speed and applications.

Table 6.1 : Comparision between various types of ADC's wrt to their speed and applications

Name	Speed	Number of bits	Applications
Sigma-Delta	1-50ks/s	14-22	Sensor and audio band
SAR	0.1-1Gs/s	10-12	Data Acquisition, Wireline and wires less sensing
Pipeline	0.5-2Gs/s	8-14	IF sampling, Software-defined radio and high-speed instrumentation
Flash	2-15Gs/s	Up to 7 bits	Space imaging and high-speed measurements like scopes.

For wireless applications, the area and speeds are the main specifications, so the pipeline is the most suitable one, and occasionally flash is also required to meet speed specifications. Recently, sigma-delta ADC became very popular for its superior resolution (due to the noise shaping and filtering), but this is at the cost of the integrator power [89]. So for the present targeted applications, other parameters like area and

speed do not matter as much because the intention was to sense 0.1-350Hz bandwidth signals [90].

Power Supply Noise Model

The ADC power supply must be low noisy; otherwise, any synchronous tones in the power supply could compromise the SNR. The sampling/reference buffers PSRR contributes majorly towards the ADC performance [91]. For example, a 20mV peak-peak supply noise could result from the ADC's switching action. This wideband supply can be split into spurious tones as follows.

Let us say noise tone at any arbitrary frequency F with amplitude A_{in} and signal power p_{sin}. White noise (Gaussian distribution) between the zero and 200MHz with the signal power P_{sin} and standard deviation of $\sigma_{n,}$ as shown in Figure 6.1.

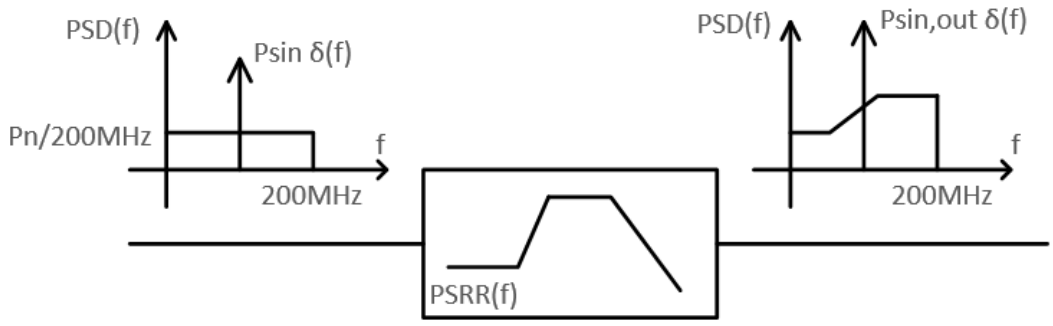

Figure 6.1 Power supply noise Model.

The noise parameters can be related as follows.

$$P_{sin} = \frac{A_{sin}^2}{2} \quad \text{and } \sigma_n = \frac{A_{sin}}{\sqrt{2}} \tag{6.1}$$

Usually, Gaussian noise will be spread with +/- 3sigma for 99.97% of the occupancy. Hence the peak-to-peak value of the max power supply can be expressed as follows.

$$A_{PSRR} = 2A_{sin} + 6\sigma_n \tag{6.2}$$

$$A_{PSRR} = 2A_{sin} + 6\frac{A_{sin}}{\sqrt{2}} \tag{6.3}$$

From the above equations (6.2) & (6.3), it can deduce acceptable noise amplitude (A_{sin}) as 3.2mV and standard deviation (σ_n) as 2.265μV. The single tone at arbitrary Frequency F is supposed to be placed at the peak of the PSRR [92]. The power of the resulting output signal (P_{sinout}) can be found by multiplying P_{sinout} by $PSRR^2_{max}$. The white noise component is filtered by a transfer function - the PSRR transfer function (PSRR(f)). Then the power of the resulting output signal ($P_{n,out}$) can be found by integrating the power spectral density (PSD) as shown in the following equations.

$$P_{sin,out} = \frac{A^2_{sin}}{2} 10^{\left(\frac{PSRR_{max,dB}}{10}\right)} \tag{6.4}$$

$$P_{n,out} = \int_0^{BW} \frac{\sigma_n^2}{200MHz} |PSRR(f)|^2 \, df \tag{6.5}$$

The resultant noise at the output ($P_{tot,\ out}$) is obtained by summing $P_{sin,out}$ and $P_{n,out}$ to the noise contribution of the reference generator itself ($P_{ref,out}$)

$$P_{tot,out} = P_{sin,out} + P_{n,out} + P_{ref,out} \tag{6.6}$$

Apart from the noise through the power supply and thermal noise, there is a significant amount of switching noise at the sampling clock frequency, mainly due to the clock feedthrough and charge injection. Ripple voltage can be modelled as a uniform noise (between $-\frac{\Delta_R}{2}\ and\ \frac{\Delta_R}{2}$) added to the reference voltage in each cycle [92][93]. The Effective Number of Bits (ENOB) as a function of the peak-to-peak amplitude Δ_R with the full-scale signal at the input (full amplitude A_{in}). The SNR at the o/p can be expressed as:

$$Ripple\ Power = P_n = \frac{\Delta_R^2}{12} \tag{6.7}$$

$$Modulated\ Ripple\ power = P_{REF} = P_n \frac{1}{2} \left(\frac{A_{in}}{V_{REF}}\right)^2 \tag{6.8}$$

$$SNR\ due\ to\ Modulated\ Ripple = SNR = \frac{V^2_{REF}}{P_n} \tag{6.9}$$

The above equations (6.8) and (6.9) were plotted in Matlab as well did a perfect component simulation. Figure 6.2 shows the ENOB degradation versus the amplitude of the ripple on the reference. As it shows, even a 2mV ripple voltage is causing 0.1 bits' loss, meaning 20mV degrades ENOB by 1bit or SNR will be dropped by 6dB. In this thesis, 9.5Bits were targeted in the worst case and budgeted 0.1bit loss due to the ripple; hence I will have to limit the ripple to 5mV as shown in the plot. ENOB of a ADC indicates the real effective resolution rather it's physical o/p bits. For example, a poorly 15-bit ADC could have ENOB of 10 (means SNR of 60dB), in that one should call that as a 10-bit ADC even though it has 15 physical o/p's.

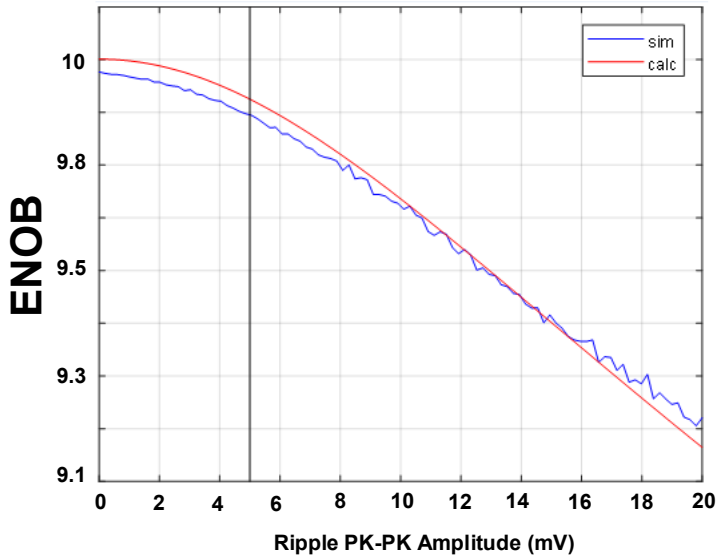

Figure 6.2 Effect of the ripple on ENOB

6.2 Proposed Time Domain ADC

In the present thesis work, I proposed an ultra-low-power time-domain ADC, which works on the charge balance principle [94]. This is mainly to convert the ratio of the signal to the reference into a duty cycle modulated signal, and a digital duty cycle to digital converter will be used to get the digital output out of the ADC. Figure 6.3 shows the concept of the proposed ADC. First, the signal and reference from the bandgap are buffered through a unity gain opamp (buffer). The main purpose of the buffer is to eliminate the charge injection from integrator into the signal input by providing very low input o/p impedance. Also the buffer will reduce the interaction between the multiple channels of the ADC.

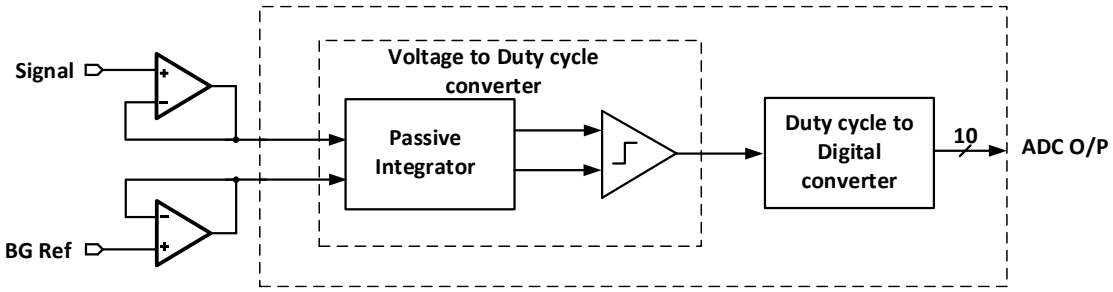

Figure 6.3 Time-domain ADC concept

6.2.2 Buffer design

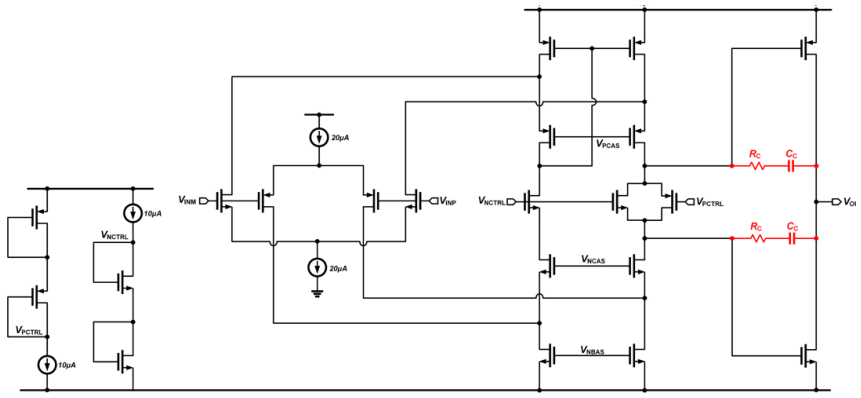

Figure 6.4 Class-AB buffer amplifier [94]

As shown in Figure 6.3, the signal and reference voltage needs to be buffered by a low output impedance buffer to minimize the glitch input to the sampler. In addition, the

sampling capacitor charging current needs to be supplied by the buffer. Hence a high-gain rail-to-rail input opamp is required [94]. Figure 6.4 shows the conventional Class-AB opamp, where M_0, M_1 forms the NMOS differential pair and M_2, M_3 forms the PMOS differential pair [90]. $M_{3\text{-}12}$ forms the class-AB output cascade stage with the floating battery formed by the $M_{13\text{-}14}$. Miller's compensation has been used for unconditional stability. The overall DC gain of the buffer is 89dB in the worst corner.

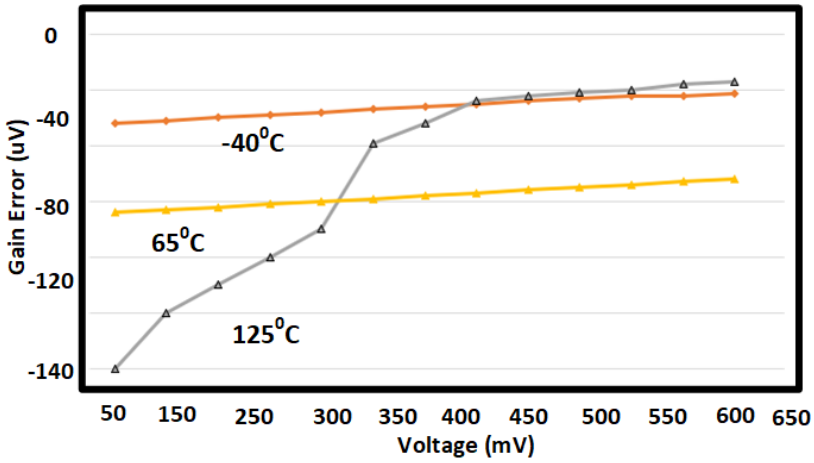

Figure 6.5 The gain error of the buffer.

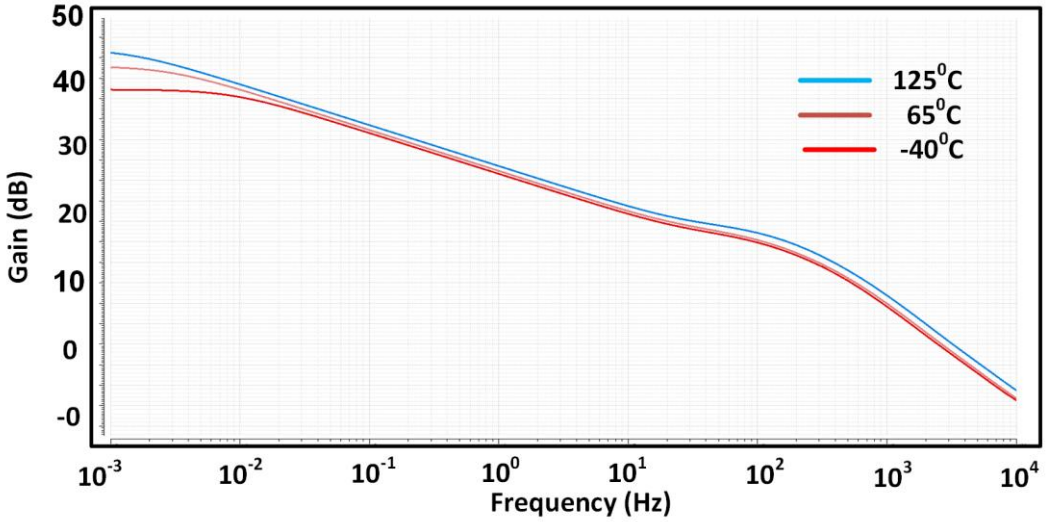

Figure 6.6 Bode plot of the buffer across PVT.

Figure 6.5 shows the gain error of the buffer due to the finite gain bandwidth. The worst-case error is 0.17mV in the fast corner and 125^0c temperature, this is because the gain of the opamp is significantly degraded due to the poor o/p impedance. Finally, Figure 6.6

depicts the bode plot of the buffer, which clearly shows 15MHz Unity gain bandwidth (UGB) and 67.5^0 Phase margin [95].

6.2.3 Passive Integrator

A switch cap sampling network is proposed to convert the input signal as the digital duty cycle. The inputs to this block are the ADC input signal and reference from the bandgap reference. Figure 6.7 shows the proposed switch capacitor; it samples as follows:

1. When CLK is 'low'--If Comparator output (q) is zero, C1 charges to the V_{signal}. If q=1, then C1 charges to V_{signal} - V_{Ref}.

2. When Clk is 'high', the charge on C1 will transfer to C2. Therefore, the charge on each capacitor during each clock phase is given as follows.

    a. If q=1, then the charge on C1 is given as $\frac{T_{on}}{T} C_1 \left(V_{signal} - V_{Ref}\right)$

    b. If q=0, then the charge on C_1 is given as $\frac{T_{off}}{T} C_1 V_{signal}$

At the end of each cycle, the total charge on the C_1 has to be zero. Hence we can express the net charge on C_1 as follows, and the duty cycle can be derived according to the equation (6.11).

$$\frac{T_{on}}{T} C_1 \left(V_{signal} - V_{Ref}\right) + \frac{T_{off}}{T} C_1 V_{signal} = 0 \quad (6.10)$$

$$Duty\ Cycle = \frac{T_{on}}{T_{on}+T_{off}} = \frac{V_{signal}}{V_{Ref}} \quad (6.11)$$

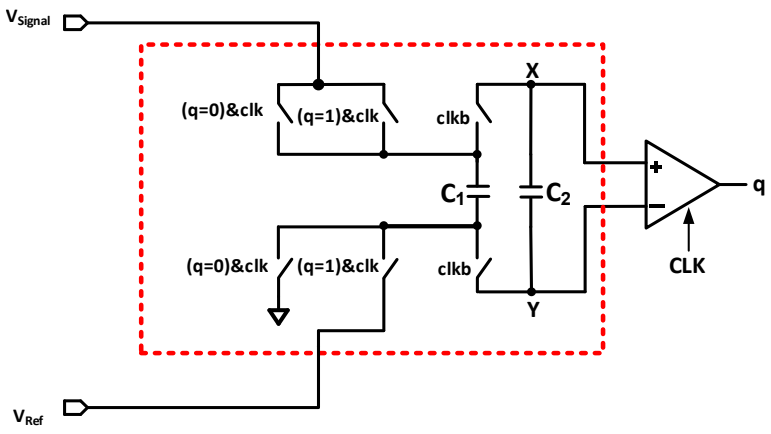

Figure 6.7 Proposed passive switch capacitor sampler.

6.2.4 Comparator Design

A comparator is required to convert the continuous-time signal from the switch capacitor network to a digital signal to do anti-aliasing filtering in the digital world. There have been several clocked comparators in the literature, mainly strong-arm and dual-tail comparators [97]. They both work exactly on the same principle, but a strong-arm latch does not require multiple phases of the clock, whereas a dual tail requires a multi-phase clock generator which demands higher power consumption. Also, this architecture has more branches than the strong-arm counterpart, so there is more thermal noise and power. Strong-arm latch also has single stage and every operation has been merged in one stage, hence low power. Therefore, a strong-arm latch (SRM) was chosen for the above-specified reasons.

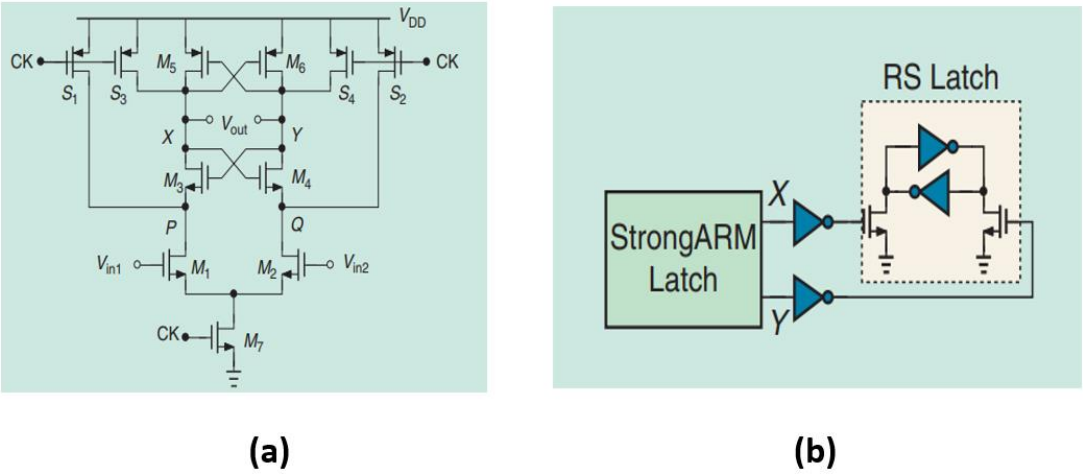

Figure 6.8 (a) Strong Arm latch schematic (b) SR latch [97]

Figure 6.8 (a) shows the latch circuit diagram. In this one, M_1 and M_2 form the differential pair, which will decide the offset and noise of the ADC. M3 and M4 form the regenerative devices, and switches S1-S4 form the reset switches. This circuit operates in the following phases:

1. In the first phase, when the clock is low, node voltages P, Q, X, and Y charge to the supply voltage. Hence this phase is called the reset phase.

2. In the second phase, when the clock is high, all switches S_1-S_4 turn-off and differential input voltage V_{in1}-V_{in2} forces the current to discharge the nodes P and Q with different slopes. As Vp and Vq fall to V_{DD}-$V_{TH,}$ M_3 and M_4 will turn on, allowing the regeneration process. The differential output voltage and average voltage gain can be expressed as follows. Where I_{CM} is the common mode current and Cp,q is the parasitic capacitance at the nodes P, Q.

$$V_P - V_Q = \frac{g_{m1}(V_{in1}-V_{in2})}{C_{P,Q}} t \tag{6.12}$$

$$A_V = \frac{g_{m1}V_{TH}}{I_{CM}} \tag{6.13}$$

3. In the third phase, M_5 and M_6 turn on, and Node X and Y try to diverge from each other for the final decision, though they were initially discharged from Vdd. The regenerative time constant can be expressed as follows.

$$T_{reg} = \frac{C_{x,y}}{g_{m3-4}\left(1-\frac{C_{x,y}}{C_{P,Q}}\right)} \tag{6.14}$$

The main purpose of the switches is to reduce the memory effect or dynamic offset voltages [97]. Without M_3 and M_4, there will be a significant amount of the crowbar current. At the end of the decision, both outputs will go back to Vdd; hence they are invalid for half of the clock phase. Hence this circuit must be followed by an SR latch, as shown in Figure 6.8(b). This latch makes both of its outputs valid and complimentary. A pair of inverters is used as an interface between these two to make the Strong Arm's output capacitance constant to minimize the dynamic offset. The power consumption of the latch is a strong function of the parasitic capacitance, as given in the following equation (6.15), where F_{olk} is the clock frequency

$$Power = F_{clk}\left(2C_{P,Q} + C_{X,Y}\right)V_{DD}^2 \tag{6.15}$$

The input decides the minimum input differential voltage required for a proper decision, referred offset and thermal noise. In a typical design, offset is mostly dominated by M1-M2. The other transistor's noise/mismatch is much less because of the high gain due to the input devices given in equation (6.13). Therefore, the static offset would not significantly affect the ADC performance, whereas the dynamic offset will degrade the SNR. In the second regeneration phase, the charge from capacitance at the P, Q would create a random offset as given in the following equation.

$$V_P - V_Q = -\frac{g_{m1}}{2}\frac{C_P+C_Q}{C_P C_Q}(V_{in1} - V_{in2})t + \frac{C_P-C_Q}{C_P C_Q} I_{CM} t \tag{6.16}$$

The noise power due to the transistor mismatch will compromise the ADC's distortion performance, which mainly depends on the common-mode current of the tail transistor. Therefore, the integrated noise power can be defined as follows.

$$V_{rms}^2 = \frac{8KT\gamma}{C_P}\frac{g_{m1}V_{th}}{I_{CM}} \tag{6.17}$$

Simulation of the comparator is tricky as it is a varying time circuit rather than a linear circuit like opamps. Usually, comparator performance is simulated with non-linear periodic simulations like PSS and PNOISE, considering the noise fold back into the signal band and accurately estimating the total noise floor [98]. Figure 6.9 shows the input-referred noise of the comparator versus process corners. The maximum offset occurs in the fast process corner, low voltage and low temperature, which is 1.9mV. This is happening in this corner because the g_m of the transistor is very poor in the cold temperature and low voltage.

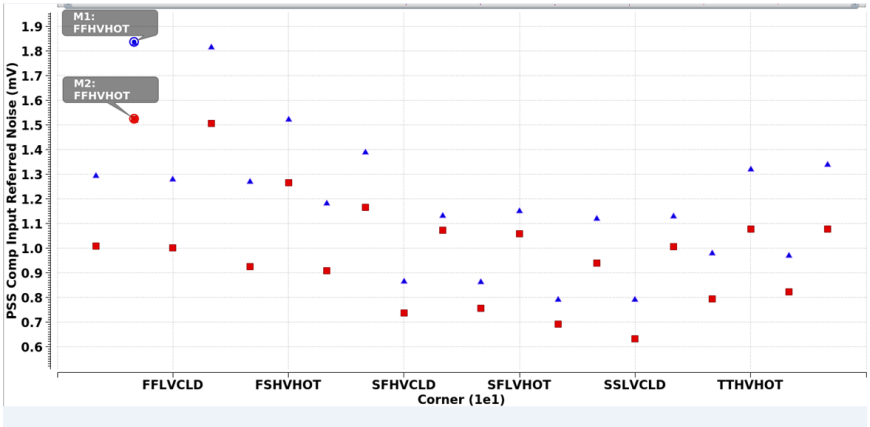

Figure 6.9 Simulated input-referred noise of the comparator.

6.2.5 Decimation Filter Design

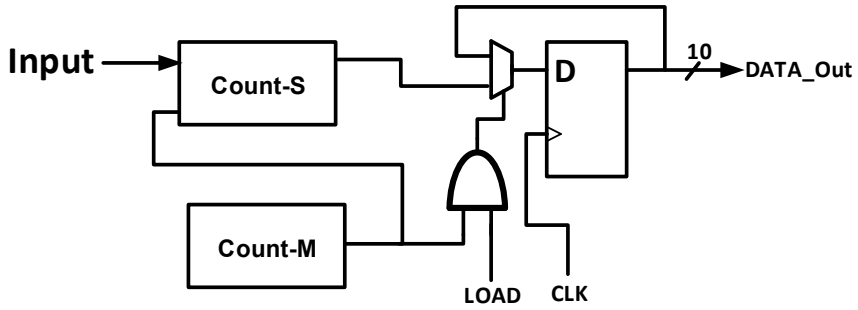

Figure 6.10 Proposed decimation filter

As shown in Figure 6.3, the output of the comparator will have single-bit information with shaped noise, which has to be filtered through a sharp digital filter to recover the narrowband signal. Usually, digital filters are synthesized through CAD tools to design in less time, but they usually result in a complicated area. In this thesis, a custom counter-based decimation filter has been proposed, as shown in Figure 6.10. The main idea is that there is two 10-bit digital up counters, mainly one slave counter (Count-S) and another master counter (Count-M). The slave counter increments its output by 1 bit whenever the comparator output is high and keeps it in the same state when the comparator output is low [99]. The master counter keeps counting up – meaning it is incrementing its output by one LSB, irrespective of the output of the comparator. After 1024 cycles, the M-count will reach its maximum output; this freezes the slave counter, and its stage will be fed to a D-latch. A load signal allows us to read the ADC digital output without having any timing error or glitch in the output in the dynamic input. This represents the digital equivalent of the input signal. Hence this acts as a time-to-digital converter. If the number of logic 'high' states in the comparators is stated, the output state can be expressed as Equation 6.18, where D_{out} represents the output state, and T_{alk} is the sampling clock period.

$$D_{out} = \frac{V_{in}}{T_{clk}} 2^M \tag{6.18}$$

The main advantage of this architecture is extremely low power due to the usage of only two 10b counters and one final loadable flip-flop. Mathematically this can be modelled as an integrator with maximum amplitude corresponding to a 1024 clock cycles duration input signal. The counters are implemented with the TSMC standard flipflop and XOR gate inputs. The strength of the logic gates was minimized to decrease the power while maintaining adequate operating speed.

6.3 ADC Simulation Results

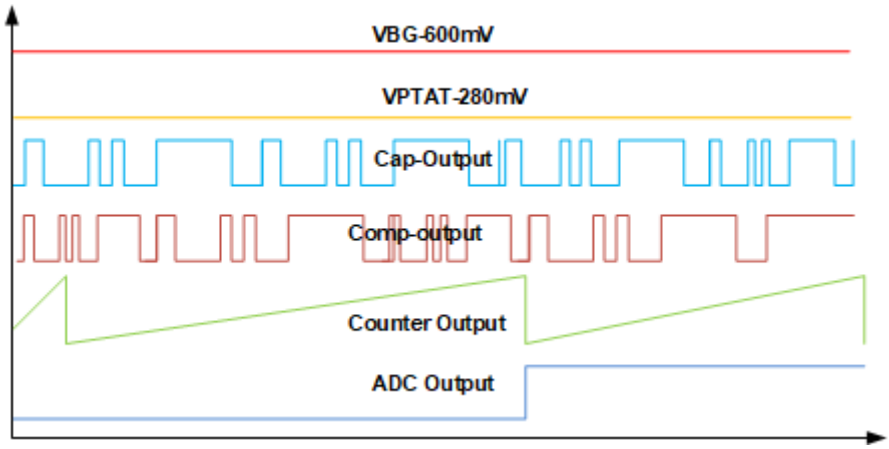

Figure 6.11 Critical signal waveforms over the ADC signal path.

A behavioural model of the ADC was built in Verilog-A to ensure all the loop filter parameters and sampling capacitors are good enough for the present application. Then with the same specifications, a transistor-based schematic was developed and simulated. For the target resolution of 10bits and 60dB signal-to-noise ratio (SNR), a 100KHz sampling rate was chosen: too high sampling frequency would result in very high clocking power consumption and too low results in loss of SNR due to the sampling switch leakage current, especially at very high-temperature condition. Figure 6.11 shows the various signals' time-domain behaviour corresponding to typical process, room temperature and supply voltage of 1V simulation conditions. The first trace shows the reference voltage of 750mV and bio-medical signal of 250mV. The second and third traces show the voltage on the sampling capacitor and comparator output. At the same time, the fifth and sixth traces show the output of both counters. The master counter is outputting quickly compared to the slave comparator and freezes at 41µs time, and digital output is available after 41µs. Thus, the total conversion time is 41µs, and the main contribution to this latency is the decimation filter integration time constant.

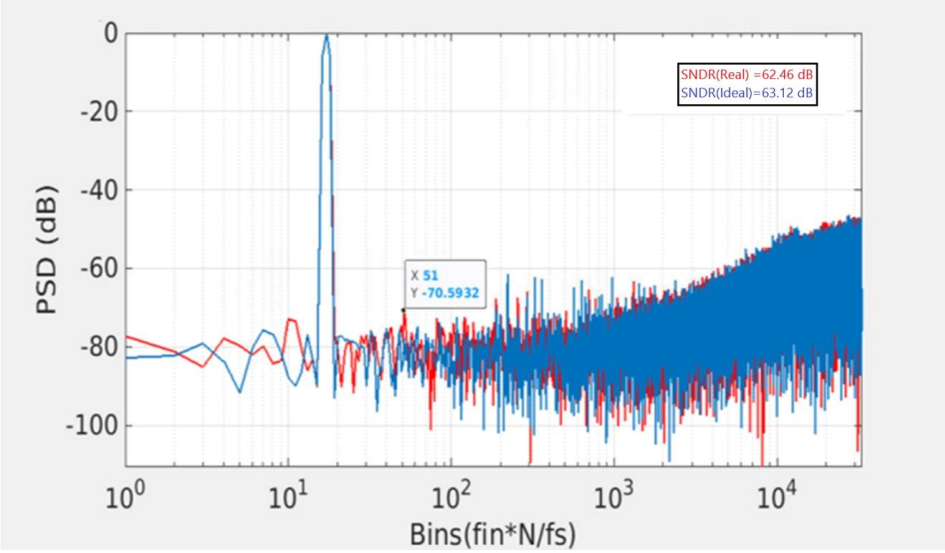

Figure 6.12 FFT of the ADC output in a Typical corner

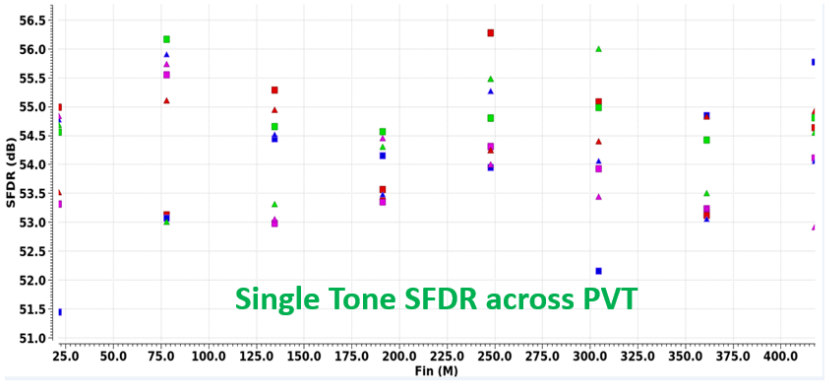

Figure 6.13 ADC SFDR versus input frequency across PVT

Characterizing the SNR is a critical part of the ADC evaluation, revealing how many bits of resolution the ADC has instead of the ten physical output wires [100]. A 50mV single-ended peak-to-peak signal with a frequency of $\frac{7}{128} f_s$ has been applied at the ADC input and simulated the output spectrum. Figure 6.12 depicts the Fast Fourier Transform (FFT) of the signal over 1024 cycles of the input across PVT. It reveals that there is no clock feed through the spectrum, and this means the decimation filter is filtering every signal except the input signal efficiently. The noise floor is around -61.2dB. Therefore, the SNR

mainly depends on the quantization noise and thermal noise integrated into the sampling capacitor (c_s), as described in equation 6.19.

$$SNR = \frac{\frac{v_p^2}{2}}{\frac{KT}{2C} + \frac{\beta^2}{12}} \tag{6.19}$$

Figure 6.13 shows the Spurious Free Dynamic Range (SFDR) versus input frequency for different PVT corners. The worst SFDR is 52.1dB. Mostly SFDR is limited by the thermal noise and flicker noise of the switch capacitor network. Figure 6.14 shows the layout of the proposed ADC, which occupies 98*34um^2. A significant area is occupied by the filter capacitor, distributed all around to save the area. The Metal oxide metal (MOM) capacitor has been used to save the area while minimizing the leakage current, especially at higher temperatures. Special care has been taken to improve the matching of the current mirrors by exploiting the inter-digitization technique [97] and keeping the surroundings of the matched transistors the same [101].

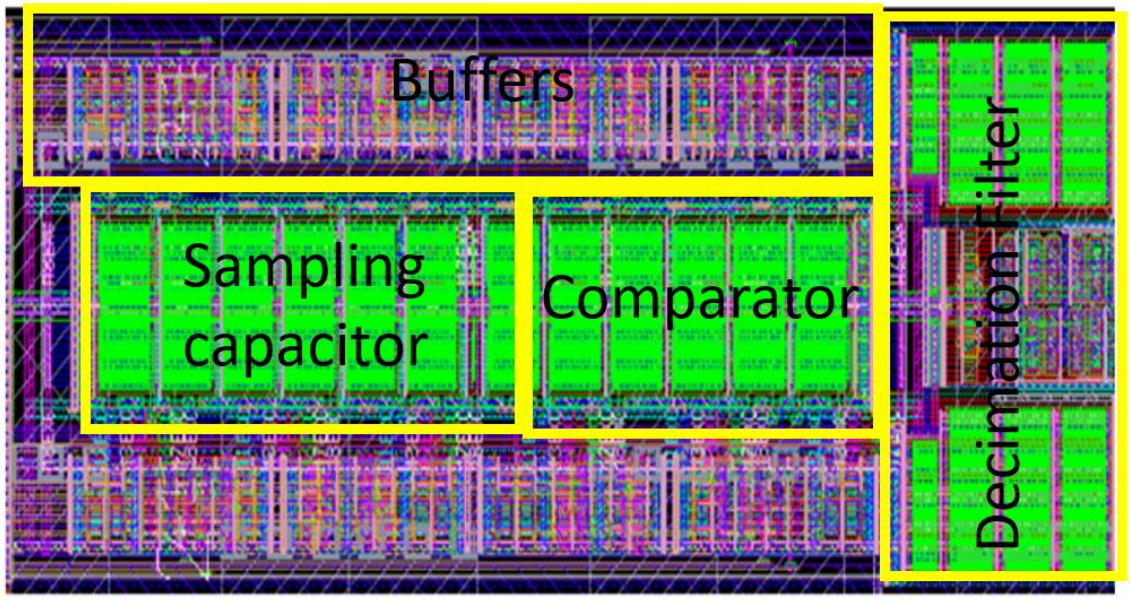

Figure 6.14 Proposed ADC Layout

6.4 Summary

In this chapter, a new class of low-power ADC has been proposed. In the conventional ADC architecture, most of the power was consumed by the opamp in the loop filter. This is because it has to be much faster than the rest of the components. Hence the g_m of the input device has to be maximized by increasing the bias current. Bandwidth can also be increased by decreasing the compensation capacitor, but this will, unfortunately, increase the thermal noise of the system; hence SNR will be compromised. In this work, an opamp-less passive time-domain ADC has been presented, relayed on the switch capacitor network, converting the input signal into the digital bits in two stages. In the first stage, a slowly varying analog signal is converted into a single stream of bits, and in the second stage, a single-bit digital stream pulse width modulated (PWM) signal is converted into digital bits. In this work, a low voltage 10b ADC with 123μW power consumption has been designed with a 52.5dB dynamic range (SFDR).

The next chapter discusses system-level integration issues in the interface between the blocks like IA, VGA and ADC. Also, post-layout simulation results were explained in a detailed manner.

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Chapter 7: SYSTEM INTEGRATION

7.1 System design introduction

This chapter focuses on the integration of the blocks that have been discussed in the previous chapters, namely IA, VGA and ADC. This also describes the realization of a full chip for reliable sensing while consuming minimal power and generating acceptable input-referred noise [102]. Previous chapters described the design trade-offs and simulation results of the individual blocks. Also explained the main reason behind selecting the specific architecture. The Analog Front End (AFE) circuit consists of primary blocks like IA, VGA and ADC. However, I have chosen high-gain IA with low-resolution ADC (10b) compared to the low-gain IA with high-resolution ADC (like 16-20b) [102]. This is because high gain IA will reduce the impact of the low ADC resolution and makes the SNR high and independent of the ADC noise. Also, a high gain in the front-end reduces the input-referred noise because the ADC and IA noise will be divided by the IA gain [103].

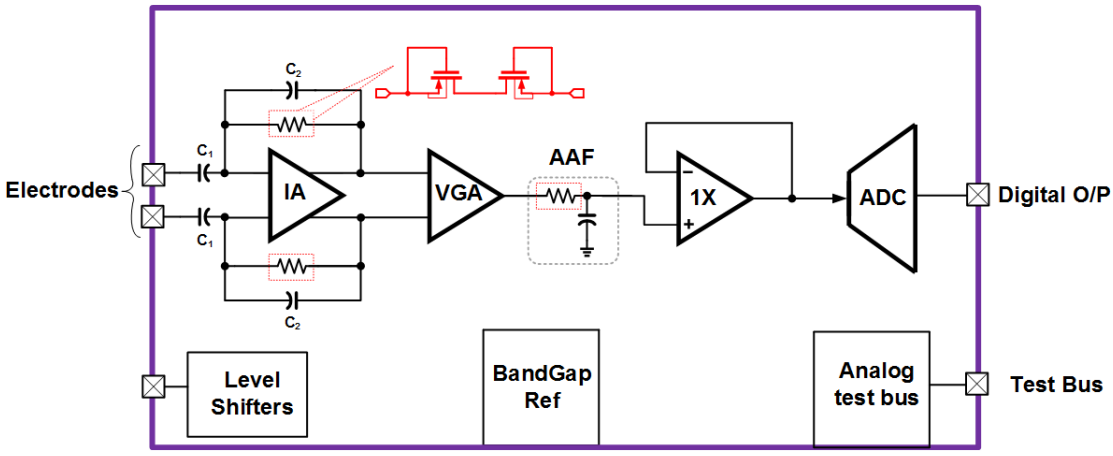

Figure 7.1 TOP level Chip Implementation Diagram

The main challenge of this specific system design is to minimize the input-referred noise while consuming lower power and achieve around 1mV input sensitivity such that this AFE can be used to sense different biological signals explained in chapter 2. Figure 7.1 shows the implementation diagram of the proposed solution. It consists of all previously explained analog blocks (IA, VGA and ADC) and several peripheral blocks, including

Level shifters and Analog Test Bus (ATB). Every core analog block (IA, VGA, ADC) needs a few digital control signals for the following reasons.

A. A power-down signal disables the power supply when the circuit is not in active mode, so that power can be saved and enables duty-cycled operation. Another important reason for the power down state is that when the circuit starts from zero power supply, every node in the circuit starts from a known low impedance state hence no unexpected time constant-based settling. Furthermore, without a power-down signal, a critical node may start from an unknown potential due to the leakage of the transistors [104].

B. Sometimes there will be a need to adjust the bias voltage or current of the critical circuit due to poor manufacturing of the transistors or unexpected input signal behaviour. This requires a programmable current (like a simple current DAC), especially at very high temperatures [105].

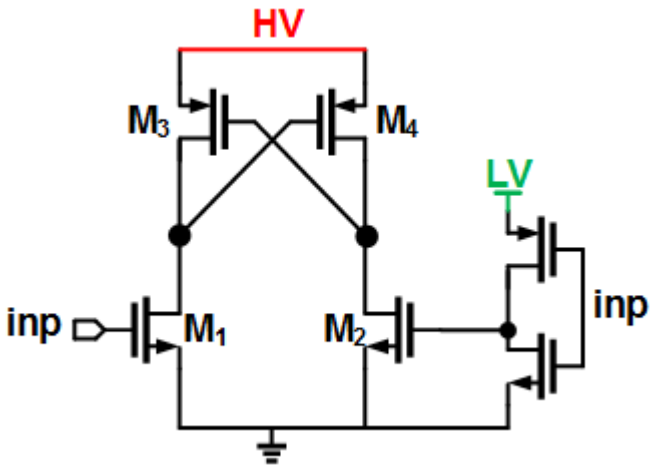

Figure 7.2 level shifter

All the control signals come from the 0.8V digital core supply; hence they need to be level-shifted. It uses 1.2V as the main supply (powering up IA, VGA, ADC) and 0.8V for the core supply, which is mainly to power up the output buffers. The digital control signals feeding into the analog circuit should be referred to high voltage, otherwise significant

leakage will be resulted, hence here is a need to level shift the signals so there is need to design level shifter. Figure 7.2 depicts the conventional level shifter circuit, where M_1 and M_2 form the main differential pair powered from the HV(1.2V), and inputs were driven from LV(0.8V). Due to the regeneration action of M_3 and M_4 transistors, there won't be any leakage, crow bar current from either of the supply to the ground while shifting the input dc level from low voltage to high voltage [105].

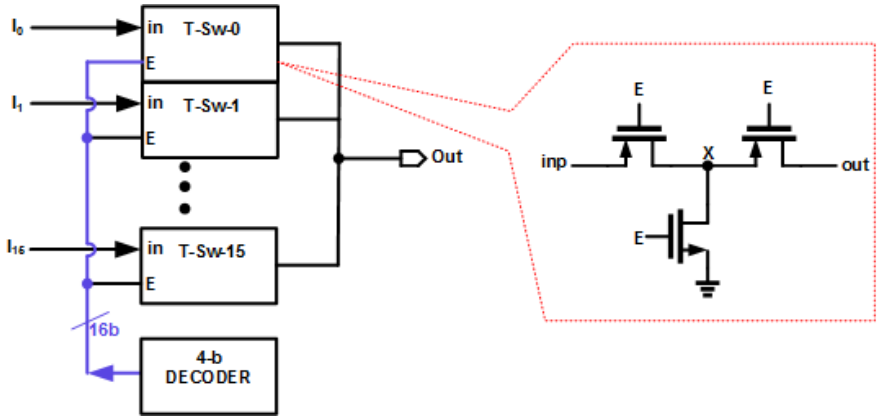

Figure 7.3 Analog test Bus (ATB) schematic and T-gate implementation.

For most of the complex analog chips, the design for testability (DFT) feature is a very important diagnostic option in case of any unexpected silicon behaviour [108]. In this particular chip, a simple Analog Test Bus (ATB) has been added, which is a high-voltage multiplexer driven by a decoder, as shown in Figure 7.3. It consists of a Transmission gate (T-SW-0/15) with an enabled signal driven from a 4*16 decoder. Hence this ATB bus chose any of the inputs (I-0/15) based on the decoder setting [108]. Each transmission gate has been implemented with 3 transistors, as shown in the zoomed version. Whenever the enable signal is low-the, two pmos transistors between the input and output will turn on and enables the connectivity, and when the enable signal is in logic 'high' state, they will be off so that it provides greater isolation. The isolation in the off state is generally around -60dB, so any high voltage coupling noise outside could create noise inside the circuit, which is a serious problem for the present solution because the average signal strength is lesser than that. Hence we have added a pull-

down switch from node X to the ground, which will enhance the isolation by shunting the noise from the out to the ground rather out to input [108].

Electrostatic discharge (ESD) became a primary concern for modern VLSI chip implementation. Human beings and machines carry a large amount of electric charge due to electric interaction, but this charge may not be a very big issue for humans because of the large human capacitance (a typical body has 200pF capacitance). Whenever a human being touches the chip, there will be charge transfer from the human body to the chip, depending on the capacitance ratio of the human and chip. Due to this sharing, the chip experienced unacceptable current and voltage for a very short time. This current could damage the metals/via's, and high voltage could rupture the MOSFET thin oxide, or in the rare case, the drain/source to bulk diode will breakdown [109] [112]. Hence ESD protection is mandatory for any chip. IEEE classified ESD events into three main categories. The first one is the HBM model, which replicates the human interaction through a 100pF discharge capacitor and 1.5K ohm conduction resistance. The 100pF capacitor will be charged to 1.5KV and discharged to all possible pin combinations of the chip. Usually, this discharge consists of 1.2A current in the order of 1-5us, and the chip should with-stand this electrical stress [106]. The second model is Charge Discharge Model (CDM); this is a very dangerous event which discharges a 100V power supply into the chip without having much series resistance when this will have >20A in a few ns[110]. Depending on the package size of this chip, some of this current could go even above. Compared to the HBM event, CDM is very stressful to the chip in terms of the peak current and span of the event, so usually, if any chip passes the CDM event, most probably that will work for the HBM case too.

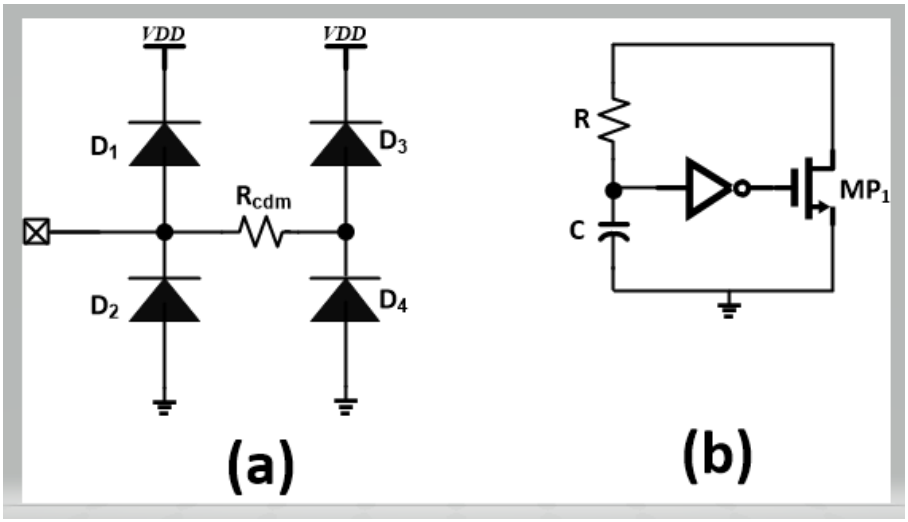

Figure 7.4 (a) primary and secondary ESD protection for HBM (b) Supply clamp configuration through a timer.

Every chip needs some protection against the ESD event. Figure 7.4 (a) shows the HBM protection circuit for the signal bumps. D_1 and D_2 form primary diodes. These anti-parallel diodes will turn for every ESD event and clamps the bump voltage to the supply voltage; hence circuits connected to the bumps will not experience any stress during this event. However, the diodes should be sized according to the current requirements as they will carry the ESD current [107]. The ESD current will be diverted to the supply rather than the chip. If any discharge current does not go through the main diode, a secondary path will be formed by D_3 and D_4, which takes the rest of the current. R_{cdm} is a series of resistance connected in between the diodes to limit the current. This will reduce the CDM event current going to chip, because of the resistive nature (also CDM driver resistance is low) and hence protect against CDM events. This resistor value can't be too high; otherwise, it will affect the circuit. At the same time, it can't be low so as to make it a little effective. Generally, it will be somewhere between 20-100ohms. In this work, 50Ω has been used as a compromise [108]. Now the question is how the ESD current entered into the V_{dd} will find its own path. Fig:7.5(b) shows the supply clamp ESD protection circuit, which consists of a timer (with R&C) and discharge transistor. In case of no event, the RC circuit will charge the capacitor to Vdd, due to the inverter transistor input will be

at zero potential; hence the discharge transistor MP1 will be off-state so that it will not interfere with the normal operation. When there is an ESD event occurs in the supply pin, the capacitor voltage does not change (which means a charge to the supply voltage), but due to the high voltage on the inverted supply, it will treat the input V_{dd} as logic 'low' and turns on the discharge transistor, and the entire ESD charge will be directed to V_{ss} bump. The RC time constant will play a vital role while designing the supply clamp [109]. The clamp should distinguish the difference between the supply ramp and the ESD event. Generally, an ESD event will have a rise-time of several hundreds of nano seconds (typically 200ns), whereas the supply ramp rise time will be in typically several milli-seconds. Hence the RC product used in this work is 250us.

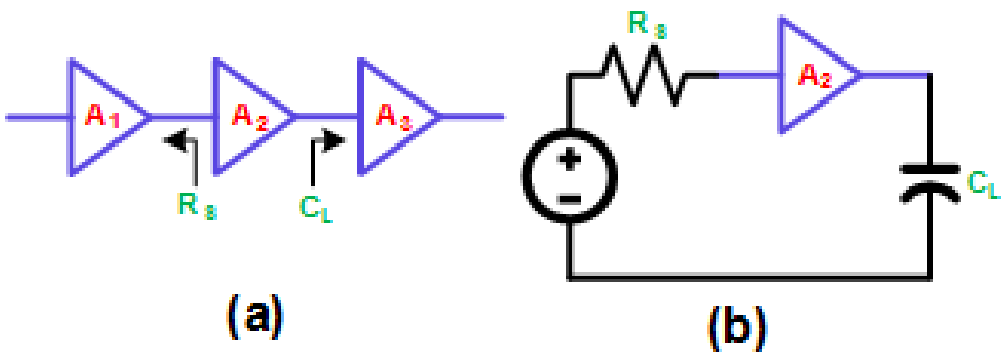

Figure 7.5 (a) Cascade of amplifiers (b) Simulation setup for the A_2

7.2 Integration Challenges (Loading)

As a part of the chip fabrication, every block will be designed and simulated individually with a little consideration of what kind of load it is going to be driven and from what kind of source impedance it will be driven. Most often, the general practice is to add an estimated load capacitance and input resistance [109]. Figure 7.5(a) depicts this simulation test bench, where A_{v1}, A_{v2}, and A_{v3} represent the chain of amplifiers. To simulate the A_{v2} amplifier on its own, the input impedance looking into the A_{V1} has been represented as Rs, and the load capacitance of the output stage A_{v3} is represented as C_L. Fig:7.5(b) represents how to simulate the Av2 on its own by adding a voltage excitation at the input. However, this may not be sufficient if the circuit has any dynamic non-linearity because the load capacitance and source resistance that has been added is purely linear elements; hence they can't display any nonlinearity in the simulation results.

Nevertheless, there are ways to solve this simulation issue. The first method is adding a voltage-dependent resistor and capacitor models in Verilog-A [110];. Although this works very well in the actual simulation and takes very little time, creating Verilog-A models takes considerable effort and time and requires several sets of simulations to validate the models. The second one is by adding the output stage of AV1 as the input resistance and the input stage of Av3 as the output load representation; this works really well from an accuracy point of view but takes considerable time. Therefore, I have chosen the second method for accuracy and simulation speed requirements in this work.

The previous section explained the simulation method for a large analog system. Another important design methodology is designing several blocks when they have cascaded together. The output DC voltage of the preceding block must always be compatible with the next block input common-mode range. For example, if the first circuit produces a

common mode voltage close to the power supply (Vdd), then the second stage has to be designed with NMOS input devices to make the compatible design.

7.3 Systems- level Simulation Results

7.3.1-Overall Closed-gain: The sensitivity determines the Low-frequency gain of the ECG sensor. In this work, a gain of 50dB has been targeted to keep the sensitivity less than 100uV, which is the minimum detectable ECG signal amplitude, while producing less than 1mV. Out of the target 50dB gain, the Instrumentation Amplifier (IA) contributes 40dB, and the variable gain Amplifier (VGA) contribution varies from 10 to 30dB (since it has variable gain).

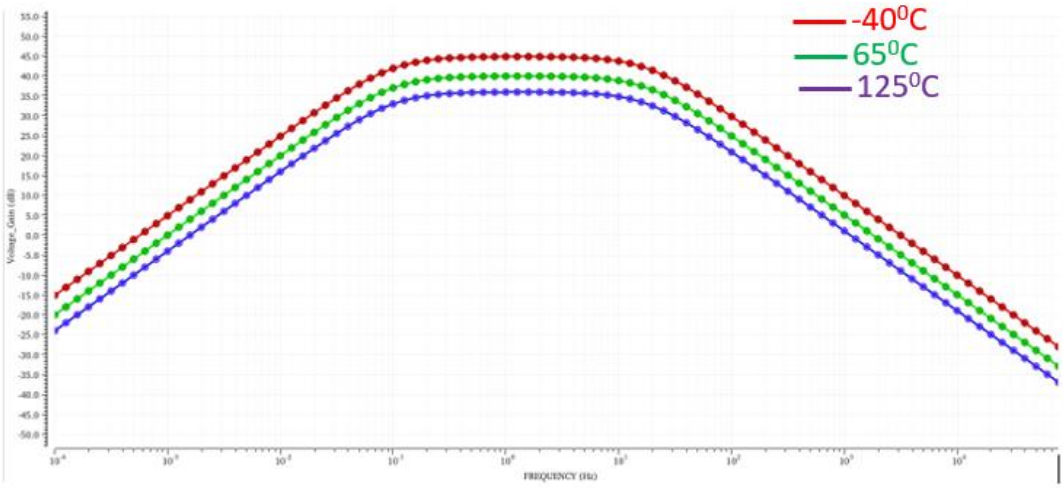

Figure 7.6 (a) Closed loop gain of the amplifier chain

One consideration while budgeting the gain between IA and VGA is to maximize the first block gain (IA) so that it will have less input referred offset. IA distortion will have very less effect on the over THD because of the preceding block VGA. With those considerations, I have chosen a 40dB gain for the IA and the rest of the 10dB from the VGA. When there is a 100uA signal at the input of the chip and with 50dB voltage gain, the Analog to Digital Converter (ADC) input signal amplitude can be expressed as follows (equation 7.1) (Where Amp_{input} is the input amplitude and ADC_{input} is the output of the VGA).

$$ADC_{input} = Gain_{IA}Gain_{VGA}Amp_{input} \quad \text{=300x100uV= 30mV} \qquad (7.1)$$

Since VGA has a gain range of 20dB, if the input signal is weaker than the specified 100uV or due to the PVT variation if the IA gain is reduced by some amount, the VGA gain control voltage can adjust to maintain the ADC input amplitude constant [111]. Figure 7.6 shows the simulated gain of the signal path. The PVT gain variation of IA is 8.9dB, which means its gain varies from 36 to 44.9dB with an average of 40dB.

7.3.2-input referred Random noise:

As explained in the previous chapters, noise determines the power consumption of the sensor, which means that for the same sensitivity at the input, low power consumption indicates higher noise. The main issue with the random Gaussian noise is that, over time, it will accumulate and corrupts the signal when the noise amplitude is closer to the signal amplitude (pk-pk 100uV). Typical analog circuit performance will be limited by either bandwidth (due to the excessive load capacitance) or Signal to Noise ratio (SNR). In the present work, we are not limited by the bandwidth because the CMOS process Gain Bandwidth product (GBW) is around 100GHz, hence designing a 1GHz bandwidth circuit would be very easy without using any special bandwidth enhancement techniques like inductive peaking or active negative miller capacitance. So the main gaol of this thesis work is to design the entire sensor with target SNR without consuming much power. Unfortunately, for most analog circuits, there is a trade-off between the bandwidth, SNR and power, as described below. The noise of a simple 1^{st} order amplifier can be expressed as follows (7.2). Where K, T, C_L, and g_{m1} are Boltzmann constant, the temperature in kelvin, load capacitance and small signal trans-conductance [111]. Equation (7.3) shows the trade between the power and SNR for a given bandwidth, this has been mainly derived for a first-order low pass filter, but it will hold true for complex order linear network. However, this doesn't work for non-linear amplifiers or circuits like oscillators. Fortunately, we are considering only linear amplifiers in this work, which will give the required design on-site. (7.3) reveals that if power consumption is constant, then lower SNR will enhance the bandwidth and vice versa.

$$v_n^2 = \beta \frac{KT}{C_L} g_{m1} \qquad (7.2)$$

$$Power_{amp} = BW \frac{V_{pp}^2}{v_n^2} \quad (7.3)$$

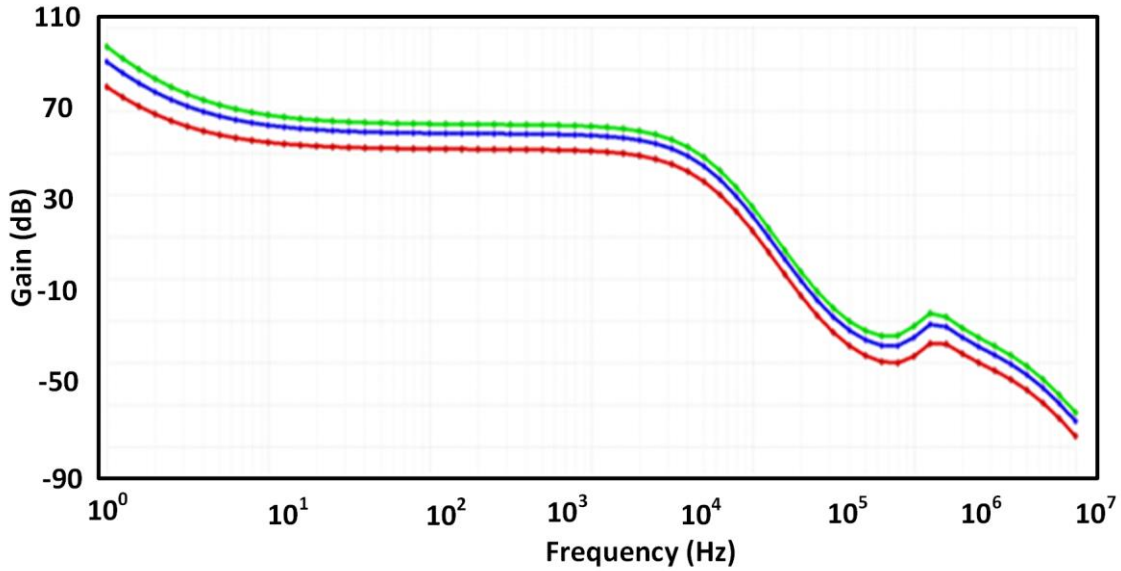

Figure 7.7 Noise at the VGA output.

From equation (7.2), it can be shown that to improve the noise spectral density, the load capacitance has to be increased. To make noise less by 2 times, the cap has to be doubled, and gm has to be increased by 2X to maintain the same bandwidth. This intuitive explanation explains the trade-off between power and noise. In other words, SNR. Figure 7.7 depicts the noise at the VGA while capturing the IA output referred noise also into the picture. The main contributors to the noise are the Input devices in the IA (70%) and VGA output devices (30%). Generally, input-referred noise will be dominated by IA, but here the main focus is output-referred noise; hence the last stage will contribute less noise because it has not been amplified by any gain stage [111]. In this design, noise is quite sensitive to the temperature because VGA gain has almost 2.5dB variation over the industrial temperature range (-40-125^{0}C). The noise at low temperature is 2.89uV and at high temperature is 8.9uV.

7.3.2-Linearity of the amplifier:

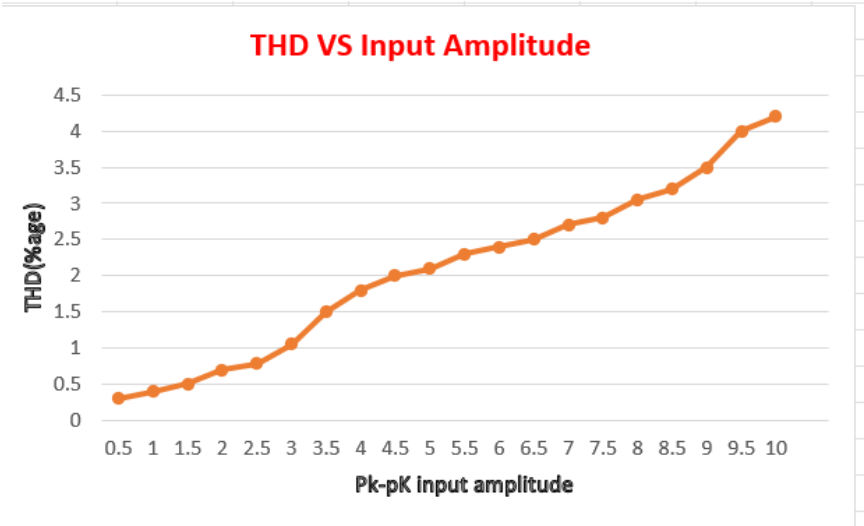

Figure 7.8 Linearity versus input amplitude.

Linearity represents how accurately a random waveform (whose bandwidth is well within the amplifier bandwidth) will be represented at the amplifier output, which means the ideal linear amplifier should scale the waveform amplitude without altering the time domain information [112]. As explained in the chapter-5, linearity can be measured with the Total harmonic distortion (THD) or Harmonic Distortion$_3$ (HD$_3$) according to equation (7.4). Where H_1, H_3, and H_5 represent the peak power spectral density of the signal corresponding to different harmonics, usually 3rd harmonic is the major contributor, and even harmonics were not included in this expression due to the differential symmetry of all differential amplifiers for IA and VGA implementation [112].

$$THD = \frac{H_1^2}{H_1^2+H_3^2+H_5^2+H_7^2} \qquad (7.4)$$

Figure 7.8 represents the linearity of the VGA output signal versus IA input amplitude, as expected that linearity became worse with the input amplitude, especially at VGA high

gain compared to low gain. This degradation is happening because with increase in the input signal, the signal current is considerably high compared to the bias current, hence small signal gain will deviate from the nominal value and THD as well. Usually THD can be improved by increasing bias current, which will be power in-efficient. To improve the THD without increasing bias current, here are the following design practices have been adopted. 1. A strong degeneration for the open loop differential pairs with loop gain of 4 at least in the worst PVT corner [112]. Open-loop gain of a differential pair can be expressed as (7.5), where I_D, R_s, and V_{TH} represent the bias current, degeneration resistance and the Threshold voltage of the NMOS differential pair transistor, respectively [113].

$$Loopgain_{open-loop} = g_m R_s = \frac{2I_D R_S}{V_{gs}-V_{Th}} \quad (7.5)$$

The open loop gain can be increased by increasing the bias current or increasing the degeneration resistance. 2. Make sure the small signal current is not more than 20% of the current such that the linear model of the transistor represents the dynamic behaviour. 3. Adjusting the output common mode voltage of the differential pair such that every transistor drain to source voltage (V_{DS}) is greater than the over-drive voltage (V_{OV}) of the devices [113]. 4. By using Metal Oxide Metal (MOM) or Metal Insulator metal (MIM) capacitors instead of the active capacitor formed with the MOS transistors will improve the linearity. 5. Choosing the input common mode voltage of the differential pair close to the V_{th}+2*V_{OV} will ensure the desirable voltage across the tail transistor to ensure the bias current is alive under PVT corners. Figure 7.9 shows the ADC output (Digital) for the 100uV pk-pk differential input to the IA. This has been simulated with the RCC extracted netlist under 125^0C temperature and slow process corner. The y-axis represents the Kilo LSB, and the x-axis represents the time.

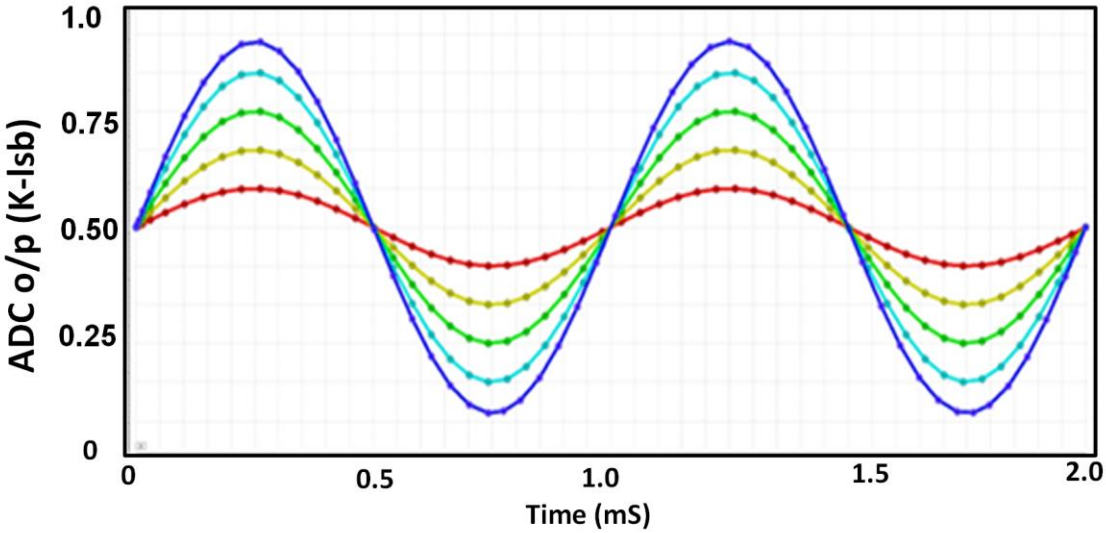

Figure 7.9 ADC output waveform.

7.4 Full Chip Layout Design

The full chip schematic was implemented, which consists of all the blocks given the block diagram. It consists of the following pins, as shown in the table7.1

Table-7.1: Pin Description

Pin name	In/Out	Description
Vdd_1V	In	High voltage supply used for the analog blocks
Vdd_0.8V	In	Low voltage supply used for the digital core.
Vss	In	Global ground pin
Inp&Inn	In	Differential input signals (Connected to the ac coupling capacitors)
Clk	In	10MHz sampling clock for the ADC
RST	Reset	This is to rest the internal states in the ADC decimation filter counters.
Cont<3:0>	In	Digital Control signals
ADC_Out	Out	ADC outputs digital signals
Atb	Out	Analog testing bus

The complete chip layout was developed in 45nm TSMC CMOS High performance (HP) technology with 11 metals for the routing and 1poly layer. It is a very standard technology, and no native or special devices were used in part from thin, thick oxide transistors and poly resistors, whose sheet resistance is 700 ohms per square sheet.

Full chip layout has been developed with the cadence layout-XL tool, which occupies a 2mm*1.1mm active silicon area and includes 10pF decoupling capacitors (to filter the supply noise generated by DSP) and bond pads.

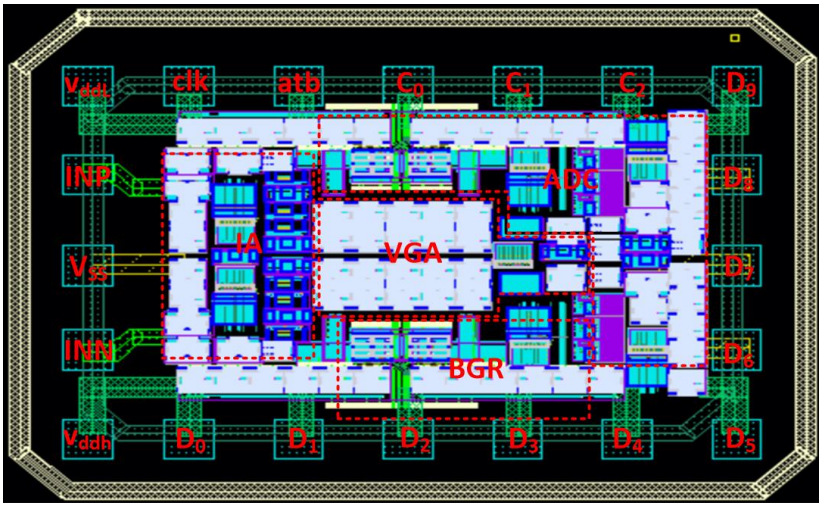

Figure 7.10 Full-chip layout.

Figure 7.10 shows the snapshot of the layout, where all respective bumps were named as follows. INP&INN represents the ECG signals from electrodes, and VDDL & VDDH represents different voltages used for the entire circuit. $OP_{0\text{-}9}$ represents ADC output. The consideration required for each block has been given in a detailed manager corresponding to that chapter. Apart from integrating all the blocks, added a power ring in the 10^{th} metal layer around the chip to connect the solid power supply to the respective block because any higher series resistance will cause not only a DC drop but also create switching noise at 10MHz frequency. A ground pad ring in M9 has been distributed around the chip. A 2pF (at least) decoupling capacitor is added locally to each block. Also, a distributed 20pF accumulation MOS capacitors (kind of n+ diffusion in n-well) based decoupling capacitor was added wherever there is some area available and filled the MIM caps underneath the pads. Vertical symmetry has been used for the differential pairs and matched output lines (which means interconnects between the IA and VGA). Signal bumps are placed on top of the n-well islands to reduce the parasitic capacitance, whereas power bumps are placed on top of the normal P-substrate [114].

7.5 Summary

A low-power and high sensitive sensor for ECG signal extraction have been developed in 45nm CMOS technology, and performed post-layout simulation was presented at the chip level. The type of extraction used was RCC couple type, which means it includes every metal resistance and coupling capacitance between all the nets. Compared to the published results, the presented work pushes state in the art by several aspects like high-frequency CMRR in the IA by 18dB, and VGA gain range variation has been stabilized by 5.6dB. Furthermore, a time domain ADC has been introduced, which will be very compatible with CMOS technology, and the main important achievement is the elimination of the opamp required for the integrator. Also, VGA noise has been reduced due to the limited usage of the degeneration gain reduction in the VGA stage. The developed chip area is 2mm*1.1mm, mostly dominated by the decoupling capacitors and bond pads.

The next chapter summarizes the thesis work and explains directions for future work to push the state-of-the-art ahead.

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Chapter 8: CONCLUSIONS AND FUTURE WORK

8.1 Conclusions and future work

8.1.1-Conclusions

The main aim of the present project is to Analyse, design and simulate a biological signal Sensor (to be specific ECG signals) with an input sensitivity of 100uV while consuming low power. Also, the existing circuits are operated from a higher power supply (mostly 1.5V and above), so the objective is to develop new circuit architectures to operate under supply voltage as low as 1V. Integrating the ECG sensor with a microcontroller or a small DSP is necessary to process the digital input data. DSP-based data processing is relatively easy compared to analog due to the existing mathematical operations like multiplications. The achievements in this thesis are listed as follows.

1. **Bandgap Reference(BGR)**: Traditional BGR is designed with many BJTs (typically 25 with some dummy devices) and consumes very high power because it runs from a 1.5V supply. I proposed a single BJT-based solution (hence a very compact layout and area) in this work. This BGR design achieved 1% pre-trim accuracy and 12.4ppm/^{0}C temp coefficient over the industrial temperature range of -40-125^{0}C. This solution operated from a 1V supply and has a PVT variation of 0.5% while providing 520mV output voltage. Also, a new start circuit simulation methodology has been proposed by forcing a high-impedance node in the circuit from an external voltage source and searching for zero current operating points. This will enable the designers to know about any hidden, stable unwanted operating points; hence it improves the reliability over the volume production [115]. In the existing papers, designers exploited running a large number of simulations over Monte Carlo to catch the start-up problem. Unfortunately, this is time-consuming as well as model dependent. Opamp design has been explained from the BGR systematic offset results point of view, and design methodologies have been explained. As well as the technique to bias the opamp with bandgap

core PTAT current, such that the opamp output will track the bandgap required voltage with respect to the temperature.

2. **Instrumentation Amplifier (IA)**: In this work, a current re-using folded cascade opamp has been proposed, which results in 6dB better-integrated Root Mean Square (RMS) noise for the same power consumption. A capacitive feedback-based IA has been designed, which achieved 40dB voltage with 18MHz upper cut-off frequency and 100mHz lower cut-off frequency. This solution consumes 8.67uW power from a 1V operating power supply. Also, due to the low noise nature, the Noise Efficiency Factor (NEF) has been improved to 2.41, which is 20% better than the state-of-the-art. NEF is a very good Figure of Merit (FOM) parameter to compare this work design with respect to other designs from power, bandwidth and noise perspective. Ideal NEF is 1 for a noise-less single transistor-based design.

3. **Variable Gain Amplifier (VGA)**: Existing VGA architectures use degeneration resistor-based voltage gain tuning. Though this has excellent linearity, the noise resulting from the tail transistor is a serious problem. Because without degeneration, tail current source noise will not appear at the output, whereas due to the degeneration, the noise will be converted as differential and results in poor SNR. Also, the conventional VGA has more than 12dB PVT variation due to the on-chip resistance variation (23%). The minimum gain setting value has to be adjusted according to the PVT range to meet the specific gain range. For example, if the minimum voltage gain is 20dB and the PVT variation is 12dB, then the maximum gain would be around 32dB. So in this work, a PVT-insensitive VGA has been designed with a negative feedback loop, which adjusts the bias current to maintain the target range. Simulation results show that 5.4dB decrease in the PVT spread while consuming 56uW power, which is 43% lower than the existing start of design power.

4. **ADC**: This work demands a very low sampling rate ADC with moderate resolution (~10b) because the input signals are very low bandwidth nature while consuming very minimal power. A common choice would be a continuous time Sigma delta ADC with op-amp based integrator. Unfortunately, this architecture heavily depends on the transistors' Analog properties. In CMOS, 45nm technology transistors are digitally friendly and designing high-gain opamp would very challenging without using gain enhancement techniques like cascade and regulated cascade techniques. In this work, a passive integrator-based time-domain ADC has been proposed. Mainly input voltage was converted as a duty-cycle modulated digital signal. A master-slave counter-based decimation filter is designed to extract the duty cycle from the comparator output and convert it into the digital output. This is the first in literature without using any op-amp in the ADC. This solution achieves 52.5dB SFDR and consumes 123uW power from a 1V supply. This ADC works up to 800mV supply voltage by design due to its highly digital nature.

8.1.2-Future work: The results that have been achieved in this work pushed the state significantly and showed different directions in the design, like time domain ADC. Here are the potential directions to improve the results further.

1. Bandgap reference: The single BJT-based design that has been proposed is successful in decreasing the area and mismatch, but there is little room to improve the PSRR and noise of the circuit, which may improve the sensitivity of the sensor. As explained in the introduction, the BJT occupies a lot of area in the silicon. Also, it requires special steps to have better quality devices like high current gain and lower leakage current. Hence there could be a different option for designing BJT less design. Probably NMOS transistor Vth can be used as a CTAT generator instead of the V_{BE} of the BJT.

2. **IA and VGA:** A current re-using IA has been discussed in this work, which shows 6dB better noise for the same power consumption. However, the achieved NEF is 2.41, which is 241% larger than the ideal. Hence there is room for its improvement. This can be done by exploiting noise cancellation techniques in wireless communications, where they create a phase inversion for several noise transistors and add them to get cancelled. This is one of the best ideas to exploit. Also, there has to be some method to stabilize the feedback pseudo resistance, which is often designed with sub-threshold transistors. This scheme provides very large resistance, but they are sensitive to the VT corner variation.

3. ADC: The presented time-domain ADC concept without using any operational amplifier is starting step for CMOS compatible ADC design innovative direction. Especially the opamp elimination reduced the power consumption significantly and made the design scalable for different technologies. Hence porting the design is simple. However, there are several potential circuit architectural improvements that can be done to improve the input referred offset and SNR. Especially the counter-based decimation filer can be improved by using synchronous counters. Also, a reference clock must be generated with-in the decimation filter to make ADC and DSP integration easy and to maintain the proper timing reference. Also, ADC can be designed to make it insensitive to clock jitter; at the moment, a large amount of clock jitter, around 2ps, will degrade the SNR performance.

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Appendix

Appendix A: Miller compensation used in the ADC buffer design

In this section, a detailed qualitative and quantitative explanation of Miller has been explained. The frequency compensation is required when there are several poles in the closed loop, which turns negative feedback into positive feedback due to the excessive phase lag. For instance, Figure A.1(a) shows a traditional amplifier (ignore C_C for the time being); the first and second stages will have parasitic resistance and capacitance of R_1, R_2 C_1, and C_2, respectively. The DC gain and poles are expressed as follows.

$$A_{dc} = g_{m1}R_1 g_{m2}R_2 \tag{A.1}$$

$$P_1 = \frac{1}{R_1 C_1} \qquad P_1 = \frac{1}{R_1 C_1} \tag{A.2}$$

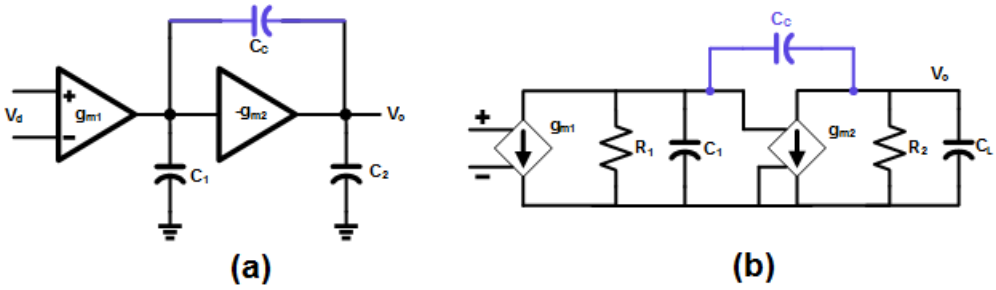

Figure A.1 Miller compensation scheme (b) Small signal Representation

Since P_1 and P_2 are relatively close, the Phase margin (PM) is very poor. Occasionally this will be less than 30^0, so there will be several ringing in the time domain or step response. Hence there must be a way to separate the poles either by increasing the transistor g_m or the load capacitance. Several compensation techniques were presented in the literature, in that dominant compensation is simple and widely used. A large capacitor will be added to the node corresponding to the dominant pole; hence its phase shift due to that capacitance reaching 90^0 and decreases the Unity Gain Bandwidth (UGB); hence Phase margin will improve at the cost of the UGB. One advantage of this technique is circuit will be un-conditional stable, which means under any load

current/capacitance circuit step response will be well-behaved (which means over-damped). Due to the large compensation capacitor usage, this is the on-chip solution and is preferred mostly in the discrete opamps. From the area point of view, on-chip solutions are often miller compensation preferred. In this section, miller compensation has been explained qualitatively and quantitatively. Fig:8.1(a) shows the concept of the compensation, a small compensation capacitor (C_C) will be added around a large negative gain stage to enable the capacitor multiplication action. Looking from the output node of the first stage, the voltage across the C_C will be bootstrapped, and hence the amount of charge it draws will be amplified. This means the resultant capacitance will have increased by the gain of the second stage, and it can be expressed as follows.

$$C_{1st-stg} = C_1 + C_C(1 + g_{m2}R_2) \tag{A.3}$$

The capacitance amplification holds true only if the second stage bandwidth is higher than the P_1 location. Otherwise, the input impedance is dominated by virtual resistance [116]. Also, there must be negative feedback around the second stage; otherwise, the DC operating point will not be defined when the devices mismatch includes in the simulations. The stand-alone amplifier shown in 8.1(a) doesn't work since there is no dc feedback, but every op-amp will be considered in either inverting/non-inverting mode always; hence the external global feedback will enable the miller amplification. Due to the capacitance amplification, the first pole frequency decreases by the gain of the second stage, as expressed in (A.4)

$$P_1 = \frac{1}{(C_1 + C_C(1 + g_{m2}R_2))R_1} \tag{A.4}$$

This is the same as the dominate compensation without using the large capacitor. However, there is some additional advantage compared to dominate compensation while considering the P_2. Once the frequency exceeds the P_1, the second stage input is an AC ground. Hence the output resistance looking from the stage will decrease due to the

negative feedback around g_{m2}. The approximate output resistance and pole frequency can be expressed as follows. Compared to the pre-compensation second pole location, post-cost compensation pole frequency has increased significantly. This is called pole splitting, and in a way, it will improve the damping as it is directly proportional to the ratio of P_1 and P_2.

$$R_2 = \left(1 + \frac{C_1}{C_C}\right)\frac{1}{g_{m2}} \tag{A.5}$$

$$P_2 = \frac{g_{m2}}{C_2}\frac{1}{1+\frac{C_1}{C_C}} \tag{A.6}$$

The above explanation about pole splitting is very intuitive and gives several insights into design optimization. Even if the first-stage output pole and second-stage output poles swap their positions, pole splitting still happens. So this compensation makes the dominant pole more dominant and makes the non-dominate pole more non-dominate in-order to split the poles. A small signal analysis is very useful for finding the exact pole location. Fig: 8.1(b) shows the small signal equivalent of Fig:8.1(a), where the output resistance of both amplifier stages hasn't been drawn to simplify the circuit. The following equations represent the KCL at the output of the stages.

$$V_1(g_{01} + sc_1 + sc_c) - V_0(sc_c) = -g_{m1}V_{id} \tag{A.7}$$

$$V_1(g_{m2} - sc_c) + V_0(g_2 + sc_2 + sc_c) = 0 \tag{A.8}$$

Solving the (A.7) & (A.8) for the output voltage will result in a 2nd order transfer function with a right half zero as expressed in (A.9).

$$\frac{V_0}{V_{id}} = \frac{g_{m1}g_{m2}\left(1-\frac{sc_C}{g_{m2}}\right)}{As^2+Bs+C} \tag{A.9}$$

Where A=$c_1c_2 + c_1c_C + c_Cc_2$

And B=$c_C(g_{01} + g_{02} + g_{m2})$+$c_2g_{01}$+$c_1g_{02}$

And C=$g_{01}g_{02}$

We can infer several interesting points from the transfer function. There is Right Half zero (RHZ), whose value depends on the compensation cap, so there will be little compromise on the phase margin. Any feedforward path around an amplifier will create a zero. If the feed-forward path and amplifier have opposite gain polarities, then the zero will be a right-half plane. Here G_{m2} is inverting stage (to ensure negative feedback for comp cap), and C_C will provide positive gain; hence the zero is on the right side.

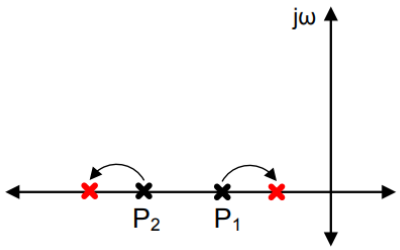

Figure A.2 Pictorial representation of pole movement with the Miller compensation.

Figure A.2 shows how the poles will move with the compensation in the Pole Zero plane. Before compensation, they were represented as P_1 and P_2 (black colour), but after the compensation, they moved according to the arrow directions. This is exactly the same as the dominate compensation without using the large capacitor. Due to the pole movement, the Unity Gain bandwidth (UGB) mostly depends on the g_{m1} and Cc, as expressed below.

$$UGB = \frac{g_{m1}}{2\Pi C_C} \qquad \text{(A.10)}$$

From (A.10), it is easy to infer that small C_C will result in better bandwidth, but this is only valid when C_C is very large compared to C_1. There have been several techniques to mitigate the RHZ to improve the Phase margin. By some means, the feed-forward path around the gm2 needs to be a break but without removing the feedback through C_C. This can be done in three ways.

1. Adding a resistor in series with the capacitor like a Proportional and Integral(PI) controller. If the resistance is equal to $1/g_{m2}$, then the zero will move to a very high frequency. However, whenever the gm2 changes the PVT variation, resistance becomes different than required and decreases the zero frequency. Some researchers increased the resistance beyond this value to boost up the phase margin but the cost of making the circuit sensitive to the device mismatches.

2. Adding a current buffer in series with the resistor (which will only absorb the current from g_{m1}, not from g_{m2}). This is the best known Zero compensation technique due to PVT's insensitive nature, and there are no limitations on the output swing. This is also called Ahuja compensation, just by reusing the current of the current buffer to make it power efficient.

3. Adding a source follower (SF) in series with the second stage blocks the feedforward current and presents low impedance. Unfortunately, this will limit the output swing. Hence it is not useful for high-swing applications.

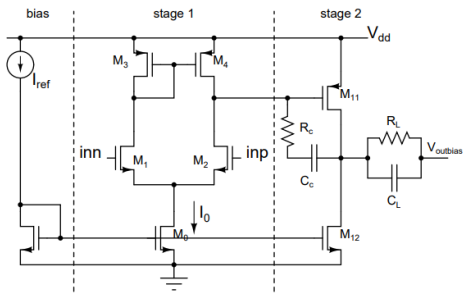

Figure A.3 Transistor implementation of miller compensation.

Figure A.3 shows the typical transistor implementation of the miller technique with zero nulling resistors (R_C). Where M_1 and M_2 form the first-stage differential pair, M_{11} forms the second stage and R_L and C_L form the external load. Though this compensation is area efficient, it has the following disadvantages, so it must be used carefully.

1. The Power Supply rejection ratio (PSRR) is very important for the circuit applications like reference buffers for ADC and bandgap references. PSRR indicates the sensitivity of the output for a given disturbance in the supply voltage. Usually, PSRR at low frequency is dominated by the loop-gain (or opamp gain); hence it will be at least -40dB (means for a 1mV change in the supply, the output has 10uV output). For the Miller compensation, the high-frequency PSRR is problematic because there is direct capacitive coupling between the output and V_{dd}. Figure 8.3 shows that V_{dd} is connected to the first stage output by C_{gs} of the M_{11}, and this will be coupled to the output through C_C. Hence at a very high frequency, PSRR will be very poor. Hence Miller's compensation has to be used very carefully. In the present work, I have chosen lag compensation (next section) for better PSRR while sacrificing a little bit of area for ADC buffers.

2. The slew-rate of the will be limited by the I_1/C_C, whereas for other compensations techniques, this will be limited by the load capacitor. This is a serious trade-off because higher C_C is required for low noise (KT/C_C), but this will compromise the slew rate. Slew rate is an important parameter where the circuit senses fast edges (like ECG signals)

3. Here Compensation capacitor is connected between two nodes rather than references to a known potential like Vdd or Vss. So using a MOS capacitor is very challenging here as the two node potentials change over the PVT variation. Hence metal capacitors are the best option though they are not area efficient. Unlike supply decoupling capacitors, where one terminal is connected to Vdd, PMOS accumulation or inversion capacitors can be used. Usually, MOS capacitors result in 18 times capacitance while implemented in the same size. This is also another reason there will be significant results discrepancies between the design and lab measurements.

Appendix B: Lag Compensation

The main motivation for the present technique is to improve the PSRR, so there should be any capacitor connected in such a way that it will create a direct path from the V_{dd} to the output. Figure B.1 shows the traditional lag compensation. Here a series compensation network (R_Z-C_Z) has connected from the first stage output to the ground.

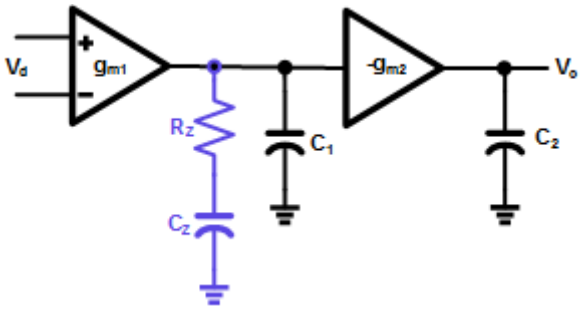

Figure B.1 Lag Compensation (Pole-Zero cancellation)

This technique will work based on the pole-zero cancellation technique, as the zero created by the series network will cancel the existing non-dominate pole and creates a high-frequency third dominant pole. The Compensation resistance R_z should be far lesser than the first stage output impedance (R_1) because adding R_z at the first stage output should have an impact that is only possible by adding a small resistance in parallel. Similarly, the compensation capacitor (C_z) should be very large compared to C_1 because we need to increase the capacitance at that node. Before adding the compensation network, let's say both poles are located before UGB and described as follows.

$$P_1 = \frac{1}{R_1 C_1} \quad \text{and} \quad P_2 = \frac{1}{R_2 C_2} \tag{B.1}$$

With the addition of the series network, the P_1 location will be decreased because the pole will depend on the sum of C_1 and C_C. Also, it creates a zero at a relatively high

frequency because it depends on R_z and C_z. The new pole-zero locations can be expressed as follows (B.2).

$$P_1^1 = \frac{1}{C_C(R_1+R_C)} \qquad Z_1 = \frac{1}{C_C R_C} \qquad P_2^1 = \frac{1}{C_1 R_C} \tag{B.2}$$

By design, we need to make sure Z_1=P_2 to enable the pole-zero cancellation (equation B.3) and place the P_2^1 close to the new compensated Unity Gain bandwidth of the amplifier (B.4). Using these relations, the compensation network values can be expressed as follows (B.5 & B.6).

$$\frac{1}{R_2 C_2} = \frac{1}{C_C R_C} \tag{B.3}$$

$$\frac{g_{m1} R_1 g_{m2} R_2}{R_2 C_C} = \frac{1}{R_C C_1} \tag{B.4}$$

$$R_C = \sqrt{\frac{C_2}{C_1 g_{m1} g_{m2}}} \tag{B.5}$$

$$C_C = R_2 \sqrt{C_1 C_2 g_{m1} g_{m2}} \tag{B.6}$$

The above equations were designed under the 45^0 Phase margin condition; anything above that phase margin demands more R_2. This has superior PSRR compared to the Miller compensation and better area compared to the dominant pole compensation, so I have used this compensation technique for the ADC buffer (interface between the Bandgap reference and sampling network). Generally, any frequency compensation results in a decrease in the bandwidth due to the dominant pole nature. Fortunately, in this compensation, the bandwidth degradation is not severe due to the pole-zero cancellation. One can easily mathematically prove that for 45^0 Phase margin, the achievable bandwidth is exactly the same as the open loop bandwidth. This bandwidth-preserving property makes the pole-zero/lag compensation very attractive for high bandwidth solutions.

Although this technique looks good, it relies on the pole-zero cancellation technique; hence, greater attention is needed towards Monte-Carlo sims as mismatch significantly alters the pole-zero location. Also, pole-zero cancellation techniques are prone to settle as there is a low-frequency long-tail settling component in the steps, which often limits the amount of bandwidth anyone can get from this kind of amplifier/buffer. In the present scenario, this is not a very big issue, as the ADC used in this project is having very sampling rate.

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