RADAR
Research Archive and Digital Asset Repository

OXFORD BROOKES UNIVERSITY

Mathew, M, Hart, BL and Hayatleh, K

Minimal Power Start-Up Circuit Design for Self-Biased CMOS Current Generators

Mathew, M, Hart, BL and Hayatleh, K (2014) Minimal Power Start-Up Circuit Design for Self-Biased CMOS Current Generators. *International Journal of Electronics Letters*, 2 (2). pp. 65-71.

doi: 10.1080/21681724.2014.880748

This version is available: https://radar.brookes.ac.uk/radar/items/77c24c04-fd67-4db9-9706-ce6682c6d224/1/

Available on RADAR: March 2016
Copyright © and Moral Rights are retained by the author(s) and/ or other copyright owners. A copy can be downloaded for personal non-commercial research or study, without prior permission or charge. This item cannot be reproduced or quoted extensively from without first obtaining permission in writing from the copyright holder(s). The content must not be changed in any way or sold commercially in any format or medium without the formal permission of the copyright holders.

This document is the post print version of the journal article. Some differences between the published version and this version may remain and you are advised to consult the published version if you wish to cite from it.

WWW.BROOKES.AC.UK/GO/RADAR

Minimal Power Start-Up Circuit Design for Self-Biased CMOS Current Generators

M. Mathew, B. L. Hart, and K. Hayatleh
Oxford Brookes University, Wheatley Campus, Oxford, OX33 1HX, U.K.
E-mail:khayatleh@brookes.ac.uk.

***Abstract*—A new start-up circuit configuration, with minimal standby power dissipation, is proposed for CMOS self-biased current generators. Using standard 0.13µm CMOS technology, simulation results show that for a supply voltage range 1.8V to 2.5V, and a temperature range −40ºC to +85ºC, the circuit standby power dissipation is less than 20nW.**

***Key Words*—CMOS Start-up circuit, Current- generator, Self-biased CMOS current generator.**

I. INTRODUCTION

THE self-biased current generator (SBCG) is a circuit scheme widely used for the generation of DC currents that are rail-voltage insensitive and , in some cases, PTAT (Proportional to Absolute Temperature) [1]. However, the SBCG is inherently bi-stable in nature and requires a start-up circuit to guarantee operation in the desired stable mode. Requirements that may be considered essential in a start-up design are that it operates from the same rail voltage as the SBCG, is isolated electrically from the SBCG when the latter is operating correctly and dissipates minimum standby power, certainly significantly less than that of the SBCG itself. Additional desirable requirements are the use of few components, preferably MOSFETS only, and simplicity in circuit design. These two sets of requirements constitute a useful list for a critical comparison of the performance of existing and proposed start-up schemes. A number of such circuits have been described in text books [2],[3] and in the patent literature (see, e.g., [4],[5]). That appearing [3] to satisfy all of the requirements of the list suggested above is discussed initially here. However, the analysis in Section II and simulated performance presented in Section IV below show it to be inferior with respect to standby power to that of a proposed circuit.

In the analysis, the MOSFET symbols and parameters have their usual meanings: thus, e.g, $|V_{TP}|$ is the magnitude threshold voltage of a P-channel device. Additionally for convenience in future discussion, nodal voltages, with respect to earth, are also used: thus the DC and time-dependent voltages at node 4 are, respectively, V_4 and v_4.

II. THE COMPARISON CIRCUIT ANALYZED

In Fig.1 the circuit configuration within the dashed contour is the start-up circuit [3] to which the proposed circuit is going to be compared. The rest of the circuit comprises an existing type of SBCG producing a rail-voltage-insensitive reference current $I_o=V_4/R$. The available output currents are I_3 and I_6. Ideally $I_3=I_6=I_o$ but channel length modulation in T_3 and T_6 causes each of I_3 and I_6 to be somewhat greater than I_o. Briefly, the operation is as follows: if the SBCG does not operate as intended when $V_1(=V_{DD})$ is applied then $V_4=0$, so T_7 is off, and T_8 is on because $(V_{DD} - |V_{TP}|) > 0$. The gate of T_9 is pulled towards V_1, consequently T_9 switches on and its drain current forces the SBCG into its intended operating mode.

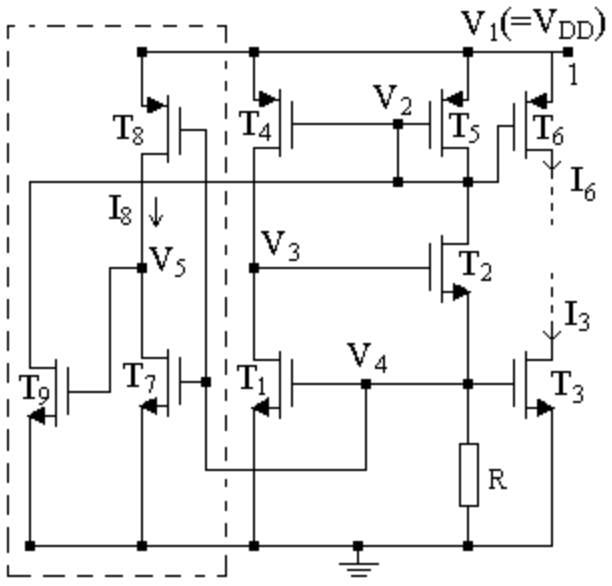

Fig.1 An existing SBCG, with the start-up circuit shown within the dashed contour.

Then $V_4 = I_oR > V_{TN}$, so T_7 switches on and V_5 falls below V_{TN}, thereby cutting off T_9 and isolating the start-up circuit from the SBCG. When the SBCG is on and operating correctly the following circuit equations hold.

$$V_1 \geq (V_3 - V_{TN}) + V_{SG5} \quad (1)$$

T_8 is on if,

$$V_1 - V_4 - |V_{TP}| > 0 \quad (2)$$

Substituting for V_1 from (1) into (2),

$V_1 - V_4 - |V_{TP}| \geq V_3 - V_{TN} + V_{SG5} - V_4 - |V_{TP}|$

(3)

But, $(V_3 - V_4) = V_{GS2}$ so (3) can be rewritten,

$V_1 - V_4 - |V_{TP}| \geq [(V_{GS2} - V_{TN}) + (V_{SG5} - |V_{TP}|)]$

(4)

The right hand side of (4) is greater than zero because, if T_2 and T_5 are both on then $(V_{GS2} - V_{TN}) > 0$ and $(V_{SG5} - |V_{TP}|) > 0$. The conclusion is that V_1 cannot be low enough for T_8 to be off when SBCG is operating correctly. Assuming T_8 operates in strong inversion its drain current is given by,

$I_8 = (\mu_p C_{ox} W_8/2L)[V_1 - V_4 - |V_{TP}|]^2$

(5)

To sink this current, T_7 must operate in the triode region with $V_5 << V_{TN}$ if T_9 is to be cut off with minimal sub-threshold drain current , I_9. As pointed out in [2] this means $W_7 >> W_8$. The standby power dissipation is $P_D = (I_8 + I_9)V_D \approx I_8 V_{DD}$, as $I_8 >> I_9$ because T_8 is on and T_9 is off. The non-negligible magnitude of P_D makes this start-up circuit unattractive for use in those systems where power dissipation is required to be minimal.

III. THE PROPOSED CIRCUIT

Fig. 2 shows the proposed circuit. In this case, time dependent variables refer to the waveforms describing the switching process in Section IV. Comparison with the configuration of Fig.1, to which it is similar, reveals one apparently small change in that the gate of T_8 is not connected to that of T_7 but is connected, instead, to the rail voltage, V_{DD}.

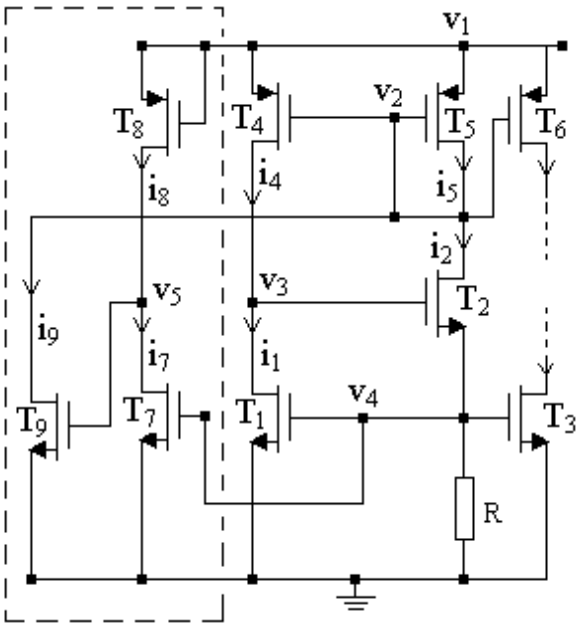

Fig.2 As in Fig.1 the proposed start-up circuit is shown within the dashed contour.

However, the change is not trivial but fundamental, because the design and operation are different. First, T_8 and T_7 always operate with sub-threshold drain leakage currents; second, as will be seen, a required condition is that $W_8 >> W_7$ whereas it is $W_7 >> W_8$ for the circuit of Fig.1. It is known [6] that, for a given drain voltage, the sub-threshold drain leakage current of a MOSFET is proportional to the ratio $\mu C_{ox} W/L$. Thus the drain leakage current of T_8 exceeds that of T_7 if , for the case $L_p = L_n$, $(\mu C_{ox})_p W_P >> (\mu C_{ox})_n W_N$. Now, for short channel lengths [7], $(\mu C_{ox})_p \approx (\mu C_{ox})_n/4$ so we require $W_8 >> 4W_7$. Using an engineering design factor of 10 to replace the 'much greater' sign the inequality can be met by having $W_8 \geq 40W_7$. The significance of this choice is clear from Fig.3. Curves A and B refer respectively, to the DC characteristics of T_8 and T_7 as a function of V_5. To cater for the general case the I_D axis is not dimensioned. The choice $W_8 >> W_7$ ensures that curve A lies well above curve B up to the intersection point at $V_5 = V_X$ and that V_X is significantly greater than the gate source voltage (V_{TN}) at which T_9 starts conducting. After V_1 is applied, the drain voltage of T_7 rises towards the DC equilibrium point V_X. However, T_9 switches on when its gate voltage reaches V_{TN} and activates the SBCG. As in the case of Fig.1 the gate voltage of T_1, now at $V_4 = I_o R$, switches on T_7, causing T_9 to cut off and isolate the start-up circuit from the SBCG. The standby power dissipation of the start-up circuit is now minimal because only sub-threshold drain current leakage currents flow in T_7,T_8 and T_9.

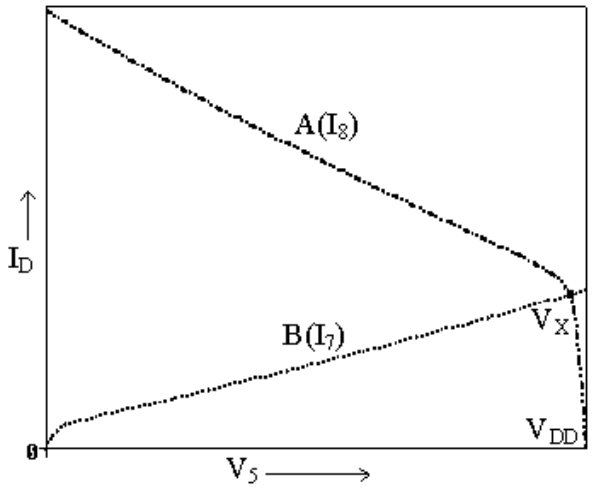

Fig.3 Curves A and B refer, respectively, to the DC characteristics of T_8 and T_7 in Fig.2.

IV. RESULTS AND DISCUSSION

TABLE I

POWER DISSIPATION (P_D) DATA FOR FIGS.1,2

		V_{DD} (V)	
	T(ºC)	1.8	2.5
P_D(start-up circuit) Fig.1	-40	375µW	1056µW
	+27	303 µW	951µW
	+85	253.14 µW	888.20 µW
P_D(start-up circuit) Fig.2	-40	48.24pW	96.15pW
	+27	1.33nW	2.51nW
	+85	9.08nW	16.50nW
P_D(current generator)	-40	360.23µW	550.16µW
	+27	369.16 µW	560.44 µW

Figs. 1,2	+85	378.05μW	572.62μW

The circuits of Fig.1 and Fig. 2 were simulated using CADENCE PSpice Level 7 parameters.

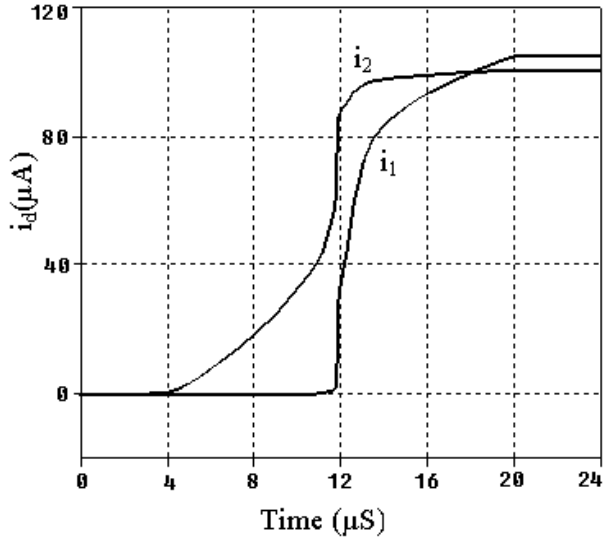

Fig.4 Current waveforms for Fig.2: T=27ºC.

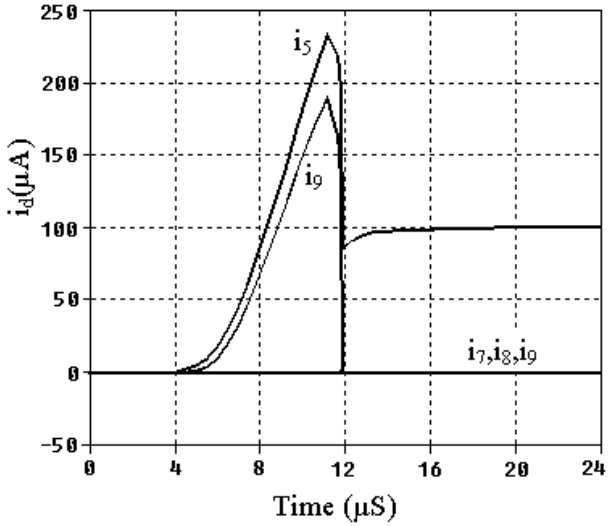

Fig.5 Further current waveforms for Fig.2: T=27ºC.

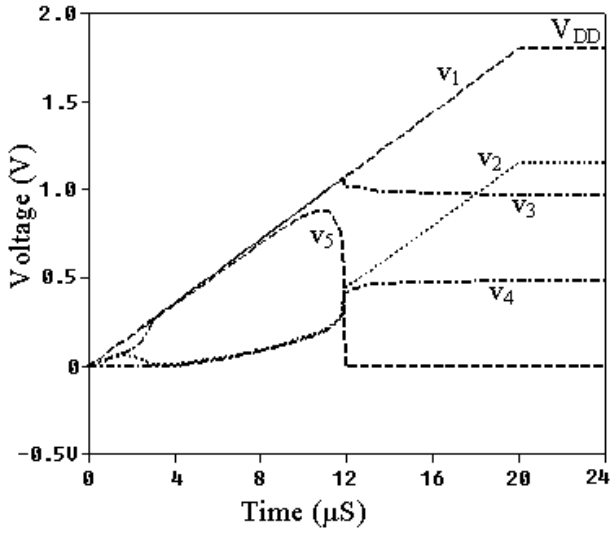

Fig.6 Voltage waveforms for Fig.2: T=27ºC.

V_{DD} was chosen to be 1.8V and I_o to be 100μA for which R=4.8kΩ, corresponding to V_4=0.48V. For all the MOSFETs L=0.13μm; for both circuits W_1=W_2=W_4=W_5=W_6=5μm and W_9=1μm; for Fig.1, W_7=40μm and W8=1μm, whereas for Fig.2, W_7=1μm and W_8=40μm. The choice W=40μm satisfies the suggested design choice mentioned in Section III. DC tests were made to determine V_X in Fig.3 and the start-up power dissipation, P_D(su) and the SBCG power dissipation, P_D(cg) for the circuits of Fig.1 and Fig.2 for the temperature range +85ºC≥T≥−40ºC: T=27ºC is taken to represent room temperature. It was established that Vx>1.4V for V_{DD}=1.8V and Vx>1.77V for V_{DD}=2.5V. Power dissipation data is presented in Table 1. The case V_{DD}=2.5V was simulated to show the increase in P_D(su) for Fig.1 compared with that of Fig.2 when V_{DD} was increased. The comparative constancy of I_o with variation V_{DD} and T, a characteristic of the SBCG for the case of a temperature-independent R (assumed here) accounts for the P_D(cg) figures shown.

It is clear that P_D(su) is significantly lower for the proposed circuit than that of Fig.1 for V_{DD}=1.8V. The start-up circuit of Fig.1 is obviously inappropriate because its power dissipation is comparable with that of the SBCG at V_{DD}=1.8V and exceeds it for V_{DD}=2.5V. The operation of the proposed start-up circuit in Fig.2 is clarified by cross-referencing the drain current waveforms of Fig.4,5 with the voltage waveforms of Fig.6. To obtain these waveforms the power supply rail (v_1) was applied in the form of a continuous train of trapezoidal voltage pulses with base level zero, amplitude V_{DD}, voltage-level transition times t_t, and a pulse duration t_d (>> t_t). As t_t is not known to the designer beforehand, four widely spaced values of t_t were used in simulation tests: 20ns, 20μs (that shown), 2ms and 2s. Following the application of v_1 at t=0, v_5 rises as the current (i_8-i_7) charges up the capacitance associated with the gate of T_9 and i_9 rises from a sub-threshold level, at about t=4μs when v_5>V_{TN}. Then i_9 rises to a peak, the duration of which depends on the time taken for the SBCG, and hence T_7 to switch on. The switch-on process involves a regenerative feedback action that causes a jump in

i_1 and is responsible for the fast trailing edge of i_9. Note that i_2 leads i_1; that is because T_1 cannot switch on until the potential difference i_2R exceeds V_{TN}. The drain currents i_7, i_8, and i_9 after t=12μs, appear to lie on the current axis because they are too small to register on the current scale used. When the SBCG is on, I_1 is slightly different from $I_2(=I_o)$, despite the fact that $W_4=W_5$, because their drain-source voltages are different. Tests for t_t=20ns, t_t=2ms and t_t=2s produced waveforms similar in shape to those of Fig.4,5 and Fig.6 but with different time scales. The energy consumed by the start-up circuit in switching on the SBCG, estimated from the product $V_{DD} \times \int_{t=4\mu s}^{t=12\mu s} i_9 dt$ is approximately 1nJ.

V. CONCLUSIONS

A list of requirements has been suggested for comparing the performance of existing and proposed start-up circuits for self-biased current generators (SBCG). An important requirement of the list is minimum standby power because once the SBCG is on and operating correctly the start-up circuit performs no useful function.

A new start-up configuration has been presented and shown to meet all the requirements of the list. The standby power dissipation, in the nW range, has been shown to be minimal and current and voltage waveforms have been obtained to illustrate circuit operation

Although the design dealt with a particular SBCG and particular values of V_{DD} and I_o, the configuration can be considered universal in that it can be used , or adapted for use, with other types of SBCG (see e.g,[1]) and other value of I_o and V_{DD} provided the MOSFETs employed have the appropriate voltage ratings and associated channel lengths.

VI. ACKNOWLEDGMENT

The authors thank Professor F. J Lidgey of Oxford Brookes University, Oxford, U.K, for helpful comments during the course of the work described.

REFERENCES

[1] M. Mathew, B.L Hart, and K. Hayatleh, " Rail-supply insensitive CMOS current generator," *International Journal of Electronics*, Nov.2012, Vol.99, No.11,pp 1569-1574.

[2] P.E Allen and D.R Holberg, Chapter 4, in *CMOS Analog Circuit Design*, 2nd Edition, Oxford University Press, 2002, pp149-150.

[3] P.R Gray, P.J Hurst, S.H Lewis, R.G Meyer, Chapter 4, in *Analysis and Design of Analog Integrated Circuits*, 5th Edition, John Wiley and Sons Inc, 2010, pp310.

[4] Chang-Yang Hsiao , "Current bias circuit and current bias start-up circuit thereof," U.S Patent US7,342,439 B2, March 11,2008.

[5] A. Stellberger and F. Schwiderski , "Start-up circuit for band-gap voltage reference generators," U.S Patent US2011/0006749 A1, Jan. 13, 2011.

[6] F. Fallah, and M. Pedram), "Standby and active leakage current control and minimization in CMOS VLSI circuits," *IEICE Transactions on Electronics*, April 2005,Vol.E88-C,No.4, pp 509-519.

[7] T.C Carusone , D.A Johns and K.W Martin, Chapter 1, in *Analog Integrated Circuit Design*, 2nd Edition, John Wiley and Sons,2013, p54.