A Novel Sub-1V Bandgap Reference with 17.1 ppm/^{0}C Temperature coeficient in 28nm CMOS

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***Abstract*— Traditional Banba bandgap is very popular in deep sub-micron CMOS technologies because of its sub 1V output nature. But unfortunately, it won't provide PTAT nature current and has several operating points, unlike two in the voltage mode BGR. This work analyzes the Banba circuit in a detailed way so that it's easy to demonstrate multiple stable operating and lists some of its other shortfalls. This paper presents a novel sub-1V bandgap architecture, which can provide PTAT current and sub-1V output without having multiple operating points. A modified self-bias opamp has been proposed to minimize the systematic offset and its temperature drift. A prototype was developed in 28nm TSMC CMOS technology and post-layout simulation results were performed. Proposed BGR targeted at 500mV works from 1V supply without having any degradation in the performance while keeping the integrated noise of 18.2µV and accuracy of 17.1ppm/^{0}C, while the traditional Banba was resulting 23.4ppm/^{0}C. Further, the circuit consumes 29.8µW of power and occupies 71*39µm^{2}silicon area.**

Keywords—BGR, noise, operating points, self-bias, offset phase-margin.

I. INTRODUCTION

Internet of things (IOT) and smart sensors are getting a lot of traction in the present era. The main bottleneck of these circuit realizations is to have an accurate reference voltage/current generator, which is through a Bandgap reference (BGR). The accuracy requirement of the BGR is becoming tight due to the high precision ADC development in sub-micro CMOS technologies, mainly under the low supply voltage domain. For example the least significant bit (LSB) of a 10b ADC in 1V is approximately 1mV. To keep the SNR close to the ideal value (66dB), the accuracy of the bandgap should be very less compared to this.

[1][2] proposed the very first BGR principle in 1977, which is basically scalled summation of Proportional To Absolute Temperature (PTAT) and Complimenray to Absolute temperature (CTAT) voltages. Afterwords this became very popular in CMOS as a voltage mode BGR. Unfortunately this circuit delivers an output voltage of 1.23V and requires a higher power supply voltage. A hidden advantage of this voltage mode architecture is having inherent PTAT current, which is very useful to bias circuits like Voltage Controlled Osillators (VCO) and temperature sensors. [3] Banba proposed a current mode BGR, which results in flexible output voltage rather than flexible 1.23V hence supply voltage can be close to 1V. This is very much desirable in the 45nm and advanced CMOS technologies. But unfortunately this circuit doesn't have any PTAT current availability and several other problems. [5] provides a modified version of the Banba to solve some of the problems, though this has a poor temperature coefficient.[5] provides several derivatives with few improvements but haven't provided a solid solution.

There is strong motivation to minimize the number of BJT's used in the BGR and several people proposed a single-BJT based low-area circuit, unfortunately they have demonstrated poor accuracy[6]. Also there has been tremendous research on the pure MOS-based BGR reference, through which very compact and nano power solutions are possible but they require a multi-point temperature trim.

The rest of the paper has been organized as follows. Section II analyses the Current mode bandgap reference and its limitations. section III explains the proposed solutions and it's comparison with the existing architectures. Section IV explains the concept of the proposed technique and finally, section V summarizes the simulation results.

II. CONVENTIONAL CURRENT MODE BGR

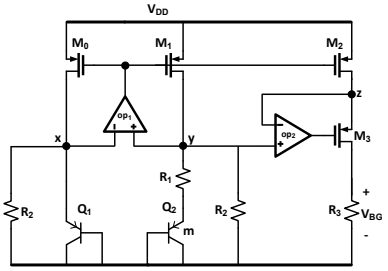

Fig. 1. Current mode Bandgap Schematic.

The main principle of bandgap reference is the scaled summation of CTAT and PTAT voltages. The V_{BE} of a BJT has -1.6mV/^{0}C temp coefficient, hence it can be used as CTAT voltage. The delta of the V_{BE} of two BJT's having different current densities will have a +ve temp coefficient, hence it can be used as PTAT voltage. Fig:1 shows the current mode BGR (Banba), where the voltage across R_1 is having a PTAT nature, hence the current will have a PTAT nature as expressed in (1), where n is the ratio of BJT's emitter area and V_T is the thermal equivalent of the diode[7].

The current through R_2 is having CTAT nature as expressed as (2).

$$I_{R1} = \frac{V_T \ln n}{R_1} \quad (1) \qquad I_{R2} = \frac{V_{BE1}}{R_2} \quad (2)$$

The sum of R_1,R_2 currents will flow through $M_{1,2}$ and by adjusting the ratio of the resistance, CTAT and PTAT component slopes can be canceled and hence Zero Temperature coefficient voltage can be generated across R_3 as shown in (3). As it is clear from this equation, the o/p voltage temperature can be minimized by adjusting R_2/R_p value. By adjusting the R_F, the output voltage can be achieved by less than 1V, and the supply voltage can be very less compared to the voltage mode BGR. This is the biggest advantage of the Banba BGR compared to the voltage mode BGR.

$$V_{BG} = \frac{R_3}{R_2}\left[\frac{R_2}{R_1} V_T \ln n + V_{BE1}\right] \quad (3)$$

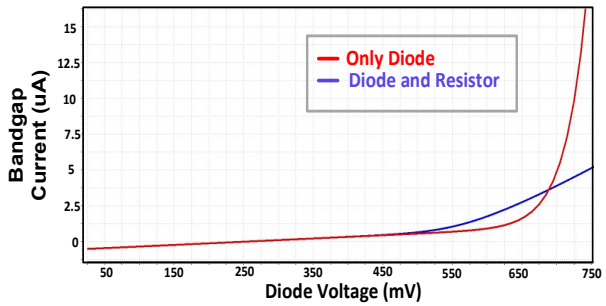

Fig. 2. BJT V_{BE} versus Bias current.

However this has several disadvantages as listed follows. 1. Typically V_{BE1} will have a slope of -1.7mV/^{0}C. For a typical BJT ratio choice of 24, the PTAT slope would be 0.274mv/^{0}C, hence the ratio of R_2 to R_1 has to be 6.2 for proper slope cancelation. For a 3uA bias current, the PTAT resistance R_P has to be 17KΩ. To get the zero temp coefficient-R_2 has to be 6.2 times compared to R_1, hence R_2 will be around 105.74 KΩ. To realize such a big resistance, need a large silicon area. Unfortunately in this architecture, there are two resistors were used, hence this architecture is area in-efficient. 2. Traditional voltage mode BGR has two stable operating points, one is desired and another one is undesirable zero current state. This architecture has multiple operating points. This is because the BJT's were shunted by pretty large equal resistors (R_2). So when the bias current is very low, it flows through R_2 because diodes/BJT's are in the off state. Until the voltage reaches close to the cut-in voltage of the diode, the current through the resistors is same hence all are stable operating points. Fig:2 shows a pictorial representation of the multiple operating points. In fig:1, PMOS and opamps were removed, injected a current and plotted the voltage of the X,Y, nodes. As shown in the fig:2, it has so many undesired operating points till 400mV and one desired solution at 683mV. This makes the start-up circuit design very complicated and needs to be designed to avoid all these points [8]. Whereas in the voltage mode BGR, there are only two operating points and hence very simple startup ckt is sufficient. Intuitively multiple operating points can be expected as follows, in the voltage mode BGR circuit the circuit is asymmetric by construction, whereas in the Banba circuit, it is symmetric by construction until the diodes reach on-state 3. The Bamba circuit only ZTAT current as an output, so in case of PTAT current requirement (for VCO or temperature sensor) there must be a separate circuit required, which will cost additional power 4. Also this architecture amplifies the opamp offset by a larger gain factor compared to the conventional BGR, because the opamp input terminals were loaded by the resistance and its resistance will go down. Hence any residual input-referred offset will be amplified by the larger gain, which will compromise the output temp-co. Expression (4) &(5) shows the output voltage only due to the opamp offset in the voltage mode and Banba circuits respectively.

$$V_{out} = V_{os}\left(1 + \frac{R_3}{R_1}\right) \quad (4)$$

$$V_{out} = V_{os}\left(1 + \frac{R_3}{R_1} + \frac{R_3(R_1+R_2)}{R_1 R_2}\right) \quad (5)$$

According to the authors, the main disadvantage of the Bamba circuit is its symmetry. Hence breaking the symmetry will solve the operating point issue. We are proposing a mixed-mode circuit, which keeps the main bandgap core same as voltage mode, while providing the sub-1V by adding a new auxiliary circuit to add PTAT current and V_{BE}, which results in ZTAT voltage.

III. Proposed Technique

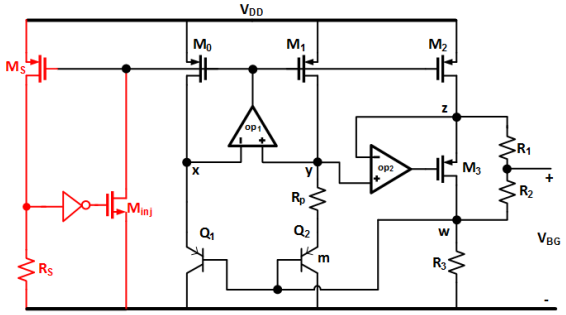

Fig. 3. Proposed mixed mode BGR.

Fig:3 depicts the proposed architecture, which consists of two sections. One is the PTAT loop formed by Op_1,Q_1,Q_2,R_p loop generate PTAT current, the only difference between the conventional one and this one is the base terminal of the BJT's were connected to a resistor rather vss. The current in the R_P is having PTAT nature. The second section consists of op_2,M_3,R_1,R_2,R_3, which will generate the adjustable output voltage (sub-1V) by adding the scaled summation of the PTAT current and V_{BE}. The PTAT current through M_2 will generate PTAT nature voltage at nodew. Op2 maintains V_W potential same as V_X and V_{DS} of M_3 is CTAT.

The voltage across R_2 is scaled version of the CTAT and output voltage can be expressed as (6). As it is clear that the output voltage can be achieved anything less than 1V by adjusting the R_1/R_2 ratio, while zero temperature coefficient can be achieved by adjusting the ratio of R_3/R_p.

$$V_{BG} = \frac{R_2}{R_1+R_2}\left(V_{BE1} + \frac{R_1+R_2}{R_2}\frac{R_3}{R_P}V_T \ln n\right) \quad (6)$$

The proposed solution doesn't have multiple operating points because the PTAT loop is asymmetric and there is no loading at the opamp input[9]. The only shortfall of this circuit is the finite beta effect of the Q_1,Q_2 which will corrupt with PTAT nature of the V_Z. Through simulation, we observed that the temperature coefficient degradation is very less due to this compared to the opamp offset amplification in the Bamba. The circuit shown in red colour represents the standard startup circuit, it basically senses the current and pull down the opamp o/p when there is no current.

IV. Self Bias Opamp and Design Techniques

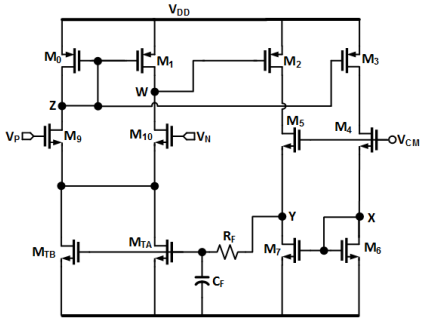

Fig. 4. Proposed self-Bias opamp.

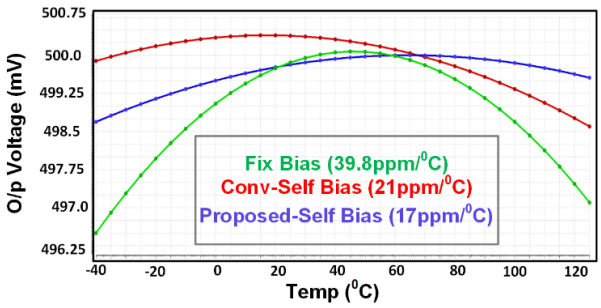

Fig. 5. Temp co comparision of the proposed self-bias..

Opamp design plays a significant role in the bandgap output performance easpecially output temp-co. Because the temperature drift of the opamp offset will be amplified and corrreputs output. In this design, two opamps have been used. Op1 which is in the PTAT current generation loop, whose offset has to be very low and mainly it has to be constant across the temperature[10]. Traditional fixed bias opamps will have an unacceptable offset because the bandgap current is PTAT and opamp current is constant, so both both won't track eacth other. [8] uses a self-bias technique, whose bias current tracks the BGR core current. By doing this opamp outputs (z,w nodes in fig:4) will be very close, hence less systematic offset. Unfortunately this proposal has very little gain in the bias network. Fig:4 shows the proposed self-biased opamp used in this design, where M_0,M_1,M_9,M_{10},M_{TA},M_{TB} forms the main opamp and M_2-M_7 forms the self-bias circuitry. M_2-M_3 senses the opamp current and produces a voltage at node y. In the traditional self-bias, only M2 and M7 exist and loop gain is lower. Equation (7) shows the loop gain of the conventional and proposed circuits. Self-bias loop should respond very slowly compared to the main bandgap loop, hence a 10KHz cutoff frequency lowpass filter has been included in the loop so that it doesn't influence the phase and gain margin[7][12].

$$LG_{traditional} = \frac{g_{m2}}{g_{m7}} \qquad LG_{Proposed} = \frac{g_{m2}}{g_{ds7}+g_{ds2}} \quad (7)$$

Fig:5 shows the simulated BGR output for fixed bias (means an external tail current reference to opamp), conventional self-bias and proposed self-bias and their ppm's are 39.8,22,17ppm/^{0}C respectively. Apart from the opamp design, bias current selection and BJT ratio and size also plays a vital roll in the performance[11]. A very high BJT ratio reduces the required PTAT gain (eq-6), hence opamp offset has less impact on the o/p, but very high ratio might create

V. Simulation Results.

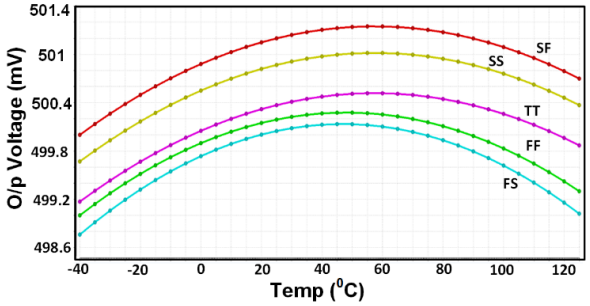

Fig. 6. O/p voltage vs temperature across PVT.

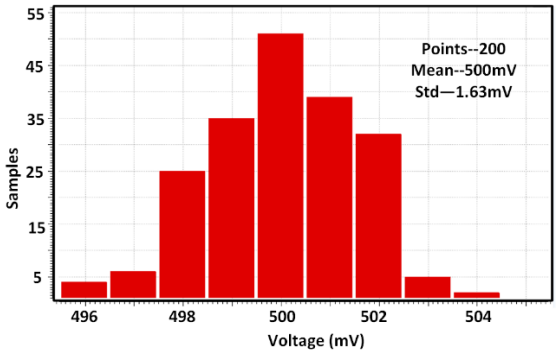

Fig. 7. Output mismatch histogram

The proposed BGR has been implemented in 28nm CMOS technology and post-layout simulations have been carried out. A mean voltage of 500mV has been targetted with 1V

supply voltage. Fig:6 shows the temperature drift of the o/p wrt Process, voltage corners. The worst case maximum voltage variation is ~1.41mV, means 17.1ppm/^{0}C temp-co over the temp range of -40-125^{0}C. Fig:7 shows the output voltage histogram as a result of 200 point MC sim, it reveals that standard deviation of 1.63mV, means +/-1% 3-sigma accuracy[15].

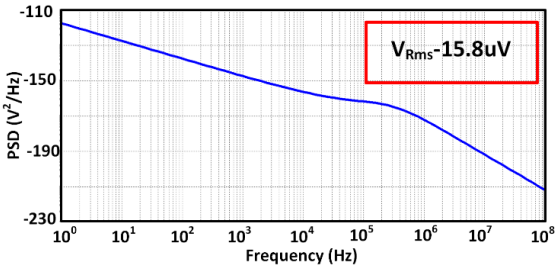

Fig. 8. Noise in Worst PVT corner

The opamp (op1) and pmos current mirrors are the major contributors, a chopping technique can be used to reduce this, but the major motivation in this paper is to solve the problems in the Banba architecture not to demonstarte the high accuraccy and also chooping requires a complicated output filter design[16]. Opamp input devices have been sized very high to reduce the threshold voltage mismatch and current source length has been decreased to minimize the g_m.

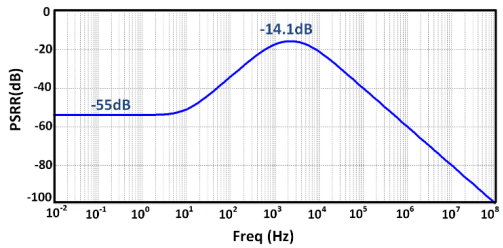

Fig. 9. Power supply rejection ratio (PSRR)

Fig:8 shows the simulated noise in the worst case PVT corner, the integrated noise ~ 15.8uV over the frequency band. Compared to existing current mode architecture, this is 12% lower due to the reduction of the opamp offset amplification gain. The main contribution is the opamp input referred noise. Fig:9 shows the PSRR of the proposed opamp, which has -14.1dB at 10KHz. Fig:10 depicts the layout of the BGR, which occupies 71*39um^2, which is almost 46% smaller than the Banba architecture (mainly because of CTAT resistance elimination).

VI. Conclusion

In this paper, a state of the art compact sub-1V bandgap reference has been proposed with 17.1ppm/^{0}C temperature coefficient. The main advantage of the proposed solution is it has PTAT current output availability and less number of operating points. Dis-advanatages of the Banba BGR have been studied qualitatively and quantitatively.

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