Minimising Impact of Wire Resistance in Low-Power Crossbar Array Write Scheme

Adedotun Adeyemo[1], Abusaleh Jabir[2], Jimson Mathew[3]

[2]Department of Computing and Comm. Technologies, Oxford Brookes University, UK.
ajabir@brookes.ac.uk.

[3]Department of Computer Science and Engineering, Indian Institute of Technology Patna, Patna 801103, India. jimson@iitp.ac.in.

[1]corresponding author: Adedotun Adeyemo

Address:
Oxford Brookes University
Department of Computing and Communication Technologies
Wheatley Campus
Oxford, OX33 1HX, UK

Email: 13121679@brookes.ac.uk

Date of Acceptance: 5 July 2017

Date of Publication: Dec. 2017

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

Minimising Impact of Wire Resistance in Low-Power Crossbar Array Write Scheme

Adedotun Adeyemo, Abusaleh Jabir, Jimson Mathew

Abstract– This paper presents a circuit level analysis of write operation in memristor crossbar memory array with and without line resistance. Three write schemes: floating line, V/2 and V/3 are investigated. Analysis shows that floating line scheme could also be considered reliable in arrays with aspect ratio of 1:1 and negligible line resistance just like the latter two schemes. Further analysis also shows that high density crossbar structures cannot be designed using any of the three schemes with worst case line resistance and data distribution within the array. To solve this problem, we propose a voltage compensating technique for write voltage degradation caused by line resistance during write operation on crossbar array. This technique is able to enhance write voltage in the presence of worst case line resistance and thus enable the design of higher density and reliable crossbar array.

Keywords– memristor, write operation, line resistance, crossbar array

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

1 INTRODUCTION

The demand for high density memory has motivated designers to further explore the use of crossbar architectures as the building block for emerging memory technologies. Emerging memories such as Resistive Random Access Memory (ReRAM), Phase Change Memory (PCM), [1, 2] and Spin-Transfer-Torque RAM (STTRAM) [3] are being aggressively investigated as a potential replacement for traditional memories. Continuous growth of traditional CMOS memories are currently being challenged by the scaling problem facing the transistor, hence the need for the semiconductor industry to speedily address reliability and other compatibility issues in emerging technologies. Crossbar architecture has been favoured for high density structures because of its simple structure and suitability with emerging two terminal devices. These emerging crossbar memories have a footprint of $4F^2$ and can be further optimised to $4F^2/n$ by stacking n-layers of crossbar arrays, where F is the minimum feature size. Memristive crossbar arrays are also applicable in the design of neuromorphic systems where the crosspoint memristor cells act as synapse in the network [4,5]. Information processing systems [6, 7] and logic circuit design are other areas that benefit immensely from the crossbar architecture [8–10].

Despite the simplicity of the crossbar structure, reliable read and write operation in passive crossbar memory structures could introduce some complexity into the structure. Reliability of read and write techniques have become key issues in emerging memory technologies and as integration complexity continues to grow, the problem becomes increasingly important [11]. Ideally, memristor-based memories are resistant to radiation induced soft errors but error might occur while accessing or writing into the memory [12]. Write error occurs when the voltage reaching the target cell(s) is insufficient to switch it to the desired state and/or the state of unselected cells are perturbed. Write voltage decay and sneak-path are some of the challenges with crossbar array during the write operation. Authors in [13] proposed a two-step write scheme to minimise the effect of sneak-path in the crossbar array, authors in [11, 14] also proposed techniques to apply voltages from both sides of the crossbar during the write operation but this alone does not offer proportionate improvement compared to the extra area taken by the peripheral circuitry.

This work focuses more on the write operation in crossbar arrays and presents a more detailed analyses of the performance of three crossbar write schemes. This will facilitate quick simulation of crossbar write operation analytically with improved accuracy. With these models, any $m \times n$ crossbar array can be solved analytically without the need to assume that all resistance values are the same. This paper also propose a novel compensated voltage technique for addressing the voltage degradation problem caused by wire resistance during write operation in larger crossbar arrays. This technique benefit from the existing technique of applying voltages from both sides of the crossbar as well as additional voltage from another voltage rail involved in the operation. The next section gives some background on memristive device as used in ReRAM. Section 3 explains the crossbar array model and its corresponding analytic model. Three crossbar write schemes are investigated in Section 4 with and without the effect of line resistance. Section 5 introduces a new write voltage compensating technique and we conclude in Section 6.

2 BACKGROUND

2.1 Memristive Devices and Memristive Memory

Memristor is a newly discovered fourth fundamental circuit element alongside the existing trio of resistor, inductor and capacitor [15–17]. Memristor was first theoretically proposed by Leon Chua in 1971 as the missing relationship between flux and charge [15]. It was argued that if the four basic circuit variables (voltage (v), current (i), charge (q), flux (φ)) are arranged in symmetry there are six possible combinations. All of these relationships are already established except for the relationship between flux and charge. Capacitor (C) is defined by the relationship between charge and voltage as $dq = Cdv$, resistor (R) is defined by the relationship between voltage and current as $dv = Rdi$. Similarly, an inductor (L) is defined by the relationship between magnetic flux and current $d\varphi = Ldi$. The two other relationships are $i = dq/dt$ (current is the time integral of charge) and $v = d\varphi/dt$ (Faraday's law, voltage is the time integral of φ). HP Labs announced

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

the first physical realisation of Chua's theoretically predicted memristor in 2008 [18], made of a thin film of semi-doped titanium dioxide sandwiched between two platinum electrodes. Research interest in memristor and its applications have increased significantly since HP Labs' announcement. Its memory application is the most widely explored area because of the possibility to design a memristor-based universal memory [18] - a memory that combines the density of DRAM, nonvolatility of Flash and speed of SRAM among others.

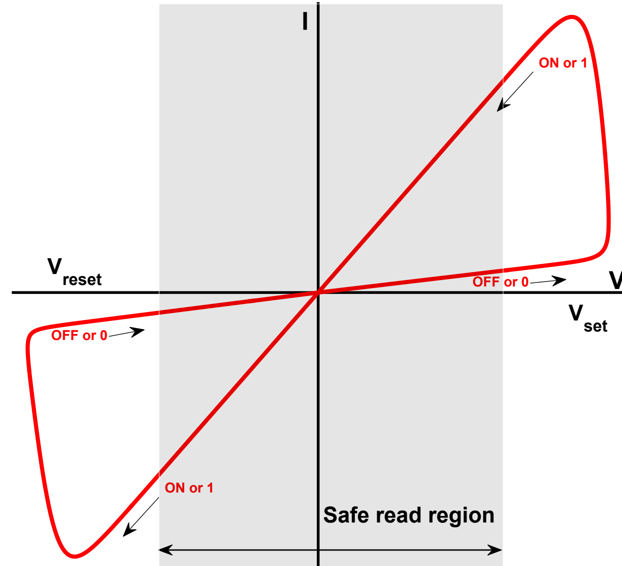

Figure 1: Memristor linear I-V curve showing switching between high and low resistance state in the presence of sinusoidal voltage source. V_{reset} and V_{set} are the write voltages required to write a logic 0 and 1 respectively.

Memristor stores data as resistance and the resistance value of the device can be changed by applying a voltage (V_{set} or V_{reset}) greater than its threshold voltage V_{th}. This causes the device to switch between High Resistance State (HRS) R_{off} and Low Resistance State (LRS) R_{on} depending on the amplitude and polarity of the applied voltage as shown in Fig 1. The switching from R_{on} to R_{off} is regarded as the RESETting process while the transition from R_{off} to R_{on} is known as the SETting process. The write voltage must be greater than the SET and RESET threshold voltage. Reading from a memristor involves applying a smaller voltage less than the threshold voltage of the memristor to one end and sensing the output at the opposite end of the cell. The region shaded grey in Fig. 1 represent the safe range for the read voltage where the state of the selected cell cannot be accidentally perturbed.

3 Memristor Crossbar Array

Crossbar architecture consist of two parallel sets of nanowires perpendicularly placed on one another. In memristor-based memories, a memristor cell is placed at every crosspoint in the crossbar. Crossbar architecture offers the possibility of building high density memories. Cells in the same row are connected together by the horizontal nanowires and cells in the same columns are connected together by the vertical nanowires. During the ideal write operation on cells in the crossbar array, a write voltage is connected to the wordline (bitline) of the target memristor cell and the bitline (wordline) is grounded. Other unselected lines can be left floating or partially biased as discussed in a later section.

Shown in Fig. 2 is a typical m rows (wordlines) and n columns (bitlines) crossbar array of memristors. Each memristor is represented by $R_{i,j}$, where i and j are the row and column index respectively. Assuming memristor $R_{1,1}$, circled in red is selected for write illustration, cells on the same lines (wordline and bitline) with $R_{1,1}$ are classified as *partially-selected* cells while others are unselected. All unselected and partially-selected cells are classified together as *unselected* cells. In summary, during the write operation on a single

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

cell, the crossbar array can be categorised into four groups as shown in Fig 2:

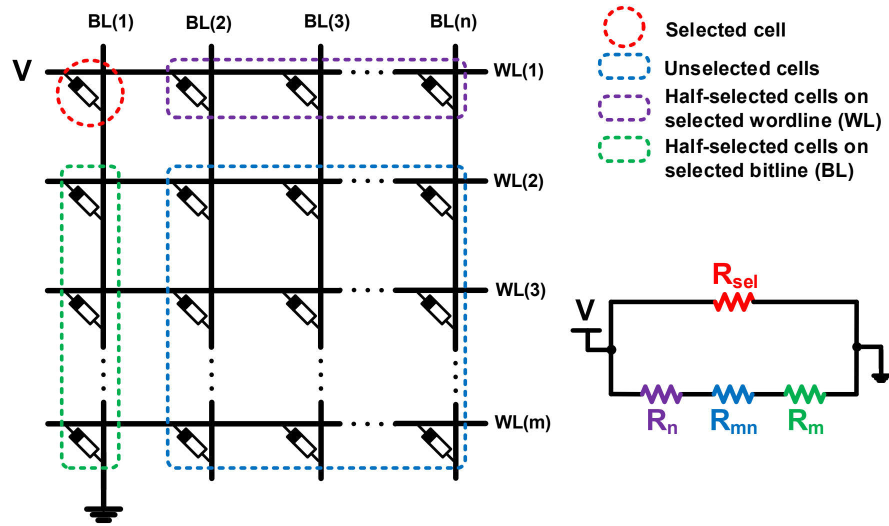

Figure 2: An $m \times n$ memristor-based crossbar memory structure set-up for write operation.

- Group I (R_{sel}): Cell selected for writing (red).
- Group II (R_m): Partially-selected $m-1$ cells on the selected bitline (green).
- Group III (R_n): Partially-selected $n-1$ cells on the selected wordline (purple).
- Group IV (R_{mn}): Unselected $(m-1)(n-1)$ cells that are neither on the selected bitline nor wordline (blue).

The groupings are made possible because all memristors in each group are in parallel with each other. Group II, III and IV will be collectively referred to as unselected cells in this work. If line resistances are ignored, the overall resistance of any $m \times n$ crossbar array can be simplified to the equivalent circuit shown in Fig. 2 with four resistance values. R_{sel} represents the selected cell $R_{1,1}$. R_m and R_n represent the row and column partially-selected cells respectively and R_{mn} simplifies the unselected cells [19]. Eqns. 1 - 3 shows the derived closed form solution for each group of resistance depending on the resistance value.

$$R_m = \frac{\prod_{i=1,i\neq i_s}^{m} R_{i,j_s}}{\sum_{i=1,i\neq i_s}^{m} R_{i,j_s}} = \begin{cases} \dfrac{R}{m-1} & \text{if all } R_{i,j_s} \text{ are equal} \\ \dfrac{R_{on}R_{off}}{(m-1)R_{off} - K_{off}(R_{off}-R_{on})} & \text{otherwise} \end{cases} \tag{1}$$

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

$$
\begin{aligned}
R_{mn} &= \frac{\prod_{j=1,j\neq j_s}^{n} \prod_{i=1,i\neq i_s}^{m} R_{i,j}}{\sum_{j=1,j\neq j_s}^{n} \sum_{i=1,i\neq i_s}^{m} R_{i,j}} \\
&= \begin{cases} \dfrac{R}{(m-1)(n-1)} & \text{if all } R_{i,j} \text{ are equal} \\[2ex] \dfrac{R_{on}R_{off}}{(m-1)(n-1)R_{off} - K_{off}(R_{off} - R_{on})} & \text{otherwise} \end{cases}
\end{aligned} \tag{2}
$$

$$
\begin{aligned}
R_{n} &= \frac{\prod_{j=1,j\neq j_s}^{n} R_{i_s,j}}{\sum_{j=1,j\neq j_s}^{n} R_{i_s,j}} \\
&= \begin{cases} \dfrac{R}{n-1} & \text{if all} R_{i_s,j} \text{ are equal} \\[2ex] \dfrac{R_{on}R_{off}}{(n-1)R_{off} - K_{off}(R_{off} - R_{on})} & \text{otherwise} \end{cases}
\end{aligned} \tag{3}
$$

Where i_s and j_s are the selected wordline and bitline respectively. K_{off} is the number of memristor cell in the off state (logic 0). When all the cells in the group are in the same resistance state, the equivalent total resistance is the ratio of the resistance value and the number of devices involved. However, this is usually not the case, each group will contain both low and high resistance state cells in reality. Hence, the need to derive models to cater for this real case as done in the 'otherwise' part of Eqns. 1 - 3 where each group is free to work with both high and low resistance state cells simultaneously. With these equations, any $m \times n$ crossbar array can be solved analytically without the need to assume that all resistance values are the same [20]. Each equation is derived from the assumption that all memristors in each group have similar resistance value of R or the more realistic case of each memristor having a value of R_{on} or R_{off}.

4 Analysis of Write Schemes

Write operation in resistive-based memories suffers from leakage current through other undesired paths in the crossbar. In traditional memories, selectors such as diode and transistor are used to prevent flow of unwanted current in the circuit but this usually introduces extra area overhead. As earlier mentioned, a write operation is carried out on cells in the crossbar array by passing a write voltage across the selected cell while biasing other lines in the crossbar. A write operation can be termed successful if the following conditions are satisfied: a) the selected cell(s) switches to the desired state and b) the state of the unselected cells are preserved. For the first condition to hold, the applied write voltage $|V_w|$ must be ideally greater than the SET (RESET) threshold voltages of the selected cell, this will ensure the cell switches to the desired new state. To preserve the state of unselected cells, the maximum voltage reaching them must be sufficiently less than their threshold voltages. A write failure occurs if one or both conditions are not satisfied. State of unselected cells can be disturbed if the unselected lines are not biased properly. Write failure could also be triggered by line resistance in the crossbar array. Line resistance weakens the magnitude of the write voltage reaching the selected cell(s) depending on its distance from the voltage driver, line resistance can be neglected in smaller arrays but becomes more prominent as array size increases. High line resistance prevents the selected cell(s) from receiving sufficient voltage across it in large crossbar arrays. An important figure of merit for write operation is the "write voltage window" - difference between the voltage reaching the selected cell and the maximum voltage reaching any of the unselected cells. Line resistance, data distribution and the choice of

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

biasing scheme are the major factors that affect the “write voltage window”, both will be further discussed in subsequent sections.

4.1 Write Operation without Line Resistance

This section analyses the operation of the three common crossbar write scheme in smaller crossbar arrays or arrays with negligible line resistance.

4.1.1 Floating Line Scheme

In the floating line scheme shown in Fig. 3, a voltage of $V(V_w)$ and zero are applied to the wordline and the bitline of the target cell respectively while other lines are unbiased. The selected cell in this scheme usually switches successfully, however, the state of the partially-selected cells on the selected wordline and bitline (group II and III in Fig. 2) might not be preserved depending on the structure of the crossbar array. In the floating line scheme, maximum voltage to unselected cells depends on the aspect ratio of array. Voltage disturbance in this scheme does not exceed $V_w/2$ when the aspect ratio is 1:1 ($m = n$) irrespective of the array size. This invariably implies that write operation will always succeed with this scheme when the crossbar array is square shaped as demonstrated by Fig. 4. It is also worthy of mention that a voltage of $V_w/2$ can cause a partial change of memristance value if applied long enough [13]. This analysis assumes that the voltage is only applied for the duration required to switch the selected cell.

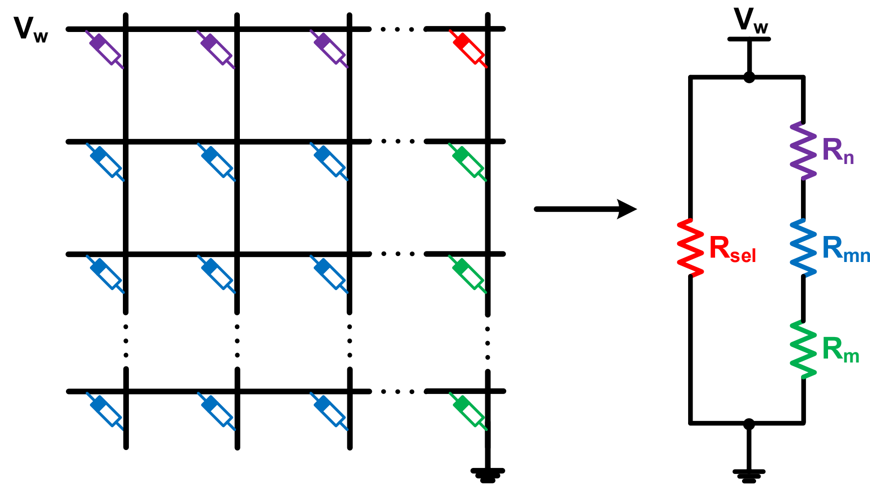

Figure 3: Structure of floating line write scheme and its equivalent circuit level model.

	Voltage Drop Formula	**Voltage Drop**	**Current**
Selected cell(s)	$V_{sel_word} - V_{sel_bit}$	$V_w - 0 = V_w$	V_w/R
Group II cell(s)	$V_{word} - V_{sel_bit}$	$f(m,n) - 0 = \frac{V_w(m-1)}{m+n-1}$	$\frac{V_w(m-1)(n-1)}{R(m+n-1)}$
Group III cell(s)	$V_{sel_word} - V_{bit}$	$V_w - f(m,n) = \frac{V_w(n-1)}{m+n-1}$	$\frac{V_w(m-1)(n-1)}{R(m+n-1)}$
Group IV cell(s)	$V_{word} - V_{bit}$	$f(m,n) - f(m,n) = \frac{V_w}{m+n-1}$	$\frac{V_w(m-1)(n-1)}{R(m+n-1)}$

Table 1: Voltage drop across the various group of cells using the floating line write scheme.

On the other hand, a partially-selected cell could have a voltage of almost V_w across it in an array where $m \neq n$, a definite write failure. Fig. 5 shows a simulation result of voltage drop on the three groups of

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

unselected cells for different array sizes, the worst case write disturbance in the floating scheme occurs in arrays with nonsquare aspect ratio ($m \neq n$). Partially-selected cells in group II (green) and group III (purple) have an undesired voltage of approximately V_w across them when $n \gg m$ and $m \gg n$ respectively. The disturbance impact increases as the gap between m and n widens. However, group IV (blue) cells get less voltage as size increases irrespective of the array shape. In summary, success of the floating scheme depends heavily on the array size and its structure. Table 1 shows a summary of voltage drop and current across each group of cells in the crossbar array during write operation with floating line scheme. V_{sel_word} and V_{sel_bit} are the voltages applied to the selected wordline and bitline respectively. V_{word} and V_{bit} are the voltages applied to unselected wordlines and bitlines respectively, $R \in \{R_{on}, R_{off}\}$. In this scheme, no voltage is applied directly to the unselected wordlines and bitlines as V_{word} and V_{bit} are dependent on the values of m and n. The voltage drop on the unselected groups of cells can thus be computed by solving the equivalent circuit on the right of Fig. 3.

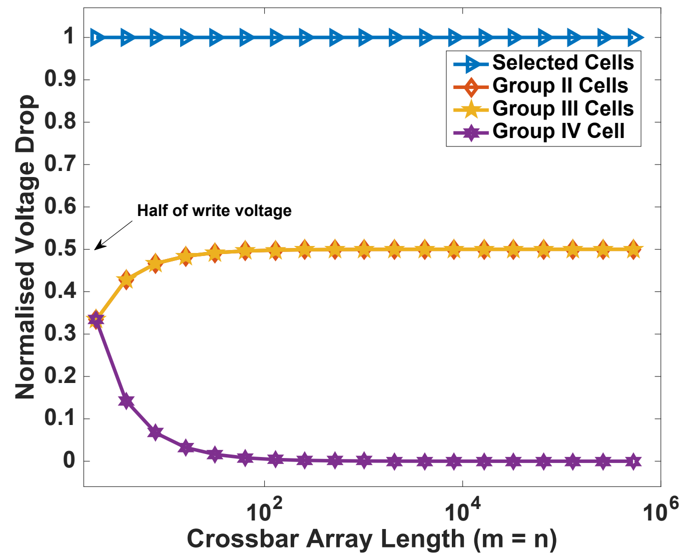

Figure 4: Simulation result of floating line scheme showing voltage drop across the four groups of cells. The voltage drop on the unselected cells are guaranteed not to exceed $V_w/2$ irrespective of the array size if $m = n$.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

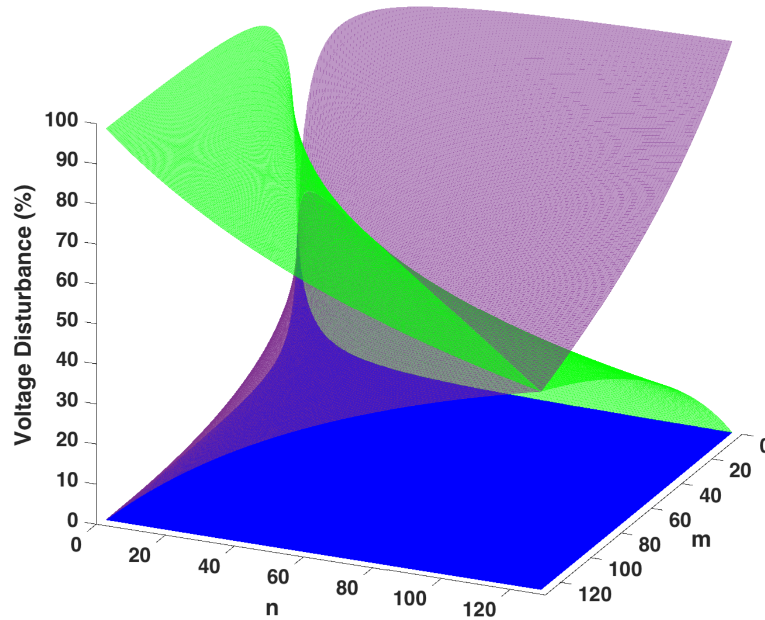

Figure 5: Voltage drop on unselected cells as array size varies. Voltage on partially-selected cells (group II and III) are depicted in purple and green, while unselected cells (group IV) are represented in blue. Partially-selected cells might reach up to V_w in non-square array structures but guaranteed not to exceed $V_w/2$ only if $m = n$.

4.1.2 V/2 Scheme

The structure of the $V/2$ scheme is shown in Fig. 6, a voltage of V_w and zero are applied to the wordline and the bitline of the target cell respectively and all other lines are biased with a voltage of $V_w/2$ to minimise current leakages to some of the unselected cells. In this scheme, the majority of the unselected cells are totally protected against disturbance, to be specific $((m-1)(n-1))$ cells are protected, these are the cells in group III. The remaining $m+n-2$ cells in group I and II in the $m \times n$ array are exposed to a voltage drop of $V_w/2$, which will ideally keep the cells safe. The number of cells $(m+n-2)$ susceptible to voltage disturbance in this scheme is less than 50% of the total cells in the array (mn) (percentage reduces as the array size grows). However, the probability of write error is slightly high in the V/2 scheme, as partially-selected cells $(m+n-2)$ have a voltage of $V_w/2$ across them constantly, their state could be perturbed if the voltage is applied long enough [13]. Table 2 shows a summary of voltage drop and current across each group of cells in the crossbar array during write operation with the V/2 scheme.

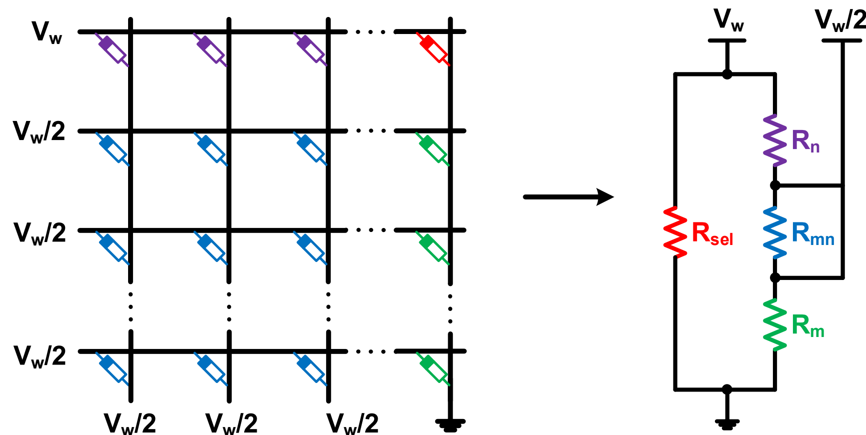

Figure 6: Structure of $V/2$ write scheme and its equivalent circuit level model

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

	Voltage Drop Formula	Voltage Drop	Current
Selected cell(s)	$V_{sel_word} - V_{sel_bit}$	$V_w - 0 = V_w$	V_w/R
Group II cell(s)	$V_{word} - V_{sel_bit}$	$V_w/2 - 0 = V_w/2$	$V_w/2R$
Group III cell(s)	$V_{sel_word} - V_{bit}$	$V_w - V_w/2 = V_w/2$	$V_w/2R$
Group IV cell(s)	$V_{word} - V_{bit}$	$V_w/2 - V_w/2 = 0$	≈ 0

Table 2: Voltage drop across the various group of cells using the V/2 write scheme.

4.1.3 V/3 Scheme

In the $V/3$ scheme shown in Fig. 7, the lines of the target cell are biased with the usual V_w and zero voltages but the other cells have a voltage of $V_w/3$ and $2V_w/3$ applied to their wordline and bitline respectively [21]. V/3 scheme offers the best protection against voltage disturbance to unselected cells. The maximum amount of voltage applied to any of the unselected cell is reduced to $V_w/3$ in this scheme as against $V_w/2$ in the floating line and the V/2 scheme. Although more cells $(mn - 1)$ are affected by leakage in the V/3 scheme but the probability of their state being disturbed is low. Each of the unselected cell in the V/3 scheme has a current of $V_w/3R$ sneaking through them. Table 3 shows a summary of voltage drop and current across each group of cells in the crossbar array during write operation with the V/3 scheme.

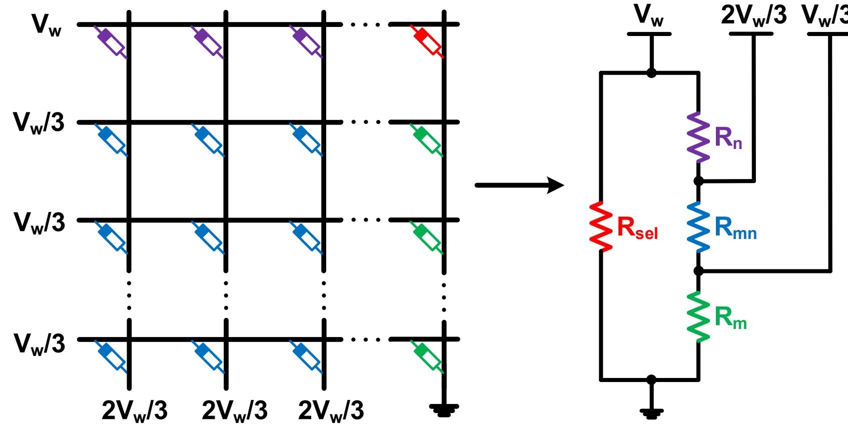

Figure 7: Structure of $V/3$ write scheme and its equivalent equivalent circuit level model

	Voltage Drop Formula	Voltage Drop	Current
Selected cell(s)	$V_{sel_word} - V_{sel_bit}$	$V_w - 0 = V_w$	V_w/R
Group II cell(s)	$V_{word} - V_{sel_bit}$	$V_w/3 - 0 = V_w/3$	$V_w/3R$
Group III cell(s)	$V_{sel_word} - V_{bit}$	$V_w - 2V_w/3 = V_w/3$	$V_w/3R$
Group IV cell(s)	$V_{word} - V_{bit}$	$V_w/3 - 2V_w/3 = V_w/3$	$V_w/3R$

Table 3: Voltage drop across the various group of cells using the V/3 write scheme.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

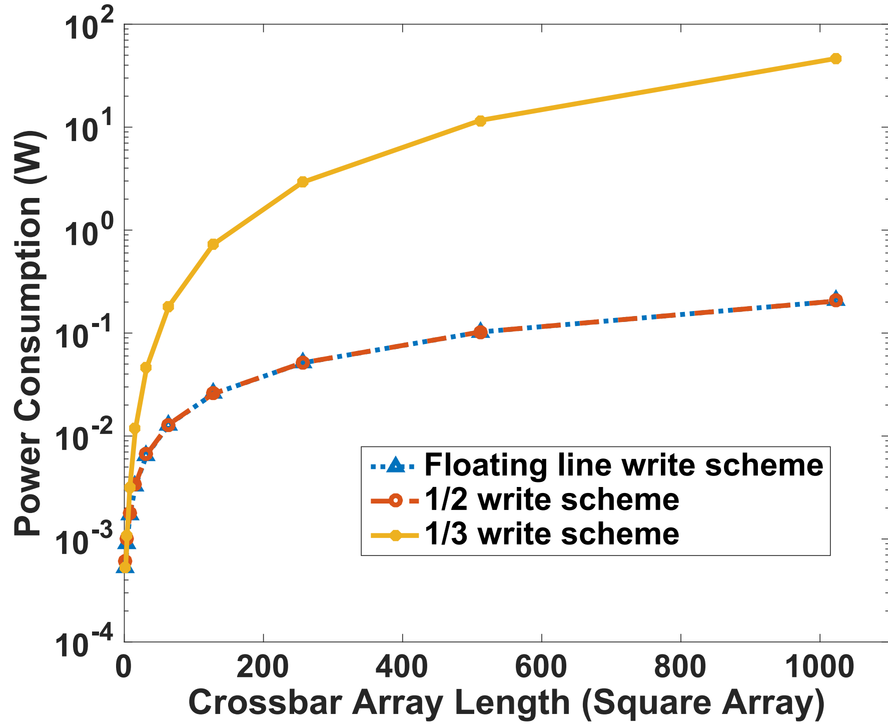

Figure 8: Comparison of power consumption in the three write schemes. $R_{on} = 10k$, $R_{off} = 100K$

In summary, all the three aforementioned write schemes have their pros and cons without the effect of line resistance. The floating scheme is only considered reliable when the array is square shaped; otherwise state of unselected cells are perturbed. The V/2 scheme protects more cells than any other scheme but the state of the $m+n-2$ cells constantly exposed to a voltage of $V_w/2$ can be overwritten if exposed to voltage for long time. The V/3 scheme on the other hand, exposes all the groups of unselected cells to a more reasonable low voltage of $V_w/3$. Analysis of these schemes will be incomplete without considering their power consumption. Fig. 8 shows an ideal power consumption comparison between the three schemes. The V/3 scheme which seems like the best write scheme initially consumes enormous power. The huge power consumption of the V/3 scheme is as a result of frequent switching between the $V_w/3$ and $2V_w/3$ power rail as well as the fact that all the cells in the array experience sneak-path leakages. Floating line and $V/2$ schemes have similar low power consumptions when $m = n$ and floating line gets better when $m \neq n$ but at the expense of its reliability. Fig. 9 shows the power consumptions of the floating line scheme compared against the V/2 write scheme so as to show cases where the array are unsquare ($m \neq n$). As m deviates from n, there is more power saving with the floating line than the V/2 scheme but the inequality between m and n causes further disturbance to the unselected cells which could lead to write failure as explained in section 4.1.1. Table 4 shows a performance summary of the three schemes with their corresponding analytical models for their performance metrics.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

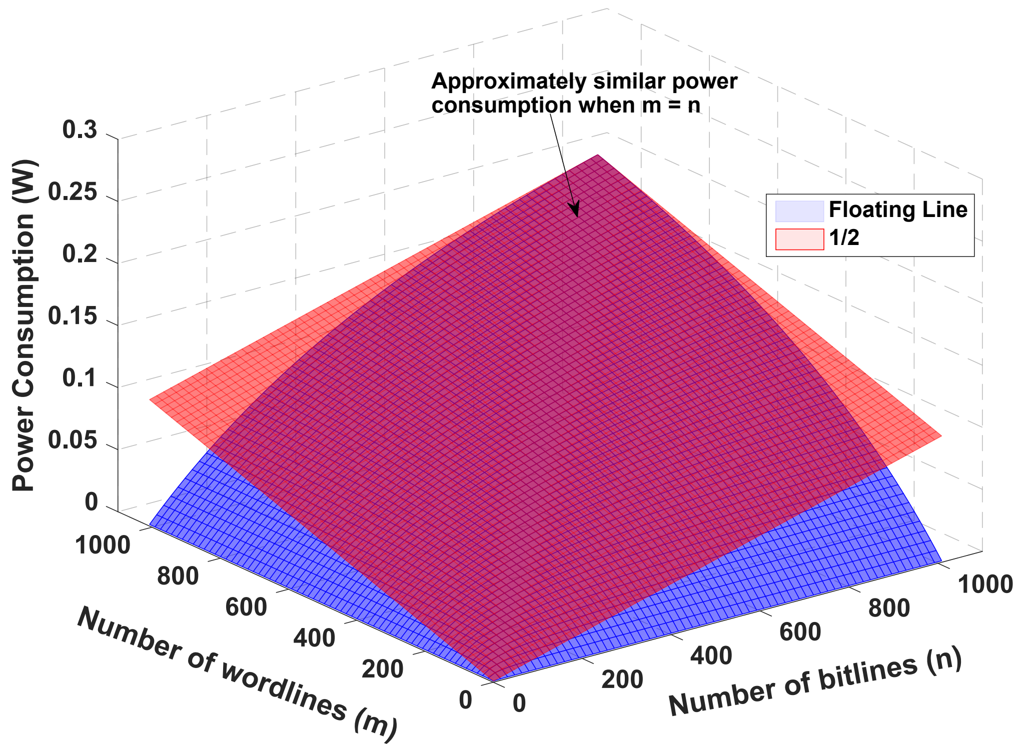

Figure 9: Comparison of power consumption between the floating line and V/2 write schemes over varying range of array sizes and structures.

Table 4: Comparison summary of write schemes performance without the effect of line resistance

	Voltage on selected cell(s)	Voltage on unselected Cells		Total Current Leakage	No. of disturbed cells	Dependence on Array Size/ Aspect Ratio	Probability of un-selected Switching
		Min. Voltage	Max. Voltage				
Floating Line	V_w	$\frac{V_w}{m+n-1}$	$\max\left(\frac{V_w(m-1)}{m+n-1}, \frac{V_w(n-1)}{m+n-1}\right)$	$\frac{V_w(m-1)(n-1)}{R(m+n-1)}$	$mn-1$	Yes	≤ 0.5 (if $m=n$)
V/2 Bias	V_w	0	$V_w/2$	$\frac{V_w(m+n-2)}{2R}$	$m+n-2$	No	0.5
V/3 Bias	V_w	$V_w/3$	$V_w/3$	$\frac{V_w(mn-1)}{3R}$	$mn-1$	No	0.33

4.2 Write Operation with Line Resistance

In smaller arrays, line resistance could be negligible but as array size increases, the effects of line resistance becomes more prominent. Therefore, it is important to factor in line resistances for an accurate analysis of write operation in crossbar architectures. Fig. 10 shows a resistance model of a $m \times n$ crossbar array. Each memristor in the array has a wire resistance adjacent to either sides of its bitline and wordline. In the presence of line resistance, the voltage reaching the farthest cell from the voltage source might not be sufficient to switch the cell to the desired state, thereby leading to a write error. Similarly, unselected cells closer to the voltage source could be written in error as a result of voltage deflected to/from them.

There is no single closed form formula that can accurately describe the voltage drop on each of the cells in the crossbar array of the resistance model depicted by Fig. 10. In order to determine the voltage drop on any memristor of resistance $R^m_{i,j}$ in any $m \times n$ array, where $1 \leq i \leq m$ and $1 \leq j \leq n$, the voltage on its wordline (row) and bitline (column) denoted by $V^w_{i,j}$ and $V^b_{i,j}$ must be solved. For the entire array, there are $2 \times m \times n$ unknown voltages as each memristor has two unknown voltages. A set of $2mn$ linear

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

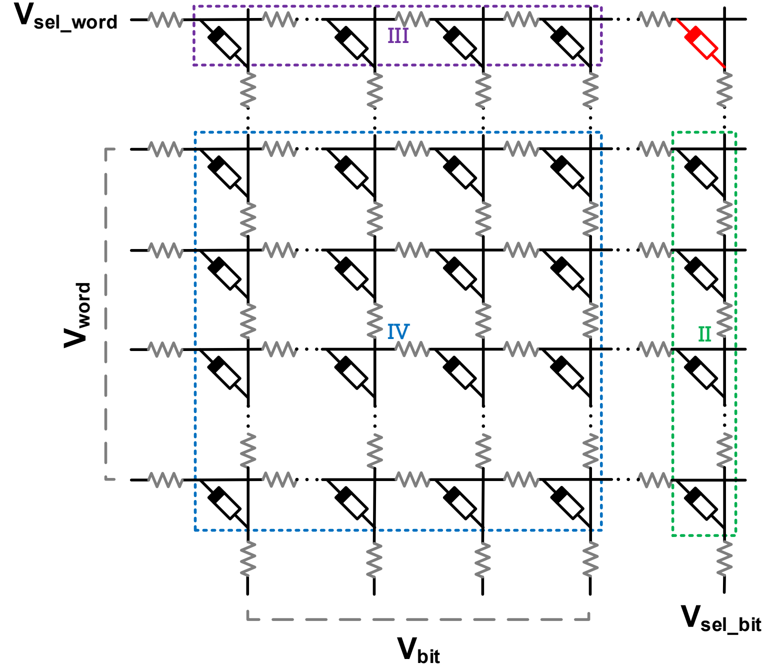

Figure 10: Resistance model of the crossbar array showing resistance of nanowires.

equations are thus required in order to determine the voltage drop on the memristors [22]. The current flowing through each memristor can be described by two Kirchhoff's current law equations - each representing the current flowing through the wordline and bitline. Eqn. 4 shows the three possible wordline equations of each memristor depending on its location on the wordline (first column ($j = 1$) or last column ($j = n$) or mid-column ($1 < j < n$)). Current flowing through the bitline of a memristor will be described by one of Eqn. 5 depending on the cell's location on the bitline (first row ($i = 1$) or last row ($i = m$) or mid-row ($1 < i < m$))

Kirchhoff's Equations formed based on the voltages on the wordline junction of each memristor:

$$\frac{V^b_{i,j} - V^w_{i,j}}{R^m_{i,j}} = \begin{cases} \dfrac{V^w_{i,j} - V^w_i}{R_{wi}} + \dfrac{V^w_{i,j} - V^w_{i,j+1}}{R_{wi,j}}, & \text{if } j = 1 \\ \dfrac{V^w_{i,j} - V^w_{i,j-1}}{R_{wi,j-1}} + \dfrac{V^w_{i,j} - V^w_i}{R_{wi}}, & \text{if } j = n \\ \dfrac{V^w_{i,j} - V^b_{i,j+1}}{R_{wi,j}} + \dfrac{V^w_{i,j} - V^w_{i,j-1}}{R_{wi,j-1}}, & \text{otherwise} \end{cases} \tag{4}$$

Kirchhoff's Equations formed based on the voltages on the bitline junction of each memristor:

$$\frac{V^w_{i,j} - V^b_{i,j}}{R^m_{i,j}} = \begin{cases} \dfrac{V^b_{i,j} - V^b_j}{R_{bj}} + \dfrac{V^b_{i,j} - V^b_{i+1,j}}{R_{bi,j}}, & \text{if } i = 1 \\ \dfrac{V^b_{i,j} - V^b_{i-1,j}}{R_{bi-1,j}} + \dfrac{V^b_{i,j} - V^b_j}{R_{bj}}, & \text{if } i = m \\ \dfrac{V^b_{i,j} - V^w_{i+1,j}}{R_{bi,j}} + \dfrac{V^b_{i,j} - V^b_{i-1,j}}{R_{bi-1,j}}, & \text{otherwise} \end{cases} \tag{5}$$

$V^w_i = V_{sel_word}$ and $V^b_j = V_{sel_bit}$ are the write voltage values on the selected wordline i and bitline j respectively. $V^w_{i,j}$ and $V^b_{i,j}$ are the voltage values on the wordline and bitline of the selected memristor respectively. R_{wi} and R_{bj} are the line resistance values at source of the voltage to wordline i and bitline j respectively. $R_{wi,j}$ and $R_{bi,j}$ are the line resistance values at the wordline i and bitline j respectively.

With line resistance, the worst case write scenario occurs when all the cells are in LRS and the selected cell is farthest away from the voltage source. In addition to the weakening of the voltage drop on the selected

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

cell, maximum disturbance to unselected also increases as array size grows in all the three schemes described in section 4.1. Fig. 11 shows the simulation results of the three schemes in the presence of different line resistance values across an increasing array size. For this simulation, all cells in the array are kept at a worst case value of R_{on}. Maximum disturbance to the unselected cells using both floating line and $V/2$ schemes are kept at a maximum of $V_w/2$ as array size increases. Unlike other schemes, the $V/3$ write scheme causes voltage of up to $2V_w/3$ to reach the unselected cells nearest to the bitline and farthest from the wordline as shown in the simulation results. Crossbar array density could be highly limited depending on the resistivity of nanowire used in the crossbar design. A worst case R_L/R_{on} value of 10^{-2} lead to a negative write voltage window (difference between voltage reaching selected device and maximum voltage to unselected cell) in array with over 256 devices across all the three schemes (see Fig. 11a). The memory is not useful with a write technique and worst case nanowire resistivity that leads to a negative write window. High density and reliable crossbar memory can be realised by keeping line resistance to the barest minimum. Result with a generous line resistance of R_L/R_{on} = 10^{-6} is quite promising as shown in Fig. 11e even with a worst case data pattern where all memristor are set to R_{on}. Fig. 12 shows similar simulation results as in Fig. 11 but with a random resistance pattern. The result shows improved write voltage window as the voltage drop across the selected cell degrades at a more slower rate as array size increases.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

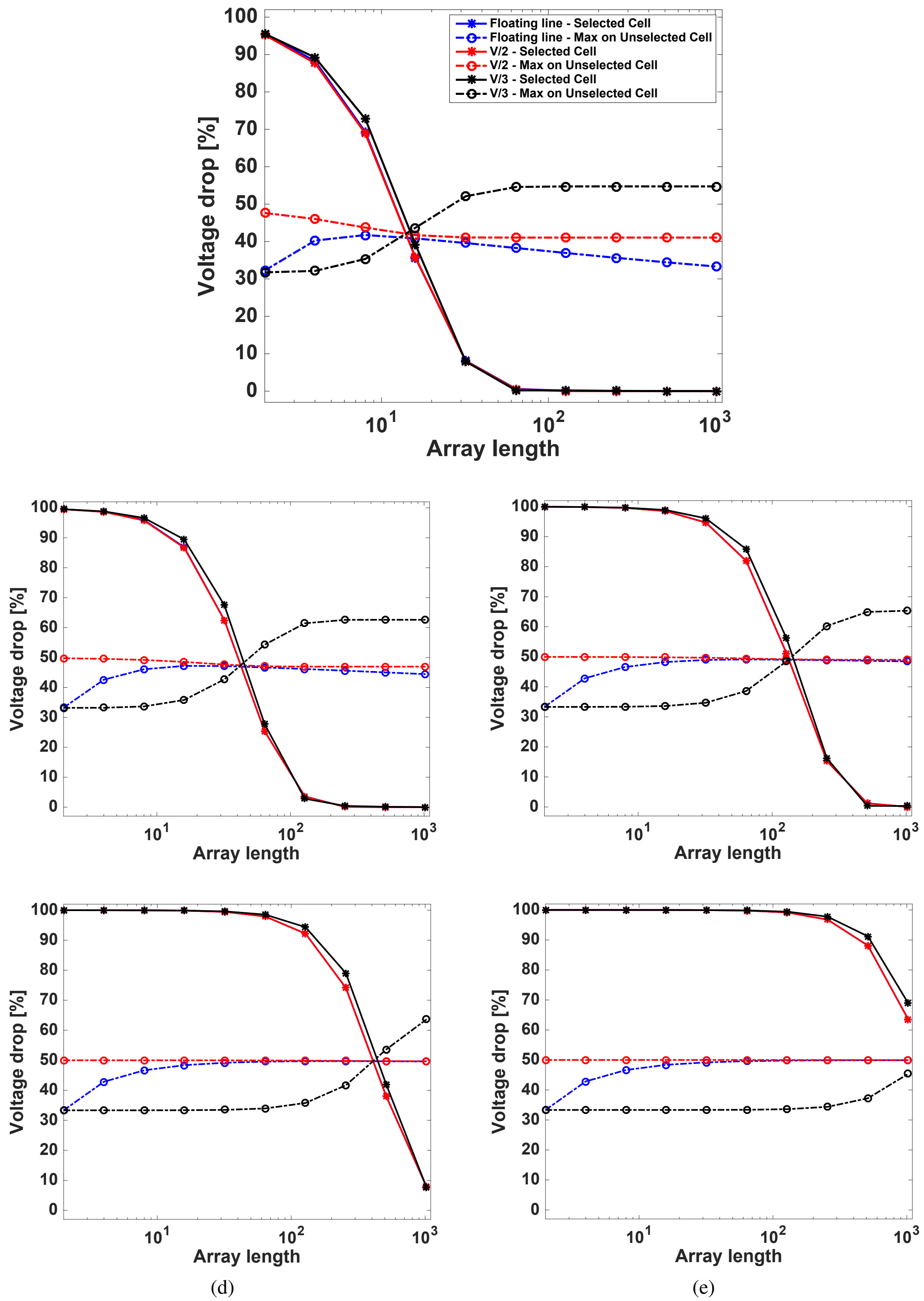

Figure 11: Voltage drop across selected and unselected cells with all memristor in the crossbar set to R_{on} and R_L/R_{on} set to: (a) 10^{-2} (b) 10^{-3} (c) 10^{-4} (d) 10^{-5} (e) 10^{-6}.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

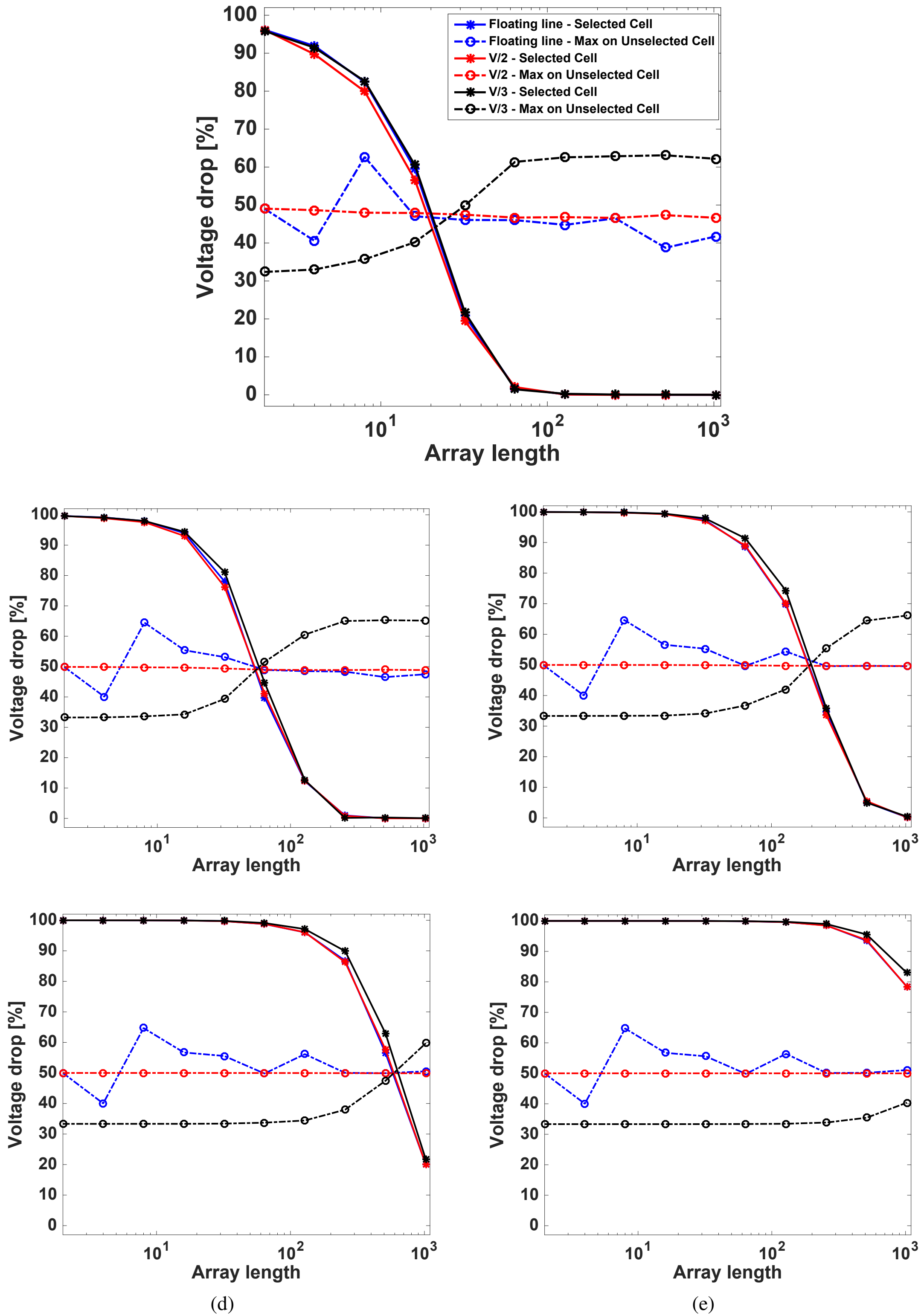

Figure 12: Voltage drop across selected and unselected cells with random resistance pattern in the crossbar with R_L/R_{on} set to: (a) 10^{-2} (b) 10^{-3} (c) 10^{-4} (d) 10^{-5} (e) 10^{-6}.

5 Compensated Write Voltage Technique

The obvious solution to the voltage drop problem caused by line resistance will be to increase the write voltage but this also increases the maximum voltage reaching the unselected cells [22]. One approach to solving this problem is the double-sided ground biasing (DSGB) approach where both sides of the selected wordline array

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

are grounded and the selected bitline is connected to the write voltage [14]. Another solution uses *dual voltage source* design where voltage are delivered via both sides of the selected wordlines [11]. Both described techniques however incur additional chip area overhead thereby reducing the array efficiency without offering much in term of preventing voltage degradation. Robust solutions to the voltage drop problem in order to prevent write failure is an important challenge that calls for further investigation.

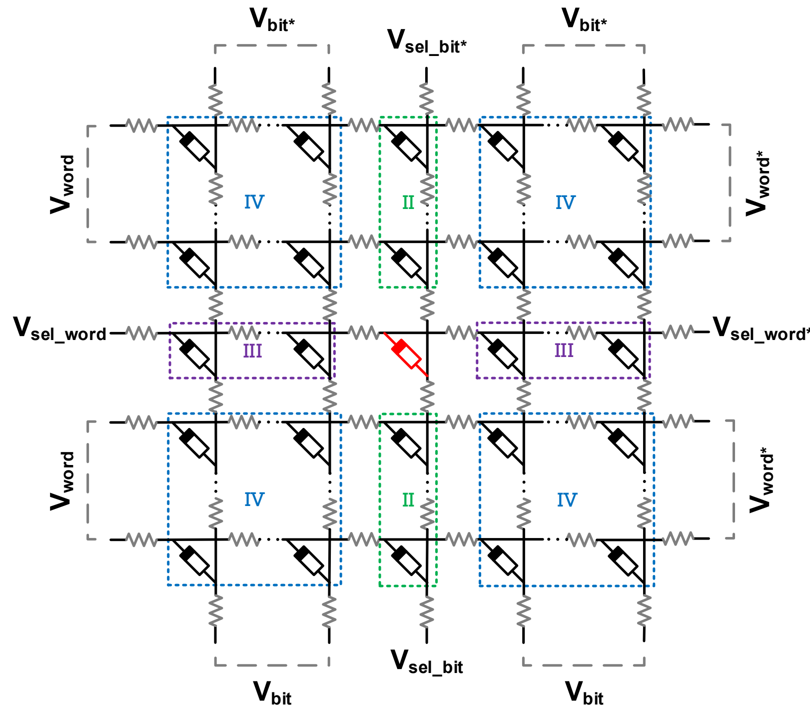

Figure 13: Resistance model of the crossbar array using the dual voltage source technique. The starred voltages will have the same value as their unstarred counterpart

We propose a novel write technique that is able to compensate for the voltage loss effect during the write operation on memristor-based crossbar using the V/2 write scheme. V/2 scheme was chosen because it is the best in terms of power consumption and reliability as long as voltage are timed correctly as discussed in section 4. This technique can also be extended to crossbars with unmemristive crosspoint cells. As mentioned earlier, the value of the line resistance, data distribution in the array and choice of write scheme are the three major parameters that causes voltage loss during write operation. The compensated voltage technique was used alongside the dual voltage technique. The schematic is depicted in Fig. 13. In the dual voltage technique, the worst case selected cell will move to the middle of the array [11]. The starred voltage sources will have the same magnitude as their unstarred counterparts. The compensated technique was implemented by adjusting the values of the voltages applied to the unselected wordlines and the selected bitline.

	Voltage Drop Formula	**Voltage Drop**
Selected cell(s)	$V_{sel_word} - V_{sel_bit}$	$V_w - (-K.V_w)/2 = (V_w(2+K))/2$
Group II cell(s)	$V_{word} - V_{sel_bit}$	$((1-K)V_w)/2 - (-K.V_w)/2 = V_w/2$
Group III cell(s)	$V_{sel_word} - V_{bit}$	$V_w - V_w/2 = V_w/2$
Group IV cell(s)	$V_{word} - V_{bit}$	$((1-K)V_w)/2 - V_w/2 = -K.V_w/2$

Table 5: Voltage drop across the various group of cells using the dual and compensated voltage technique on the V/2 write scheme in the presence of line resistance. K is the percentage of voltage to be extracted from V_{word} for onward application to V_{sel_bit} to supplement the write voltage V_w.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

Usually, voltage drop on the selected cell is determined by V_{sel_word} and V_{sel_bit} as explained in previous sections. In this proposed technique, as opposed to the usual grounding of V_{sel_bit}, a negative (positive) voltage is applied instead to supplement the positive (negative) write voltage applied at V_{sel_word}, thereby increasing the overall voltage drop on the selected cell or compensating for voltage degradation due to line resistance effect. Applying a voltage source to V_{sel_bit} also leads to an increase in the voltage drop on cells in group II. The effect of this modification can be balanced by reducing the voltage applied to V_{word} such that the summation of voltages applied to both V_{word} and V_{sel_bit} still results in $V_w/2$ therefore ensuring cells in group II are kept safe from disturbances.

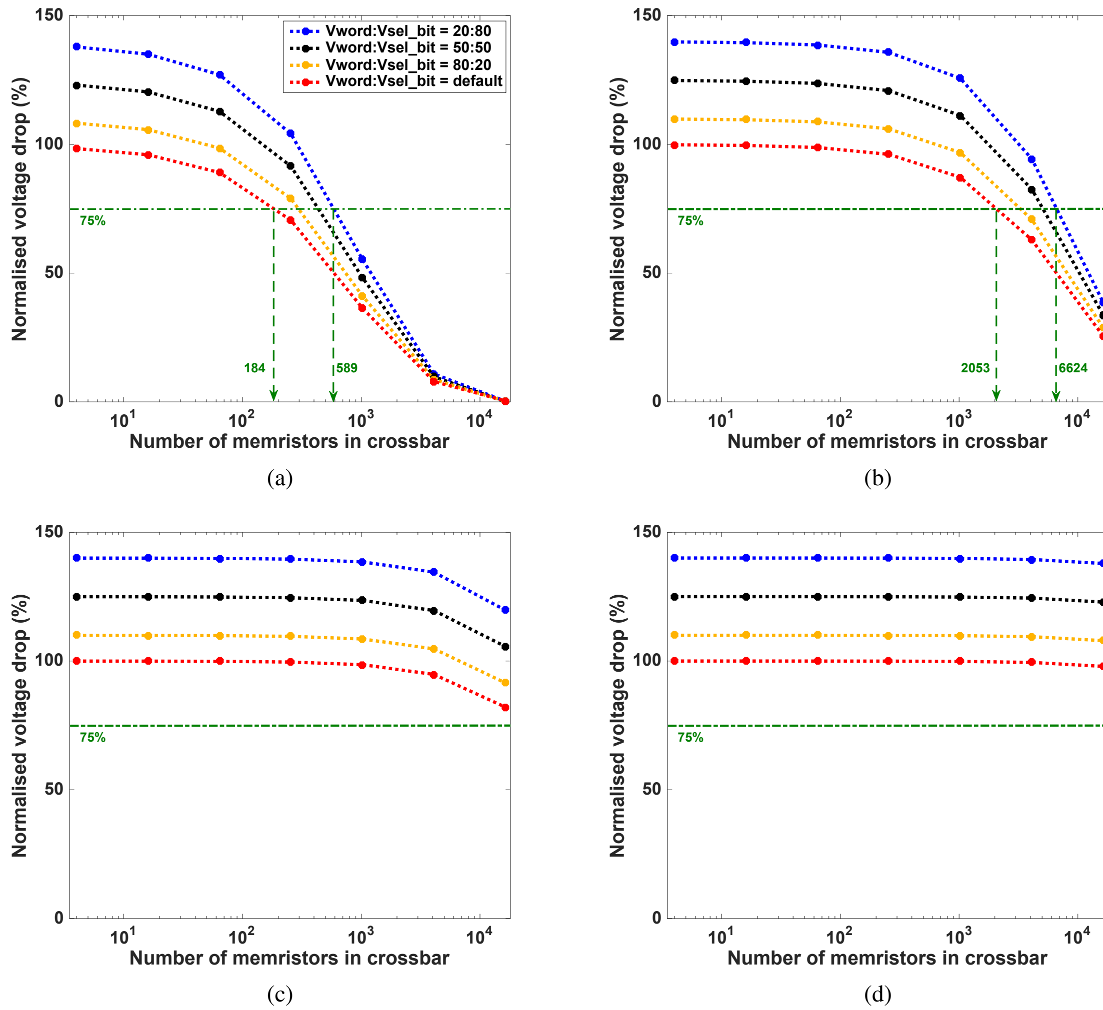

Figure 14: Simulation results showing voltage drop on the worst case selected cell over a range crossbar size using the proposed compensated voltage technique with R_L/R_{on} values set to: (a) 10^{-2} (b) 10^{-3} (c) 10^{-4} (d) 10^{-5}.

Group IV cells experience an increase in voltage drop because of the change to V_{word} but the voltage drop is guaranteed to be below $Vw/2$ depending on the sharing ratio of V_{word} and V_{sel_bit}. Cells in group III are not affected by these modifications. In order to keep the voltage drop on group II cells at or below $Vw/2$, a percentage of V_{word}'s voltage ($Vw/2$) is extracted and applied to V_{sel_bit}. Table 5 shows a summary of the new voltage drop on the various groups of cells in the new compensated and dual voltage technique. The selected cells can only benefit by this compensation as it is tolerable for the selected cell to have a voltage drop in excess of its threshold voltage.

We simulated three sharing ratios between V_{word} and V_{sel_bit} $(K$:1-$K)$ namely 0.8:0.2, 0.5:0.5 and 0.2:0.8 over a range of R_L/R_{on} values. We have used a switching voltage requirement of a minimum of $75\%V_w$ for the selected cell(s). Simulation results depicted in Fig. 14a-d show over $3\times$ improvements in the voltage

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

reaching the worst case selected cells with the 0.2:0.8 compensation technique compared to the conventional method. This technique simply helps to increase the voltage delivered to the worst case selected cell(s) without endangering the unselected cells beyond their preset thresholds.

It is expected that the power consumption of this technique will be more than the conventional V/2 scheme. This can however be managed by applying this technique to the conventional single side write method which will further reduce power consumption. A much smaller V_{word}:V_{sel_bit} ratio can also be used to drive down power consumptions.

6 CONCLUSIONS

The analytic model for the crossbar array write operation and other analysis presented in this paper was verified by comparing analytic results against simulation results from the Cadence Spectre simulation tool. In an effort to improve the reliability of write operations on crossbar memories, an accurate analytical modelling of the crossbar write operation is required especially in larger array, alongside proper consideration of array size and aspect ratio. The crossbar analytic model derived in this work caters for the real case where each group of cells in the crossbar is free to include both high and low resistance state cells simultaneously. With this model, analysis was carried out on the performances of three existing crossbar write schemes (floating line, $V/2$ and $V/3$) with and without line resistance consideration. The floating scheme is only considered reliable only when the array is square shaped. The $V/2$ scheme protects more cells than any other scheme but the state of the $m + n - 2$ cells constantly exposed to a voltage of $V_w/2$ can be overwritten if exposed to voltage for a long time. The $V/3$ scheme on the other hand, exposes all the groups of unselected cells to a more reasonable low voltage of $V_w/3$ but at the expense of power conservation. Based on these initial analyses, a compensated voltage technique was designed for the low-power $V/2$ scheme using the dual voltage method to increase the maximum array size that can be designed and in turn reduce the possibility of write failure. With this compensation technique, the maximum array size can be increased up to $3\times$ depending on selected parameters.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

REFERENCES

[1] H.-S. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, K. E. Goodson, *et al.*, "Phase change memory," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2201–2227, 2010.

[2] M. K. Qureshi, V. Srinivasan, and J. A. Rivers, "Scalable high performance main memory system using phase-change memory technology," *ACM SIGARCH Computer Architecture News*, vol. 37, no. 3, pp. 24–33, 2009.

[3] M. Hosomi, H. Yamagishi, T. Yamamoto, K. Bessho, Y. Higo, K. Yamane, H. Yamada, M. Shoji, H. Hachino, C. Fukumoto, *et al.*, "A novel nonvolatile memory with spin torque transfer magnetization switching: Spin-ram," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 459–462, IEEE, 2005.

[4] F. Alibart, E. Zamanidoost, and D. B. Strukov, "Pattern classification by memristive crossbar circuits using ex situ and in situ training," *Nature communications*, vol. 4, p. 2072, 2013.

[5] M. Prezioso, F. Merrikh-Bayat, B. Hoskins, G. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature*, vol. 521, no. 7550, pp. 61–64, 2015.

[6] X. Hu, S. Duan, L. Wang, and X. Liao, "Memristive crossbar array with applications in image processing," *Science China Information Sciences*, vol. 55, no. 2, pp. 461–472, 2012.

[7] U. Rührmair, C. Jaeger, M. Bator, M. Stutzmann, P. Lugli, and G. Csaba, "Applications of high-capacity crossbar memories in cryptography," *IEEE Transactions on Nanotechnology*, vol. 10, no. 3, pp. 489–498, 2011.

[8] A. Siemon, S. Menzel, R. Waser, and E. Linn, "A complementary resistive switch-based crossbar array adder," *IEEE journal on emerging and selected topics in circuits and systems*, vol. 5, no. 1, pp. 64–74, 2015.

[9] X. Yang, A. Adeyemo, A. Bala, and A. Jabir, "Novel memristive logic architectures," in *Power and Timing Modeling, Optimization and Simulation (PATMOS), 2016 26th International Workshop on*, pp. 196–199, 2016.

[10] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, no. 7290, pp. 873–876, 2010.

[11] A. Chen, "A comprehensive crossbar array model with solutions for line resistance and nonlinear device characteristics," *Electron Devices, IEEE Transactions on*, vol. 60, pp. 1318–1326, April 2013.

[12] H. Mostafa and Y. Ismail, "Statistical yield improvement under process variations of multi-valued memristor-based memories," *Microelectronics Journal*, vol. 51, pp. 46–57, 2016.

[13] C.-M. Jung, J.-M. Choi, and K.-S. Min, "Two-step write scheme for reducing sneak-path leakage in complementary memristor array," *Nanotechnology, IEEE Transactions on*, vol. 11, no. 3, pp. 611–618, 2012.

[14] C. Xu, D. Niu, N. Muralimanohar, R. Balasubramonian, T. Zhang, S. Yu, and Y. Xie, "Overcoming the challenges of crossbar resistive memory architectures," in *High Performance Computer Architecture (HPCA), 2015 IEEE 21st International Symposium on*, pp. 476–488, IEEE, 2015.

[15] L. O. Chua, "Memristor-the missing circuit element," *Circuit Theory, IEEE Transactions on*, vol. 18, no. 5, pp. 507–519, 1971.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.

[16] O. Kavehei, A. Iqbal, Y. Kim, K. Eshraghian, S. Al-Sarawi, and D. Abbott, "The fourth element: characteristics, modelling and electromagnetic theory of the memristor," *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Science*, 2010.

[17] O. Kavehei, Y.-S. Kim, A. Iqbal, K. Eshraghian, S. Al-Sarawi, and D. Abbott, "The fourth element: Insights into the memristor," in *Communications, Circuits and Systems, 2009. ICCCAS 2009. International Conference on*, pp. 921–927, IEEE, 2009.

[18] D. B. Strukov *et al.*, "The missing memristor found," *nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[19] A. Flocke and T. G. Noll, "Fundamental analysis of resistive nano-crossbars for the use in hybrid nano/cmos-memory," in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, pp. 328–331, IEEE, 2007.

[20] A. Adeyemo, X. Yang, A. Bala, and A. Jabir, "Analytic models for crossbar write operation," in *Embedded Computing and System Design (ISED), 2016 Sixth International Symposium on*, pp. 313–317, IEEE, 2016.

[21] J. Mustafa, *Design and analysis of future memories based on switchable resistive elements*. PhD thesis, Universitätsbibliothek, 2006.

[22] D. Niu, C. Xu, N. Muralimanohar, N. P. Jouppi, and Y. Xie, "Design trade-offs for high density crosspoint resistive memory," in *Proceedings of the 2012 ACM/IEEE international symposium on Low power electronics and design*, pp. 209–214, ACM, 2012.

OPEN ACCESS: Readers can read, redistribute and reuse the articles for free,
as long as they cite the publication details properly and do not use for any commercial purposes.