Novel approaches in current-feedback operational amplifier design

by

Amr Abdallah Tammam

School of Technology
Oxford Brookes University

A thesis submitted in partial fulfilment of the requirements of
Oxford Brookes University for the degree of

Doctor of Philosophy

September 2005

Acknowledgement

My principle acknowledgement goes to my director of research, Dr. Khaled Hayatleh for his guidance and support throughout the PhD.

Special thanks go to my second supervisor Professor John Lidgey for his positive criticism, and for his understanding.

It has been a privilege as well as a tremendous honour to learn a great deal from Mr Bryan Hart's wide experience in analog circuit design.

In addition I would like to thank my parents who afforded me the opportunity to study in the United Kingdom. The financial sacrifice that they made and their encouragement has been invaluable.

I would like to express my deep respect, and appreciation to my Father, Dr. Abdallah Tammam, as he has always been the source of my inspiration over the years and has helped me through many difficult times. I am forever indebted for his continuous support and encouragement. I am proud to have him as a father and to be a member of a family in which he is the head.

I would like to give my sincerest thanks to my mother, Dr. Afaf Ahmed Ali, who is and always will be the greatest mother anyone could ever asked for, and who has also given me the support I need and has always been there for me.

I would like to thank my beloved wife Soraya Sherin Shams El Din Abd El Bary, if it was not for her love and support this thesis would not have been possible. Similarly I would like to thank my baby girl Farida who joined us toward the end and made our life a happy one.

I would also like to thank my youngest sister Afaf who I love dearly. To my sister Aliaa who currently is undertaking her own PhD, I would also like to extend my love and best wishes.

I would also like to thank every one in my family, as well as friends and colleagues, especially in DM25 whose influences have helped both directly and indirectly towards the production of this thesis.

I would like to pay a tribute to my grandmother Safeya Mahmoud who I have lovely memories of and who always believed in me.

Finally, I would like to show my gratitude to Allah Most Gracious, Most Merciful who guides me throughout my life. It is He who has given me the ability to gain the knowledge, may He as well help me to use it in the way that He sees fit and best pleases Him.

Amr Abdallah Tammam
Oxford
September 2005

Dedicated to my Parents

my Wife, and to the memory of my Grandmother

Abstract

The aim of this research programme was to design and develop a novel bipolar junction transistor Current Feedback Operational Amplifier (CFOA) with a good Common-Mode Rejection Ratio (CMRR), suitable for radio frequency (RF) applications. This research focused on investigation of the established CFOA with the emphases of improving CMRR, bandwidth, Voltage-Offset and Slew-rate performance. The majority of the results of this work have been reported by the author in references **[1] to [6]**.

Initially a thorough analysis of the conventional CFOA was undertaken to provide an in depth understanding of the amplifier's operation, and this work revealed that the main shortcomings of the CFOA are in the design of the input stage. This initial study focussed on establishing reasons for the poor DC offset-voltage performance and CMRR and confirmed that these designs have inherently poor performance in these two elements. The analysis was carried out using both theoretical modelling and computer simulation.

Using this analysis of the conventional CFOA as a benchmark, various novel circuit techniques were investigated. Several new input circuits for the CFOA were proposed with respect to improving the three previously mentioned key characteristics, *viz.*, CMRR, offset voltage, and slew-rate. The first technique explored is based on floating the entire input stage of the CFOA which yielded significant improvements in CMRR, Offset-Voltage and bandwidth, and the results of this work were published in **[1]**, **[2]**, and **[3]**. Based on these initial findings a second major development was undertaken. This time a bootstrapping technique was employed to key sections of the input stage, leading to new, simplified input circuit topology. This development leads to low DC offset voltage, wide bandwidth and high CMRR, as well as improved gain accuracy, and was published by the author in **[4, 5]**.

A logical approach to the different input stage architectures examined by the author resulted in identification of a hierarchy of 6 different input CFOA circuit designs and

a comparative study was undertaken showing their relative performance in respect of CMRR, Offset-Voltage and Slew-rate. This work was presented by the author, **[6]**.

Publications by the author

[1] Tammam A.A, Hayatleh K, and Lidgey F.J, 'Novel high performance Current-Feedback op-amp', IEEE Proceedings of International Symposium on Circuits and Systems, Arizona, USA, May 2002, pp.705-708.

[2] Tammam A.A, Hayatleh K, and Lidgey F.J, 'High performance Current Feedback operational amplifier design', IEEE Proceedings of IEE ASP2002, Oxford, UK, 2002, pp.12-1-12-6.

[3] Tammam A.A, Hayatleh K, and Lidgey F.J, 'High CMRR Current-Feedback operational amplifier', International Journal of Electronics, 2003, Vol.90, No. 2, pp.87-97.

[4] Tammam A.A, Hayatleh K, Hart B, and Lidgey F.J, 'A new Current-Feedback operational amplifier with a high CMRR', Electronics. Letters, 2003, Vol.39, No.21, pp.1483.

[5] Tammam A.A, Hayatleh K, Hart B, and Lidgey F.J, 'High performance Current-Feedback op-amps', IEEE Proceedings of International Symposium on Circuits and Systems, Vancouver, Canada, May 2004, pp.825-828.

[6] Tammam A.A, Hayatleh K, Hart B, and Lidgey F.J, 'A hierarchy of input stages for Current Feedback operational amplifiers', IEEE Proceedings of International Symposium on Circuits and Systems, Vancouver, Canada, May 2004, pp.821-824.

List of principal symbols

A_d	Differential voltage gain
A_c	common mode voltage gain
A_{dm}	Op-amp differential-mode gain
A_{cm}	Op-amp common-mode gain
A(O)	CFOA closed-loop amplifier low frequency gain
Av, A	Op-amp open-loop voltage gain
A_{CL}	Magnitude of closed-loop d.c. voltage gain
BW	Bandwidth
β	Transistor DC current gain
CFOA	Current feedback op-amp
CCII	Current conveyor (type II)
CMRR, ρ	Common-mode rejection ratio
CM	Current-mirror
C_M	Miller capacitance
D	Diode
f_T	Unity-gain frequency
f_{-3dB}	Closed-loop -3dB frequency
fp	Full-power bandwidth
g_m	Transconductance
G, g	Conductance
I_S	Forward saturation current
Ibias	Op-amp supply bias current
KCL	Kirchoff's current law
KVL	Kirchoff's voltage law
LG	Magnitude of the first-order expression for the low frequency loop gain
λ	Current-mirror transfer coefficient
PSRR	Power-supply rejection ratio
r_π	Transistor base-emitter incremental resistance
r_{ce}	Transistor collector emitter incremental resistance
r_e	Transistor emitter incremental resistance
r_I	Input resistance
r_O	Output resistance
ε	A.C.-gain error
SR	Slew-rate

t_{ir}	Input rise-time of the op-amp
t_{if}	Input fall time of the op-amp
t_{or}	Output rise-time of the op-amp
t_{of}	Output fall time of the op-amp
τ_F	Transistor time-constant
VFOA	Voltage feedback operational amplifier
VOA	Voltage operational amplifier
V_p	Non-inverting input terminal of an op-amp
V_n	Inverting-input terminal of an op-amp
V_T	Thermal voltage $(^{KT}/_{q})$
V_A	Early Voltage
V_{OS}	Input-referred offset-voltage
V_{be}	Transistor base-emitter voltage
VF	Voltage-follower
XFCB	Extra fast complementary bipolar
Z_Z	High impedance gain-node of the CFOA

Table of Contents

Appendix 3

CHAPTER 1

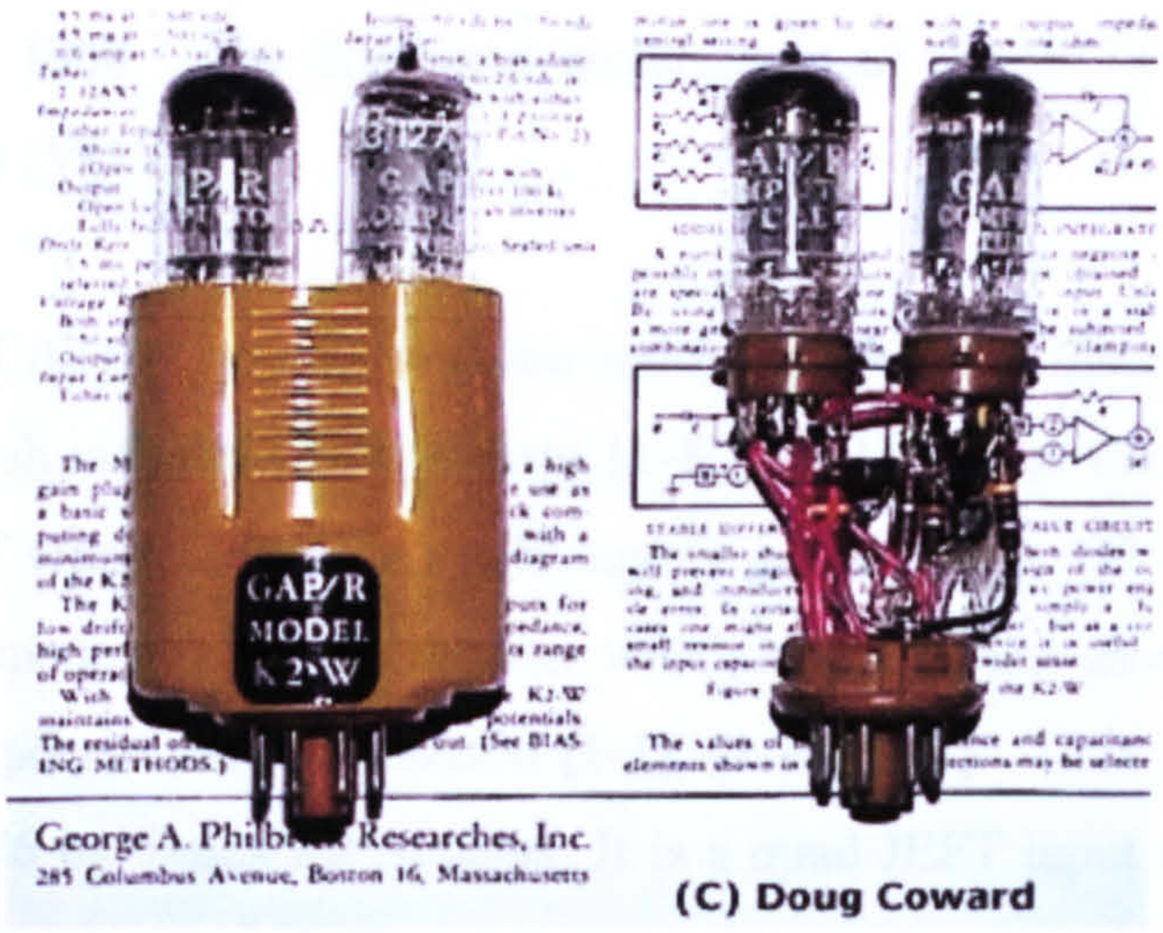
Thesis Introduction

(1.1) Historical perspective of the conventional operational amplifier

The conventional voltage operational amplifier (op-amp) was invented by the pioneer physicist at the Massachusetts Institute of Technology, George A. Philbrick in 1940s **[1-1]**, **[1-2]**, and **[1-3]**. Having said that, many engineers had a similar idea on how to design the op-amp, although they were not very successful in bringing those ideas into reality. One of these engineers was Loebe Julie **[1-3]**, hired by Professor Louis Ragazzini at Columbia University's Division of War, New York, to undertake research on amplifiers and analog computers, for deployment in military equipment. Despite the fact that Loebe Julie's amplifier had unique features, none-the-less it did not have much overall gain even with added positive feedback **[1-3]**.

Early references to the op-amp date back to 1947 and can be found in **[1-1]**, **[1-2]**, **[1-3]**, **[1-4]**, and **[1-5]**. The technical work of George A. Philbrick **[1-1]**, **[1-3]** laid the foundations of op-amp design. The op-amp became a reality during World War II, as USA National Defence Research Council set a project to build an electronic-sight simulator for fighter aircraft, and a guided bomb trainer **[1-3]**.

The op-amp is the basic building block used in analog computation, to perform mathematical operations, such as differentiation, multiplication, division, integration, and addition, on the input signals. The world's first op-amps were made out of vacuum tubes in 1952 as it is shown in Fig.1.1. The Burr-Brown Research Co. modular vacuum-tube op-amps are outstanding early examples of practical op-amps, reported in **[1-3]**. The problems with vacuum tubes are that they are bulky, high voltages and low frequencies in contrast to twenty-first century's technology.



© Philbrick Operational Amplifier

Figure 1.1 General-Purpose Computing Op-Amp Tubes (1952), **[1-1]**, **[1-2]**, and **[1-3]**

The beginning of the 1960s op-amps were built as hybrid circuits because integrated circuit fabrication was still in its infancy. Hence, they were quite expensive and normally only used for military and aerospace purposes **[1-3]** and **[1-6]**. Between 1963-1965 Fairchild Semiconductor Corp. developed and produced the first solid-state monolithic op-amp, the μA702, designed by Widler **[1-1]**, **[1-3]**, **[1-6]**. This was rapidly overtaken, and replaced, by the better performance μA709 in the late 1960s **[1-3]**, **[1-5]**. The μA709 had significant advantages, particularly with respect to bandwidth, lower input current, and more importantly it was easier to design with and to use than the μA702.

After the great success of the μA709 Widlar left Fairchild Semiconductor and moved to a young company called National Semiconductor, **[1-3]**, **[1-5]**, and **[1-6]**. National Semiconductor released several new models of op-amps designed by Widlar, including the LM101 in 1967 **[1-3]**. The majority of the characteristics of the LM101 were significantly better than those μA702, and μA709. The key characteristic that was notable was that the LM101 was the first operational amplifier to offer 'short-circuit protection' **[1-1]**, **[1-3]**, and pin-outs for external frequency compensation. Soon after general purpose op-amps such as the μA741 began to appear. The μA741was the first op-amp to have internal compensation, Fairchild Semiconductor introduced it in 1968. The functional architecture of the μA741 is typical of most voltage op-amps (VOA).

The RCA type CA3130 op-amp was introduced in 1974 for the military applications, and possible harsh industrial environment **[1-3]**, **[1-5]**. It was the first FET input op-amp, capable of working from a single supply in the range +5V to +15V. National Semiconductor made the LF355 device, which was the first monolithic JFET input op-amp to incorporate ion implantation **[1-1]**, **[1-3]**, **[1-5]**. Then followed the design of TL084 in 1976 by Texas Instruments. It is a quad JEFT input op-amp, with a low bias current, and high speed **[1-3]**.

(1.2) Voltage op-amp versus current-feedback op-amp

The op-amp has steadily evolved with performance improvements over the years by the specialist manufacturers. Although it was referred to as the op-amp, the conventional op-amp is actually a voltage op-amp (VOA), so named because it has the distinctive characteristic of a high input impedance at both the inverting and non-inverting input terminals.

Although several attempts were made to improve the performance of the basic VOA structure, the architecture of the VOA unfortunately has inherent limitations in both the gain-bandwidth trade-off and slew-rate. Typically, the gain-bandwidth product is a constant and the slew-rate is limited to a maximum value determined by input stage bias current.

The slew-rate limitations of the VOA are overcome in a new architecture op-amp, referred to as the current-feedback op-amp (CFOA) **[1-7]**, **[1-8]**, so-called because the feedback signal fed into the low input impedance inverting input terminal is current rather than voltage. Typically, slew-rate values for the CFOA range from 500V/μs to 2,500V/μs **[1-9]**, **[1-10]**, **[1-11]**, whereas the slew-rates of VOAs are much lower, in the region of 1V/μs to 500V/μs. This is a direct result of the use of current as the feedback error signal. An advantage related to the high slew-rate achieved in the CFOA is that the bandwidth is almost independent of the closed-loop gain, unlike the VOA where the gain-bandwidth product is constant. This gives the CFOA particular advantages in applications requiring variable closed-loop gains with constant bandwidth, such as in automatic gain control (AGC).

Although the idea of the CFOA existed some thirty years ago **[1-11]**, it was market demand for video signal processing that raised interest in the development of a monolithic CFOA in 1987 by Elentec **[1-11]**, **[1-12]**. Another factor that held back the arrival of the CFOA was the lack of an advanced complementary bipolar technology with PNP transistors providing electrical performances comparable with those of NPN types. The semiconductor technique that enabled this is dielectric isolation which means that both PNP and NPN devices can be fabricated as vertical transistors, and hence offer similar performances.

Unfortunately, the CFOA exhibits relatively poor DC precision, compared with the VOA. However, the nature of the many high frequency applications is such that precision may not be an issue with the result that the very high inherent slew-rate puts the CFOA in the spotlight **[1-9]**.

The CFOA can offer considerable performance advantages when used to realise IF and RF applications **[1-13]**, **[1-14]**. The CFOA design approach has worked well as evidenced by a large number of engineers who work worldwide in the field of high-speed analog design. Moreover, the CFOA is absolutely necessary to digital engineers who are involved in the design of high-speed analog to digital conversion systems, since analog-to-digital conversion depends heavily on the sampling process in order

not to obscure information **[1-9]**, and **[1-13]**. It is necessary to sample a signal at twice its highest frequency to obtain all the information from the signal. The CFOA delivers high slew-rate and, as such, is the most suitable op-amp for this operation.

For video-systems engineers there are two important specifications to be considered, namely (i) the differential gain (DG), and (ii), the differential phase (DP) **[1-11]**. DG and DP are two figures of merits of an op-amp that relate to the incremental change in closed-loop gain and phase resulting from a change in input and output referenced to zero volts for a specific frequency. The DG and DP of most VOAs are not constant when varying DC offsets are added to a constant-frequency AC input signal **[1-11]**. This can result in problems when processing composite video signals, with picture distortion resulting if the DG and DP are too high. Due mainly to circuit topology, the typical CFOA exhibits a much better DG and DP performance than the typical VOA, thus making the CFOA an excellent amplifier for dealing with composite video signals. The other significant application areas for the CFOA are in high speed active-filter design, and line drivers.

Despite the many advantages of the CFOA over the VOAs, there exist certain limitations, one of which is the common-mode rejection ratio. The CMRR of the CFOAs is generally quite poor mainly because of the asymmetrical complementary-pair input stage, and the fact that input bias currents are unequal and uncorrelated **[1-15]**.

(1.3) Aim of the research and structure of the thesis

The aim of this research programme was to design and develop a novel bipolar junction transistor CFOA with a CMRR suitable for RF applications. The research focused on investigation of existing CFOAs with the goal of improving CMRR, Bandwidth, Voltage Offset and Slew-Rate performance.

The thesis is divided into seven main chapters and, to make the reading of the thesis more straightforward, only the results of longer mathematical derivations are included in the relevant text: the full calculations are given in an Appendix at the end of each chapter.

Following this introductory chapter, the work in Chapter Two is concerned with the definition and measurement of the terminal parameters of the CFOA regarded as a 'black box'. Chapter Two illustrates that there are many ways in which the CFOA can be tested, where they are forms of inspection to ensure that they functional tests that check the operation. Moreover various testing methods for circuits with SPICE simulation software are studied and evaluated. These include determining a wide range of techniques of simulating and testing 'industry standard' circuits used and in analogue amplifier design.

Chapter Three and Four are both critical review chapters of conventional CFOA designs. In Chapter Three a bench-mark for the conventional CFOA is established, against which future improved CFOA schemes can be compared. Chapter Four focuses on examination of the closed-loop performance of the basic CFOA, with particular emphasis on the dynamic response. Also the design, performance, and advantage of the CFOA in its ability to provide a substantially constant closed-loop bandwidth for closed-loop voltage gain and high slew-rate is reviewed.

Chapter Five contains details of six new input stage designs for the CFOA. This chapter considers the trade-offs involved in the design of these new input stages intended to improve the performance of a CFOA, over that possible using the conventional input circuit configuration, with respect to three major characteristics: CMRR, offset voltage (V_{OS}) and Slew-rate (SR). The results have been summarised in a CFOA comparative performance table presenting the features of the new input stage amplifier types in a range of different analogue signal processing applications.

Chapter Six deals with a new approach to CFOA design using bootstrapping techniques. In this chapter a family of fourteen new designs are presented, the first six of which incorporate the new input stages described in Chapter Five. These new CFOA designs exhibit low offset-voltage, wide bandwidth, high CMRR and improved gain accuracy, enabling them to be used in applications requiring variable closed-loop gains with constant bandwidth, such as in automatic-gain-control, video, graphics and multimedia applications. The Chapter concludes with a summary table comparing the relative characteristics of each design.

A further CFOA design is developed in Chapter Seven and a family of three new designs is presented, all based on an architecture using overall bootstrapping. The comparative results of the conventional and new CFOAs suggests a significant improvement is obtained from these new designs, mainly in CMRR and reduction in offset voltage as well as the majority of other parameters and characteristics.

Chapter Eight of this thesis summarises the work done and is followed by a reference list. Appended to the end of the thesis are conference and journal papers, by the author, on the design and development of new CFOAs.

(1.4) References

[1-1] IEEE Annals of History of Computing, July-September 1985 (Vol.7, No. 3)

[1-2] Analog Devices, Inc., 'Linear Design Seminar', USA, October, 1987, pp.II-1-II-16.

[1-3] Roon T.V., Operational Amplifier http://www.uoguelph.ca/~antoon/gadgets/741/741.html

[1-4] Hart B.L, 'Current feedback operational amplifiers: A tutorial', International Journal of Electrical Engineering Education. Vol. 32, no. 2, April 1995, pp. 108-23.

[1-5] Graeme J.G, Tobey G.E, Huelsman L.P, 'Operational amplifier design and applications', Burr-Brown Research Corporation, USA, 1971, pp.xvii.

[1-6] Truitt. T.D, and Rogers,A.E , 'Basics of Analog Computers', International John F. Rider Publisher Inc. 1960.

[1-7] Franco S, 'Current-feedback amplifiers benefit high-speed designs', EDN, January 5, 1989, pp.161-172.

[1-8] Wong J, 'Current-feedback op-amps extend high-frequency performance', EDN, October 26, 1989, pp.211-216.

[1-9] Soliman A.M, 'Design of high-frequency amplifiers', IEEE Circuits and Systems, June 1983.

[1-10] Harold P, 'Current-feedback op amps ease high-speed circuit design', EDN, July 7, 1988.

[1-11] F J Lidgey, and K Hayatleh. 'Current-feedback operational amplifier and applications', IEE, Electronics & Communication Engineering Journal, Aug.1997, pp.176–182.

[1-12] Elantec Inc., 'EL2020C 50MHz current feedback amplifier, ' datasheet,1996 Tarob Court, Milpitas, CA 95035

[1-13] Krabbe H, 'A high performance monolithic instrumentation amplifier', ISSCC Dig. Tech. Tech. Papers, Feb.1971.

[1-14] 'CCII01 Current Conveyor Amplifier', Data sheet. LTP Electronics Ltd., Oxford, UK, 1993.

[1-15] Smither M.A, Pugh D.R, and Woolard L.M, 'CMRR analysis of the 3 op-amp instrumentation amplifier', Electronics Letters, Vol.13, August 1977.

CHAPTER 2

Amplifier Parameter Definition and Testing Techniques

(2.1) Introduction

This Chapter concerns the definitions and measurements of the terminal parameters of the CFOA, regarded as a 'black box' **[2-1]**. It does not deal with the way that these parameters are related to the properties of the active and passive components of a particular circuit configuration: that is covered in Chapters Three, and Four.

As is often the way with measurement techniques, prior knowledge of the orders of magnitude of parameters to be measured is put to good use in their measurement. PSPICE simulation is used in terminal parameter determination: this brings with it the luxury of using test conditions that would not normally prevail in a laboratory test on silicon implementations of proposed CFOAs. Thus, we can apply 1μA and 1μV test signals from, respectively, infinite and zero source impedances that range from d.c to some tens of GHz.

Also, we can assume the existence of resistors of identical Ohmic value and very large ideal capacitors. Where appropriate, practical test methods are referred to physical laboratory prototypes.

(2.2) Differential and common-mode operation

(2.2.1) Differential voltage gain, A_d

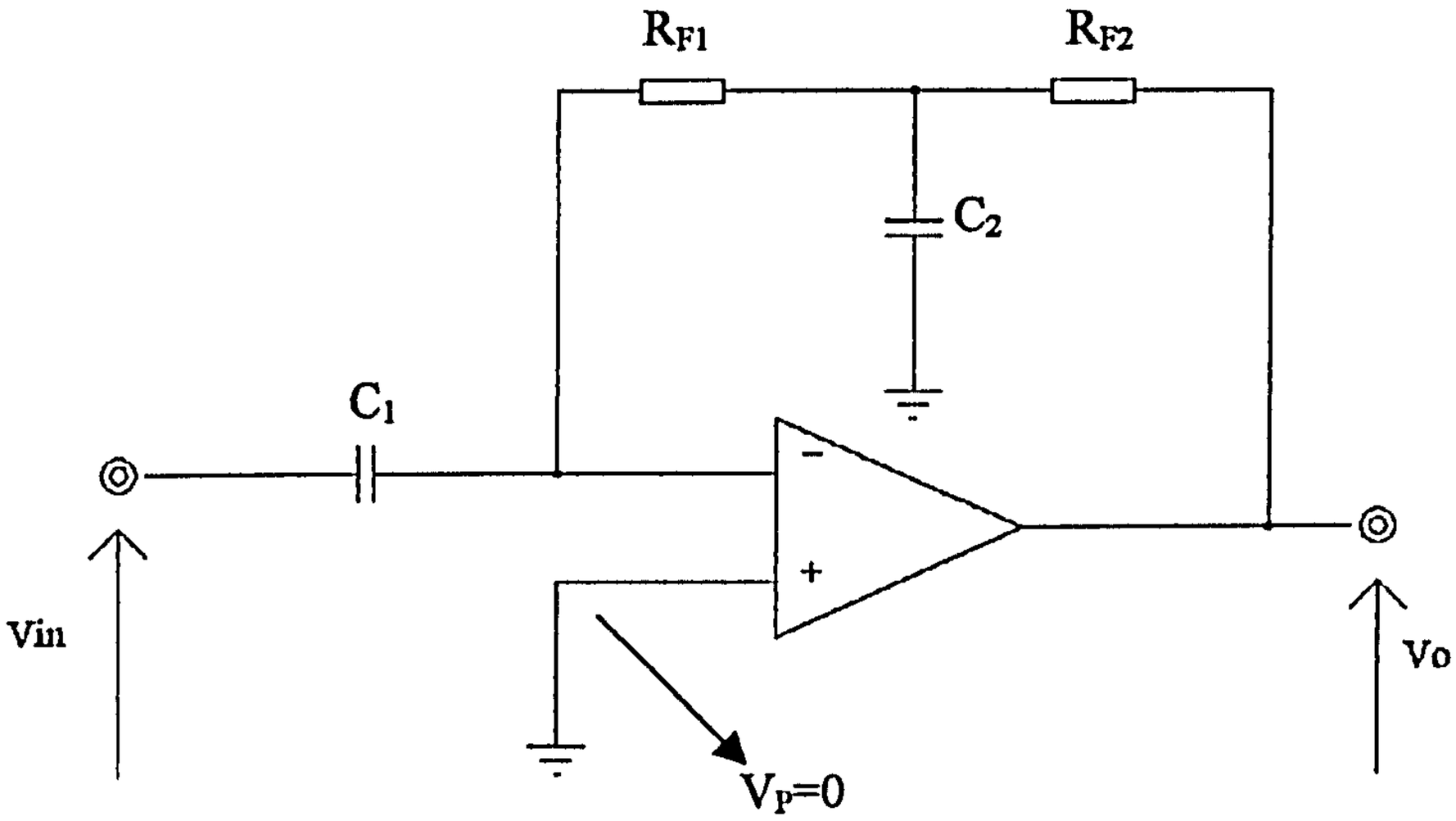


Figure 2.1 Measurement circuit for A_d

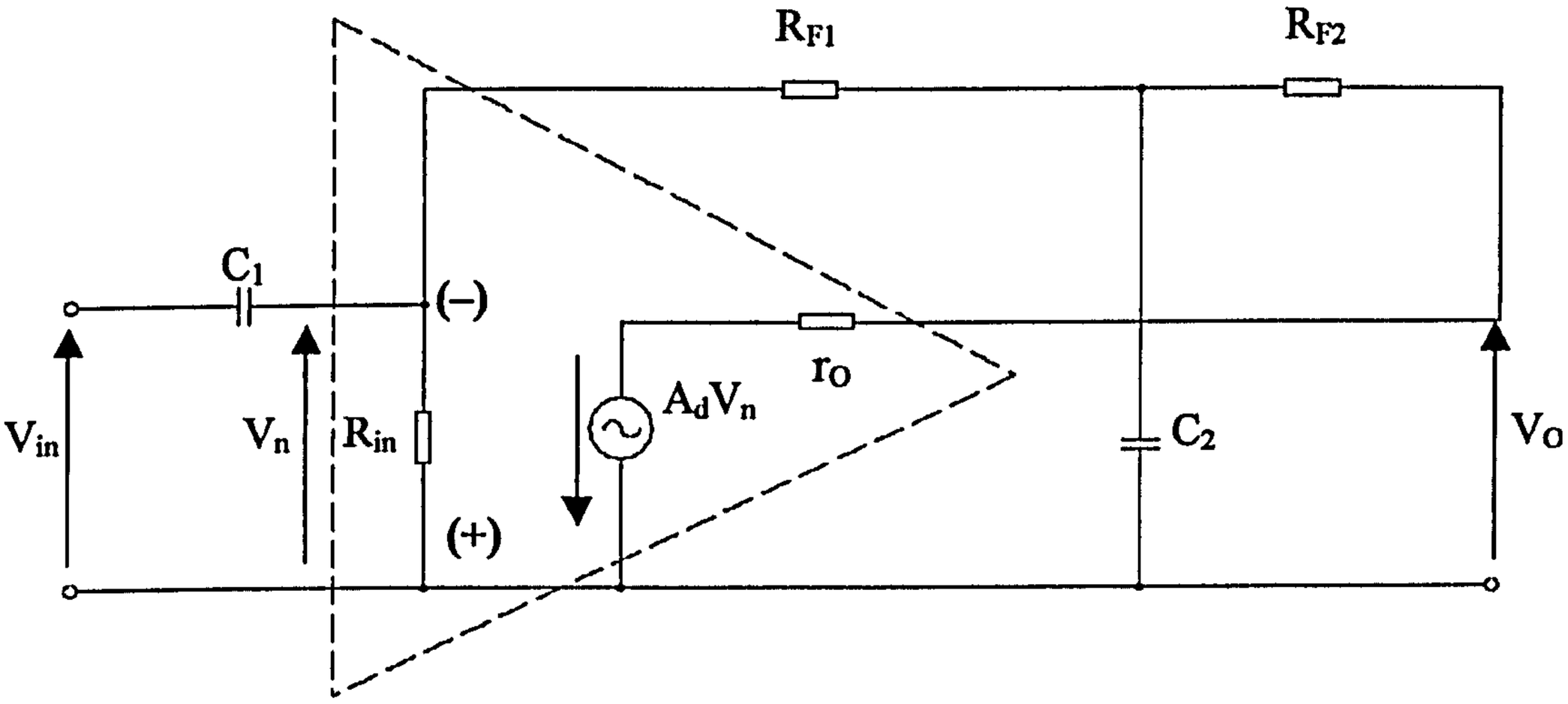


Figure 2.2 Small signal equivalent circuit

Fig.2.1 shows an appropriate measurement circuit for A_d. R_{F1}, R_{F2} provide d.c. negative feedback, necessary to ensure that the CFOA operates in the linear mode. In the small-signal equivalent circuit of Fig.2.2, the CFOA is represented by the

components within the dashed triangle. If over the test-frequency range C_2 is chosen so that $(1/\omega C_2) << (R_{F1} // R_{F2})$ the ac. feedback is de-activated.

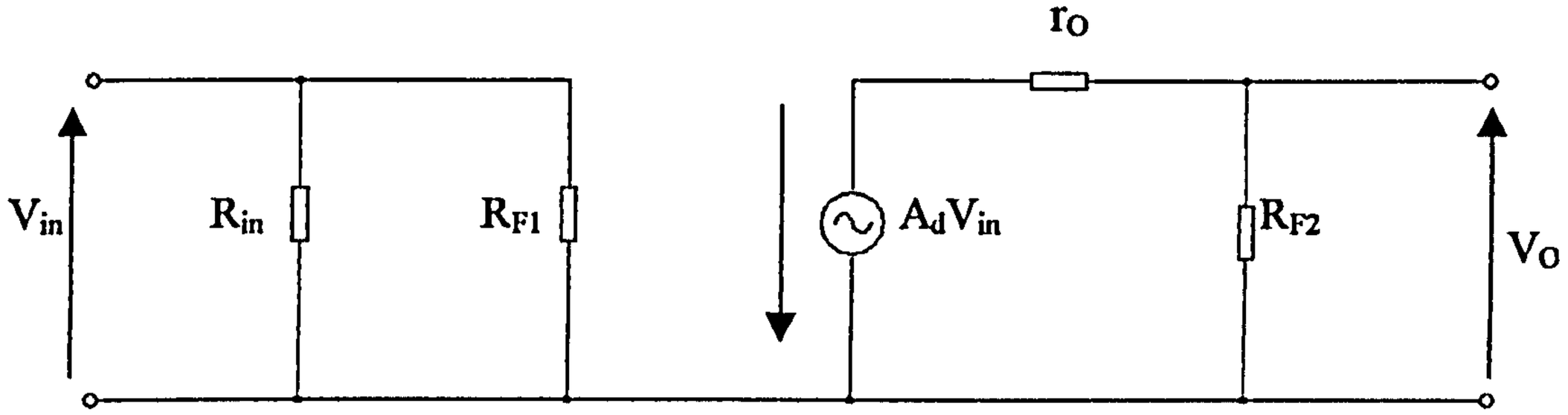


Figure 2.3 Reduced from of (Fig.2.2) for very large C_1, C_2

If, furthermore, $(1/\omega C_1) << (R_{in} // R_{F1})$ and $(R_{F2} >> r_O)$, then by inspection,

$$A_d = \left(\frac{V_o}{V_{in}}\right) \tag{2.1}$$

In simulation measurements; R_{F1}=1KΩ; R_{F2}=1KΩ; C_1=1000mF; C_2=1000mF. The full analysis involves considerable equation manipulation and can be found in Appendix 2.1 at the end of this Chapter.

(2.2.2) Common mode gain, Ac, and common mode rejection ratio, CMRR, ρ

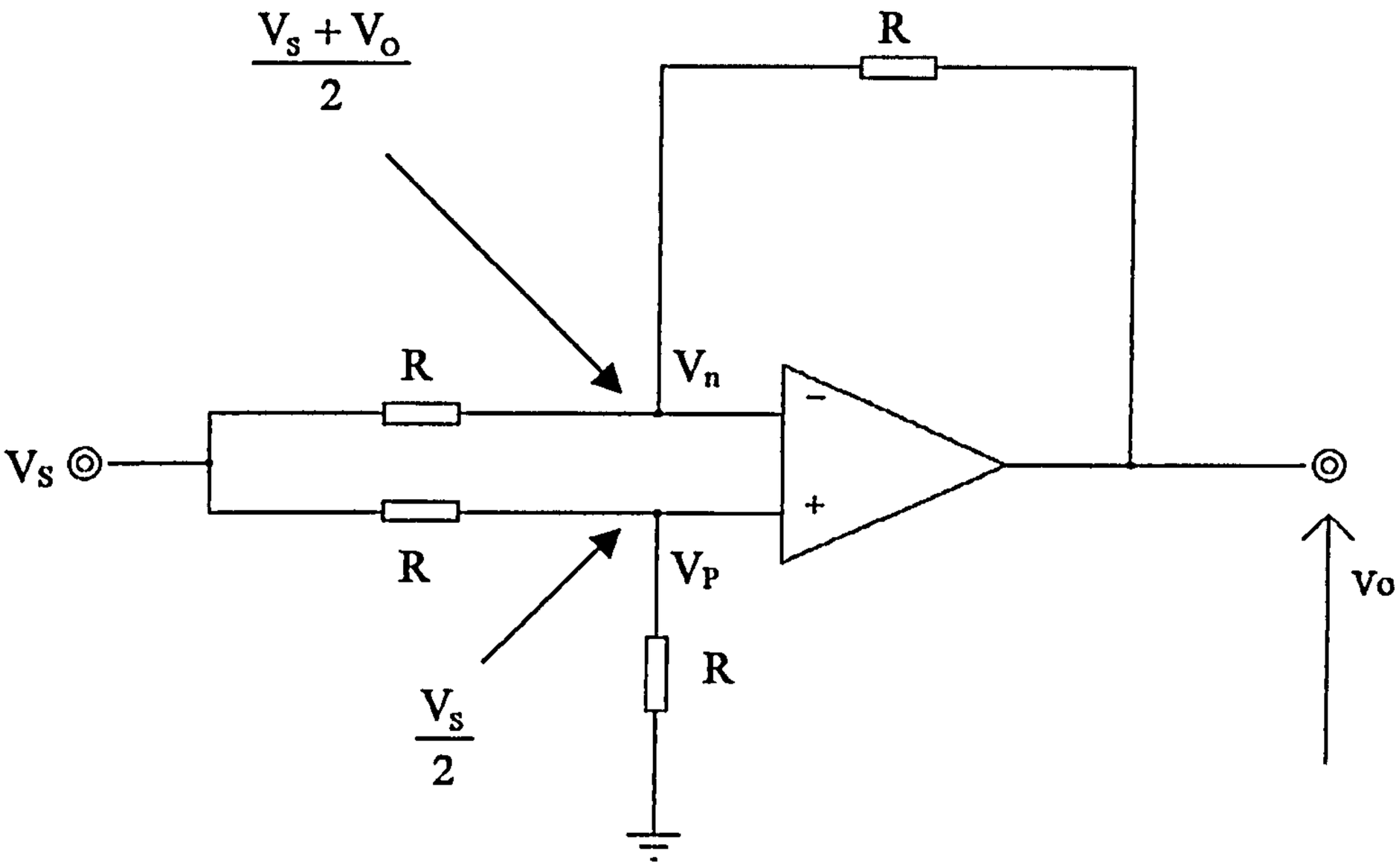


Figure 2.4 Circuit to find the CMRR, ρ
(In tests, R=1KΩ, V_S=10mV)

Fig.2.4 illustrates a circuit configuration for determining ρ as far as the CFOA is concerned. Again, the full derivation is given in Appendix 2.2

$$V_O = A_d(V_P - V_n) + \frac{A_c(V_p + V_n)}{2} \qquad (2.2)$$

In this Ac is the common-mode gain. But, by inspection, $V_p = \frac{V_S}{2}$ and $V_n = \frac{V_S + V_O}{2}$. Substituting these values in equation (2.2), **[2-2]** gives:

$$(\frac{V_O}{V_S}) = \frac{A_c}{[A_d - (\frac{A_c}{2}) + 2]} \qquad (2.3)$$

Since A_d>>Ac, equation (2.3) simplifies to equation (2.4), the full common mode voltage calculations are included in Appendix 2.3.

$$(\frac{V_O}{V_S}) \approx \frac{A_c}{A_d} \approx \frac{1}{\rho} \qquad (2.4)$$

A knowledge of A_d and A_c in dB permits a determination of ρ which is, otherwise, not easy to determine. By comparison, a practical measurement of ρ, particularly as a function of frequency is somewhat complex.

One of these **[2-3]** makes use of the fact **[2-4]**

$$\frac{1}{\rho} = \frac{\partial V_{OS}}{\partial V_c}\Big|_{V_O} \qquad (2.5)$$

Where V_{OS} is the offset voltage, discussed in the next section, and V_C is the common-mode input voltage. The requirement to hold V_O constant is what leads to circuit complexity. It should be noted that the test circuit of Fig.2.4 is not appropriate for laboratory tests because of the problems of accurate resistor matching **[2-2]**.

(2.3) Input offset voltage, V_{OS}

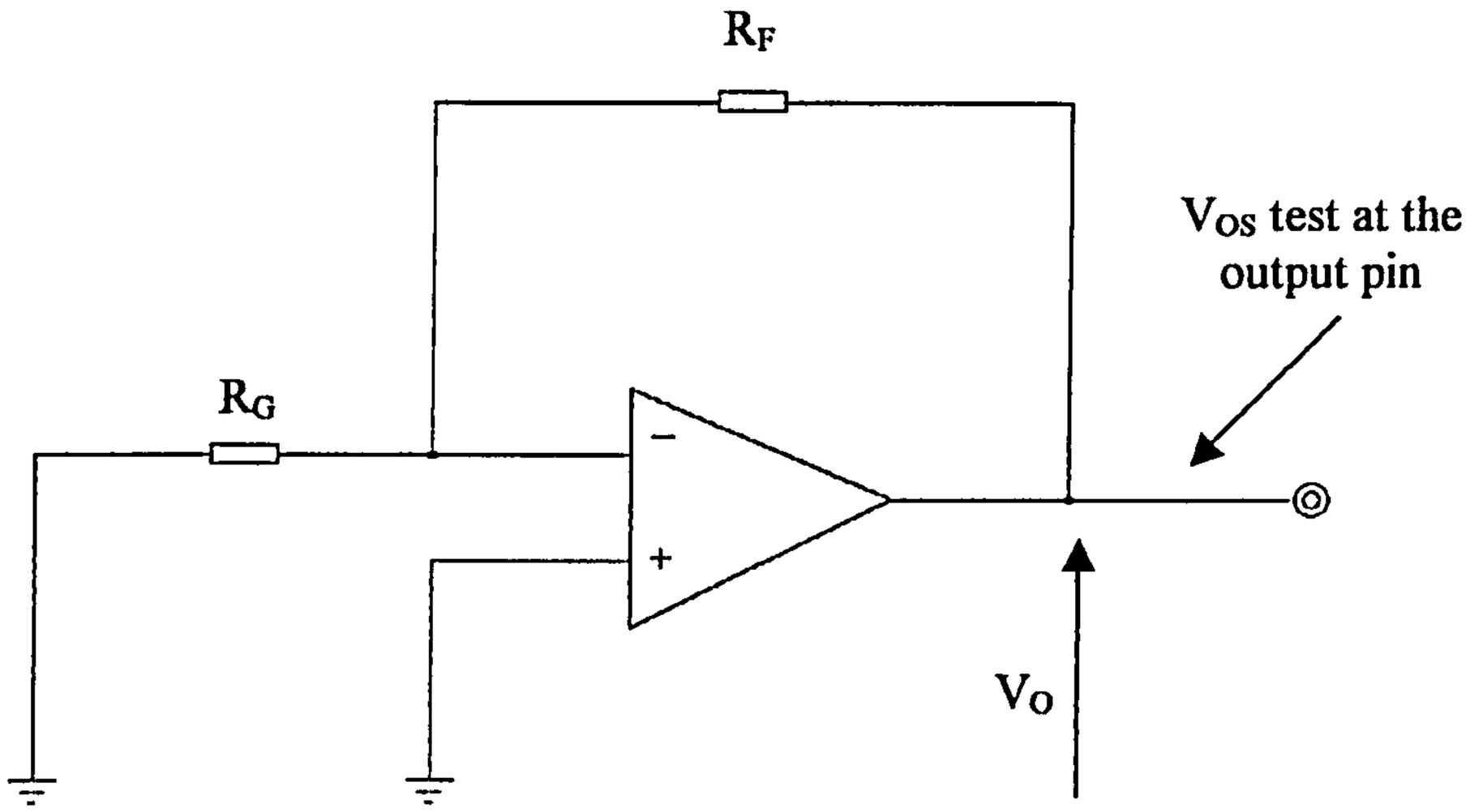


Figure 2.6 Voltage offset test circuit

Ideally, the d.c. output voltage of a CFOA, like that of a VOA, should be zero when differential input voltage is zero **[2-5]**. However, because of slight imbalances in the amplifier, examined theoretically in Chapter 3, the output voltage of a real CFOA is not zero when the input terminals are at the same potential (normally, earth potential).

The magnitude of the voltage that must be applied between the input terminals to reduce the output voltage to zero is the input offset voltage (or, differential input offset voltage), V_{OS}. Since it is normally quite small, e.g. a few millivolts, measurement of it under laboratory conditions are normally achieved by using the CFOA itself to amplify it. The circuit for this is shown in Fig.2.6, which is also used in PSPICE analysis.

It can be shown that subject to normally easily-met parameter relationships, discussed in Chapter 4,

$$V_{OS} = \pm \frac{V_O}{A_{CL}} \tag{2.6}$$

where A_{CL}= magnitude of closed loop d.c. voltage gain or, $A_{CL} = \frac{(R_F + R_G)}{R_G}$. The plus and minus sign allows for the possibilities of the imbalances. Table 2.1 show convenient test choices. The full calculation validating the use of equation 2.6 is given in Chapter 4.

R_G	R_F	Gain	Offset voltage V_{os}
1KΩ	10KΩ	11	$V_{os} \approx \pm \frac{V_o}{11}$
1KΩ	5KΩ	6	$V_{os} \approx \pm \frac{V_o}{6}$
1KΩ	1KΩ	2	$V_{os} \approx \pm \frac{V_o}{2}$

Table 2.1 Finding V_{os} from V_o for the circuit of Fig.2.6

(2.4) Unity-gain frequency response

This is a small-signal parameter that defines the frequency at which the a.c. gain is 3dB down its d.c/low frequency value **[2-6]**. It is normally measured with the CFOA connected as a voltage-follower (see Fig.2.7): a parallel R, C load reduces output noise.

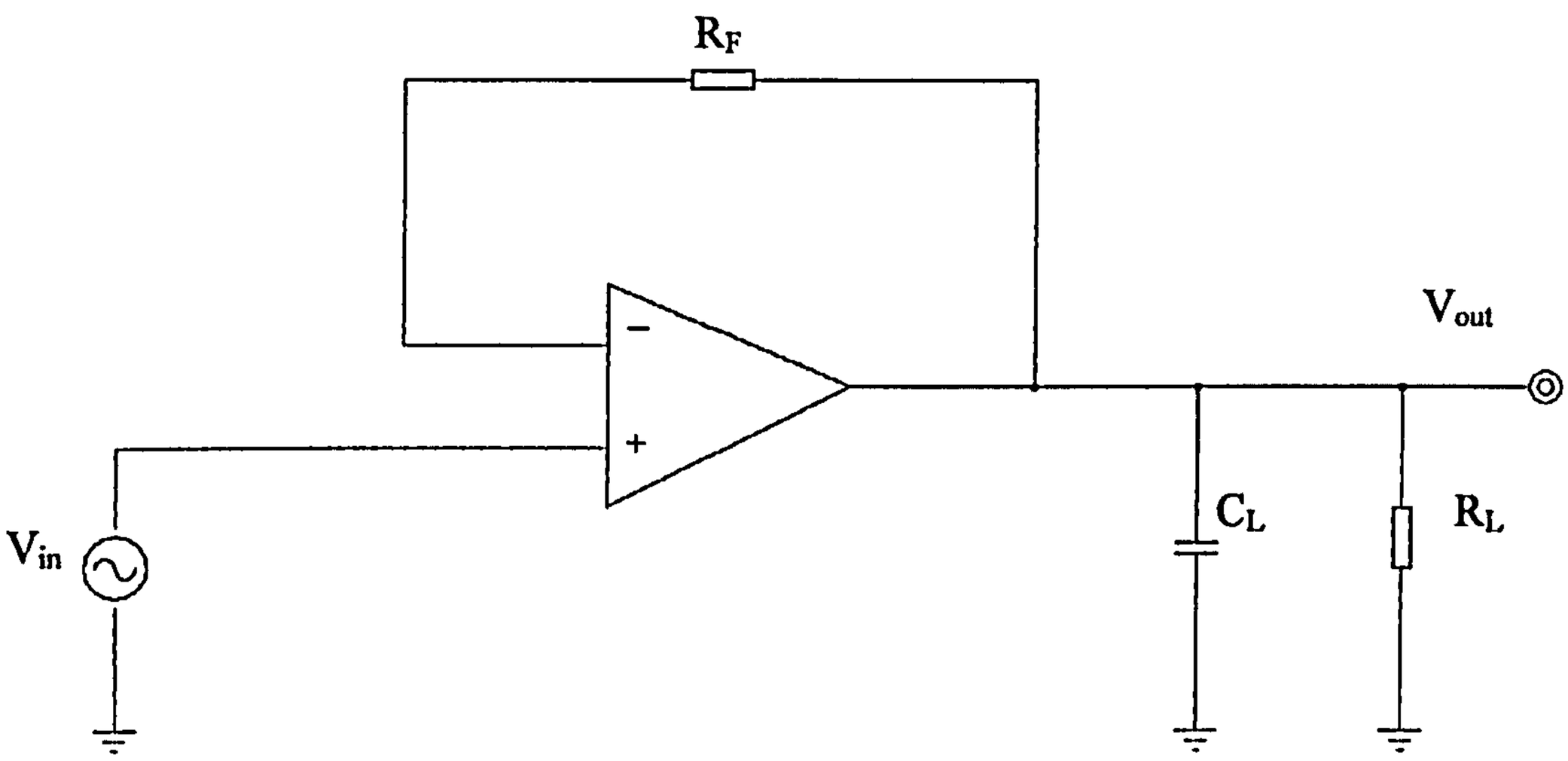


Figure 2.7 Frequency-response measurement circuit

The a.c. unity-gain error is:

$$\varepsilon = \left(\frac{V_{out} - V_{in}}{V_{in}}\right) \tag{2.7}$$

Fig.2.8 shows how it is determined from simulation.

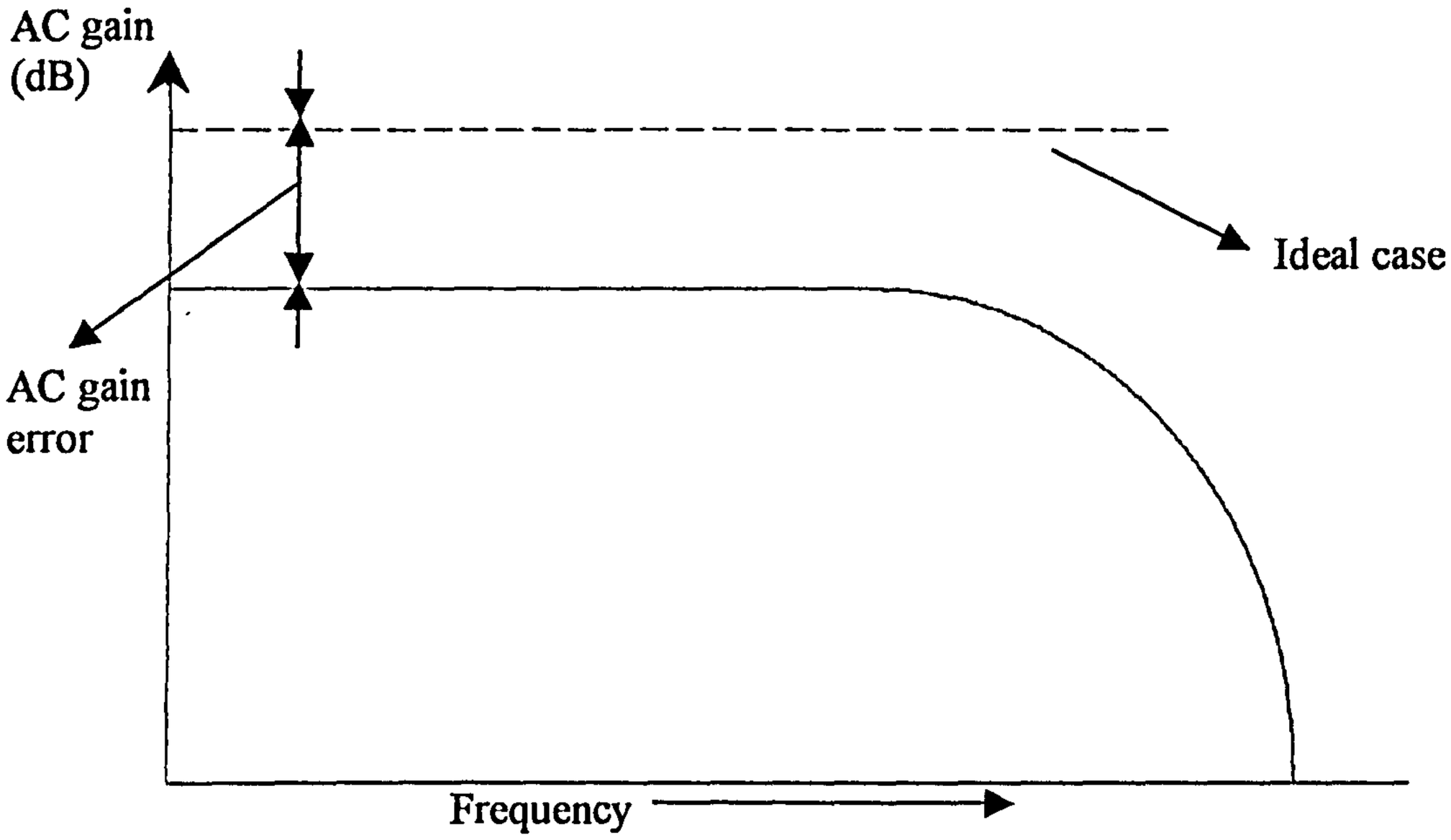


Figure 2.8 Definition of a.c.-gain error

(2.5) Slew Rate (S)

This is a large-signal parameter. It defines the magnitude of the maximum rate at which the output voltage can change when a large signal voltage is applied to the input. It is expressed in V/μs **[2-7]**.

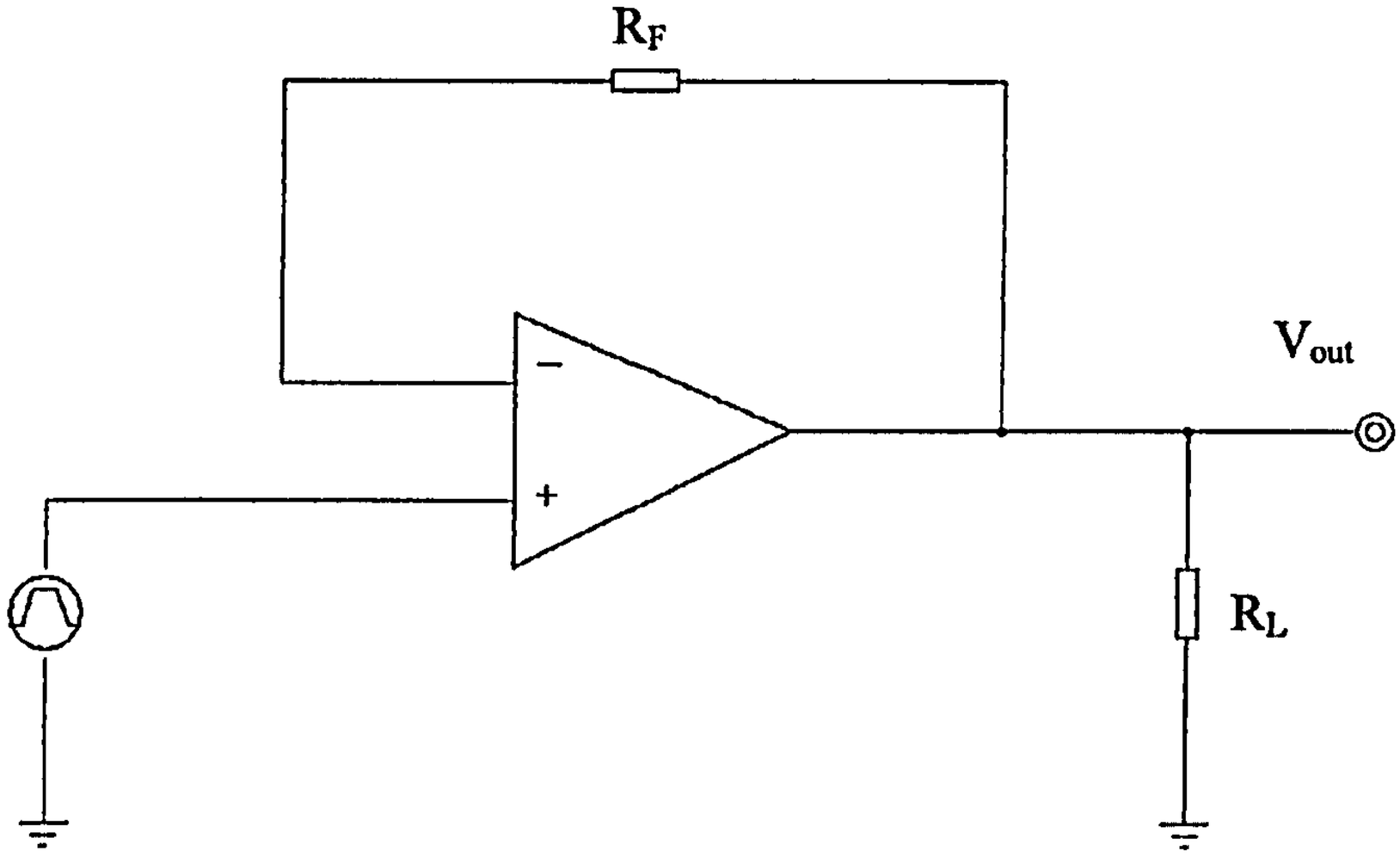


Figure 2.9 Slew rate measurement circuit

As in the measurement of the frequency response, the CFOA is connected in the voltage–follower configuration (Fig.2.9). A rectangular voltage test pulse of amplitude V and rise and fall times t_{ir}, t_{if} is applied to the input (Fig.2.10 a). The resulting output rise and fall times are t_{or}, t_{of}, respectively. The slew rate in the positive-going edge is S_+, where,

$$S_+ = \left|\frac{dV}{dt}\right| = \frac{V}{t_{or}} \qquad (2.8)$$

That for negative-going edge is S_-,

$$S_- = \frac{V}{t_{of}} \qquad (2.9)$$

Since these two parameters may differ, the smaller is taken as defining the slew-rate. To determine if 'large -signal' conditions apply V can be increased. If S_+, S_- do not change, then V is 'large' enough. Similarly to determine if t_{ir}, t_{if} are sufficiently small in comparison with t_{or}, t_{of} (so they do not play a part in determining) them, t_{ir}, t_{if} can be doubled. If S_+, S_- do not change then t_{ir}, t_{if} are sufficiently small. A good measurement choice is $t_{ir} \leq$ (expected t_{or})/10 and $t_{if} \leq$ (expected t_{of})/10.

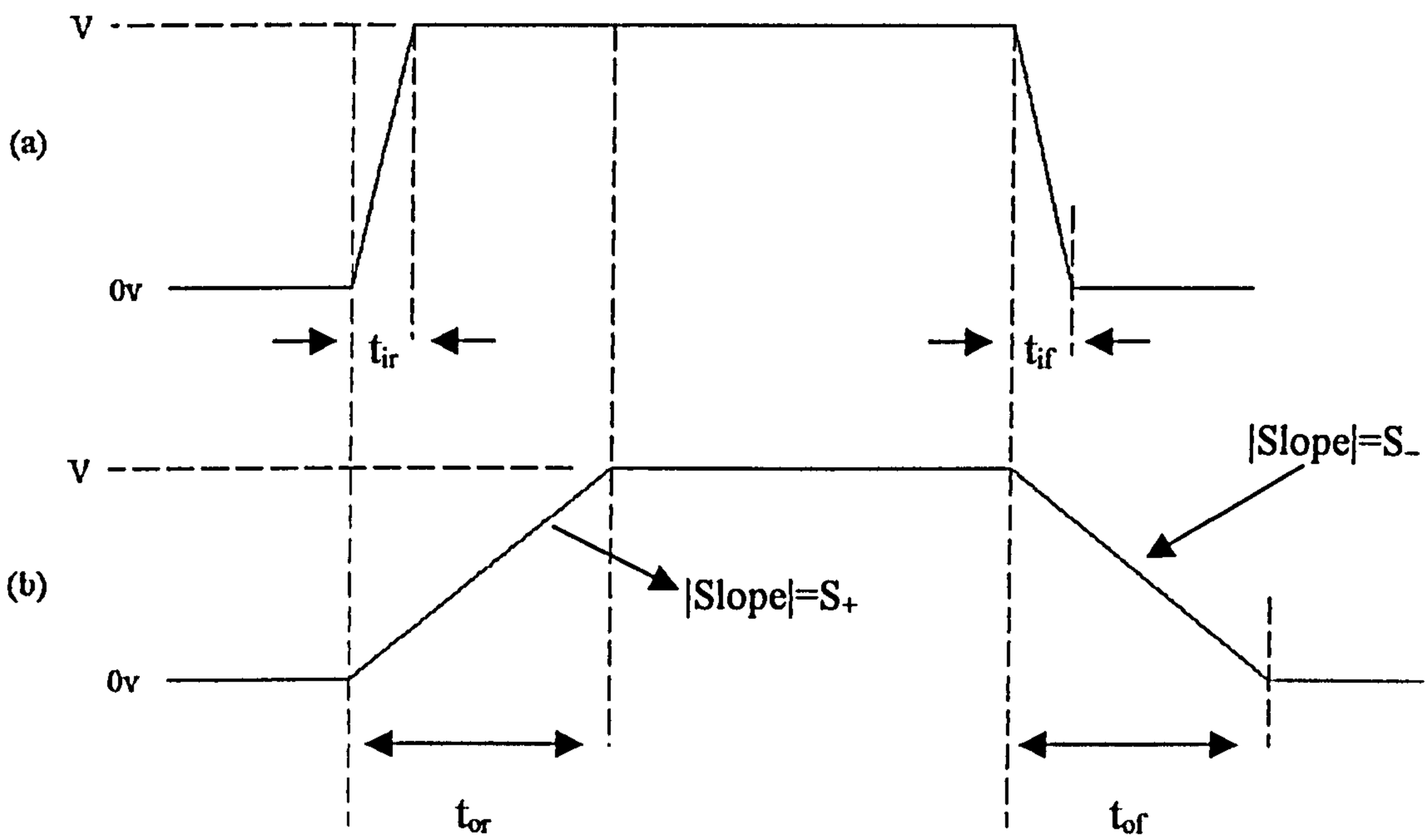


Figure 2.10 Waveforms for Fig.2.9

Related to S is the full-power bandwidth fp.

$$f_p = \frac{S}{2\pi \hat{V}_{in}} \tag{2.10}$$

(2.6) Input impedances

The input impedances of the VOA are the normally the same at each of its two input terminals because the latter is based on an emittier coupled pair input stage. However, this is not the case for the CFOA because of its different architecture.

The CFOA has a complementary-pair input stage as a replacement to the traditional long–tail pair input design. This means that a slightly different measurement technique has to be used for the two inputs.

Details of these measurements are outlined, briefly, in the following two sub-sections.

(2.6.1) The non-inverting input impedance

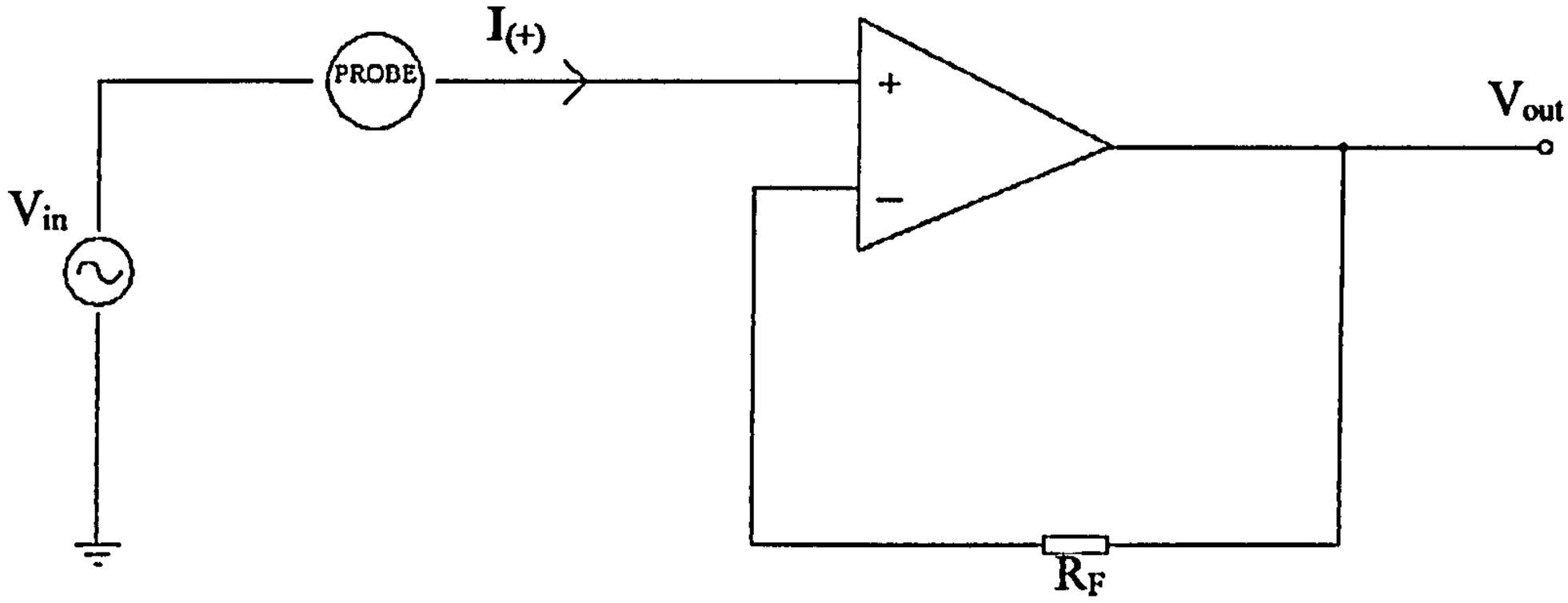


Figure 2.11 Test circuit for non-inverting input resistance

The magnitude of the input impedance, as a function of frequency, looking in at the non-inverting input of the CFOA is conveniently measured by connecting the amplifier to operate as a voltage-follower with a d.c. input bias voltage of zero volts. A small amplitude voltage signal V_{in} of variable frequency, is applied at the non-inverting input and the resulting input current, I_+, measured (Fig.2.11)

$$\text{Then, } |Z_{i(+)}| = \frac{V_{in}}{I_+} \qquad (2.11)$$

From a plot of $|Z_{i(+)}|$ versus frequency, the input impedance can be interpreted as a parallel combination of resistance and capacitance.

(2.6.2) Inverting input impedance

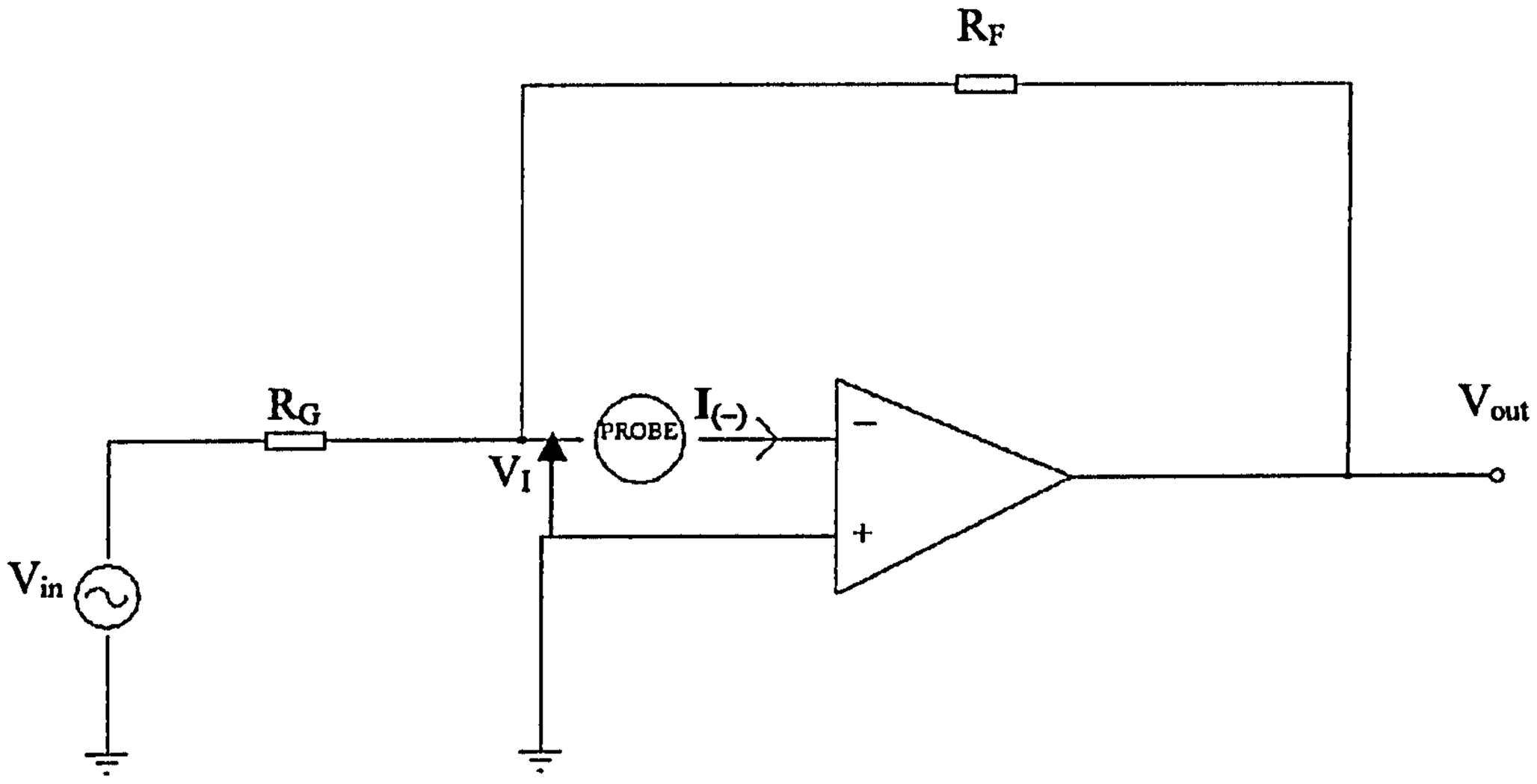


Figure 2.12 Test circuit for the inverting input impedance

Fig.2.12 shows a convenient test circuit for measuring the magnitude, $|Z_{i(-)}|$, of the impedance looking in at the inverting input terminal. As in the case of the measurement of $|Z_{i(+)}|$, V_{in} is a voltage signal of variable frequency but now V_{in} is reduced in amplitude by the presence of R_G, R_F. This is necessary because V_I the potential difference between the input terminals must be small to limit the magnitude of $I_{(-)}$.

$$|Z_{i(-)}| = \frac{V_I}{I_-} \qquad (2.12)$$

(2.7) Z-point impedance

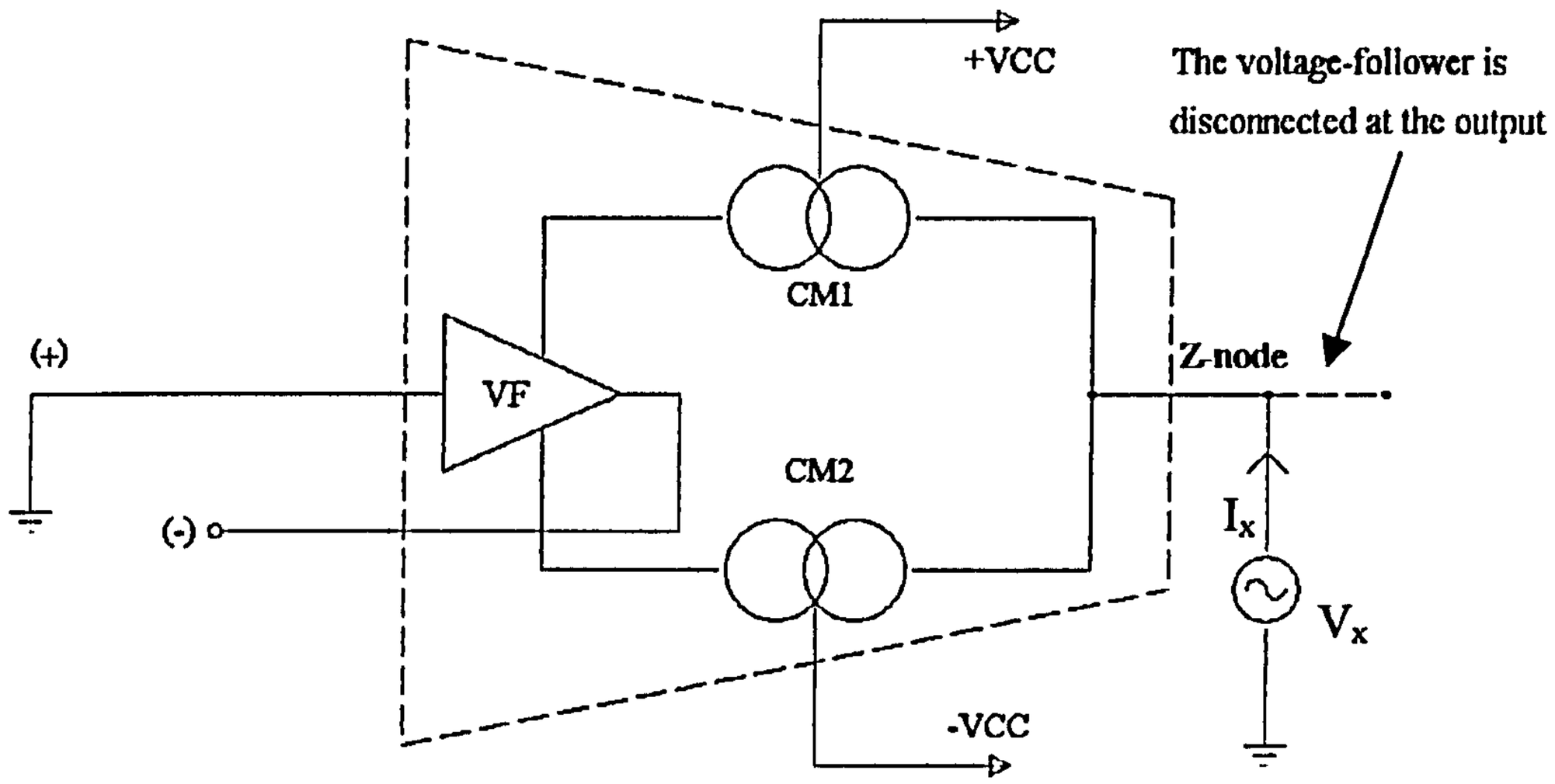


Figure 2.13 Measuring the output resistances at Z-node

The circuit of Fig.2.13 was used to obtain simulation results for the open-loop output impedances of the current-mirror section of the CFOA (i.e. Z-node). This determines the transimpedance of the CFOA, and also has a direct effect on the output impedance of the amplifier.

A sinusoidal signal, V_x, of 0.1V peak amplitude is applied, as shown, when the d.c. bias level of the current-mirror output is zero. This ensures that the current-mirrors operate in the linear region.

The resulting current, I_x, is measured then output impedance is given by the ratio V_x/I_x. The magnitude of this ratio is plotted as a function of frequency.

(2.8) Open-loop output resistance, r_o

The measurement of open-loop output impedance and, hence, output resistance, r_o, presents some difficulties.

Referring to Fig.2.13, if the non-inverting input of the CFOA is earthed and there is no feedback, the high output resistance of the two current-mirrors causes the Z-node to assume a potential corresponding to the simulation voltage of either CM1 or CM2, depending on whether the output current CM1 (nominally equal to that of CM2) is greater than that of CM2 or less.

To overcome this problem it is necessary to apply at Z-node a direct current, from an infinite impedance source, of such a magnitude and direction as is required to restore the d.c. voltage at Z-node to zero. The output impedance of the CFOA is then found by applying a small current change at the output of the voltage follower, observing the resulting voltage change and forming the appropriate ratio.

Summary

This chapter considered techniques for the measurement of key parameters of the CFOA: PSPICE simulation software was developed for this purpose. The results of the measurements are presented in later chapters alongside the theory developed to explain them. The reading of the chapter was made more straightforward, by having only the results of longer mathematical derivations included in the relevant text, with the full working given in an appendix linked directly to the end of this chapter.

(2.9) References

[2-1] Lunn C, 'The Essence of Analog Electronics', Prentice Hall Europe, 1997, pp. 60-62.

[2-2] Franco S, 'Design with operational amplifiers and analog integrated circuits', McGraw-Hill Companies, Inc., 3rd edition, 2002, pp.71-79.

[2-3] Hart B.L, 'Common-mode rejection explained', Wireless World, September 1983, pp.36-38.

[2-4] Gray P.R, Meyer R.G, 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Canada, 1984, pp.208-362.

[2-5] Maddock R.J, Calcutt D.M, 'Electronics for Engineers', Longman Scientific & Technical, UK, 2nd Edition, 1994, pp.514-590.

[2-6] Sedra A.S, Smith K.C, 'Microelectronic Circuits', Oxford University Press, UK, 4th Edition, 1998, pp.28-47.

[2-7] Boylestad R.L, Nashelsky L, 'Electronic Devices and Circuit Theory', Prentice Hall International, Inc., USA, 7th Edition, 1999, pp.630-633.

APPENDIX 2

APP 2.1 Calculation of A_d (Differential mode voltage gain) in PSPICE simulation

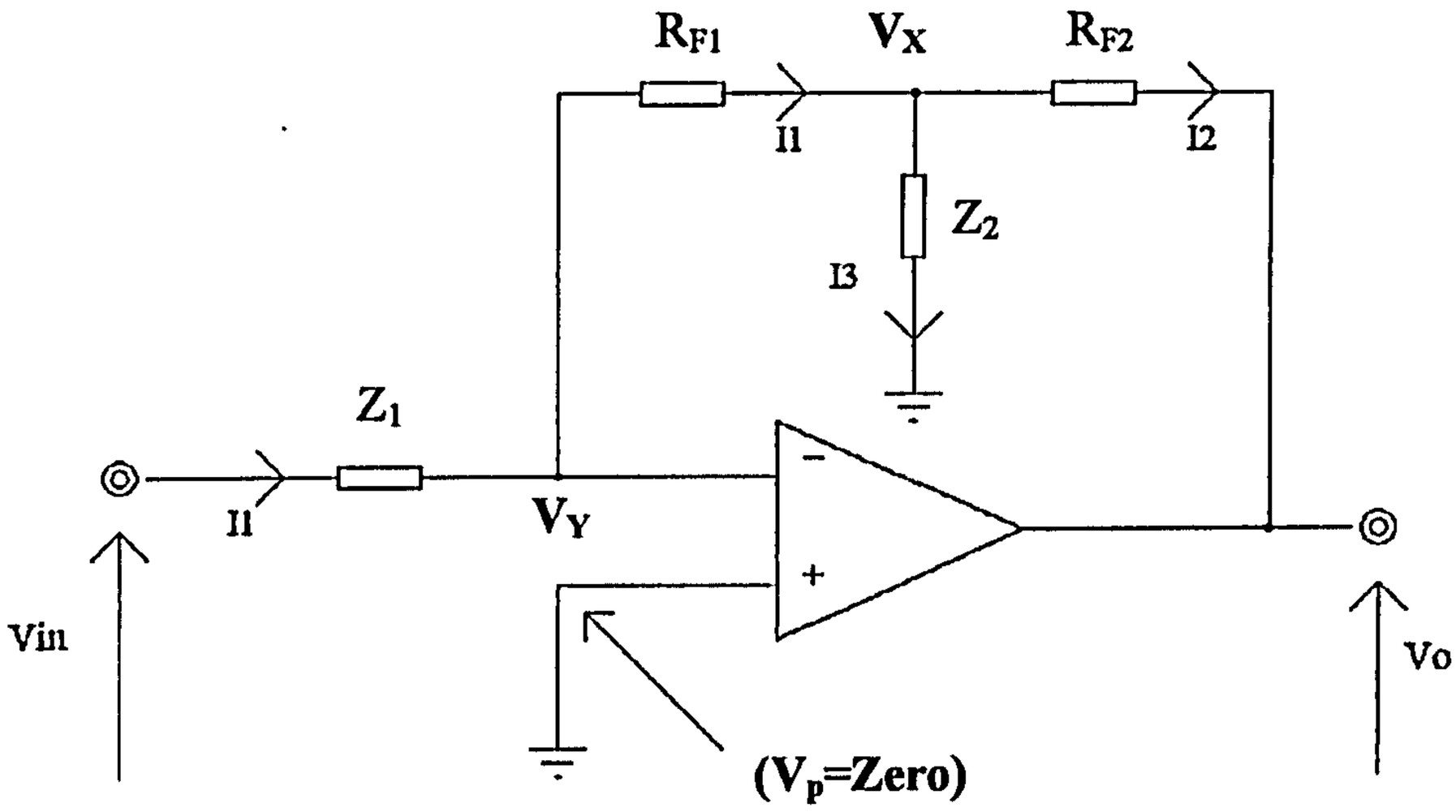


Figure A 2.1.1

$$I_1 = \frac{V_{in} - V_Y}{Z_1} = \frac{V_Y - V_X}{R_{F1}} \quad ; \quad I_2 = \frac{V_X - V_O}{R_{F1}}$$

$$I_3 = \frac{V_X}{Z_2}$$

$$\frac{V_{in} - V_Y}{Z_1} = \frac{V_Y - V_X}{R_{F1}} \longrightarrow V_Y - V_X = \frac{R_{F1} \times (V_{in} - V_Y)}{Z_1}$$

$$-V_X = \frac{R_{F1} \times (V_{in} - V_Y)}{Z_1} - V_Y \longrightarrow V_X = V_Y - \frac{R_{F1} \times (V_{in} - V_Y)}{Z_1}$$

$$V_X = V_Y - \frac{R_{F1} \times V_{in}}{Z_1} + \frac{R_{F1} \times V_Y}{Z_1}$$

Since $V_O = A\times(V_P - V_Y)$, and since V_p=Zero $\Rightarrow$ $\therefore V_O = -A\times V_Y$

$$V_Y = -\frac{V_O}{A}$$

Since $I_1 = I_2 + I_3$ K.C.L

$$\frac{V_{in}-V_Y}{Z_1} = \frac{V_X - V_O}{R_{F2}} + \frac{V_X}{Z_2} \longrightarrow \frac{V_{in}}{Z_1} - \frac{V_Y}{Z_1} = \frac{V_X}{R_{F2}} - \frac{V_O}{R_{F2}} + \frac{V_X}{Z_2}$$

Substitute for V_Y, and V_X

$$\frac{V_{in}}{Z_1} + \frac{V_O}{A\times Z_1} = -\frac{R_{F1}\times V_{in}}{Z_1\times R_{F2}} + \frac{R_{F1}\times V_Y}{Z_1\times R_{F2}} + \frac{V_Y}{R_{F2}} - \frac{R_{F1}\times V_{in}}{Z_1\times Z_2} + \frac{R_{F1}\times V_Y}{Z_1\times Z_2} + \frac{V_Y}{Z_2} - \frac{V_O}{R_{F2}}$$

$$\frac{V_{in}}{Z_1} + \frac{R_{F1}\times V_{in}}{Z_1\times Z_2} + \frac{R_{F1}\times V_{in}}{Z_1\times R_{F2}} = -\frac{V_O}{A\times Z_1} - \frac{V_O}{R_{F2}} - \frac{R_{F1}\times V_O}{A\times Z_1\times R_{F2}} - \frac{V_O}{A\times R_{F2}} - \frac{R_{F1}\times V_O}{A\times Z_1\times Z_2} - \frac{V_O}{A\times Z_2}$$

$$V_{in}\left[\frac{1}{Z_1} + \frac{R_{F1}}{Z_1\times Z_2} + \frac{R_{F1}}{Z_1\times R_{F2}}\right] = -V_O\left[\frac{1}{A\times Z_1} + \frac{1}{R_{F2}} + \frac{R_{F1}}{A\times Z_1\times R_{F2}} + \frac{1}{A\times R_{F2}} + \frac{R_{F1}}{A\times Z_1\times Z_2} + \frac{1}{A\times Z_2}\right]$$

$$\frac{V_O}{V_{in}} = -\frac{\left[\frac{1}{Z_1} + \frac{R_{F1}}{Z_1\times Z_2} + \frac{R_{F1}}{Z_1\times R_{F2}}\right]}{\left[\frac{1}{A\times Z_1} + \frac{1}{R_{F2}} + \frac{R_{F1}}{A\times Z_1\times R_{F2}} + \frac{1}{A\times R_{F2}} + \frac{R_{F1}}{A\times Z_1\times Z_2} + \frac{1}{A\times Z_2}\right]}$$

By multiplying the top and the bottom by $(Z_1\times Z_2)$

$$\frac{V_O}{V_{in}} = -\frac{[Z_2 + R_{F1} + \frac{Z_2 \times R_{F1}}{R_{F2}}]}{[\frac{Z_2}{A} + \frac{Z_1 \times Z_2}{R_{F2}} + \frac{Z_2 \times R_{F1}}{A \times R_{F2}} + \frac{Z_1 \times Z_2}{A \times R_{F2}} + \frac{R_{F1}}{A} + \frac{Z_1}{A}]}$$

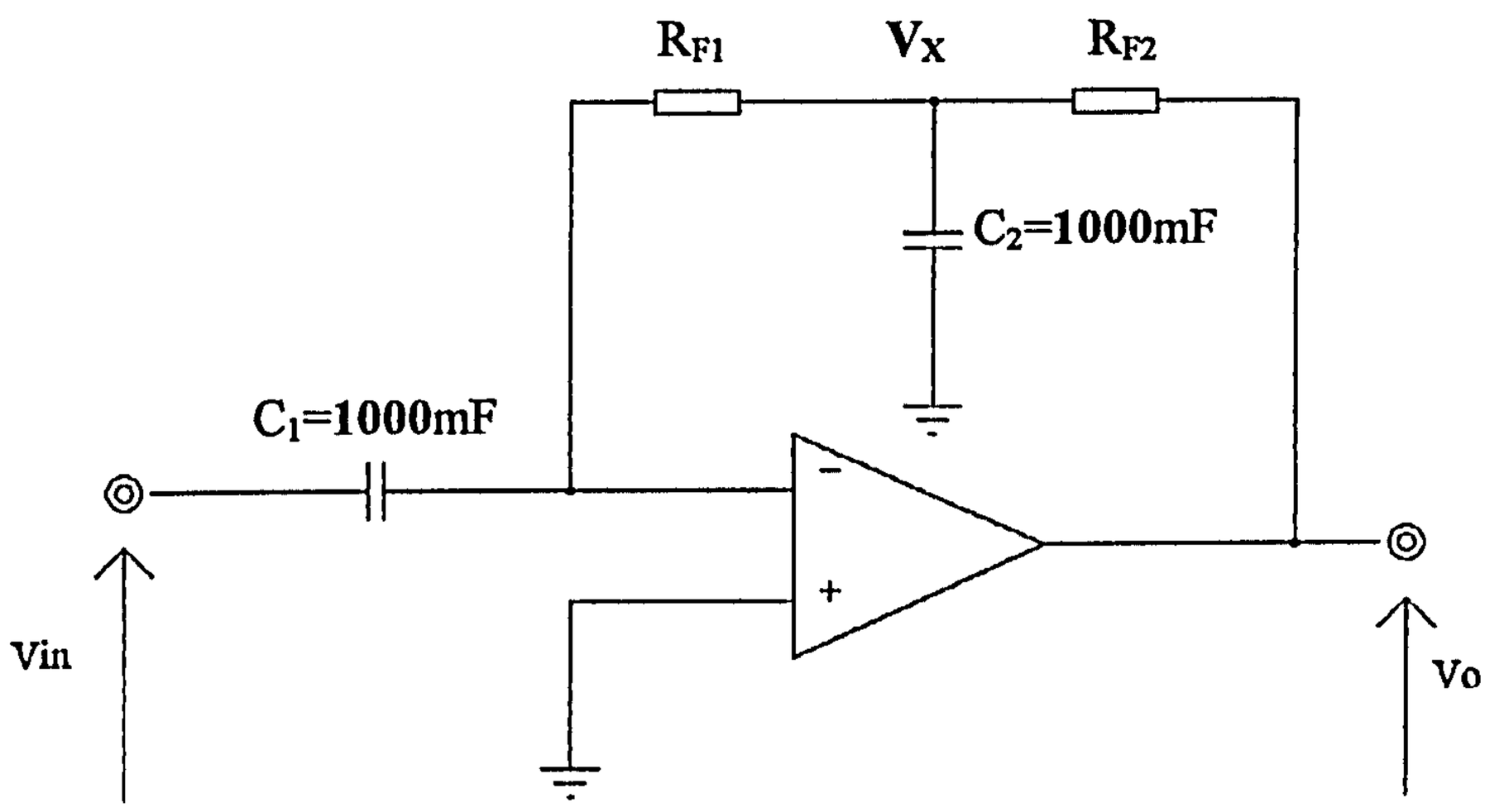


Figure A 2.1.2

In (PSPICE), (Z_1&&Z_2) ⇒Zero can be achieved at low signal frequencies if $(Z_1) = \frac{1}{j \cdot \omega \cdot C_1} \Rightarrow 0$, and ($r_{in}$⇒Zero). When ($C_1$&$C_2$) are very large ($C_1$&$C_2$=1000mF), therefore, the above equation can be reduced to:

$$\frac{V_O}{V_{in}} = -\frac{[R_{F1}]}{[\frac{R_{F1}}{A}]} = -R_{F1} \times \frac{A}{R_{F1}} = -A = A_d$$

APP 2.2 Calculation of the CMRR, ρ, (Common mode rejection ratio) in PSPICE simulation

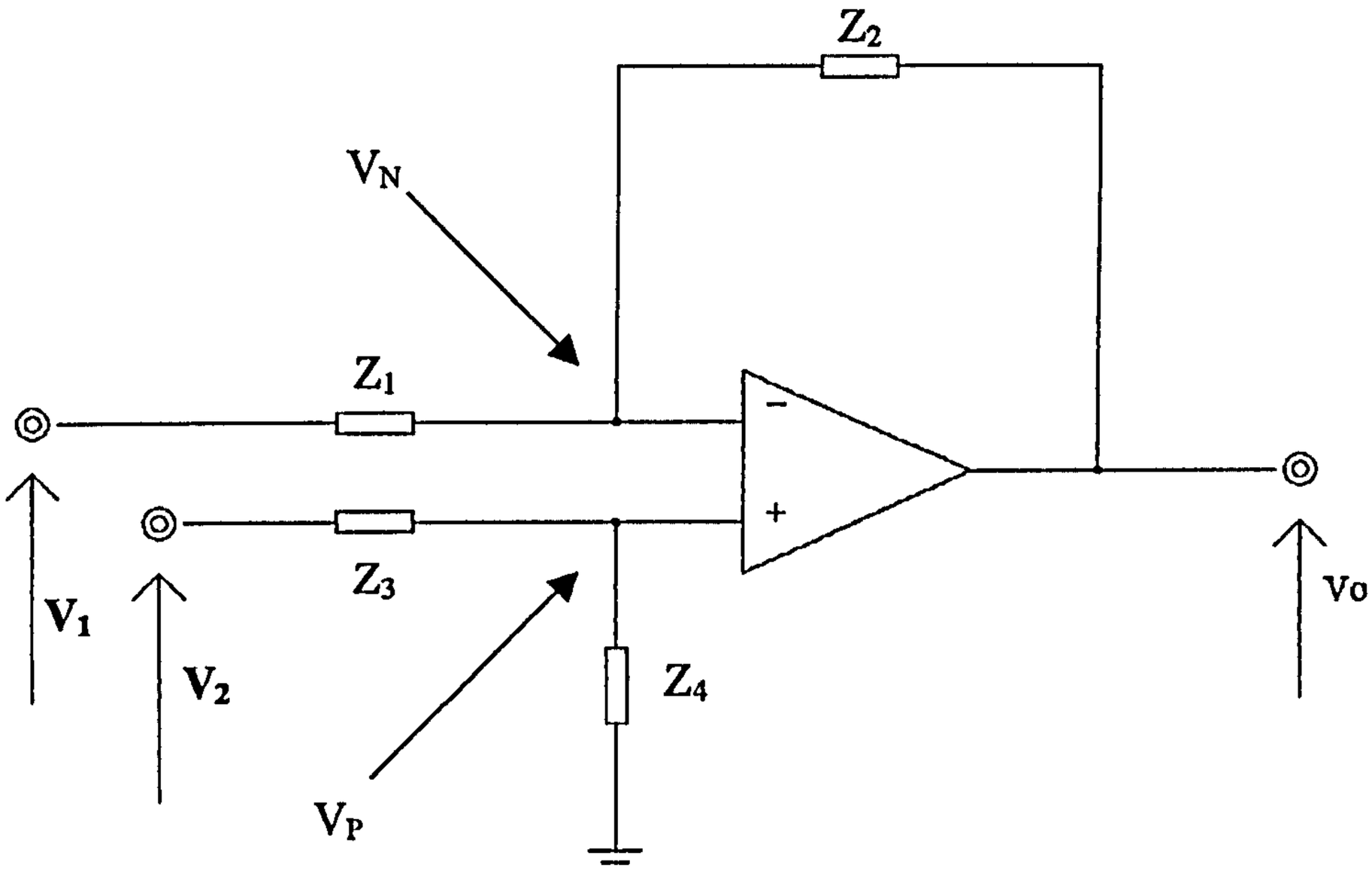


Figure A 2.2

$$V_O = A_d(V_P - V_N) + A_C\frac{(V_P + V_N)}{2}$$

$$V_P = V_2(\frac{Z_4}{Z_3 + Z_4})$$

Using the Superposition theorem

$$V_N = V_1(\frac{Z_2}{Z_1 + Z_2}) + V_O(\frac{Z_1}{Z_1 + Z_2})$$

Substitute for V_Y, and V_N

$$V_O = A_d(\frac{Z_4}{Z_3+Z_4})V_2 - A_d(\frac{Z_2}{Z_1+Z_2})V_1 - A_d(\frac{Z_1}{Z_1+Z_2})V_O + \frac{A_C}{2}(\frac{Z_4}{Z_3+Z_4})V_2 + \frac{A_C}{2}(\frac{Z_2}{Z_1+Z_2})V_1 + \frac{A_C}{2}(\frac{Z_1}{Z_1+Z_2})V_O$$

If $R_1 = Z_1 = Z_3$ && $R_2 = Z_2 = Z_4$,

$$V_O = A_d\left(\frac{R_2}{R_1+R_2}\right)(V_2-V_1) - V_O\left(\frac{R_1}{R_1+R_2}\right)\left(A_d - \frac{A_C}{2}\right) + A_C\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{V_2+V_1}{2}\right)$$

$$V_O + V_O\left(\frac{R_1}{R_1+R_2}\right)\left(A_d - \frac{A_C}{2}\right) = A_d\left(\frac{R_2}{R_1+R_2}\right)(V_2-V_1) + A_C\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{V_2+V_1}{2}\right)$$

$$V_O\left[1+\left(\frac{R_1}{R_1+R_2}\right)\left(A_d - \frac{A_C}{2}\right)\right] = A_d\left(\frac{R_2}{R_1+R_2}\right)(V_2-V_1) + A_C\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{V_2+V_1}{2}\right)$$

$$V_O\left[\left(\frac{R_1+R_2}{R_1+R_2}\right)+\left(\frac{R_1}{R_1+R_2}\right)\left(A_d - \frac{A_C}{2}\right)\right] = A_d\left(\frac{R_2}{R_1+R_2}\right)(V_2-V_1) + A_C\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{V_2+V_1}{2}\right)$$

$$V_O\left[(R_1+R_2)+(R_1\times A_d)-\left(R_1\times\frac{A_C}{2}\right)\right] = (A_d\times R_2)(V_2-V_1) + (A_C\times R_2)\left(\frac{V_2+V_1}{2}\right)$$

where $V_d=(V_2-V_1)$, and $V_C = \left(\frac{V_2+V_1}{2}\right)$

$$V_O\left[(R_1+R_2)+(R_1\times A_d)-\left(R_1\times\frac{A_C}{2}\right)\right] = (A_d\times R_2\times V_d) + (A_C\times R_2\times V_C)$$

$$V_O = \frac{(A_d\times R_2\times V_d)}{\left[(R_1+R_2)+(R_1\times A_d)-\left(R_1\times\frac{A_C}{2}\right)\right]} + \frac{(A_C\times R_2\times V_C)}{\left[(R_1+R_2)+(R_1\times A_d)-\left(R_1\times\frac{A_C}{2}\right)\right]}$$

But if V_C=Zero & $V_d \neq$ Zero

$$\frac{V_O}{V_d}\Big|V_C = \frac{\left(A_d\times\frac{R_2}{R_1}\right)}{\left[\left(\frac{R_1+R_2}{R_1}\right)+(A_d)-\left(\frac{A_C}{2}\right)\right]}$$

$$\therefore \frac{V_O}{V_d}\Big|V_C = \frac{R_2}{R_1}\left[\frac{(A_d)}{(A_d)+(\frac{R_1+R_2}{R_1})-(\frac{A_C}{2})}\right]$$

If, also, $R_1 = R_2$, then,

$$\frac{V_O}{V_d}\Big|V_C = \left[\frac{(A_d)}{(A_d)+(2)-(\frac{A_C}{2})}\right]$$

But if V_d=Zero & $V_C \neq$ Zero

$$\frac{V_O}{V_C}\Big|V_d = \frac{(A_C \times \frac{R_2}{R_1})}{[(\frac{R_1+R_2}{R_1})+(A_d)-(\frac{A_C}{2})]}$$

$$\therefore \frac{V_O}{V_C}\Big|V_d = \frac{R_2}{R_1}\left[\frac{(A_C)}{(A_d)+(\frac{R_1+R_2}{R_1})-(\frac{A_C}{2})}\right]$$

If, also, $R_1 = R_2$, then,

$$\frac{V_O}{V_C}\Big|V_d = \left[\frac{(A_C)}{(A_d)+(2)-(\frac{A_C}{2})}\right]$$

APP 2.3 Calculation of A_c (Common mode voltage gain) PSPICE simulation

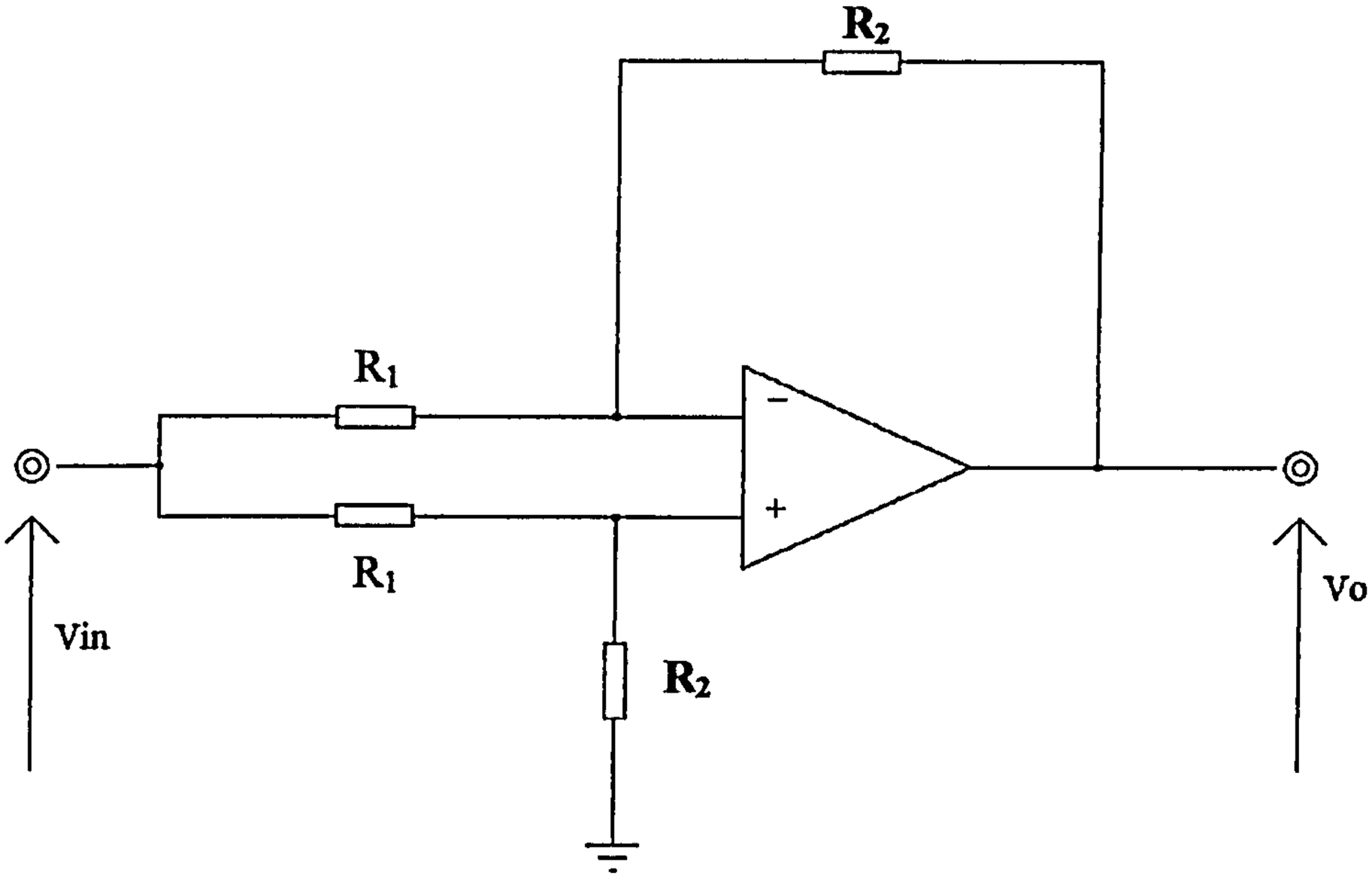


Figure A 2.3.1

Assuming (r_{in}⇒Zero), and (r_{out}⇒Zero). We also have ($R_1 = R_1$) && ($R_2 = R_2$)

$$V_O = A_d(V_P - V_N) + A_C\frac{(V_P + V_N)}{2}$$

$$V_P = V_{in}(\frac{R_2}{R_1 + R_2})$$

$$V_N = V_{in}(\frac{R_2}{R_1 + R_2}) + V_O(\frac{R_1}{R_1 + R_2})$$

Substitute for V_Y, and V_N

$$V_O = A_d(\frac{R_2}{R_1+R_2})V_{in} - A_d(\frac{R_2}{R_1+R_2})V_{in} - A_d(\frac{R_1}{R_1+R_2})V_O + \frac{A_C}{2}(\frac{R_2}{R_1+R_2})V_{in} + \frac{A_C}{2}(\frac{R_2}{R_1+R_2})V_{in} + \frac{A_C}{2}(\frac{R_1}{R_1+R_2})V_O$$

$$V_O = -(A_d \times V_O)(\frac{R_1}{R_1+R_2}) + A_C[\frac{V_{in}}{2}(\frac{R_2}{R_1+R_2}) + \frac{V_{in}}{2}(\frac{R_2}{R_1+R_2}) + \frac{V_O}{2}(\frac{R_1}{R_1+R_2})]$$

By multiplying the right and the left of the equation by (R_1+R_2)

$$V_O(R_1+R_2)=-(A_d\times V_O\times R_1)+(A_C\times V_{in}\times\frac{R_2}{2})+(A_C\times V_{in}\times\frac{R_2}{2})+(A_C\times V_O\times\frac{R_1}{2})$$

$$V_O(R_1+R_2)=-(A_d\times V_O\times R_1)+(A_C\times V_{in}\times R_2)+(A_C\times V_O\times\frac{R_1}{2})$$

$$V_O(R_1+R_2)+(A_d\times V_O\times R_1)-(A_C\times V_O\times\frac{R_1}{2})=(A_C\times V_{in}\times R_2)$$

$$V_O[(R_1+R_2)+(A_d\times R_1)-(A_C\times\frac{R_1}{2})]=(A_C\times V_{in}\times R_2)$$

$$\frac{V_O}{V_{in}}=\frac{(A_C\times R_2)}{[(R_1+R_2)+(A_d\times R_1)-(A_C\times\frac{R_1}{2})]}$$

If $R_1 = R_2$, then the above equation can be reduced to:

$$\frac{V_O}{V_{in}}=\frac{(A_C)}{[(A_d)+(2)-(\frac{A_C}{2})]}$$

But $|A_d| >> |A_C|$, therefore:

$$\frac{V_O}{V_{in}}\approx\frac{(A_C)}{(A_d)}=\frac{1}{CMRR}$$

Another way of looking at (V_O/V_{in}) in the above equation is by making $(R_1\Rightarrow$Zero). In (PSPICE), $(R_1 = Z_1 \Rightarrow$ Zero) can be achieved at low signal frequencies if $(R_1)=(Z_1)=\frac{1}{j\cdot\omega\cdot C_1}\Rightarrow 0$. When C_1 is very large (C_1 = 1000mF), the above equation can be reduced to be:

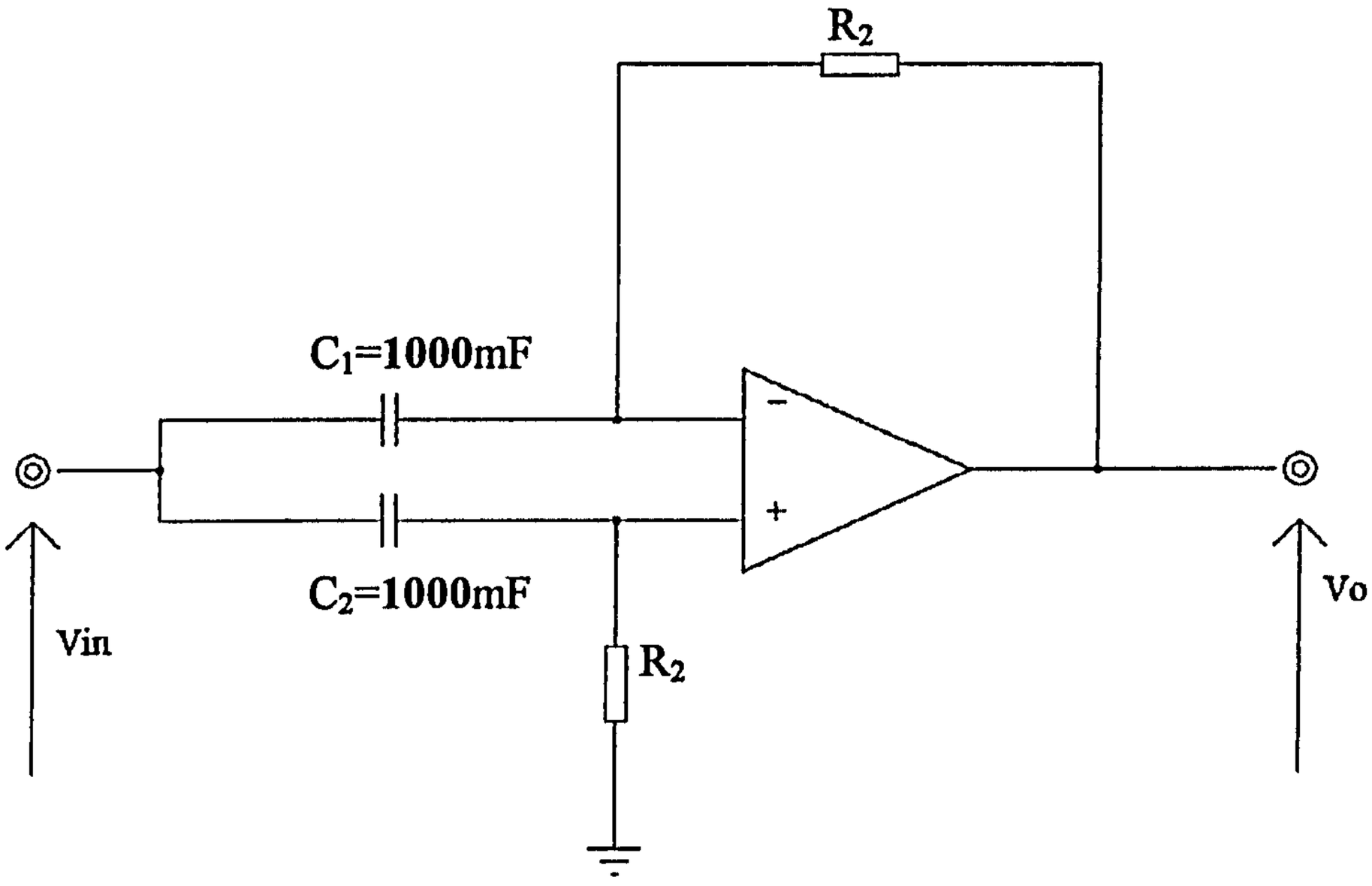


Figure A 2.3.2

$$\frac{V_O}{V_{in}}=\frac{(A_C\times R_2)}{[(0+R_2)+0-0]}=\frac{A_C\times R_2}{R_2}=A_C$$

Physical reasoning indicates that if $\frac{1}{\omega C_2}<<R_2$ and $\frac{1}{\omega C_1}<<R_2$ then the differential input voltage seen by the amplifier is V_{in}.

CHAPTER 3

Circuit Architecture Of The Basic CFOA: A Critical Review; Part I

(3.1) Introduction

With a view to establishing a base against which future improved schemes may be compared, this chapter is a study of the circuit architecture of a basic CFOA (Fig.3.1), and the ways in which this affects the terminal parameters of the amplifier. Parameter relationships that do not, as far as the author is aware, appear in the literature are derived from the first principles and examined critically.

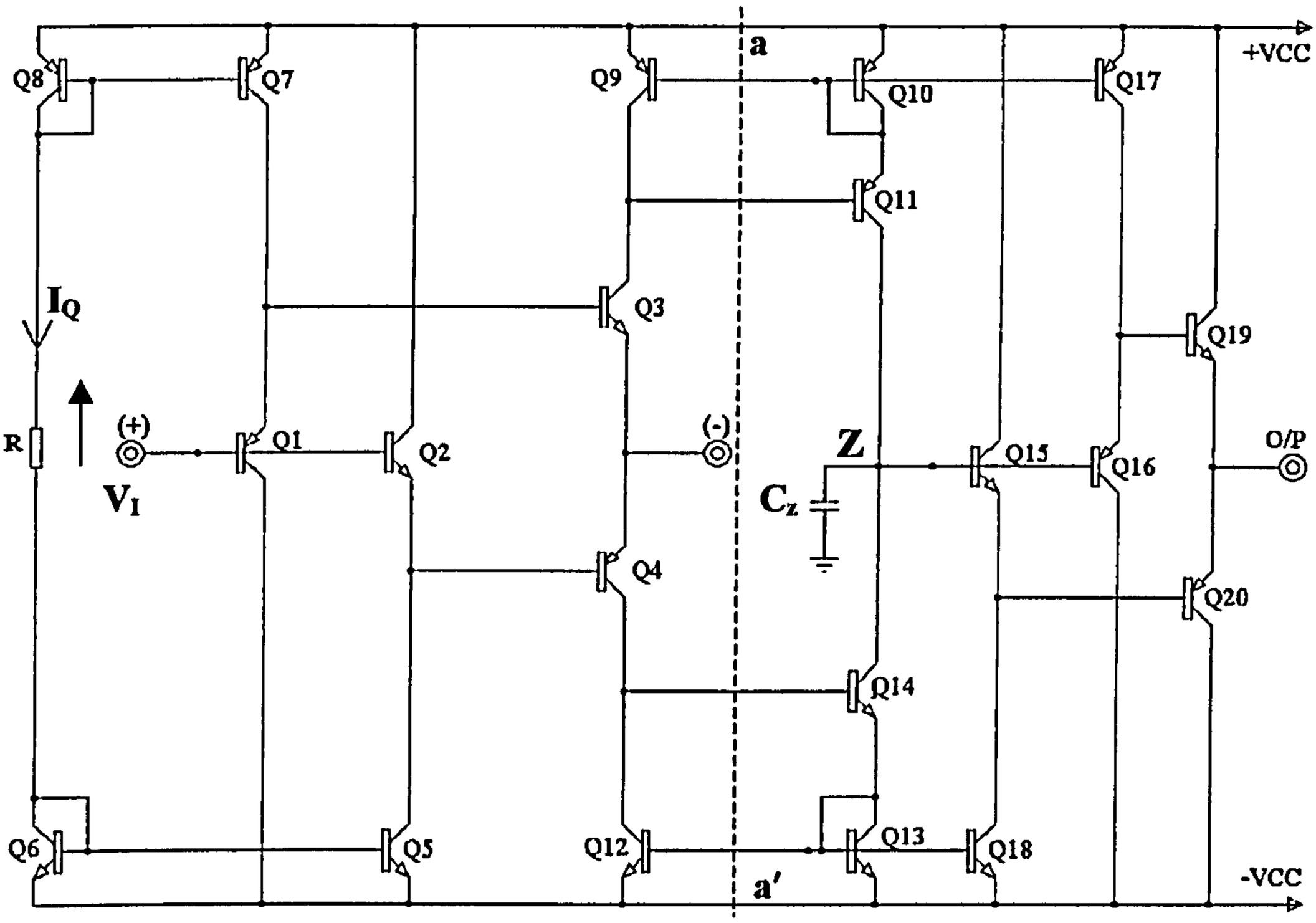


Figure 3.1 Circuit diagram of a basic CFOA

In Fig.3.1, CFOA bias current, I_Q, is set by resistor (R) and mirrored by Q_8, Q_7 to produce the emitter current of Q_1, and also mirrored by Q_6, Q_5 to produce the emitter current of Q_2.

Q_3, Q_4 fed from Q_1, Q_2 respectively, comprise a compound emitter-follower stage operating in Class AB with no crossover distortion. The collector currents of Q_3, Q_4 are mirrored by Q_9, Q_{10}, Q_{11} and Q_{12}, Q_{13}, Q_{14}, respectively, which also supply emitter

currents to Q_{15}, Q_{16} at the input to the output voltage-follower. C_z is the "compensation capacitor" chosen to set the open-loop frequency response of the CFOA: it is considered in more detail later (Chapter Four). The compound emitter-follower Q_{19}, Q_{20}, like Q_3, Q_4, operates in the Class AB mode.

(3.2) D.C. input current, I_{in}, and linear voltage range

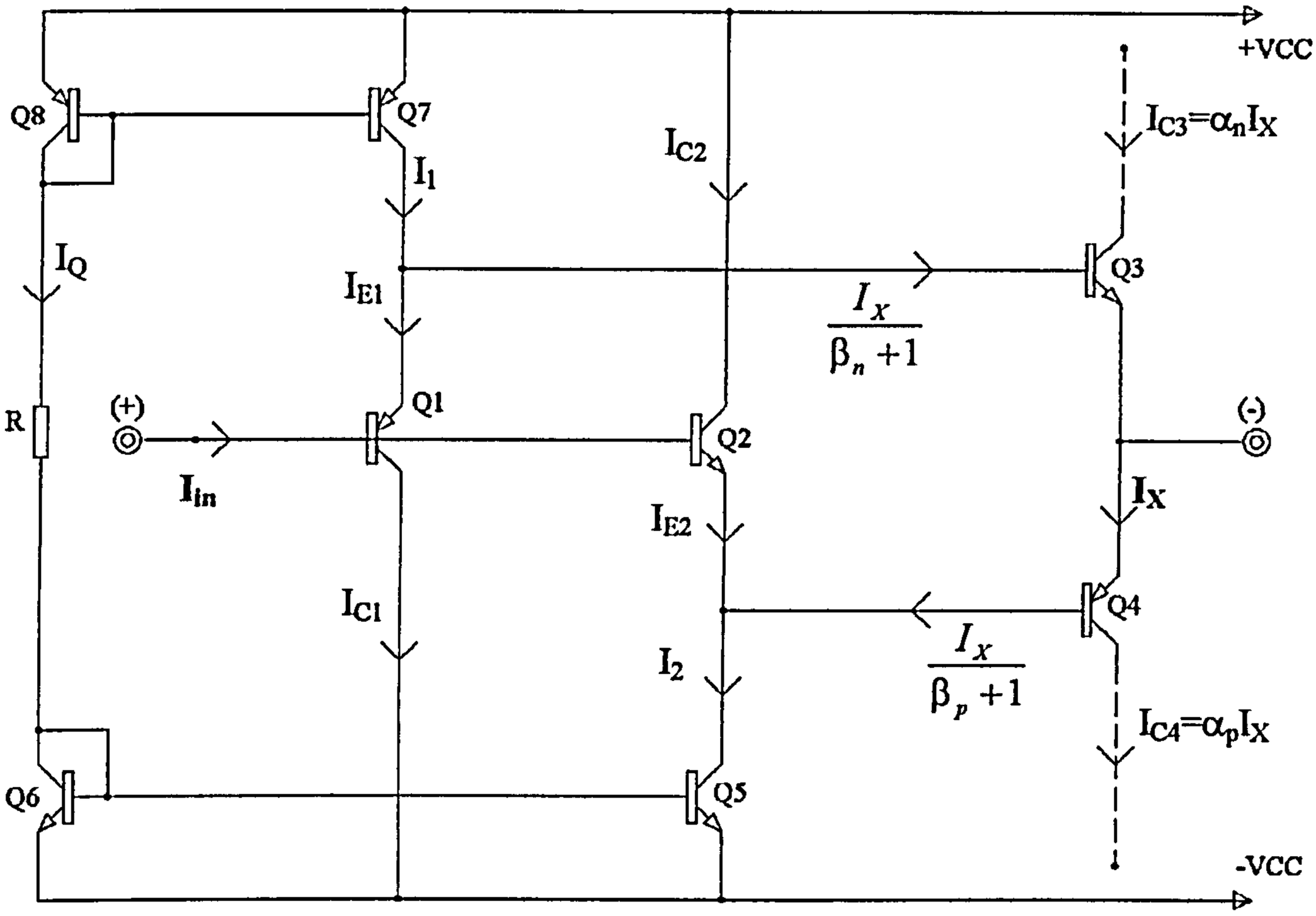


Figure 3.2 D.C. currents in the CFOA input stage

The following parameter, which refer to Fig.3.2, are defined as follows:

α_n = d.c., c.b., current gain of the NPN transistors

β_n = d.c., c.e., current gain of the NPN transistors

α_P = d.c., c.b., current gain of the PNP transistors

β_P = d.c., c.e., current gain of the PNP transistors

It is assumed that the current flowing in, or out, of the inverting input terminal is zero. Then the emitter currents of Q_3 and Q_4 are equal, to I_X, say.

$$I_{E1} = I_1 - \frac{I_X}{\beta_n + 1} \quad : \quad I_{E2} = I_2 - \frac{I_X}{\beta_P + 1} \tag{3.1}$$

$$I_{C1} = \alpha_P (I_1 - \frac{I_X}{\beta_n + 1}) \quad ; \quad I_{C2} = \alpha_n (I_2 - \frac{I_X}{\beta_P + 1}) \tag{3.2}$$

Because (V_{EB1}+V_{BE2}) = (V_{BE3}+ V_{EB4}) it follows that,

$$V_T \log_e(\frac{I_{C1}}{I_{S1}} \cdot \frac{I_{C2}}{I_{S2}}) = V_T \log_e(\frac{I_{C3}}{I_{S3}} \cdot \frac{I_{C4}}{I_{S4}}) \tag{3.3}$$

Providing that transistors Q_1, Q_2, Q_3, and Q_4 are well-matched,

$I_{C1}I_{C2}=I_{C3}I_{C4}$

Substituting for I_{C1}, etc, from (3.1), (3.2),

$$\alpha_P(I_1 - \frac{I_X}{\beta_n + 1}) \cdot \alpha_n(I_2 - \frac{I_X}{\beta_P + 1}) = (\alpha_n \cdot I_X)(\alpha_P \cdot I_X) \tag{3.4}$$

$$\therefore (I_1 - \frac{I_X}{\beta_n + 1}) \cdot (I_2 - \frac{I_X}{\beta_P + 1}) = I_X{}^2 \tag{3.5}$$

$$\therefore I_1 I_2 - I_X(\frac{I_2}{\beta_n + 1} + \frac{I_1}{\beta_P + 1}) + \frac{I_X{}^2}{(\beta_n + 1) \cdot (\beta_P + 1)} = I_X{}^2 \tag{3.6}$$

$$\therefore I_X{}^2[1 - \frac{1}{(\beta_n + 1) \cdot (\beta_P + 1)}] + I_X(\frac{I_2}{\beta_n + 1} + \frac{I_1}{\beta_P + 1}) - I_1 I_2 = 0 \tag{3.7}$$

The solution to this quadratic equation is,

$$I_X \approx \frac{-(\frac{I_2}{\beta_n + 1} + \frac{I_1}{\beta_P + 1}) \pm \sqrt{(\frac{I_2}{\beta_n + 1} + \frac{I_1}{\beta_P + 1})^2 + 4I_1 I_2}}{2[1 - \frac{1}{(\beta_n + 1) \cdot (\beta_P + 1)}]} \tag{3.8}$$

For β_n, $\beta_P >> 1$,

$$I_X \approx \pm\sqrt{I_1 I_2} - \frac{1}{2} \cdot (\frac{I_2}{\beta_n + 1} + \frac{I_1}{\beta_P + 1}) \tag{3.9}$$

Now I_X must flow in the direction shown if Fig.3.2. Hence, we must take the positive root of the square root expression

$$I_{E1} = (I_1 - \frac{I_X}{\beta_n + 1}) \approx I_1 - \frac{\sqrt{I_1 I_2}}{\beta_n + 1} + \frac{1}{2(\beta_n + 1)}(\frac{I_2}{(\beta_n + 1)} + \frac{I_1}{(\beta_p + 1)}) \tag{3.10}$$

$$I_{E2} = (I_2 - \frac{I_X}{\beta_P + 1}) \approx I_2 - \frac{\sqrt{I_1 I_2}}{\beta_P + 1} + \frac{1}{2(\beta_P + 1)}(\frac{I_2}{(\beta_n + 1)} + \frac{I_1}{(\beta_p + 1)}) \tag{3.11}$$

From I_{E1}, and I_{E2}, I_{B1} and I_{B2} can be calculated:

$$I_{B1} = \frac{I_{E1}}{(\beta_p + 1)} \approx \frac{I_1}{(\beta_p + 1)} - \frac{\sqrt{I_1 I_2}}{(\beta_p + 1)\cdot(\beta_n + 1)} + \frac{1}{2(\beta_n + 1)\cdot(\beta_p + 1)}\left[\frac{I_2}{(\beta_n + 1)} + \frac{I_1}{(\beta_p + 1)}\right] \qquad (3.12)$$

$$I_{B2} = \frac{I_{E2}}{(\beta_n + 1)} \approx \frac{I_2}{(\beta_n + 1)} - \frac{\sqrt{I_1 I_2}}{(\beta_P + 1)\cdot(\beta_n + 1)} + \frac{1}{2(\beta_P + 1)\cdot(\beta_n + 1)}\left[\frac{I_2}{(\beta_n + 1)} + \frac{I_1}{(\beta_p + 1)}\right] \qquad (3.13)$$

Finally,

$$I_{in} = (I_{B2} - I_{B1}) \approx \left[\frac{I_2}{(\beta_n + 1)} - \frac{I_1}{(\beta_p + 1)}\right] \qquad (3.14a)$$

Or, since β_n, $\beta_p >> 1$,

$$I_{in} \approx \left[\frac{I_2}{\beta_n} - \frac{I_1}{\beta_p}\right] \qquad (3.14b)$$

Before proceeding further, a note is appropriate concerning the equality of the emitter currents of Q_3, Q_4. These are both shown as I_X; it is assumed that the current flowing in the inverting input terminal is zero. In practice this is not quite true.

However, when the amplifier is used in closed-loop operation, as is normally the case, the negative feedback action ensures that this current is much smaller than I_Q under d.c. conditions. Hence there remains only a small inequality in the emitter currents of Q_3 and Q_4, and their base currents only appear as a very small correction term in the expression for I_{in} as is apparent in the equations above.

Referring, again, to (3.14b) assume I_1 and I_2 are close and that β_p and β_n are close, the variational approach can be used:

$$I_1 = I + \frac{\Delta I}{2} \quad ; \qquad I_2 = I - \frac{\Delta I}{2} \qquad (3.15)$$

$$\text{and, } \beta_P = \beta + \frac{\Delta\beta}{2} \quad ; \qquad \beta_N = \beta - \frac{\Delta\beta}{2} \qquad (3.16)$$

where I and β are average values: then (3.14b) gives,

$$I_{in} \approx \frac{I-\frac{\Delta I}{2}}{\beta-\frac{\Delta\beta}{2}} - \frac{I+\frac{\Delta I}{2}}{\beta+\frac{\Delta\beta}{2}} \tag{3.17}$$

But, the signs of ΔI, Δβ are unrelated so (3.21) must be corrected to read:

$$I_{in} \approx \pm(\frac{\Delta I}{\beta}) \pm \frac{I}{\beta}(\frac{\Delta\beta}{\beta})$$

Clearly, I_{in} may be positive or negative.

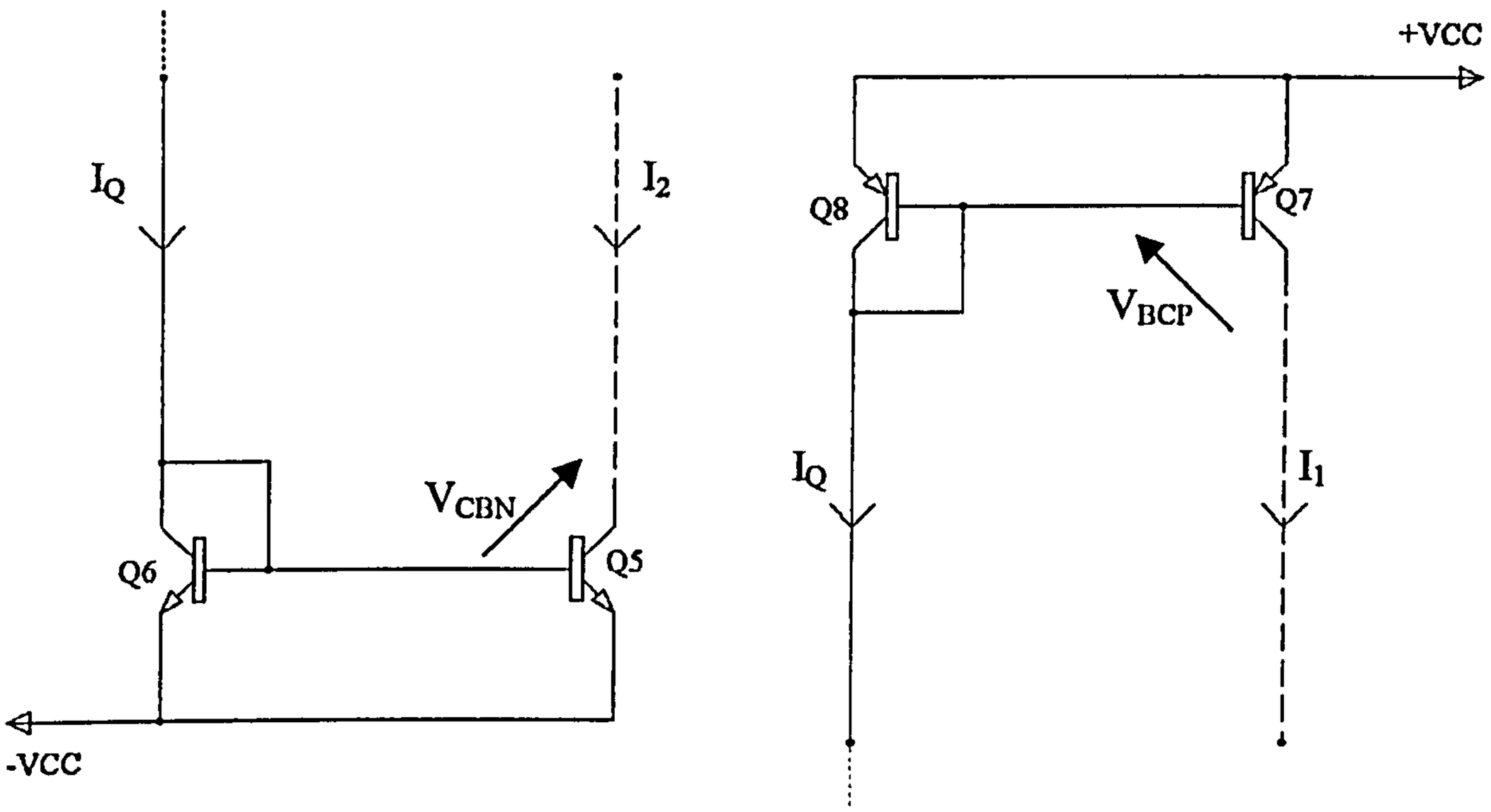


Figure 3.3 D.C. current analysis of the NPN, and PNP, simple current mirrors

For the case in which I_1 and I_2 (and β_p, β_n) are not close (3.14b) must be used.

To find the dependence of I_{in} on V_I the input current mirrors comprising Q_5, Q_6 and Q_7, Q_8, we can proceed as follows.

It is shown in Appendix 3.1 that,

$$I_1 = I_Q[1 - \frac{2}{\beta_{po}} \pm \frac{V_{OSP}}{V_T} + \frac{V_{BCP}}{V_{AP}}] \tag{3.19}$$

$$I_2 = I_Q[1 - \frac{2}{\beta_{no}} \pm \frac{V_{OSN}}{V_T} + \frac{V_{CBN}}{V_{AN}}] \tag{3.20}$$

where: β_{po}, β_{no} refer to the value of β_p, β_n and at zero collector-base voltage;
V_{AN}, and V_{AP} are the Early voltages for the NPN and the PNP transistors respectively; V_{OSN}, and V_{OSP} are the offset voltages of the NPN mirror, and the PNP mirror, respectively, which arise through mirror emitter-area mismatches in the device pair. In simulation, it is assumed that V_{OSN}, and V_{OSP} are zero, but this is not generally the case with practical devices.

Substituting for the component I_2/β_n, of I_{in}, the expression in (3.14b) and taking into account the variation with V_{CB} (=V_{CC}-V_I) of β_n,

$$\frac{I_2}{\beta_n} \approx \frac{I_Q[1 - \frac{2}{\beta_{no}} + \frac{(V_I + V_{CC})}{V_{AN}}]}{\beta_{no}[1 + \frac{(V_{CC} - V_I)}{V_{AN}}]} \tag{3.21}$$

(I_2/β_n) increases with V_I because I_2 increases and β_n decreases. Using the binominal expansion and making reasonable assumptions [1>>(V_{CC}+V_I)/V_{AN}], equation (3.21) reduces to,

$$\frac{I_2}{\beta_n} \approx \frac{I_Q}{\beta_{no}}[1 - \frac{2}{\beta_{no}} + \frac{2V_I}{V_{AN}}] \tag{3.22}$$

Similarly,

$$\frac{I_1}{\beta_p} \approx \frac{I_Q[1 - \frac{2}{\beta_{po}} + \frac{(V_{CC} - V_I)}{V_{AP}}]}{\beta_{po}[1 + \frac{(V_I + V_{CC})}{V_{AP}}]} \tag{3.23}$$

Hence $\frac{I_1}{\beta_p} \approx \frac{I_Q}{\beta_{po}}[1-\frac{2}{\beta_{po}}-\frac{2V_I}{V_{AP}}]$ (3.24)

and,

$$I_{in} \approx I_Q[\frac{1}{\beta_{no}}(1-\frac{2}{\beta_{no}})-\frac{1}{\beta_{po}}(1-\frac{2}{\beta_{po}})+2I_QV_I[\frac{1}{\beta_{no}V_{AN}}+\frac{1}{\beta_{po}V_{AP}}] \quad (3.25)$$

Clearly, if $\beta_{no}= \beta_{po}$ and $V_{AN}=V_{AP}$ then $I_{in}=0$ when $V_I=0$. Because these conditions do not hold exactly, in practice, $I_{in}\neq 0$ when $V_I=0$ but is, nevertheless, expected to be very small and proportional to I_Q. Furthermore I_{in} increases with V_I.

Consider now the input voltage range for linear operation of the CFOA as a whole. Referring to Fig.3.1, Q_4 operates out of saturation if,

$$V_I > [-V_{CC}+(V_{BE} \text{ of } Q_2)+ (V_{BE} \text{ of } Q_{13})+(V_{BE} \text{ of } Q_{14})] \quad (3.26)$$

$$\text{i.e., } V_I > [-V_{CC}+ (3V_{BE})] \quad (3.27)$$

Similarly Q3 operates out of saturation if,

$$V_I < [V_{CC}- (3V_{EB})] \quad (3.28)$$

Hence the linear input voltage range for V_I is defined by,

$$[V_{CC}- (3V_{EB})] > V_I > [-V_{CC}+ (3V_{BE})] \quad (3.29)$$

where V_{EB}, V_{BE} are, respectively, the emitter base and base-emitter voltage of a PNP and NPN transistor operating at a collector current I_Q.

Assuming $V_{BE} \approx V_{EB} \approx 0.8V$, equation (3.29) implies that ($2.6V > V_I > -2.6V$). The sweep of I_B(Y) versus V_I(X), shown in Fig.3.4, and Fig.3.5, bears out the theoretical predictions for I_{in} and the input voltage range for linear operation.

I_{in} at $V_I=0$ can be positive or negative but for the particular parameter values, here, I_{in} has a small negative value which is higher in magnitude for $I_Q=0.7mA$ than for $I_Q=0.1mA$ for ($3.5V > V_I > -3.5V$), I_B varies approximately linearly with V_I as predicted by equation (3.25) because of the non-infinite Early voltages of the transistors. The magnitude of $|I_B|$ increases rapidly for $V_I < -3.5V$ and $V_I > 3.5V$ because of the onset of transistor saturation.

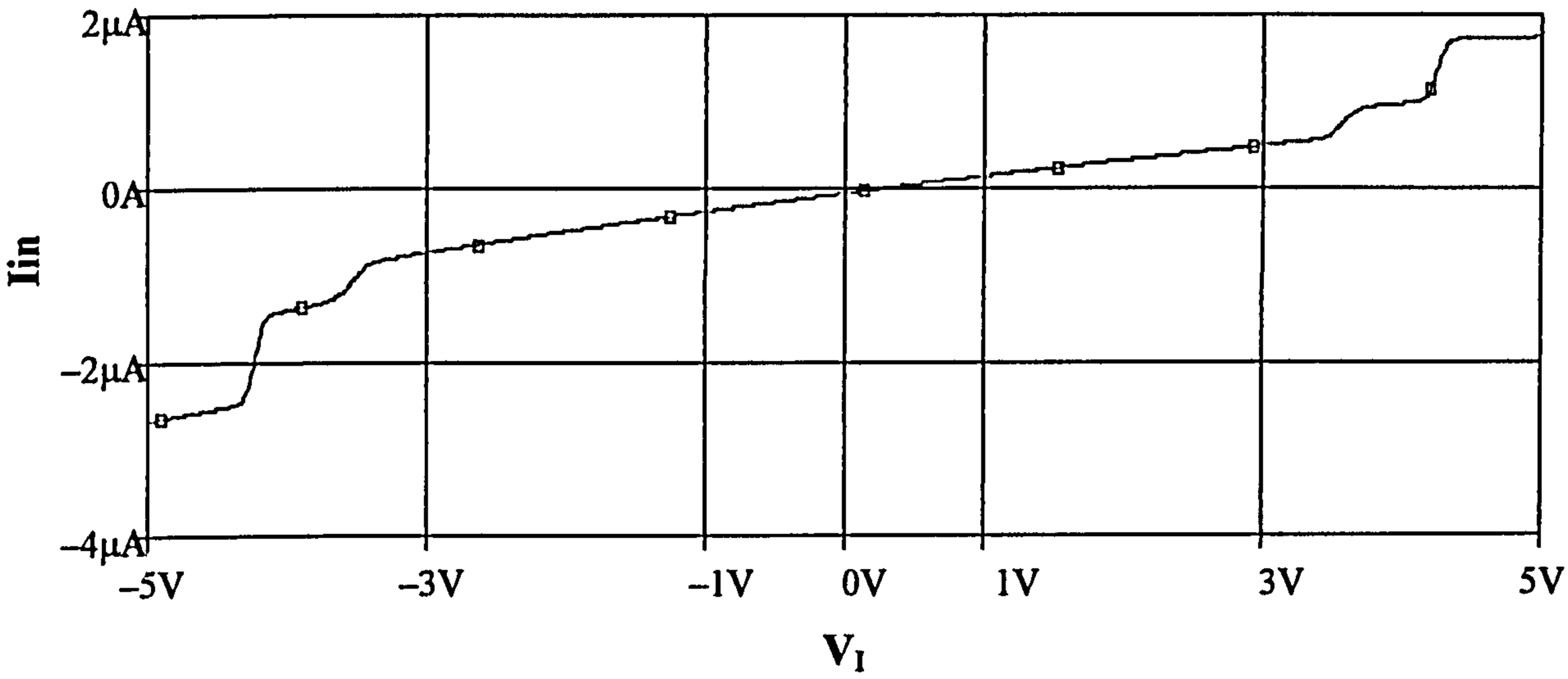


Figure 3.4 A plot of I_{in} versus V_I over the input range +5V, and –5V at a bias current of $I_Q=0.1mA$

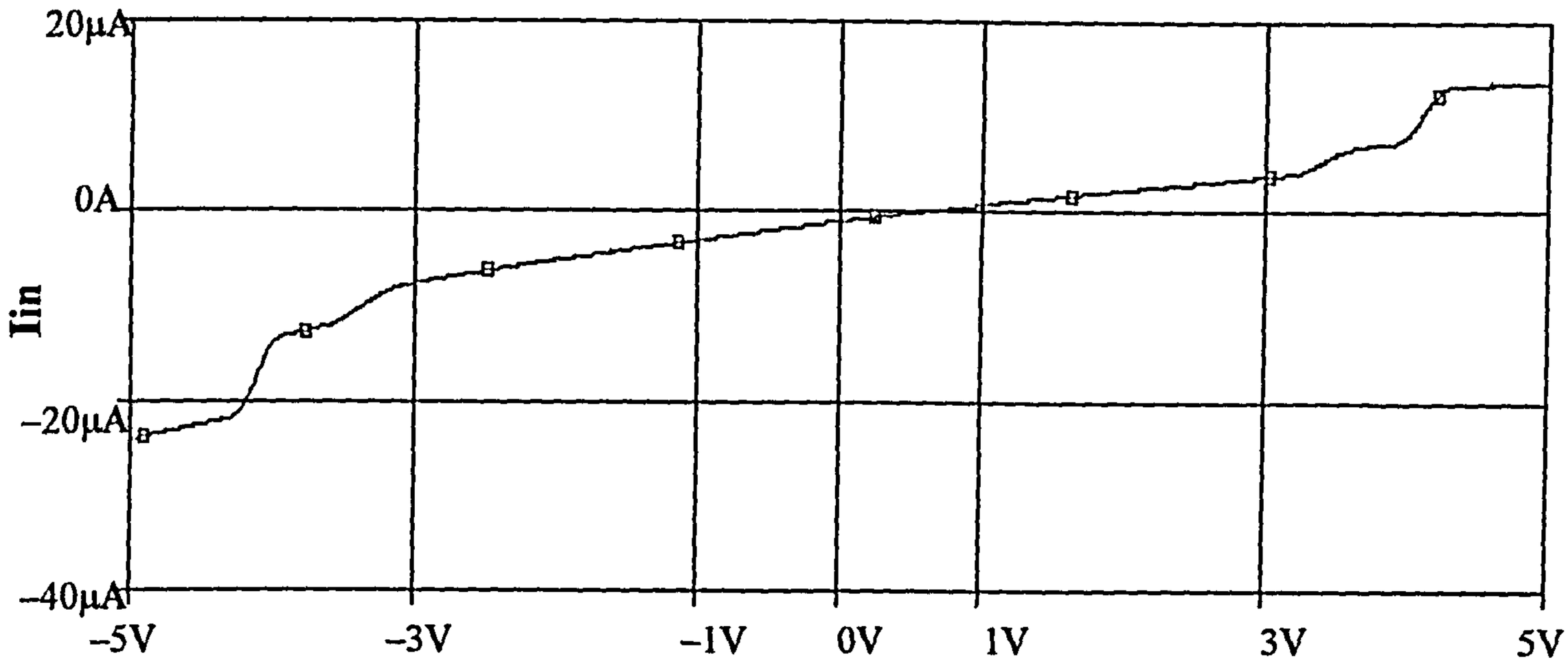


Figure 3.5 A plot of I_{in} versus V_I over the input range +5V, and –5V at a bias current of I_Q=0.7mA

(3.3) Input Offset voltage (V_{OS})

The input stage is redrawn in Fig.3.6. The input offset voltage, V_{OS}, is the differential CFOA input voltage required to make V_o=0, when V_I = 0. It will be seen that the offset voltage due to voltage-follower output stage can neglected.

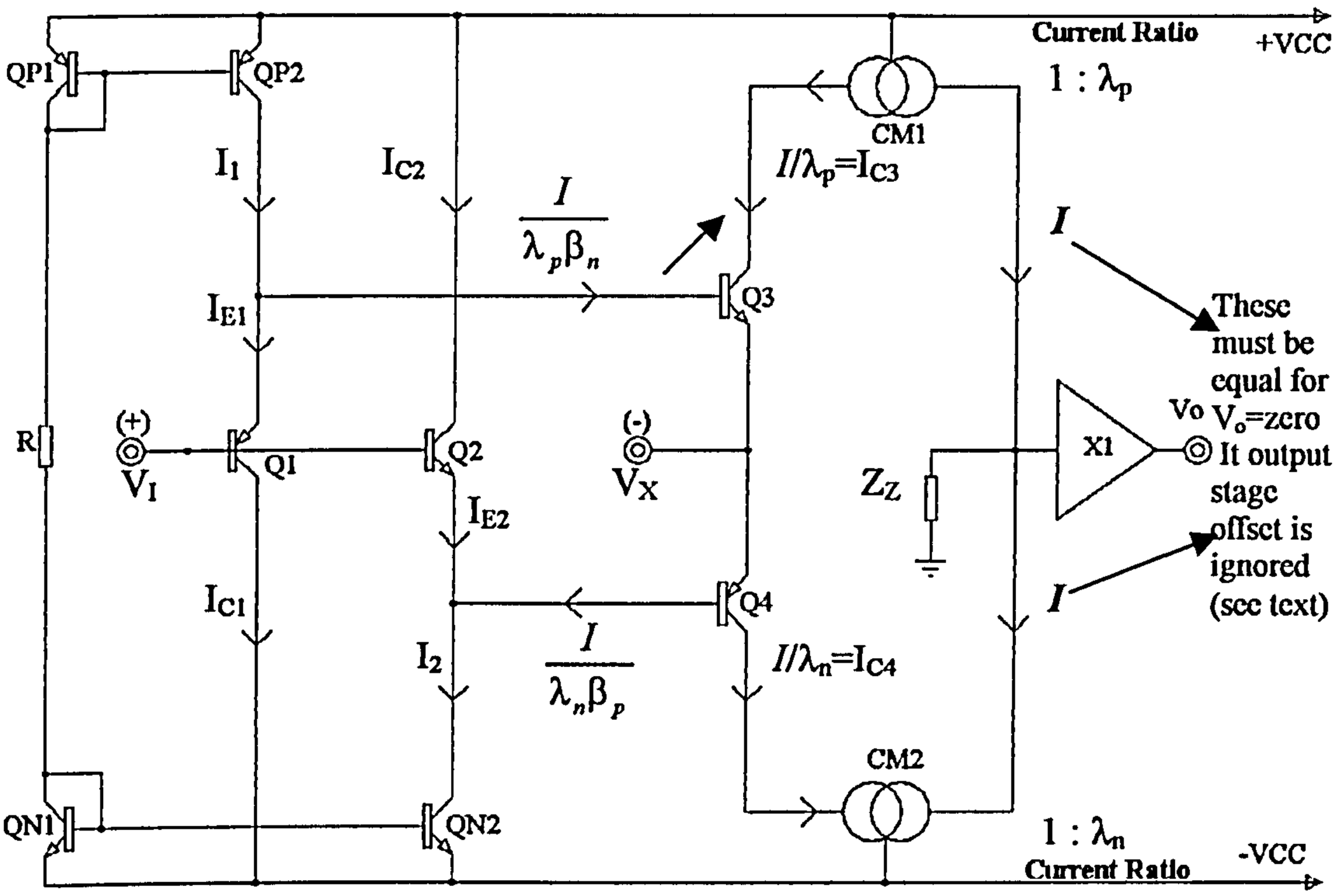


Figure 3.6 showing currents used in the calculation of V_{OS}.

By inspection, $I_{E1} = (I_1 - \frac{I}{\lambda_p \beta_n})$: $\quad \therefore I_{C1} = \alpha_p (I_1 - \frac{I}{\lambda_p \beta_n})$ (3.30)

Similarly $I_{E2} = (I_2 - \frac{I}{\lambda_n \beta_p})$: $\quad \therefore I_{C2} = \alpha_n (I_2 - \frac{I}{\lambda_n \beta_p})$ (3.31)

Now, $(V_{EB1}+V_{BE2}) = (V_{BE3}+V_{EB4})$,

Hence, $\frac{I_{C1} \cdot I_{C2}}{I_{S1} \cdot I_{S2}} = \frac{I_{C3} \cdot I_{C4}}{I_{S3} \cdot I_{S4}}$ (3.32)

Substituting for I_{C1}, I_{C2}, I_{C3}, and I_{C4},

$$\frac{\alpha_p(I_1-\frac{I}{\lambda_p\beta_n})\cdot\alpha_n(I_2-\frac{I}{\lambda_n\beta_p})}{I_{S1}\cdot I_{S2}}=\frac{I^2}{\lambda_p\cdot\lambda_n\cdot I_{S3}\cdot I_{S4}} \tag{3.33}$$

$$\therefore \frac{I^2}{\lambda_p\cdot\lambda_n}\cdot(\frac{I_{S1}I_{S2}}{I_{S3}I_{S4}})\cdot\frac{1}{\alpha_p\cdot\alpha_n}=I_1I_2-I(\frac{I_2}{\lambda_p\beta_n}+\frac{I_1}{\lambda_n\beta_p})+\frac{I^2}{\lambda_p\cdot\lambda_n\cdot\beta_p\cdot\beta_n} \tag{3.34}$$

$$\therefore \frac{I^2}{\lambda_p\cdot\lambda_n}[(\frac{I_{S1}I_{S2}}{I_{S3}I_{S4}})\cdot\frac{1}{\alpha_p\cdot\alpha_n}-(\frac{1}{\beta_p\cdot\beta_n})]+I(\frac{I_2}{\lambda_p\beta_n}+\frac{I_1}{\lambda_n\beta_p})-I_1I_2=0 \tag{3.35}$$

This is an exact expression from which (I) can be found if numerical data for other parameters is supplied. However, it gives tedious algebra, which tends to obscure physical understanding, so we proceed as follows:

Since ($\beta<<1$), all terms involving ($1/\beta$), etc, can be ignored in an approximate analysis.

Then, $$I\approx\sqrt{I_1\cdot I_2\cdot\lambda_p\cdot\lambda_n\cdot\alpha_p\cdot\alpha_n(\frac{I_{S3}I_{S4}}{I_{S1}I_{S2}})} \tag{3.36}$$

Therefore, $$I_{C3}\approx\frac{I}{\lambda_p}=\sqrt{I_1\cdot I_2\cdot\alpha_p\cdot\alpha_n(\frac{I_{S3}I_{S4}}{I_{S1}I_{S2}})(\frac{\lambda_n}{\lambda_p})} \tag{3.37}$$

But, $$I_{C3}=I_{S3}[e^{\frac{V_{BE3}}{V_T}}] \tag{3.38}$$

Hence, $$V_{BE3}=V_T\log_e\frac{I_{C3}}{I_{S3}} \tag{3.39}$$

$$\text{Or, } V_{BE3} = V_T \log_e \left[\frac{\sqrt{I_1 \cdot I_2 \cdot \alpha_p \cdot \alpha_n \cdot \left(\frac{\lambda_n}{\lambda_p}\right)\left(\frac{I_{S3} I_{S4}}{I_{S1} I_{S2}}\right)}}{I_{S3}} \right] \tag{3.40}$$

$$\text{Now, } V_{EB1} = V_T \log_e \frac{I_{C1}}{I_{S1}} \approx V_T \log_e \frac{\alpha_p \cdot I_1}{I_{S1}}$$

$$V_{OS} = V_{EB1} - V_{BE3} = V_T \log_e \frac{\alpha_p \cdot I_1}{I_{S1}} - V_T \log_e \frac{\sqrt{I_1 \cdot I_2 \cdot \alpha_p \cdot \alpha_n \left(\frac{\lambda_n}{\lambda_p}\right)\left(\frac{I_{S3} I_{S4}}{I_{S1} I_{S2}}\right)}}{I_{S3}} \tag{3.41}$$

$$V_{OS} = V_T \log_e \frac{\alpha_p \cdot I_1}{I_{S1}} \cdot \frac{I_{S3}}{\sqrt{I_1 \cdot I_2 \cdot \alpha_p \cdot \alpha_n \left(\frac{\lambda_n}{\lambda_p}\right)\left(\frac{I_{S3} I_{S4}}{I_{S1} I_{S2}}\right)}} \tag{3.42}$$

$$V_{OS} = V_T \log_e \left(\frac{I_{S3}}{I_{S1}}\right) + V_T \log_e \sqrt{\left(\frac{I_1}{I_2}\right)\left(\frac{\alpha_p}{\alpha_n}\right)\left(\frac{\lambda_p}{\lambda_n}\right)\left(\frac{I_{S1} I_{S2}}{I_{S3} I_{S4}}\right)} \tag{3.43}$$

There are thus two terms that contribute to V_{OS}.

1. $V_T \log_e \left(\frac{I_{S3}}{I_{S1}}\right)$ (Inherent offset due to the mismatch in I_S of Q_1 and Q_3)

2. $V_T \log_e \sqrt{\left(\frac{I_1}{I_2}\right)\left(\frac{\alpha_p}{\alpha_n}\right)\left(\frac{\lambda_p}{\lambda_n}\right)\left(\frac{I_{S1}}{I_{S4}}\right)\left(\frac{I_{S2}}{I_{S3}}\right)}$ (Similar parameter mismatches, shown in Table 3.1)

Mismatch pairings				
I_1, I_2	α of Q_1, Q_3	λ (current- mirror transfer coefficient) of CM1 and CM2	I_S of Q_1, Q_4	I_S of Q_2, Q_3

Table 3.1

In normal PSPICE simulator tests the condition $I_{S1}=I_{S4}$, $I_{S2}=I_{S3}$ holds true, and hence the second component of V_{OS} can be reduced to $V_T \log_e \sqrt{(\frac{I_1}{I_2})(\frac{\alpha_p}{\alpha_n})(\frac{\lambda_p}{\lambda_n})}$.

The same result for V_{OS} is obtained if we consider it to be (V_{EB4}- V_{BE2}) as, of course, it must because the offset voltage can only have a value whichever way it is calculated. In equation (3.43) the bracketed terms relate to mismatches in current or parameters that are, ideally, equal. Note that α_p, α_n,λ_p, λ_n, are dependent on the collector-base voltage of Q_1, Q_2, Q_3, Q_4, respectively, so V_{OS} is dependent on V_I. So far, we have neglected the offset of the voltage-follower output stage inducted by the triangle symbol in Fig.3.6 let this be V_{OSO}. This requires a difference between I_{C3} and I_{C4} of V_{OSO}/R_Z. Since the transconductance of the first stage is almost equal to $2g_m$ (see section 3.6).

this means an additional input-referred offset of $V_{OSO}/(2g_mR_Z)$. But $g_m \approx I/V_T$

Thus,

$$V_{OS} \approx V_T(V_{OSO}/2I \times R_Z) \qquad (3.44)$$

But, since $I \times R_Z >> V_T$, in any meaningful design, the input-referred offset is in the range of μV to nV, even if V_{OSO}=several mV, compared with the Vos given by equation (3.43).

(3.4) Quiescent power dissipation

The quiescent power dissipation for any amplifier circuit is a characteristic, which designers usually try to minimize. It is apparent from Fig.3.1 that there are eight conduction paths, from $+V_{CC}$ power supply to the $-V_{CC}$ power supply, each passing a quiescent current I_Q, defined by R, $+V_{CC}$, $-V_{CC}$.

The quiescent power dissipation P_Q is this given by

$$P_Q = 2V_{CC} \times 8I_Q = 16V_{CC}I_Q \tag{3.45}$$

where,

$$I_Q = (\frac{2V_{CC} - 2|V_{BE}|}{R}) \tag{3.46}$$

Alternatively, we can write,

$$P_Q = 16V_{CC}(\frac{2V_{CC} - 2V_D}{R}) \tag{3.47}$$

For I_Q=100μA, V_{CC}=5V

$P_Q \approx 8mW$

(3.5) Incremental input/output impedance

(3.5.1) Incremental input resistance

The incremental input resistance, R_i, can be derived from equation (3.25). Differentiating with respect to V_I,

$$\frac{1}{R_i} = \frac{dI_{in}}{dV_I} \approx 2I_Q\left[\frac{1}{\beta_{no}V_{AN}} + \frac{1}{\beta_{po}V_{AP}}\right] \tag{3.48}$$

This takes account of the variation of β_n, β_p in Q_1, and Q_2, with V_I, and the change in their collector-base voltages. However, we must include the collector-base resistances $r_{\mu 1}$, $r_{\mu 2}$ of Q_1, and Q_2.

Then, for the linear input voltage range,

$$\frac{1}{R_i} = \frac{1}{r_{\mu 1}} + \frac{1}{r_{\mu 2}} + 2I_Q\left[\frac{1}{\beta_{no}V_{AN}} + \frac{1}{\beta_{po}V_{AP}}\right] \tag{3.49}$$

For a given I_Q, R_i is sensibly constant for the voltage range specified by equation (3.29), as is evident from the straight-line relationship between I_{in} and V_I over this range in Fig.3.4 and Fig.3.5.

(3.5.2) Input capacitance

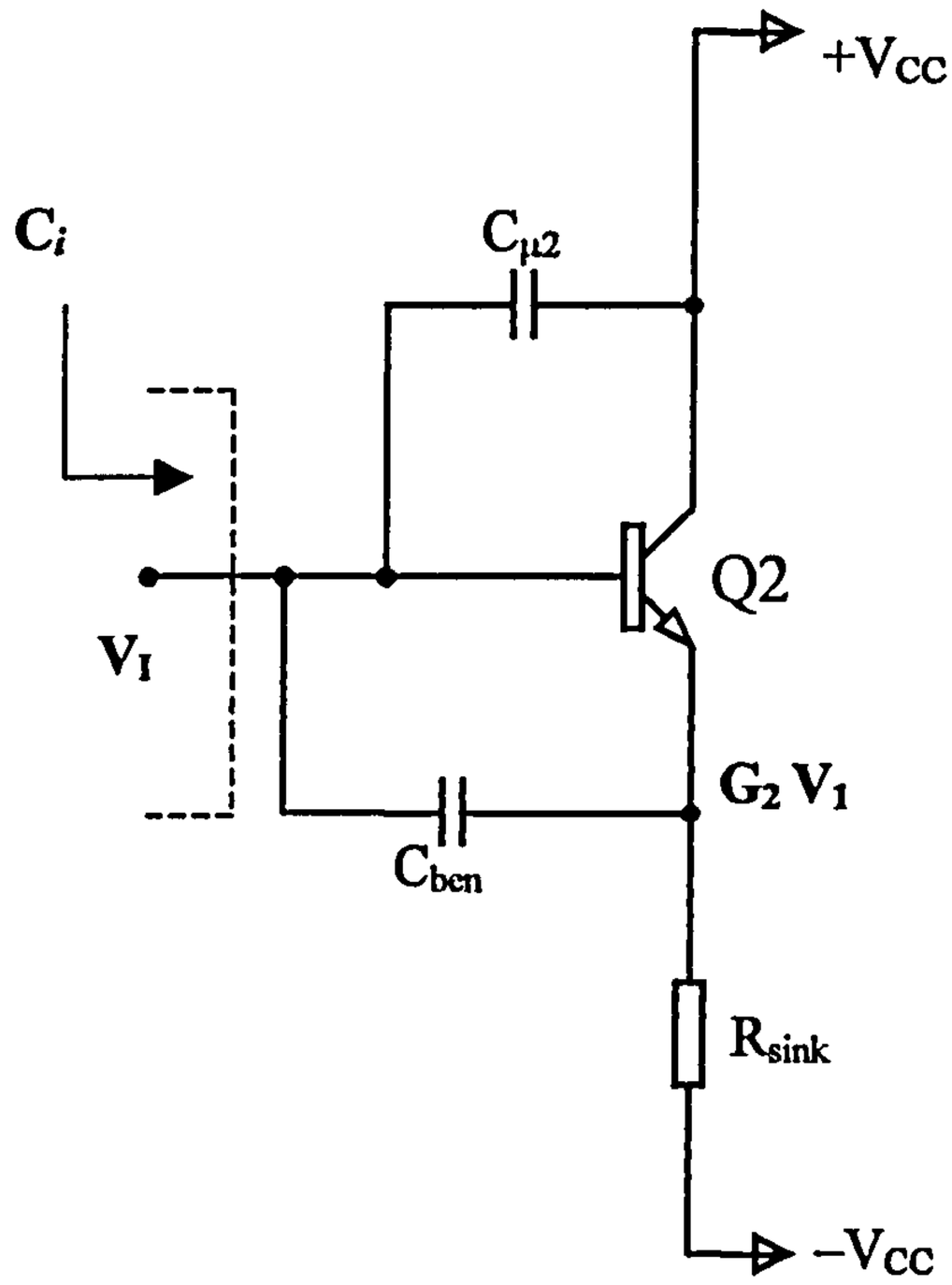


Figure 3.7 Simplified schematic of transistor Q_2 to calculate the input capacitance of the basic CFOA shown in Fig.3.1

An important aspect of CFOA performance is the input capacitance, C_i. First consider transistor Q_2: G is the small-signal emitter-follower voltage gain (which is close to unity), with a subscript corresponding to transistor number.

For Q_2,

$$(C_{in})_n = C_{\mu 2} + (1 - G_2)C_{ben} \tag{3.50}$$

Similarly for Q_1 with an emitter follower voltage gain G_1,

$$(C_{in})_p = C_{\mu 1} + (1 - G_1)C_{bep} \tag{3.51}$$

$$\text{Thus, } (C_i) \approx (C_{\mu 1} + C_{\mu 2}) + [(1 - G_1)C_{bep} + (1 - G_2)C_{ben}] \tag{3.52}$$

The term $(C_{\mu 1} + C_{\mu 2})$ dominates.

(3.5.3) Output regulation and output resistance (r_O)

The output characteristic of the basic CFOA in the linear region, on open-loop, would not appear to have been treated in the literature. This is possibly because it is not easy to determine, the problem being that the output saturates without the closed-loop connection.

In this section a theoretical discussion is presented to explain the results of simulation. The starting point is the circuit shown in Fig.3.8, this represents the output voltage follower with, for initial consideration, the 'Z' point earthed and serves to indicates the current distribution in the transistors in the presence of a finite output current, I_O.

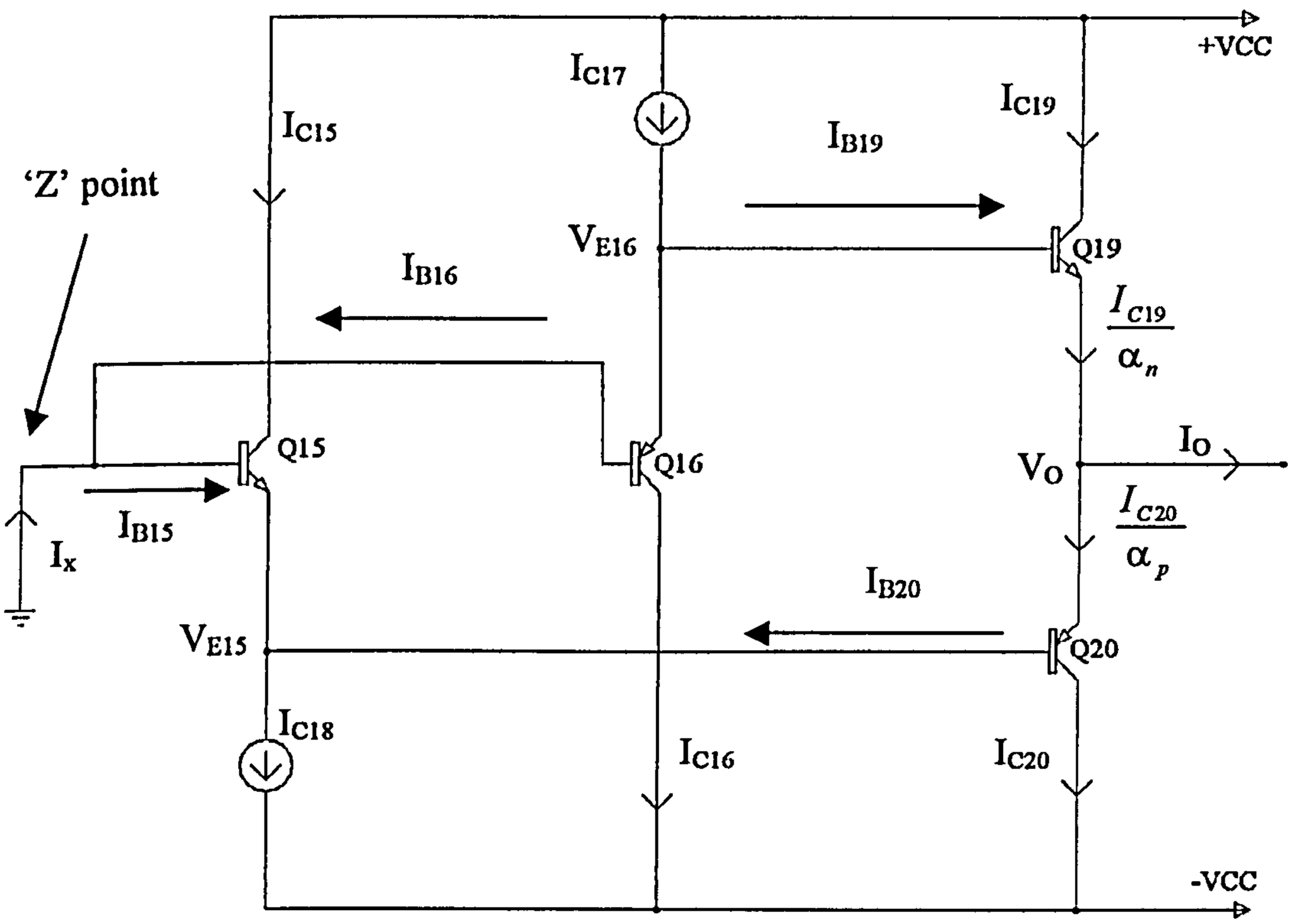


Figure 3.8 Showing currents used in the calculation of the open-loop output resistances (r_O)

Applying the 'Translinear Principle', it follows that,

$$I_{C15} \times I_{C16} = I_{C19} \times I_{C20} \tag{3.53}$$

But, $$\frac{I_{C19}}{\alpha_n} = I_O + \frac{I_{C20}}{\alpha_p} \tag{3.54}$$

α_n,α_p being the c.b. current gain of Q_{19}, Q_{20} respectively.

To find I_{C19} we substitute for I_{C20},

$$I_{C20} = \alpha_p[\frac{I_{C19}}{\alpha_n} - I_O] \tag{3.55}$$

then, $$I_{C15} \times I_{C16} = I_{C19} \times \alpha_p[\frac{I_{C19}}{\alpha_n} - I_O] \tag{3.56}$$

or, $$I_{C19}{}^2 \frac{\alpha_p}{\alpha_n} - I_{C19}\alpha_p I_O - I_{C15}I_{C16} = 0 \tag{3.57}$$

or, $$I_{C19}{}^2 - \alpha_n I_{C19} I_O - \frac{\alpha_n}{\alpha_p} I_{C15}I_{C16} = 0 \tag{3.58}$$

$$I_{C19} = \frac{\alpha_n I_O \pm \sqrt{(\alpha_n I_O)^2 + 4\frac{I_{C15}I_{C16}}{\alpha_p}\alpha_n}}{2} \tag{3.59}$$

Taking the positive sign for the square root, since $I_{C19}>0$, and re-arranging,

$$I_{C19} = \frac{\alpha_n I_O}{2}[1 + \sqrt{1 + (\frac{4 I_{C15} I_{C16}}{\alpha_n \alpha_p I_O{}^2})}] \tag{3.60}$$

Similarly, $I_{C20} = \frac{\alpha_p I_O}{2}[\sqrt{1 + (\frac{4 I_{C15} I_{C16}}{\alpha_n \alpha_p I_O^2})} - 1]$ (3.61)

For the approximations, $\alpha_n=\alpha_p=1$, $I_{C15}\approx I_{C16}\approx I_{C17}\approx I_{C18}\approx I_Q$, thus.

$$I_{C19} \approx \frac{I_O}{2}[1 + \sqrt{1 + (\frac{4 I_Q^2}{I_O^2})}] \quad (3.62)$$

and, $I_{C20} \approx \frac{I_O}{2}[\sqrt{1 + (\frac{4 I_Q^2}{I_O^2})} - 1]$ (3.63)

For $I_O=0$, $I_{C19} \approx I_{C20} \approx I_Q$.

If $I_O \ll I_Q$,

$$I_{C19} \approx (I_Q + \frac{I_O}{2}) \quad (3.64)$$

and, $I_{C20} \approx (I_Q - \frac{I_O}{2})$ (3.65)

This means that the change in I_{C19}, due to I_O, from its value at $I_O=0$, is equal in magnitude to the change in I_{C20}. If $I_O \gg I_Q$, then,

$$I_{C19} \approx (I_O + \frac{I_Q^2}{I_O}) \quad (3.66)$$

and, $I_{C19} \approx (\frac{I_Q^2}{I_O})$ (3.67)

Table 3.2 shows I_{C19}, I_{C20} calculated from equations (3.62), (3.63),

for the theoretical condition I_Q=0.1mA and various values of I_O. A plot of I_{C19}, I_{C20} versus I_O is shown in Fig.3.9

I_O (mA)	0	0.1	0.2	0.3
I_{C19} (mA)	0.1	0.162	0.241	0.330
I_{C20} (mA)	0.1	0.062	0.041	0.030

I_O (mA)	0.4	0.5	0.6	0.7
I_{C19} (mA)	0.423	0.519	0.616	0.714
I_{C20} (mA)	0.023	0.019	0.016	0.014

I_O (mA)	0.8	0.9	1.0
I_{C19} (mA)	0.812	0.911	1.009
I_{C20} (mA)	0.012	0.011	0.009

Table 3.2 (3 sections)

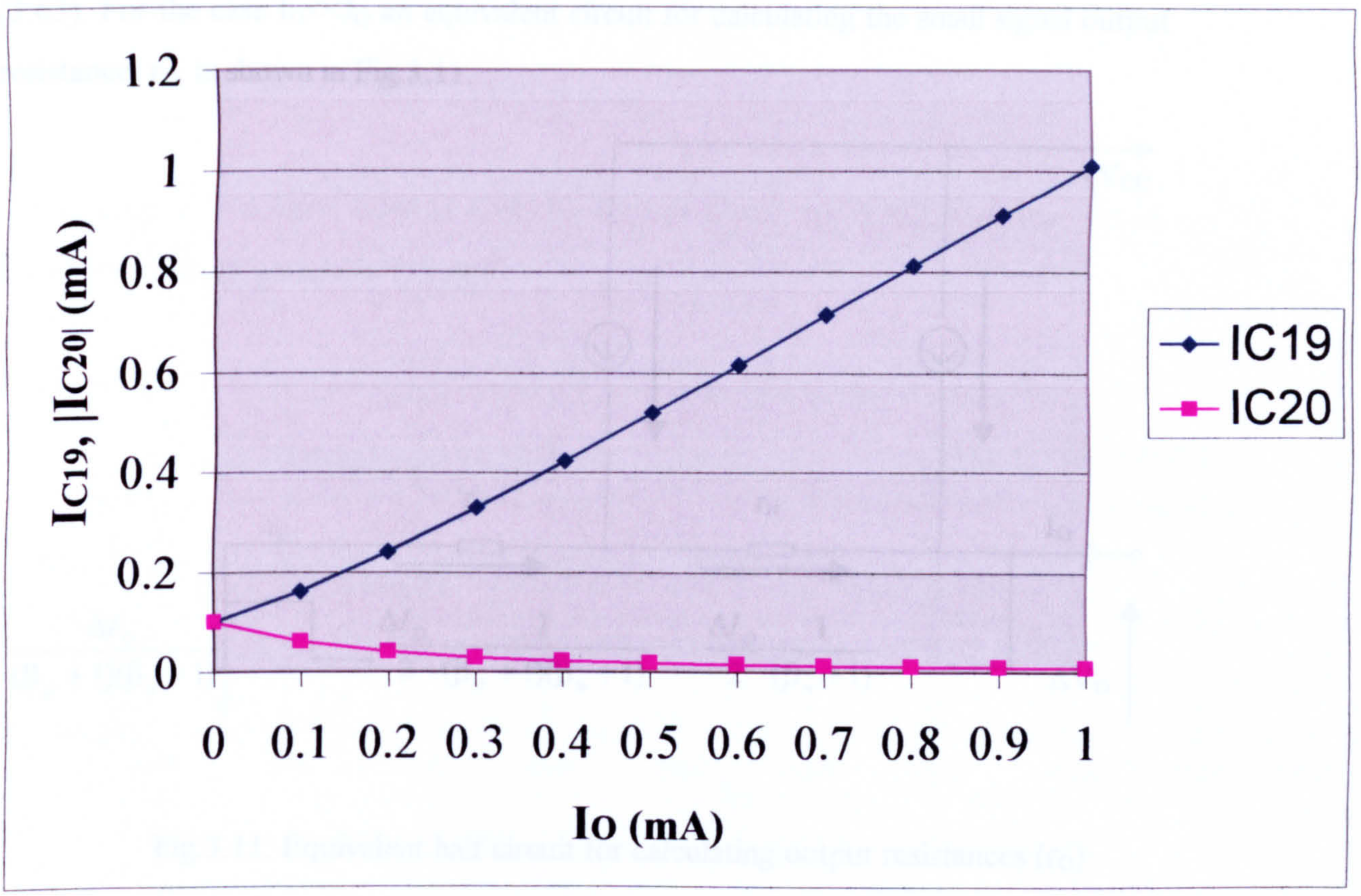


Figure 3.9 A theoretical, ideal, plot of I_{C19}, I_{C20} versus I_O

For I_O=500μA, this predicts I_{C19}=519μA. The actual value, from simulation, is 509.2μA, as shown in Fig.3.10. (Simulation measurements on I_{C15}, I_{C16}, I_{C17}, I_{C18} are given, for completeness, in Appendix 3.2)

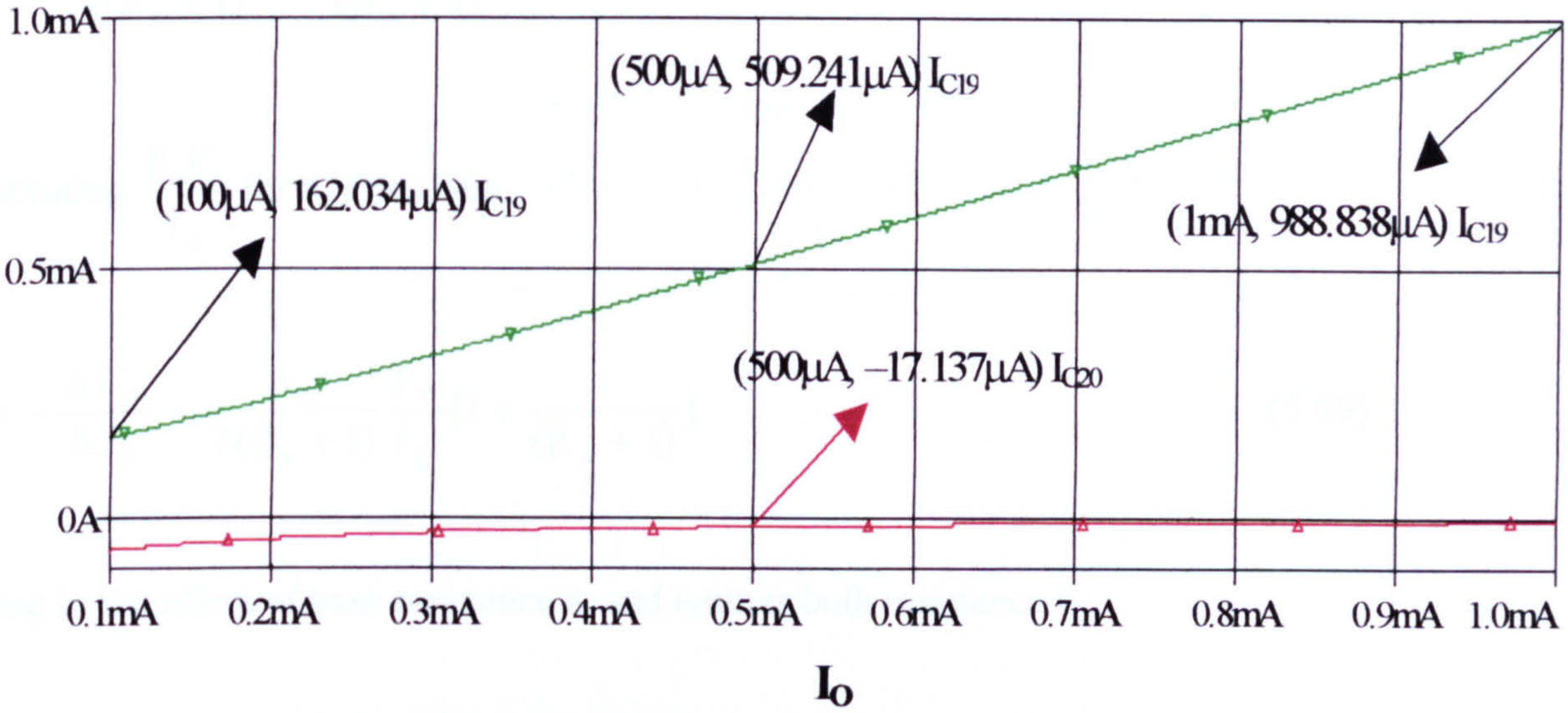


Figure 3.10 A simulated graph of I_{C19}, I_{C20} versus I_O

The difference is due to the approximations made in deriving equations (3.62), and (3.63). For the case I_O<<I_Q an equivalent circuit for calculating the small signal output resistance, r_O, is shown in Fig.3.11.

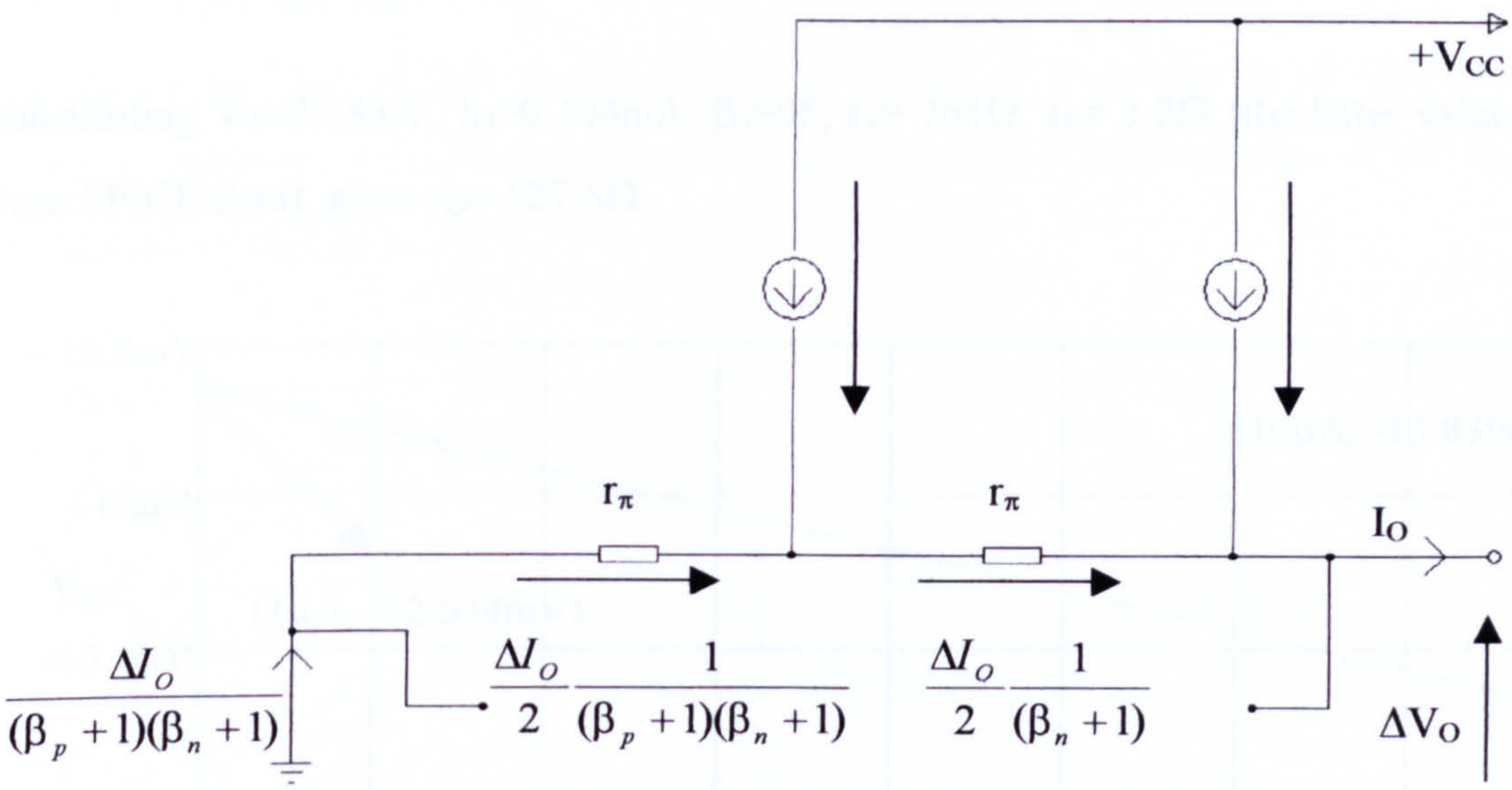


Fig.3.11. Equivalent half circuit for calculating output resistances (r_O)

Only one side is shown and base extrinsic resistance is ignored along with the collector-emitter resistance. Summing voltage drops,

$$\Delta V_O = \frac{-\Delta I_O r_\pi}{2(\beta_n + 1)}[1 + \frac{1}{(\beta_p + 1)}] \tag{3.68}$$

Substituting $\frac{\beta_n V_T}{I_Q}$ for r_π this gives,

$$r_O \approx -\frac{\Delta V_O}{\Delta I_O} = \frac{\beta_n}{2(\beta_n + 1)} \frac{V_T}{I_Q}[1 + \frac{1}{(\beta_p + 1)}] \tag{3.69}$$

Adding in the effect of base resistance r_x and emitter bulk resistance r_E,

$$r_O \approx \frac{\beta_n}{2(\beta_n + 1)} \frac{V_T}{I_Q}[1 + \frac{1}{(\beta_p + 1)}] + \frac{r_x}{2(\beta_n + 1)} + \frac{r_E}{2} \tag{3.70}$$

$$\text{or, } r_O \approx \frac{1}{2}[\frac{V_T}{I_Q} + \frac{r_x}{(\beta_n + 1)} + r_E] \tag{3.71}$$

Substituting V_T=25.8mV, I_Q=0.104mA, β_n=65, r_x= 264Ω, r_E= 3.2Ω (the latter values from SPICE data), gives $r_O \approx$ 127.6Ω.

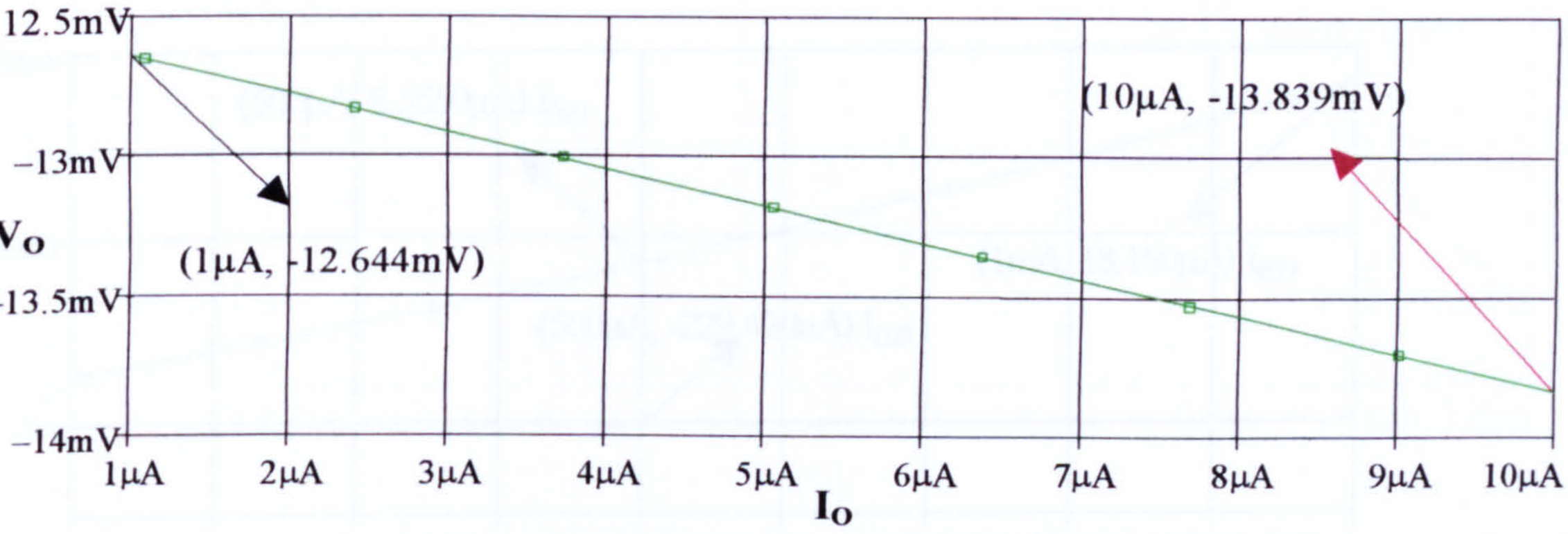


Figure 3.12 Regulation characteristic for 'low' value of I_O

The simulated value, determined from Fig.3.12, is r_O = (13.839–12.644)mV/9μA, i.e., $r_O \approx 132.77$. A possible reason for the difference could be a non-unity value for emission coefficient, η_E, of the BJTs, for if $I_C = I_S \exp(V_{BE}/\eta V_T)$, where $\eta_E > 1$, then $1/g_m = \eta V_T/I_Q$.

When a resistance R_Z, equal to the output resistance of Q_{11} in parallel with that of Q_{14}, is connected in the base circuit of Q_{15} and Q_{16} the current flowing in it is $\frac{\Delta I_O}{(\beta_n+1)(\beta_p+1)}$, so the output resistance r_O then becomes,

$$r_O \approx \frac{R_Z}{(\beta_n+1)(\beta_p+1)} + \frac{1}{2}\left[\frac{V_T}{I_Q} + \frac{r_x}{(\beta_n+1)} + r_E\right] \tag{3.72}$$

For 'large' R_Z, and the assumptions $\beta_n, \beta_p >> 1$,

$$r_O \approx \frac{R_Z}{\beta_p \beta_n} \tag{3.73}$$

Consider now the case $I_O > I_Q$. ΔV_O now comprises three components; ΔV_{O1}, the voltage change due to bulk drops; ΔV_{O2}, the change in V_{BE16} due to its change in collector currents; ΔV_{O3}, the change in V_{BE19}. For $I_O >> I_Q$, the change in the I_{B19} mirrors the change in I_{C19} (Fig.3.10), as is to be expected

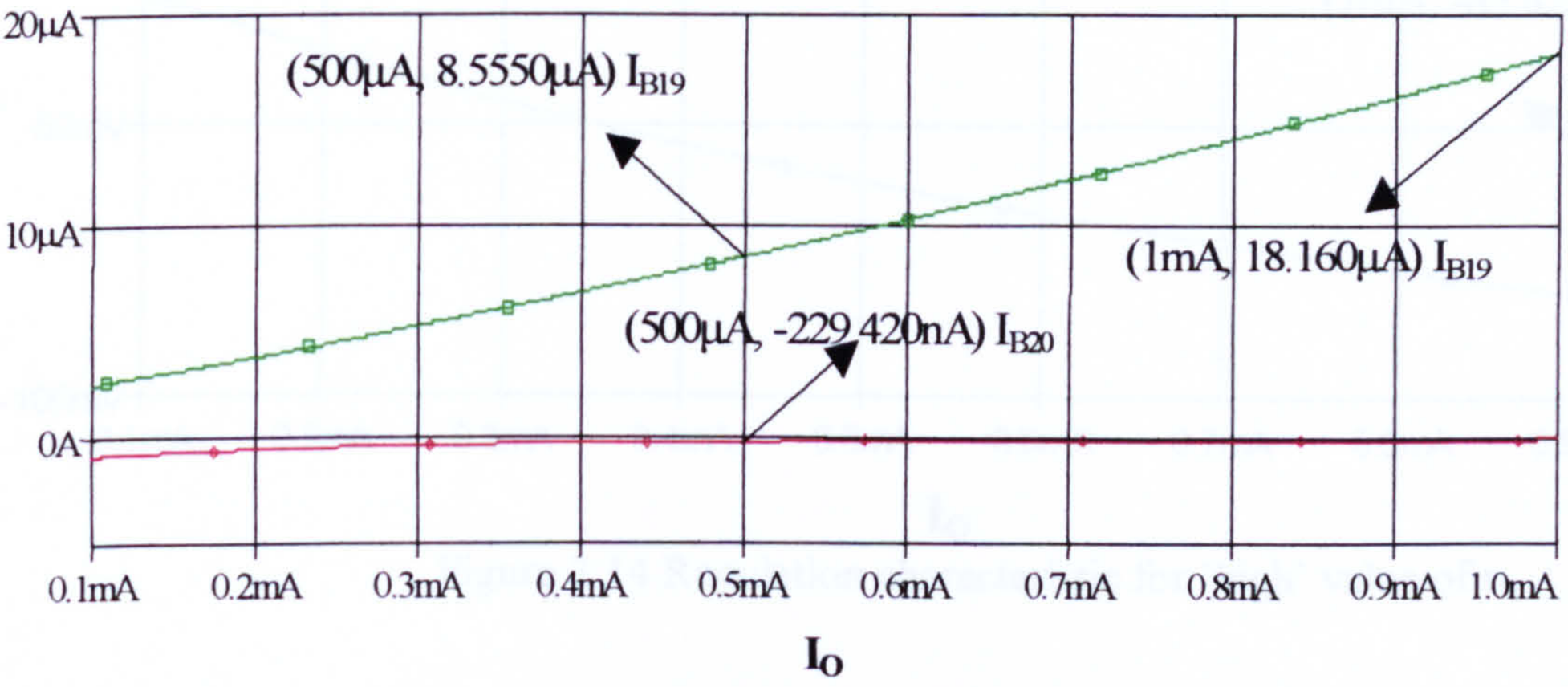


Figure 3.13 A simulated graph of I_{B19}, I_{B20} versus I_O

$$\Delta V_{O1} = -\Delta I_O [r_E + \frac{r_x}{(\beta_n + 1)}] \tag{3.74}$$

$$\Delta V_{O2} = V_T \log_e [\frac{I_Q - \frac{\Delta I_O}{(\beta_n + 1)}}{I_Q}] \tag{3.75}$$

$$\Delta V_{O3} = V_T \log_e [\frac{I_{C19}(I_{O2})}{I_{C19}(I_{O1})}] \tag{3.76}$$

Substituting measured data: ΔV_{O1}=6.5mV; ΔV_{O2}=3.63mV; ΔV_{O3}=46.57mV.

Thus ΔV_O=56.7mV which comprises with the simulated value of 60.009mV (Fig.3.14) when I_O changes from 0.1mA to 1mA. Fig.3.14 is non-linear because ΔV_{O3} dominates the expression for ΔV_O.

However, when R_Z is included in the base circuit of Q_{15}, Q_{16} the added component amounts to approximately, $\frac{R_Z}{\beta_p \beta_n}$. This normally dominates the expression for ΔV_O and effectively defines an output resistance as $\frac{R_Z}{\beta_p \beta_n}$, producing an approximately linear decay of V_O with I_O.

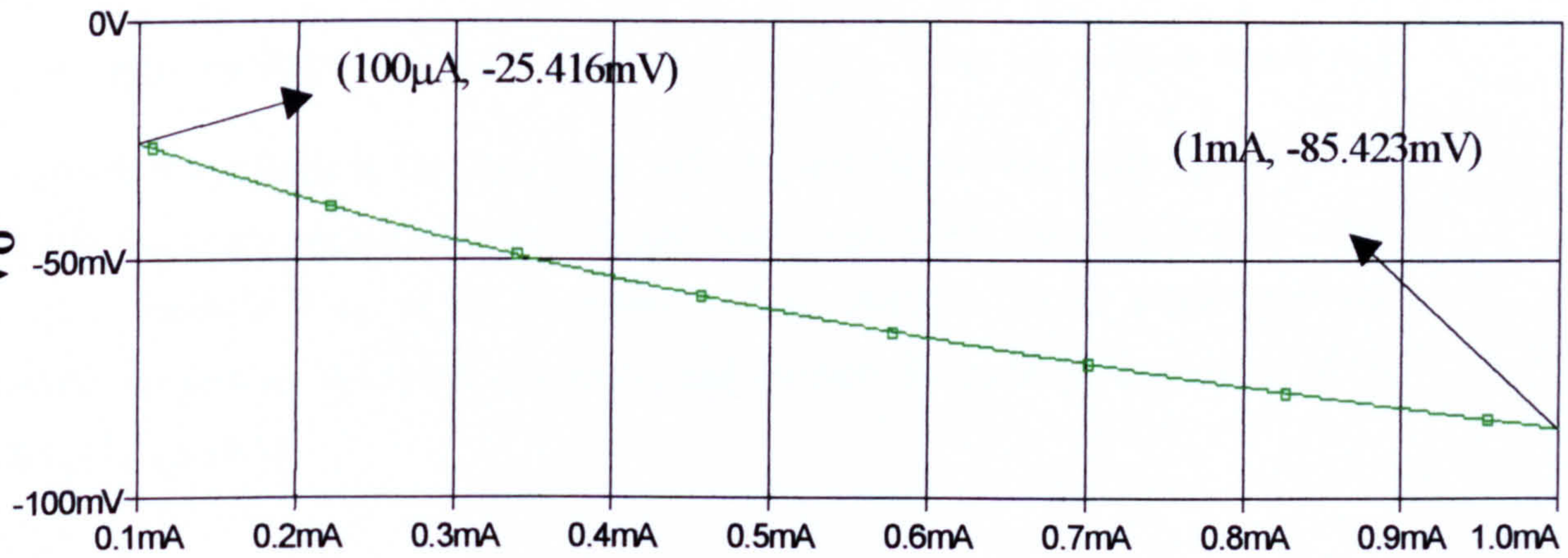


Figure 3.14 Regulation characteristic for 'high' value of r_O

The open-loop output regulation characteristic for 'high' value of output currents (Fig.3.15), determined by the method described in Chapter 2, bears this out. (For $I_Q \approx 0.1mA$, $R_Z \approx 5.2M\Omega$: see Appendix 3.3).

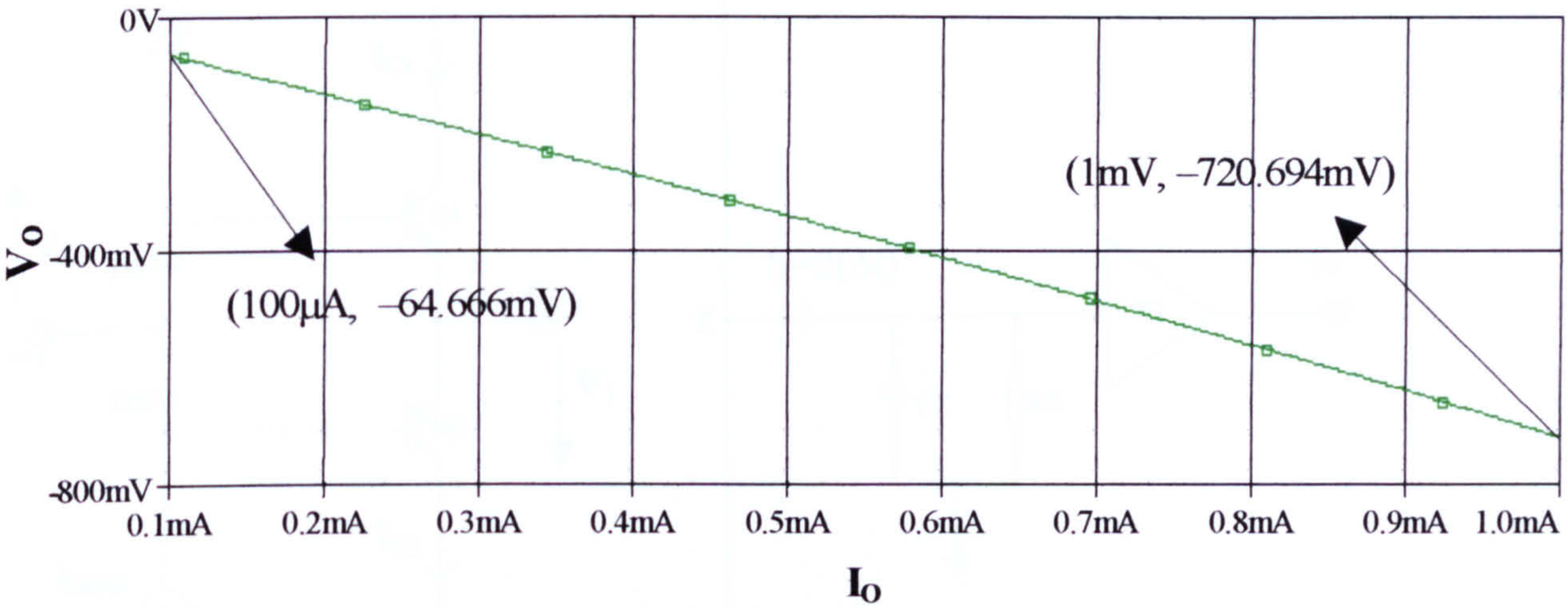


Figure 3.15 Output regulation characteristic (open-loop) for 'high' value of output currents.

(3.6) Analysis of Differential-mode operation

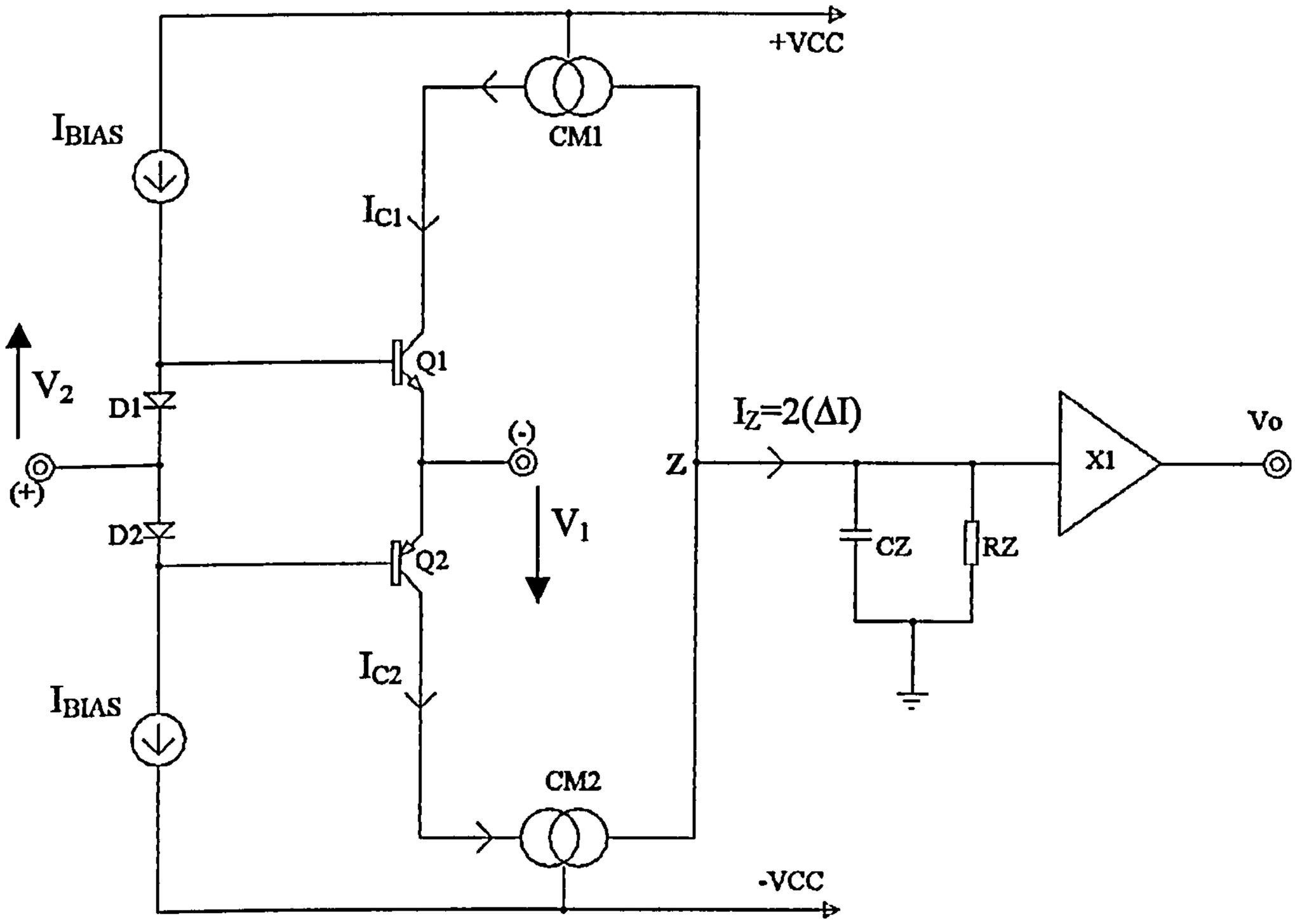


Figure 3.16 Simplified schematic of a standard CFOA

A simplified schematic of the standard CFOA architecture is shown in Fig.3.16, where the non-inverting and inverting nodes are connected to a differential input signal V_2 and V_1 respectively. The positive differential input signals is $V_2 = +\frac{V_{in}}{2}$ and the negative differential input signal is $V_1 = -\frac{V_{in}}{2}$. When the positive signal (V_2) is applied, the voltage at the base of Q_1 will rise, and the voltage at the emitter of Q_1 will fall due to the negative signal (V_1), increasing V_{BE1} of Q_1, resulting in an increase of I_{C1}. Similarly V_{BE2} of Q2 decreases and I_{C2} reduces. Under small-signal the collector current I_{C1} of Q_1 will rise by ΔI, and similarly the collector current I_{C2} of Q_2 will fall by ΔI **[3-1]**.

Currents I_{C1} and I_{C2} are then mirrored by CM1 and CM2 to a high impedance gain-node (Z), where they subtract, giving a total signal current $I_Z = 2\Delta I$, resulting in an output voltage of $V_{out} = (2\Delta I.Z(z))$. Transistors Q_1 and Q_2 are configured as a class-AB

complementary-pair stage. The operating point of these transistors is in the active region, and class-AB, with the DC current set by the bias network comprising the two diodes D_1 and D_2 and the two current sources, I_{bias}.

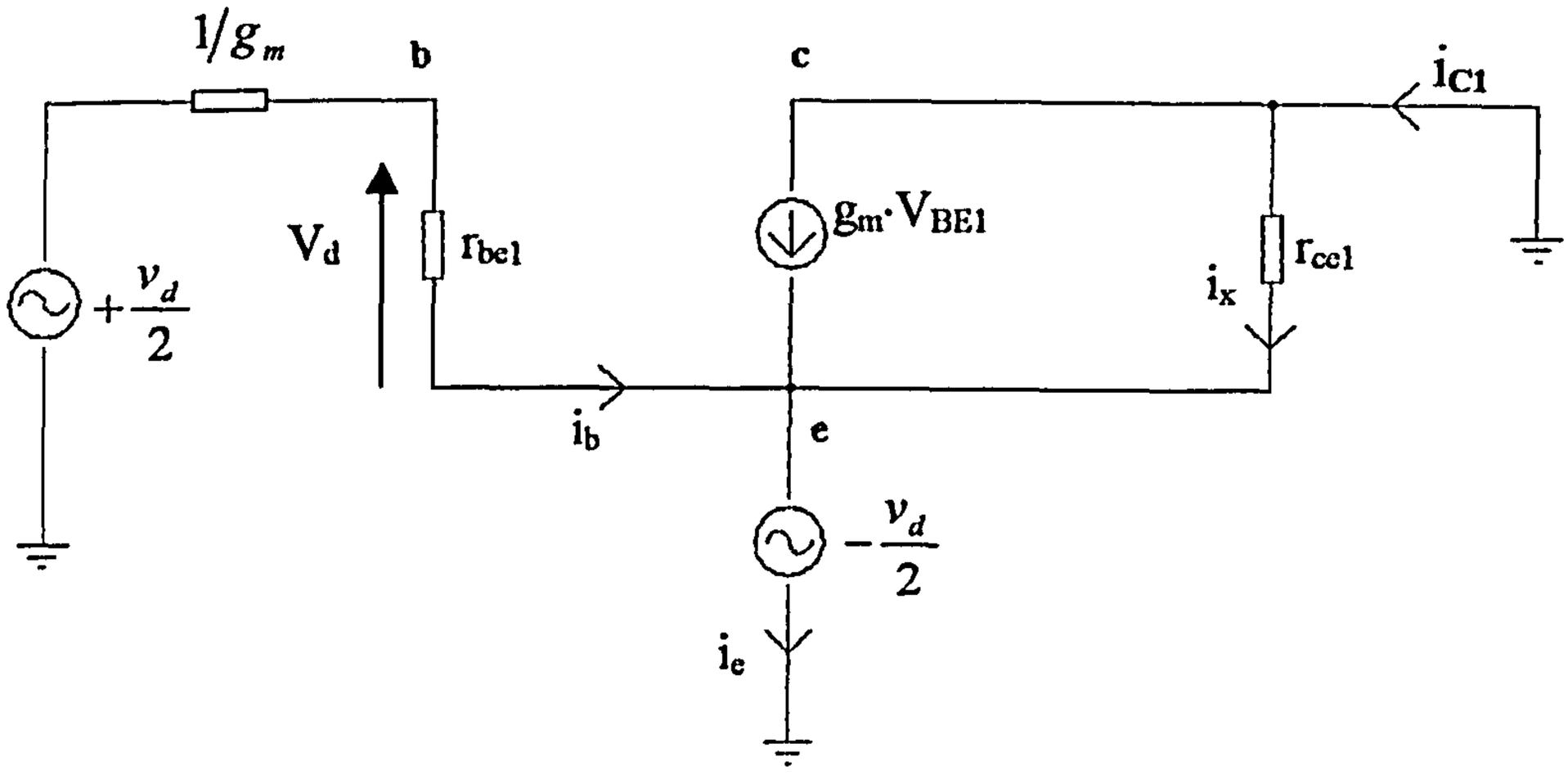


Figure 3.17 Small-signal differential-mode half circuit

Fig.3.17 shows the small-signal differential-mode half circuit, which can be analysed to predict the circuit behaviour. The output current $i_{C1} = i_{out(dm)}$ is given by

$$i_{C1} = g_m \cdot v_{BE1} + \frac{v_d}{2 \cdot r_{ce1}} \tag{3.77}$$

Since $v_{be} \approx v_d$, and r_{cc} is very high compared with $1/g_m$, so (3.77) can be reduced to

$$g_{Tdm} \approx \frac{2 i_{C1}}{v_d} = 2 g_m \approx \frac{2}{r_e} \approx \frac{2 I_{CQ}}{V_T} \tag{3.78}$$

where g_{Tdm} is the transconductance of the differential-mode operation, g_m is the transconductance of one particular transistor at a time in the input class-AB complementary-pair, I_{CQ} is the dc bias current, and V_T is the thermal-voltage. Thus the differential-mode gain (A_{dm}) of the CFOA is

$$A_{dm} = \frac{2\, i_{C1} \cdot Z_z}{v_d} = g_{Tdm} \cdot Z_z \qquad (3.79)$$

where Z_Z is high impedance gain-node of the CFOA.

(3.7) Analysis of Common-mode operation

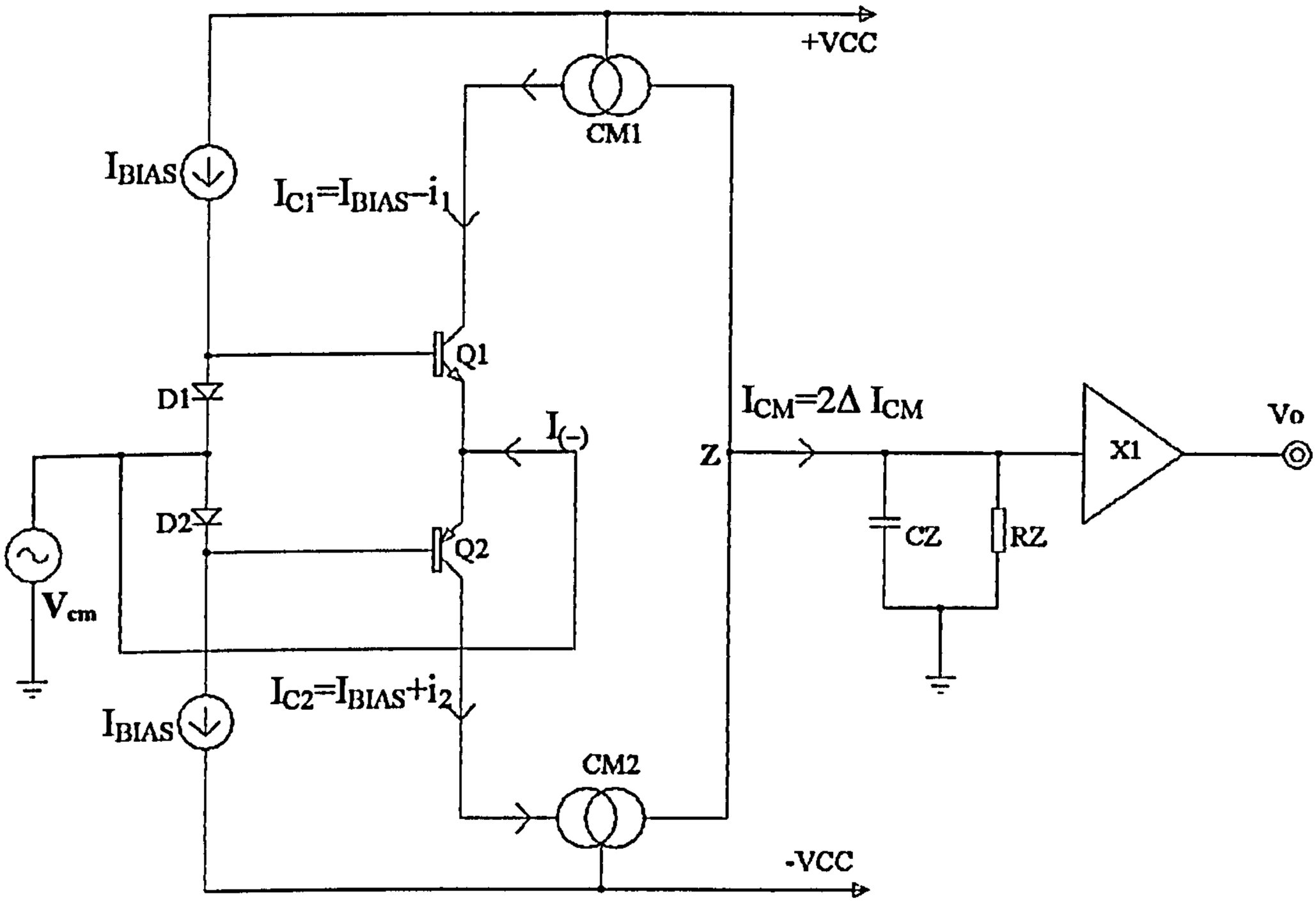


Figure 3.18 Circuit schematic of the CFOA with a common-mode input signal, V_{cm}

The input stage of the CFOA is the main factor in determining the CMRR performance of the CFOA **[3-1]**, and **[3-2]**. A further study has been made to investigate the parameter that has a direct responsibility towards the common-mode operation, in order to fully understand the inner working of the CFOA, when a common-mode signal is applied to its input. It has been reported that the drawback of the CMRR performance of the CFOA is due to the output impedances of transistors in the input stage **[3-1]**, and **[3-2]**.

Currents i_1 and i_2 flow through the output impedance of Q_1, and Q_2 respectively, as a direct result of the common-mode input voltage V_{cm}, and are

$$i_1 = \frac{V_{cm}}{r_{ce1}} \quad ; \quad i_2 = \frac{V_{cm}}{r_{ce2}} \tag{3.80}$$

These currents are then mirrored to a high impedance gain-node (Z), where they add algebraically. Thus a high common-mode voltage gain is generated, and a low value of the CMRR is produced, normally in the region of 50dB. Fig.3.18 shows a circuit schematic of the CFOA with a common-mode input signal. Applying a positive common-mode input signal decreases the value of V_{CB} of Q_1, and as the Early voltage of this transistor is finite it results in a decrease in the collector current I_{C1} of Q_1 by an amount ΔI_{CM}.

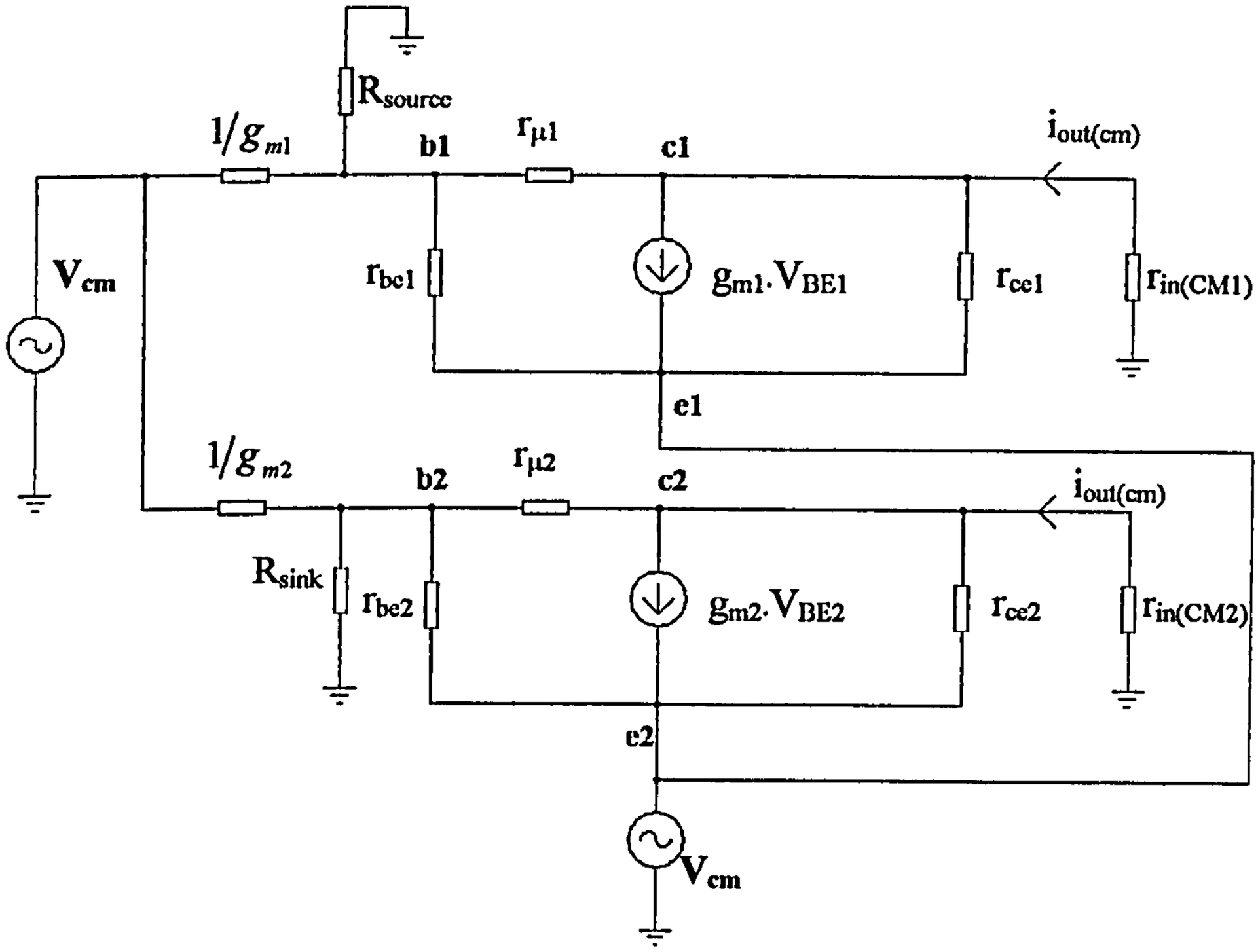


Figure 3.19 Small-signal equivalent circuit of the CFOA input stage for common-mode analysis

Furthermore the positive common-mode input voltage will cause the value of V_{CB} of Q_2 to rise and therefore the collector current I_{C2} of Q_2 to increase by the same amount **[3-1]**. Hence, when the collector currents of Q_1 and Q_2 are mirrored by CM1 and CM2 to a high impedance gain-node (Z), the net current into the Z-node is

$$I_z \approx I_{C2} - I_{C1} = (\Delta I_{CM}) - (-\Delta I_{CM}) = 2\Delta I_{CM} \tag{3.81}$$

Since $I_{C1} \approx I_{E1}$, and $I_{C2} \approx I_{E2}$, then $I_{(-)} = I_{C2} - I_{C1}$, where $I_{(-)}$ is the inverting node input current.

Thus,

$$I_Z \approx I_{(-)} \approx I_{C2} - I_{C1} = 2\Delta I_{CM} \tag{3.82}$$

To obtain a better understanding, the class AB bias voltage follower (shown in Fig. 3.18) was analysed using small-signal modelling. Fig.3.19 shows the small-signal equivalent circuit for the input stage of the CFOA, driven by an input common-mode voltage signal.

When a common-mode input voltage is applied to the circuit shown in Fig.3.19, as $1/g_m$, rin_{CM1}, and rin_{CM2} are small, and since the bases of Q_1 and Q_2 are connected together there will be no signal voltage across the base to emitter terminals of these two input transistors. Hence, both $g_{m1}V_{be1}$ and $g_{m2}V_{be2}$ signal current generators are inactive. The net result is that the circuit of Fig.3.19 simplifies to that shown in Fig.3.20 and the output current from the coupled current-mirrors, i_{out}, is given by

$$i_{out(cm)} = -V_{cm} \cdot \left[\frac{I_Q}{V_{AN}} + \frac{1}{r_{\mu 1}} + \frac{I_Q}{V_{AP}} + \frac{1}{r_{\mu 2}} \right] \approx -V_{cm} \cdot \left[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}} \right] \tag{3.83}$$

since $r_{\mu 1} \approx r_{\mu 2} >> r_{ce1} \approx r_{ce2} = r_{ce}$. Then the common-mode transconductance g_{Tcm} is,

$$g_{Tcm} \approx \frac{i_{out(cm)}}{V_{cm}} = -2\left[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}} \right] \tag{3.84}$$

Thus the r_{ce} values of Q_1, and Q_1 directly determine the A_{cm}.

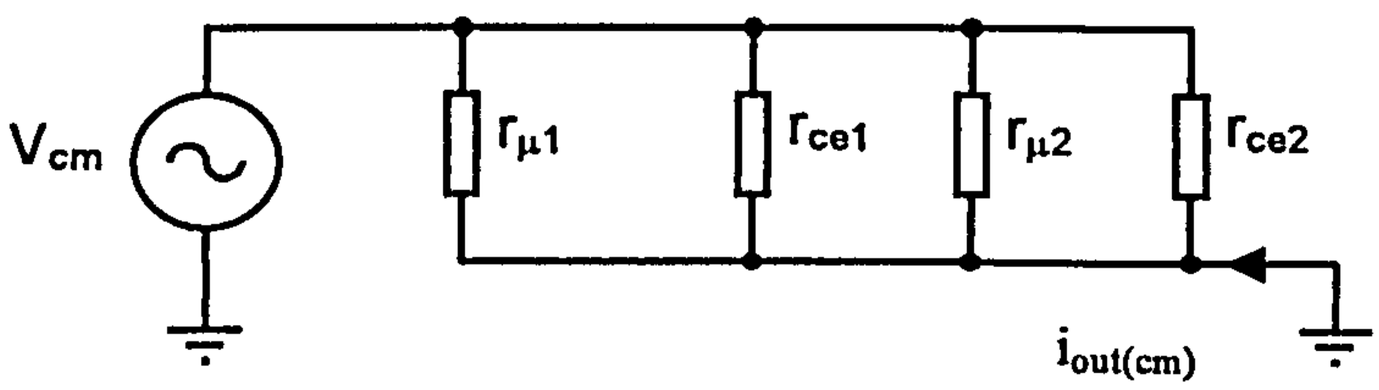


Figure 3.20 Reduced small-signal equivalent circuit for the Class AB Bias Voltage Follower

It is essential at this stage to link g_{Tcm} and the common mode gain, A_{cm}, of the CFOA, thus (3.85) is given as

$$A_{cm} = \frac{i_{out\ (cm)} \cdot Z_z}{V_{cm}} = g_{Tcm} \cdot Z_z \qquad (3.85)$$

(3.8) Common-mode rejection ratio (CMRR)

The common-mode rejection ratio (CMRR), is defined as the ratio of the magnitude of the differential gain to the magnitude of the common mode gain **[3-3]**, and it can be expressed as:

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| \tag{3.86}$$

where A_{dm}, A_{cm} is the differential mode gain, and the common mode gain respectively. Therefore by substituting (3.79), and (3.85) into (3.86) gives

$$CMRR = \left|\frac{\frac{i_{out\ (dm)} \cdot Z_z}{V_d}}{\frac{i_{out\ (cm)} \cdot Z_z}{V_{cm}}}\right| = \left|\frac{\frac{i_{out\ (dm)}}{V_d}}{\frac{i_{out\ (cm)}}{V_{cm}}}\right| = \left|\frac{g_{Tdm}}{g_{Tcm}}\right| \tag{3.87}$$

Equation (3.87) indicates that the high impedance gain-node (Z_Z) cancels. Thus, having a higher, or lower, impedance gain-node (Z_Z) will not influence the CMRR in any way. Now by substituting (3.78), which defines g_{Tdm} the transconductance of the differential-mode operation of the CFOA, and (3.84), which defines g_{Tcm} the transconductance of the common-mode operation of the CFOA into (3.87).

$$CMRR = \left|\frac{g_{Tdm}}{g_{Tcm}}\right| = \left|\frac{2I_Q}{V_T} \cdot \frac{1}{2[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}}]}\right| = \left|\frac{I_Q}{V_T[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}}]}\right| \tag{3.88}$$

In a special case where $V_A=V_{AN}=V_{AP}$,

$$CMRR = \left|\frac{V_A}{2V_T}\right| \tag{3.89}$$

Table.3.3 summaries the variations of CMRR, A_{dm} and A_{cm} with changing values of r_{cc1}, r_{cc2}, r_{c1}, and r_{c2}

Increase parameter	CMRR	A_{dm}	A_{cm}
r_{cc1}, and r_{cc2}	Increases	No change	Decreases
r_{c1}, and r_{c2}	Decreases	Decreases	No change

Table 3.3

To test this theoretical result the circuit shown in Fig.3.1 was simulated using SPICE. This was undertaken using Analog Devices XFCB device parameters, and the frequency responses of A_{dm}, A_{cm} and CMRR were obtained (see Fig. 3.21). The values of the Early voltage (V_{AP}) for the PNP device Q_7 and Q_4, and (V_{AN} the NPN device Q_5 and Q_3) were then doubled, the simulation above repeated. The results are shown in Fig. 3.22.

This was repeated for the results presented in Fig. 3.23, in which the Early voltages of the input transistors were four times greater than the actual AD-XFCB parameters. Although changing the values of V_A in practice is virtually impossible, as a simulation exercise since $r_{cc}\approx V_A/I_{CQ}$, comparison of the results does confirm the anticipated significance of r_{cc} in determining the CMRR of the CFOA. In moving from Fig. 3.21 through to Fig. 3.23 the values of A_{cm} decreased as expected by 6dB, and A_{dm} remain almost unchanged and the CMRR increased by 6dB for each step in doubling of V_A.

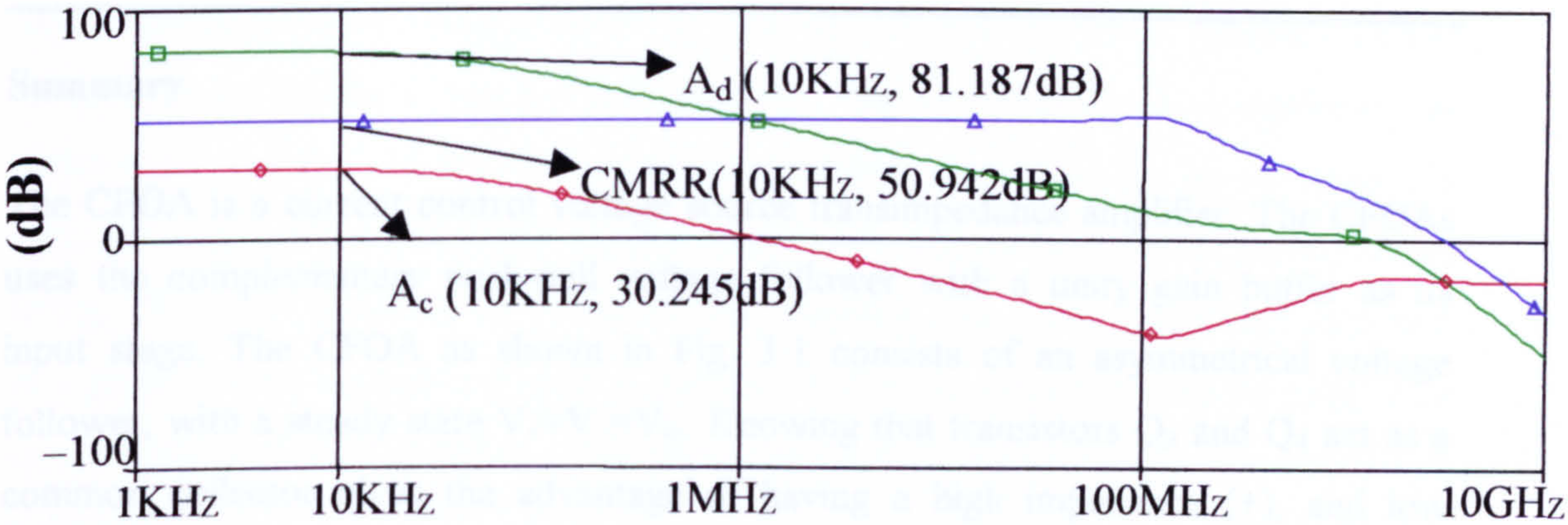


Figure 3.21. SPICE results for Adm, Acm and CMRR versus frequency for Fig.3.1 using AD-XCFB process parameters

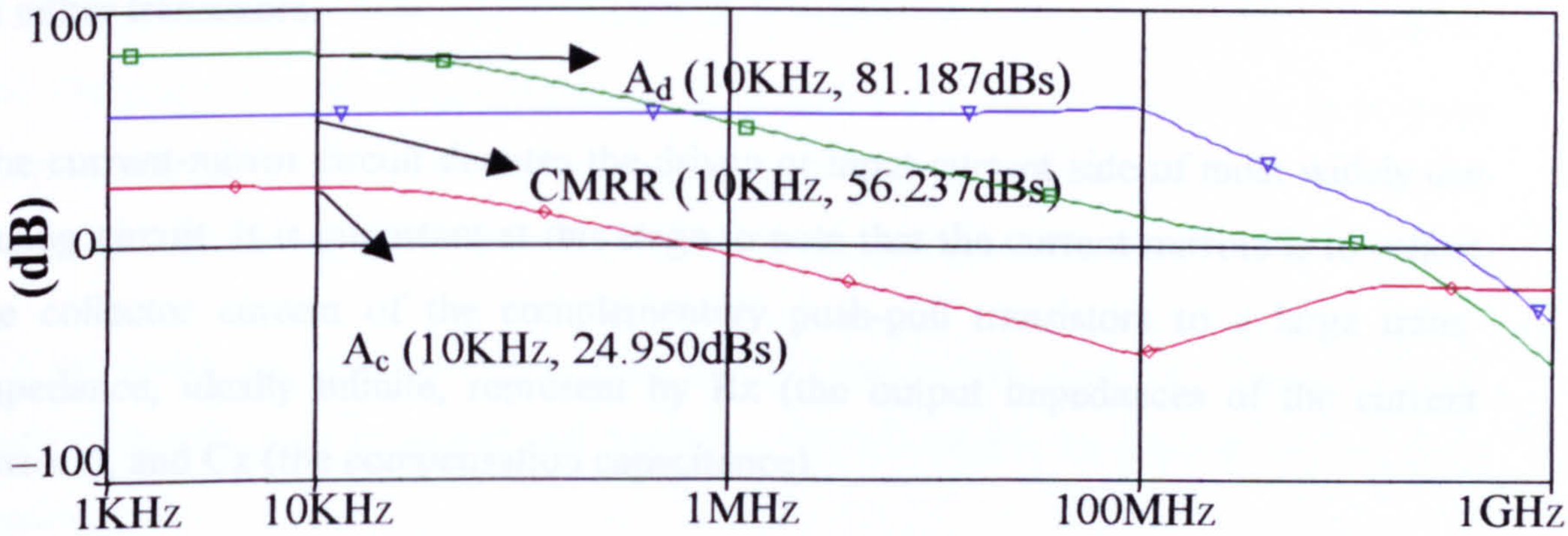


Figure 3.22. Adm, Acm and CMRR versus frequency, as in Fig.3.21, except that V_A has been doubled for the input stage devices

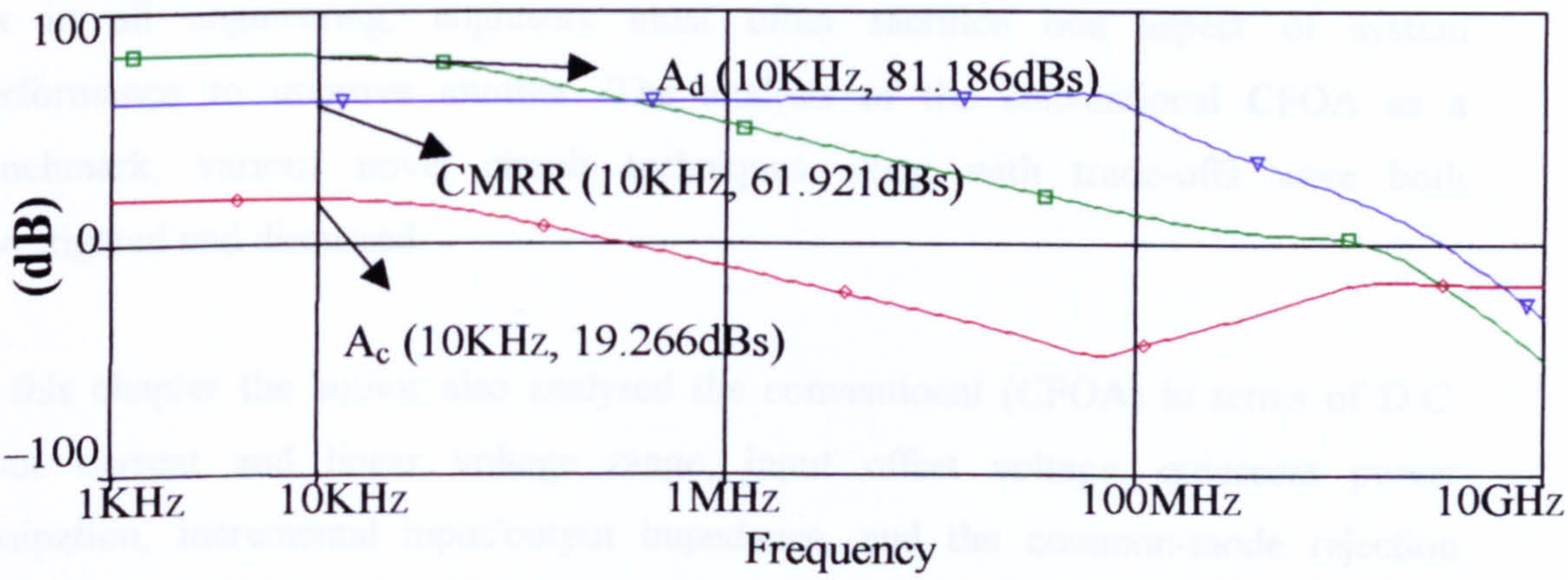


Figure 3.23. Adm, Acm and CMRR versus frequency, as in Fig.3.22, except that V_A has been quadrupled for the input stage devices

Summary

The CFOA is a current control voltage source transimpedance amplifier. The CFOAs uses the complementary push-pull voltage follower with a unity gain buffer as its input stage. The CFOA as shown in Fig. 3.1 consists of an asymmetrical voltage follower, with a steady state $V_+=V_-=V_{in}$. Knowing that transistors Q_3 and Q_4 act as a common collector gives the advantage of having a high impedance (+), and low impedance at the load (–). The reason for having Q_1 and Q_2 is to give the input drive transistors Q_3 and Q_4 a class AB input stage, as well as eliminating the cross over distortion which is caused by loss of $V_{be} = 0.7V$ from coming up or down at the base of either transistors.

The current-mirror circuit denotes the driven or input current side of most widely use analog circuit. It is important at this stage to note that the current-mirrors is to reflect the collector current of the complementary push-pull transistors to a large trans-impedance, ideally infinite, represent by Rz (the output impedances of the current mirrors), and Cz (the compensation capacitance).

The trend toward low-voltage, single-supply systems is fuelled by designers' attempts to balance the often-contradictory goals of lower product size and cost versus longer battery life and better system performance. This trend may be good for consumers, but it complicates the task of choosing an appropriate op-amp for a given application. As in all engineering, engineers must often sacrifice one aspect of system performance to improve another. The analysis of the conventional CFOA as a benchmark, various novel circuit techniques along with trade-offs were both investigated and discussed.

In this chapter the author also analysed the conventional (CFOA) in terms of D.C. input current and linear voltage range, input offset voltage, quiescent power dissipation, incremental input/output impedance, and the common-mode rejection ratio (CMRR) performance, and, has identified the mechanisms primarily responsible for these characteristics, with the objective of determining suitable techniques to enhance performance and have consequently proposed new CFOA designs.

Summary

The CFOA is a current control voltage source transimpedance amplifier. The CFOAs uses the complementary push-pull voltage follower with a unity gain buffer as its input stage. The CFOA as shown in Fig. 3.1 consists of an asymmetrical voltage follower, with a steady state $V_+=V_-=V_{in}$. Knowing that transistors Q_3 and Q_4 act as a common collector gives the advantage of having a high impedance (+), and low impedance at the load (–). The reason for having Q_1 and Q_2 is to give the input drive transistors Q_3 and Q_4 a class AB input stage, as well as eliminating the cross over distortion which is caused by loss of V_{be} = 0.7V from coming up or down at the base of either transistors.

The current-mirror circuit denotes the driven or input current side of most widely use analog circuit. It is important at this stage to note that the current-mirrors is to reflect the collector current of the complementary push-pull transistors to a large trans-impedance, ideally infinite, represent by Rz (the output impedances of the current mirrors), and Cz (the compensation capacitance).

The trend toward low-voltage, single-supply systems is fuelled by designers' attempts to balance the often-contradictory goals of lower product size and cost versus longer battery life and better system performance. This trend may be good for consumers, but it complicates the task of choosing an appropriate op-amp for a given application. As in all engineering, engineers must often sacrifice one aspect of system performance to improve another. The analysis of the conventional CFOA as a benchmark, various novel circuit techniques along with trade-offs were both investigated and discussed.

In this chapter the author also analysed the conventional (CFOA) in terms of D.C. input current and linear voltage range, input offset voltage, quiescent power dissipation, incremental input/output impedance, and the common-mode rejection ratio (CMRR) performance, and, has identified the mechanisms primarily responsible for these characteristics, with the objective of determining suitable techniques to enhance performance and have consequently proposed new CFOA designs.

Input common-mode voltage range is one of the first issues a designer should consider in specifying a single-supply op amp. The first impulse is to eliminate this concern by specifying a Rail-to-Rail input capability. As is true for all op amps, the open-loop gain for a rail-to-rail output amplifier is a function of the output voltage swing. Thus, to evaluate a rail-to-rail output amplifier, you must specify the gain both at a given output voltage and with a given load. Certain penalties must be paid, such as stacking vertical transistors to increase the CMRR, however, for true rail-to-rail operation.

Most of Maxim's low-voltage op amps have input common-mode voltage ranges that include the negative supply rail, but only some allow inputs that extend to the positive rail as well. Others allow input voltages only within one or two volts of the positive rail. Op amps that allow signals only to the negative rail will be referred to as ground-sensing amplifiers. Those that allow signals to either rail will be referred to as rail-to-rail input amplifiers which is precisely what this thesis deals with.

The emphasis has been on improving CMRR, bandwidth, and DC Voltage-Offset performance in order to design and develop a CFOA suitable for radio frequency (RF) applications.

(3.9) References

[3-1] Vere-Hunt, M. A., and Lidgey, F. J., 1991, 'A novel transconductance cell,', Proceedings of the European Conference on Circuit Therory and Design' (ECCTD), pp. 1341–1348.

[3-2] Lidgey, F. J., Su, W. J., and Hayatleh, K., Oct., 1998, 'Novel current-feedback operational amplifier design based on a floating circuit technique'. IEE Colloquium on Analogue Signal Processing', Oxford, 9/1-94.

[3-3] Gray, P. R., and Meyer R. G., 1993, Analysis and Design of Analog Integrated Circuits, 3rd Edition (New York: Wiley).

APPENDIX 3

APP 3.1 Effect of mismatches in the simple current source/mirror

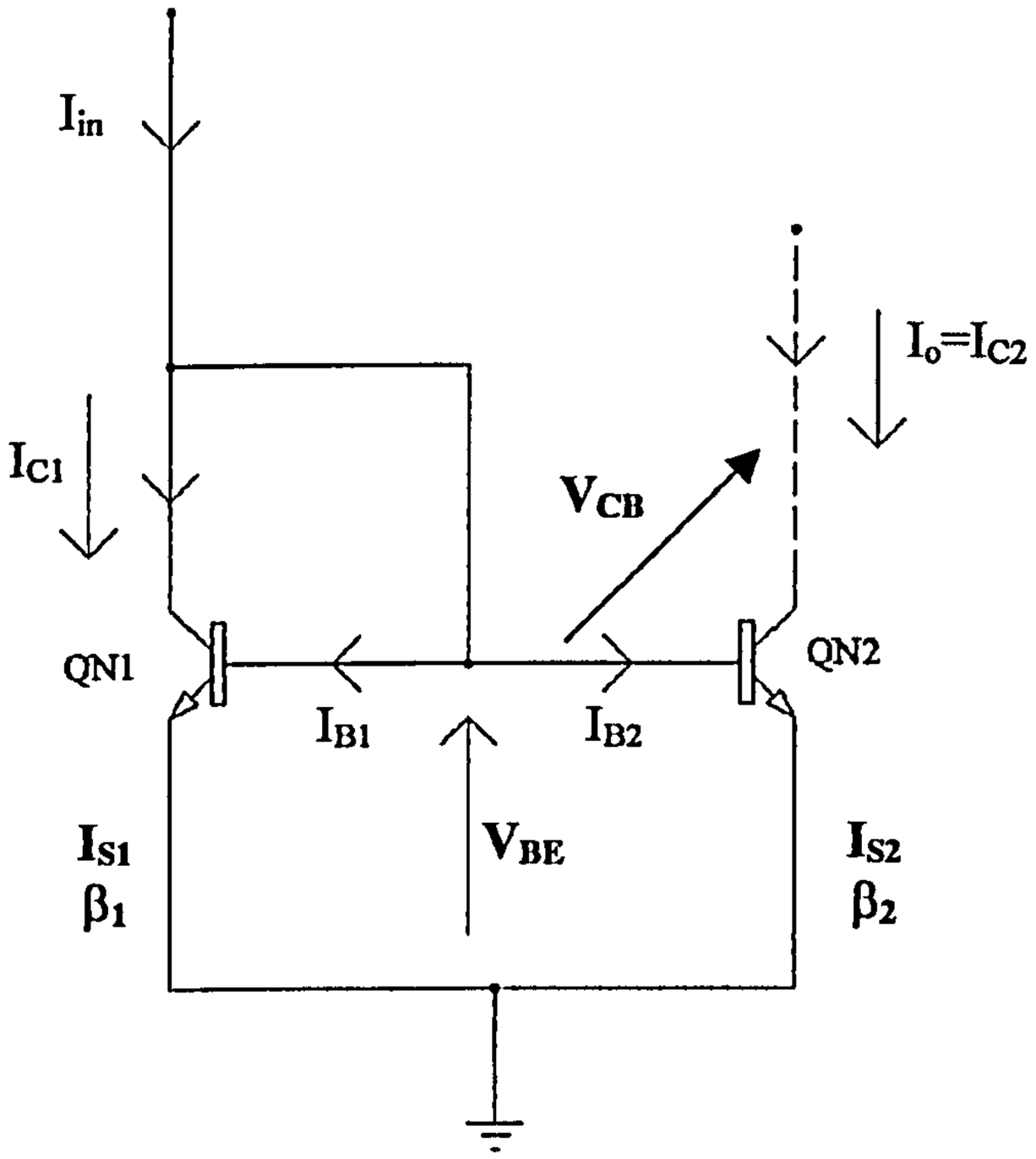


Figure A 3.1

For simplicity $e^{\frac{V_{BE}}{V_T}} = \int(V_{BE})$

$$I_{C1} = I_{S1}\int(V_{BE})$$

$$I_{B1} = \frac{I_{S1}}{\beta_1}\int(V_{BE}) \qquad I_{B2} = \frac{I_{S2}}{\beta_2}\int(V_{BE})$$

β_1, and β_2 at $V_{CB}=0$

$$I_{C2} = I_{S2}[1+\frac{V_{CB}}{V_A}]\int(V_{BE})$$

$$\therefore I_{in} = I_{C1} + I_{B1} + I_{B2} = [I_{S1} + \frac{I_{S1}}{\beta_1} + \frac{I_{S2}}{\beta_2}]\int(V_{BE})$$

$$I_{in} = I_{S1}[1+\frac{1}{\beta_1} + \frac{I_{S2}}{I_{S1}\cdot\beta_2}]\int(V_{BE})$$

and, $I_o = I_{C2} = I_{S2}[1+\frac{V_{CB}}{V_A}]\int(V_{BE})$

$$\frac{I_o}{I_{in}} = \frac{I_{S2}(1+\frac{V_{CB}}{V_A})\int(V_{BE})}{I_{S1}[1+\frac{1}{\beta_1}+\frac{I_{S2}}{I_{S1}}\cdot\frac{1}{\beta_2}]\int(V_{BE})}$$

Now V_{OS} is the difference between V_{BES} when the two transistors operate at the same, I_C, V_{CB}.

$$\therefore V_{OS} = V_T \log_e \frac{I_{S2}}{I_{S1}}, \text{ or } \qquad \frac{I_{S2}}{I_{S1}} = e^{\frac{V_{OS}}{V_T}}$$

$$\therefore \frac{I_o}{I_{in}} = \frac{e^{\frac{V_{OS}}{V_T}}(1+\frac{V_{CB}}{V_A})}{[1+\frac{1}{\beta_1}+\frac{e^{\frac{V_{OS}}{V_T}}}{\beta_2}]}$$

$$\text{or} \qquad \frac{I_o}{I_{in}} = \frac{(1+\frac{V_{CB}}{V_A})}{[(1+\frac{1}{\beta_1})e^{\frac{V_{OS}}{V_T}}+\frac{1}{\beta_2}]}$$

But for I_{S2} close to I_{S1}, $V_{OS} \ll V_T$, and $e^{-\frac{V_{OS}}{V_T}} \approx (1-\frac{V_{OS}}{V_T})$

$$\therefore \frac{I_o}{I_{in}} = \frac{(1+\frac{V_{CB}}{V_A})}{[(1+\frac{1}{\beta_1})(1-\frac{V_{OS}}{V_T})+\frac{1}{\beta_2}]}$$

Finding this up by taking into account the two cases the positive sign when $I_{S2} > I_{S1}$, and the negative sign when $I_{S2} < I_{S1}$.

$$\frac{I_o}{I_{in}} = (1+\frac{V_{CB}}{V_A}) \times [(1+\frac{1}{\beta_1})(1-\frac{V_{OS}}{V_T})+\frac{1}{\beta_2}]^{-1}$$

$$\frac{I_o}{I_{in}} = (1+\frac{V_{CB}}{V_A}) \times [1+\frac{1}{\beta_1} \pm \frac{V_{OS}}{V_T} \pm \frac{1}{\beta_1}\cdot\frac{V_{OS}}{V_T}+\frac{1}{\beta_2}]^{-1}$$

Since $\frac{V_{OS}}{\beta_1 \cdot V_T} \ll 1$, thus,

$$\frac{I_o}{I_{in}} = (1+\frac{V_{CB}}{V_A}) \times [1+(\frac{1}{\beta_1}+\frac{1}{\beta_2}) \pm \frac{V_{OS}}{V_T}]^{-1}$$

But $|X| << 1$, where $X = (\frac{1}{\beta_1} + \frac{1}{\beta_2}) \pm \frac{V_{OS}}{V_T}$

Using the Binomial expansion with sensible approximations, thus:

$\therefore (1+X)^{-1} \approx (1-X)$

$$\frac{I_o}{I_{in}} = (1 + \frac{V_{CB}}{V_A}) \times [1 - (\frac{1}{\beta_1} + \frac{1}{\beta_2}) \pm \frac{V_{OS}}{V_T}]$$

$$\frac{I_o}{I_{in}} = (1 + \frac{V_{CB}}{V_A} - (\frac{1}{\beta_1} + \frac{1}{\beta_2}) \pm \frac{V_{OS}}{V_T} - \frac{V_{CB}}{V_A} \cdot (\frac{1}{\beta_1} + \frac{1}{\beta_2}) \pm \frac{V_{OS}}{V_T})$$

But since $\frac{V_{CB}}{V_A} \cdot (\frac{1}{\beta_1} + \frac{1}{\beta_2}) \pm \frac{V_{OS}}{V_T} << 1$, therefore,

$$\frac{I_o}{I_{in}} \approx [1 - (\frac{1}{\beta_1} + \frac{1}{\beta_2}) \pm \frac{V_{OS}}{V_T} + \frac{V_{CB}}{V_A}]$$

Since that β_1, and β_2 are usually close it can be concluded that finally β is now an average figure for both β_1, and β_2, and so $\beta_1 = \beta_2 = \beta$.

$$\frac{I_o}{I_{in}} \approx [1 - \frac{2}{\beta} \pm \frac{V_{OS}}{V_T} + \frac{V_{CB}}{V_A}]$$

APP 3.2 PSPICE simulation measurements of I_{C15}, I_{C16}, I_{C17}, I_{C18}, as functions of I_O, for the study of output regulation

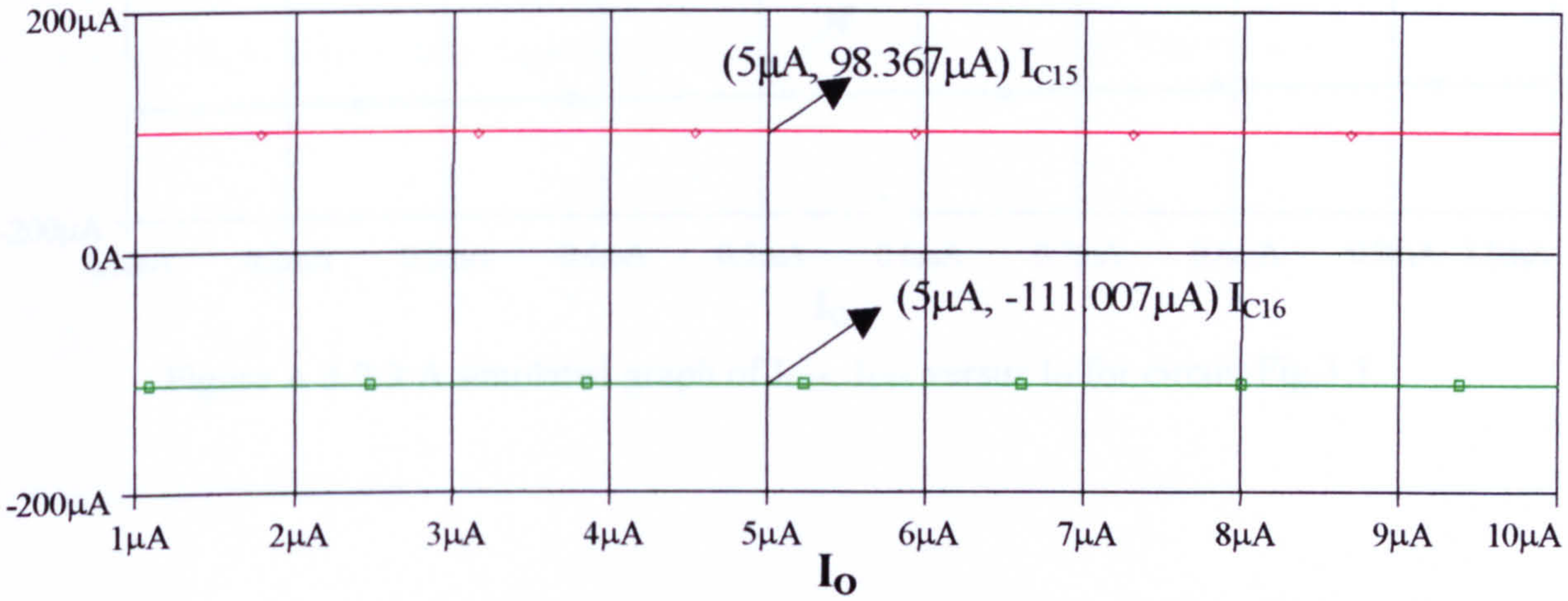


Figure A 3.2.1 A simulated graph of I_{C15}, I_{C16} versus I_O for circuit Fig.3.1

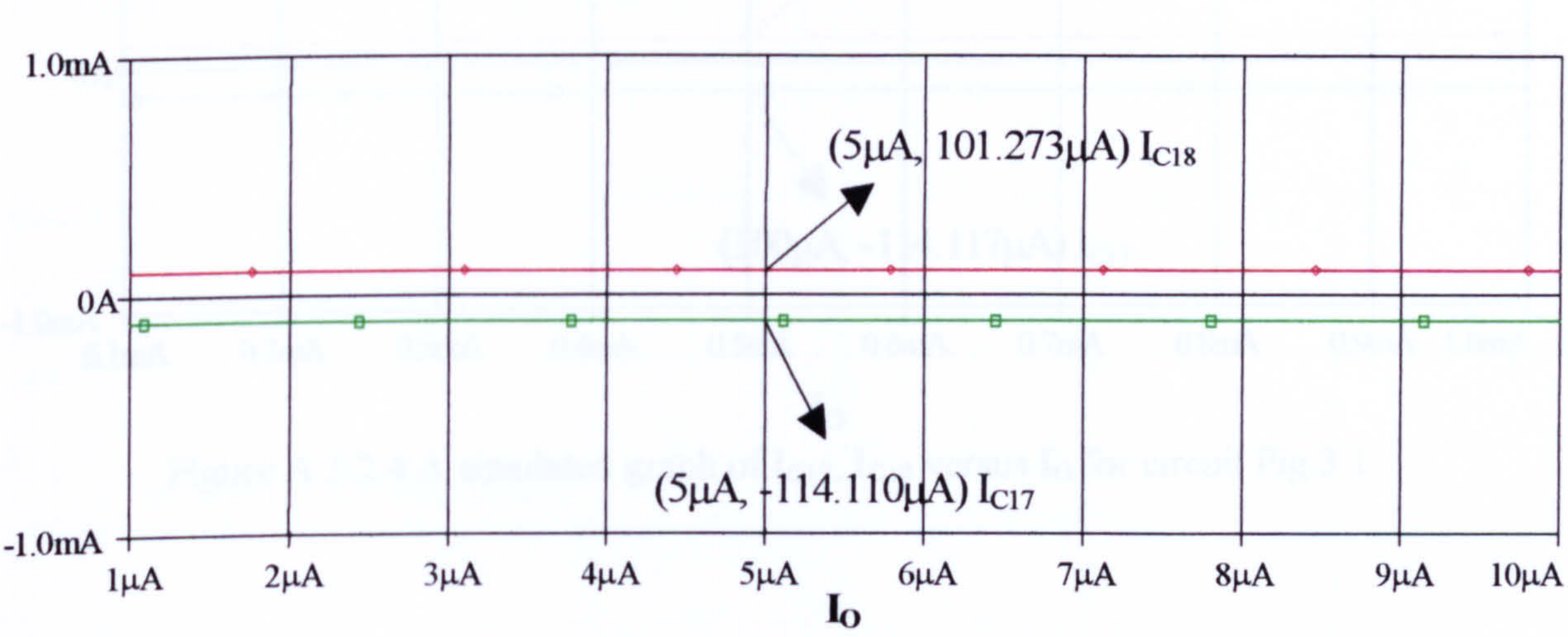


Figure A 3.2.2 A simulated graph of I_{C17}, I_{C18} versus I_O for circuit Fig.3.1

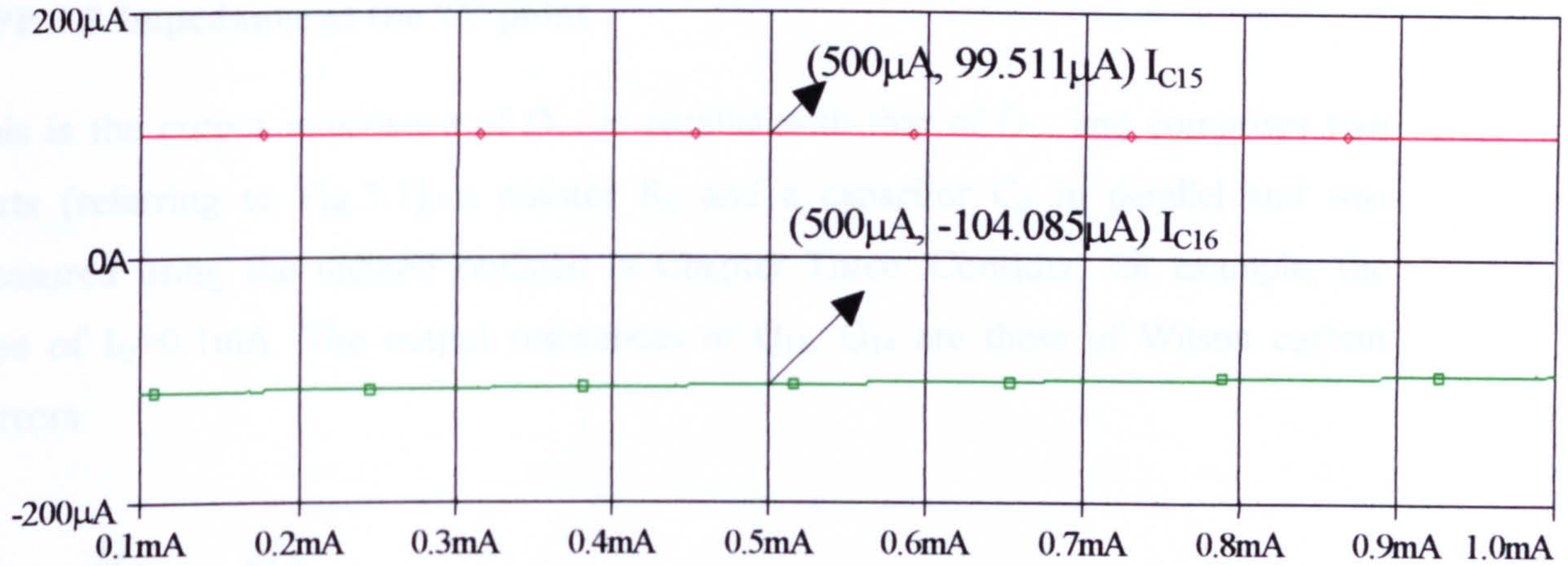


Figure A 3.2.3 A simulated graph of I_{C15}, I_{C16} versus I_O for circuit Fig.3.1

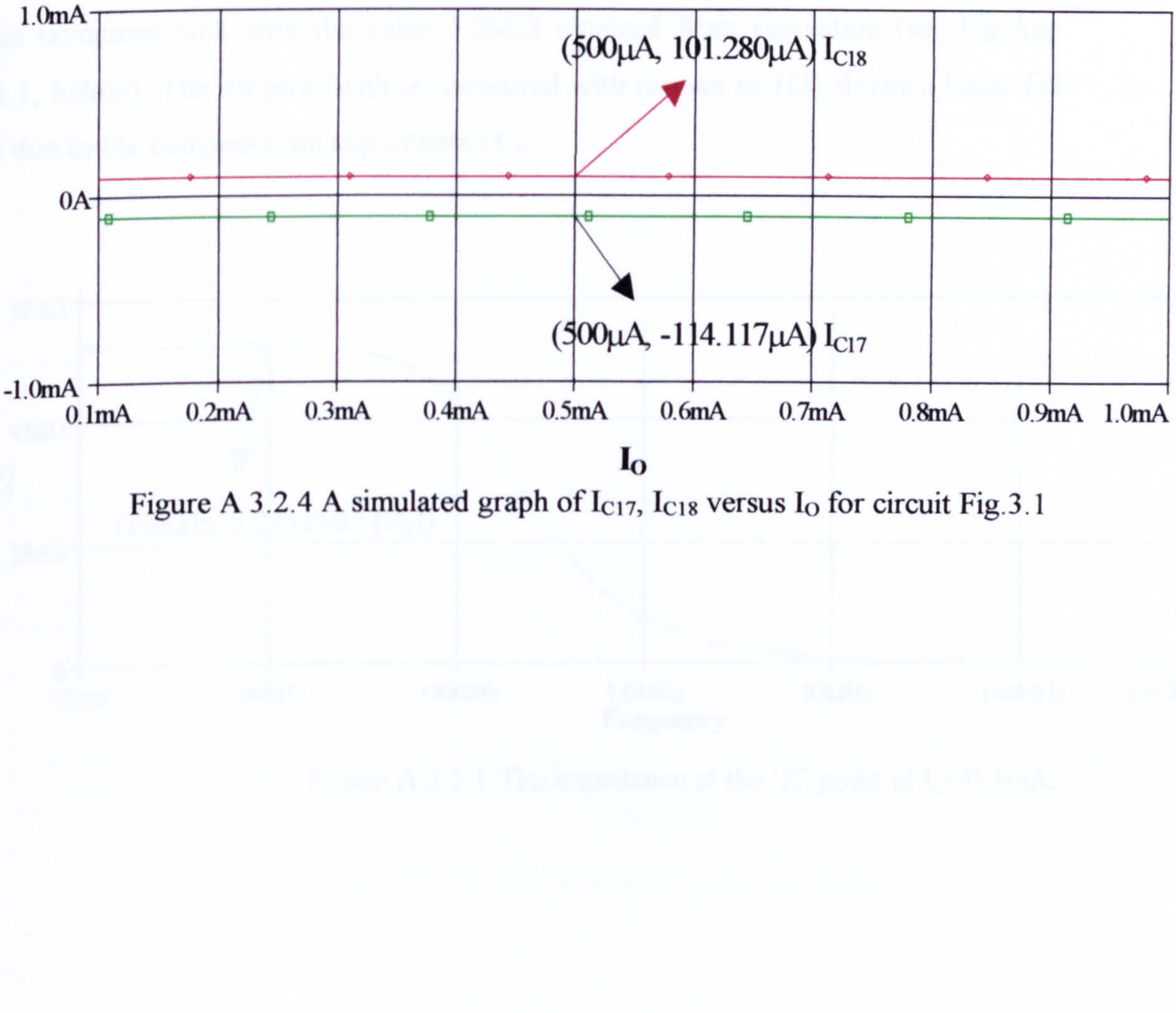


Figure A 3.2.4 A simulated graph of I_{C17}, I_{C18} versus I_O for circuit Fig.3.1

APP 3.3 Impedance at the 'Z' point

This is the output impedance of Q_{11} in parallel with that of Q_{14} and comprises two parts (referring to Fig.3.1), a resistor R_Z and a capacitor C_Z in parallel and was measured using the method outlined in Chapter Three. Consider, for example, the case of I_Q=0.1mA. The output resistances of Q_{11}, Q_{14} are these of Wilson current mirrors.

$$\frac{1}{R_Z} \approx \frac{2I_Q}{\beta_P V_{AP}} + \frac{2I_Q}{\beta_N V_{AN}}$$

Substituting numerical data,

$R_Z \approx 5M\Omega$

This compares well with the value 5.2MΩ obtained from simulation (see Fig.App 3.3.1, below). The dB plot (with |Z| measured with respect to 1Ω) shows a linear fall off due to the compensation capacitances C_c.

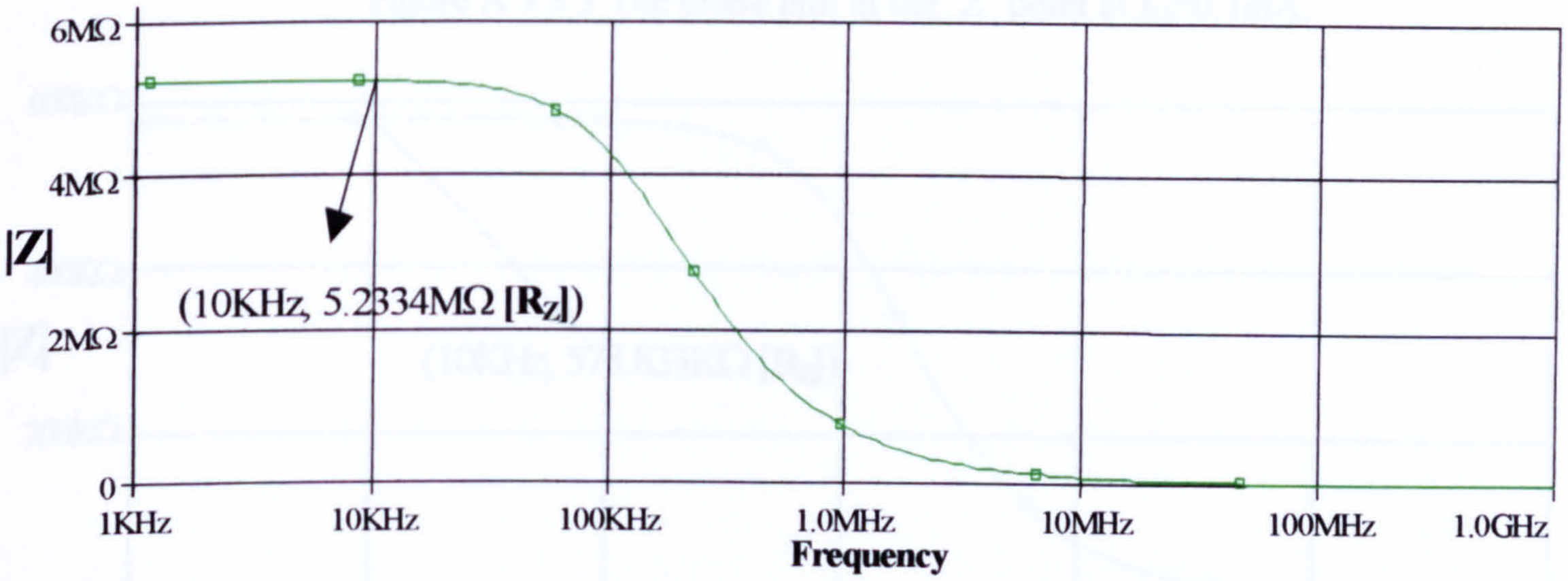


Figure A 3.3.1 The impedance at the 'Z' point at I_Q=0.1mA.

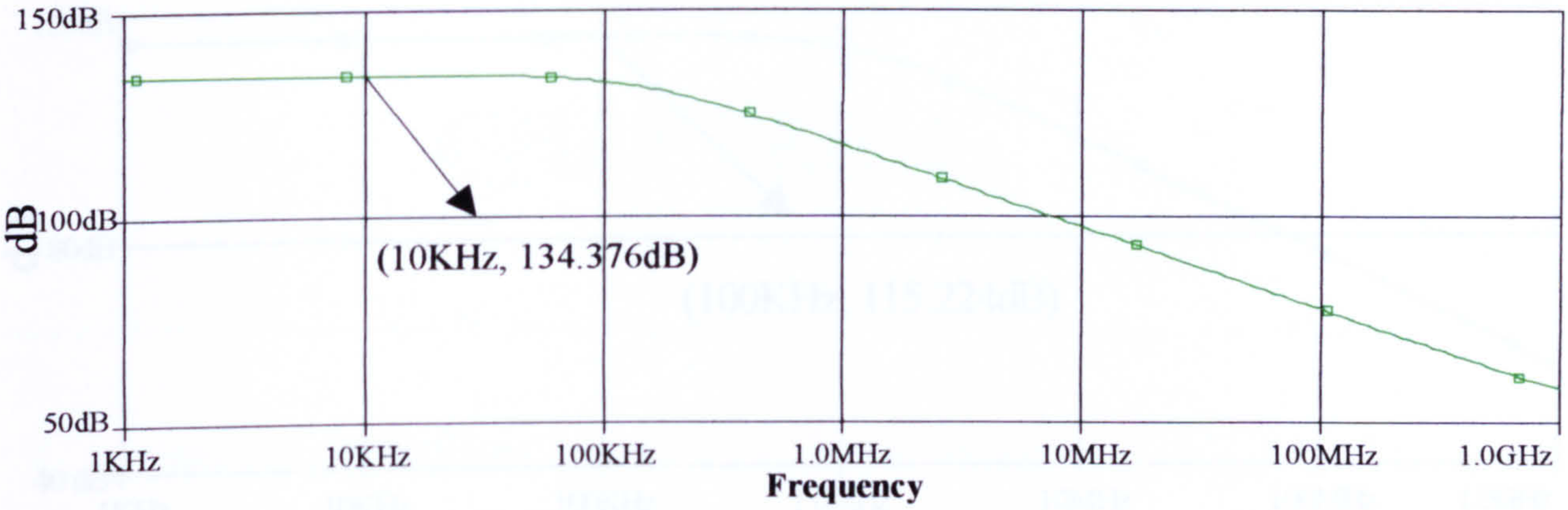


Figure A 3.3.2 The impedance at the 'Z' point in dBs at I_Q=0.1mA.

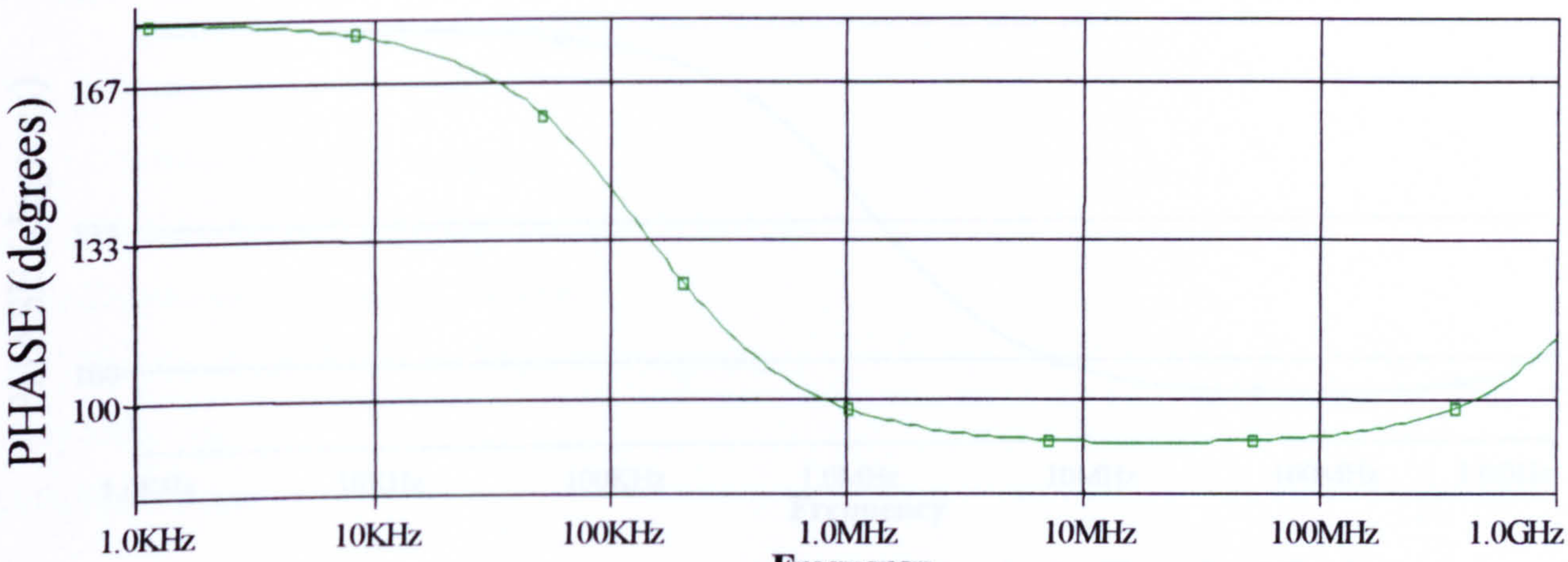


Figure A 3.3.3 The phase plot at the 'Z' point at I_Q=0.1mA.

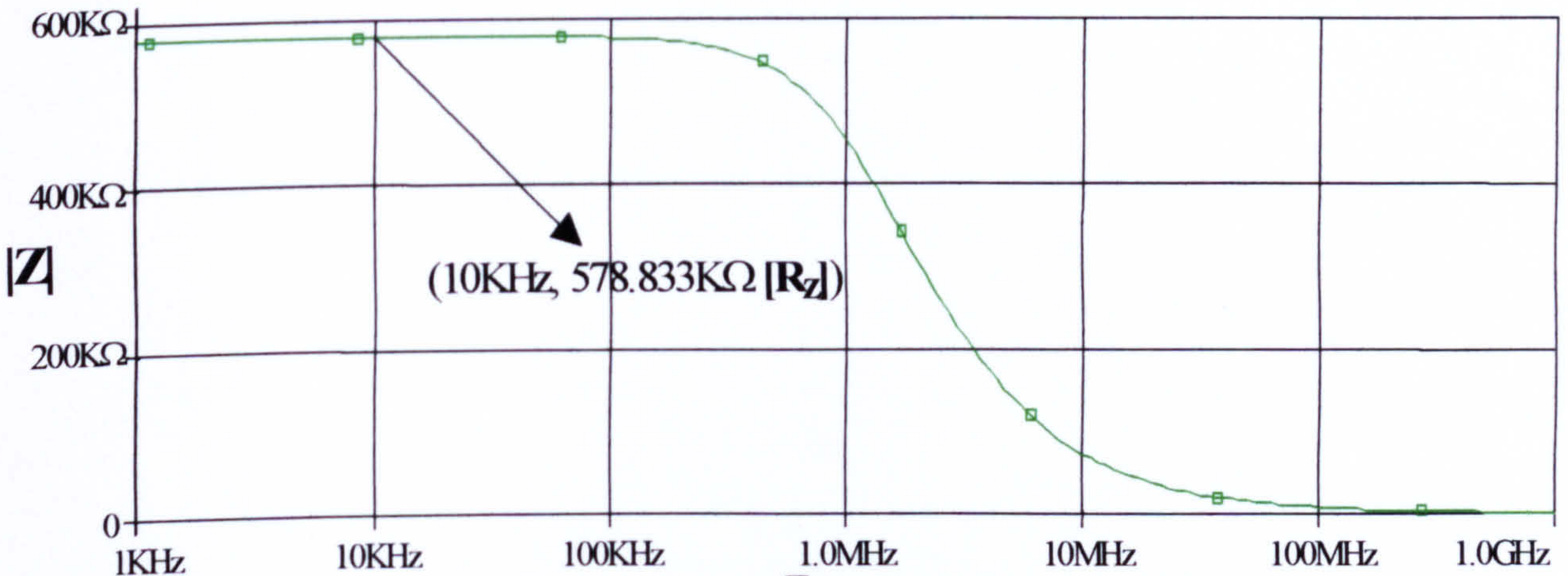


Figure A 3.3.4 The impedance at the 'Z' point at I_Q=0.7mA.

Figure A 3.3.5 The impedance at the 'Z' point in dBs at I_Q=0.7mA.

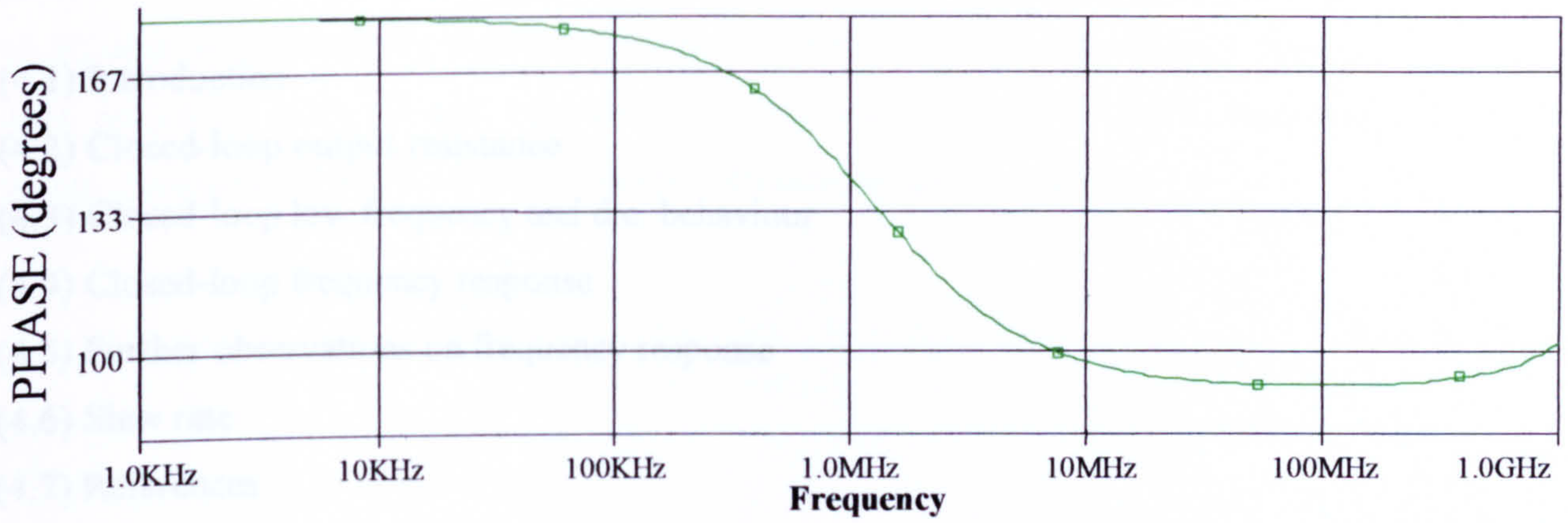


Figure A 3.3.6 The phase plot at the 'Z' point in dBs at I_Q=0.7mA.

CHAPTER 4

Circuit Architecture Of The Basic CFOA: A Critical Review; Part II

(4.1) Introduction

There exist many ways in which the advantages and disadvantages of the CFOA can be studied and understood, but the simplest, and most effective way is arguably to study the design of the CFOA topology.

This chapter continues the work of chapter three by examining the closed-loop performance of the basic CFOA, with particular emphasis on the dynamic response.

It also focuses on the design, performance, and advantages of the CFOA in its ability to provide a substantially constant closed-loop bandwidth for closed-loop voltage gain. Secondly, is the almost unlimited slew–rate due to class AB input stage that makes it superior to the VOA for video and telecommunication systems.

(4.2) Closed-loop output resistance

This section considers the closed-loop output resistance R_O of the CFOA, and its relationship to the open-loop output resistance, r_O.

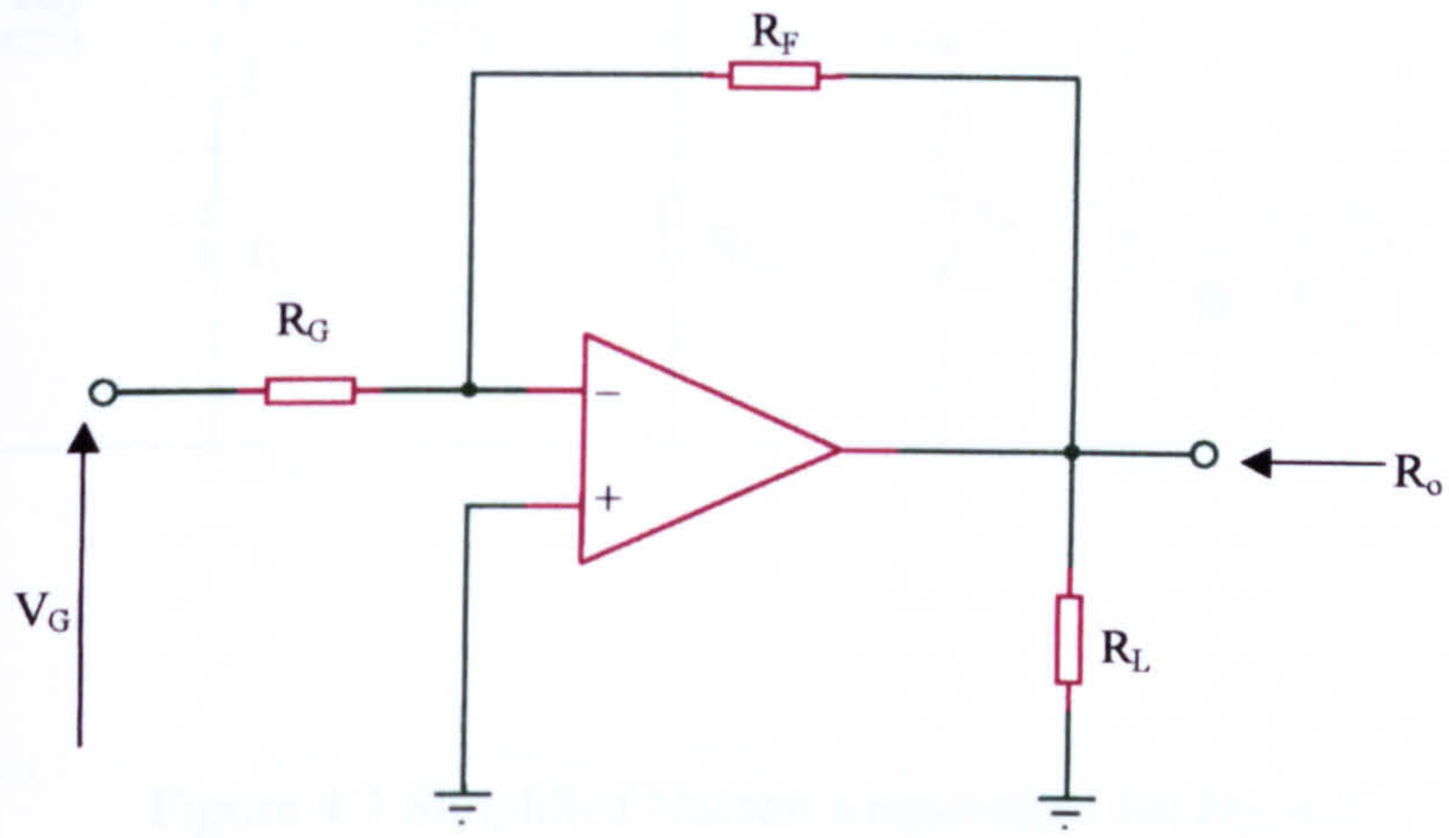


Figure 4.1 CFOA configured as a closed-loop inverting amplifier to calculate output resistance, R_O

By definition,
$R_o = V_o/I_o$

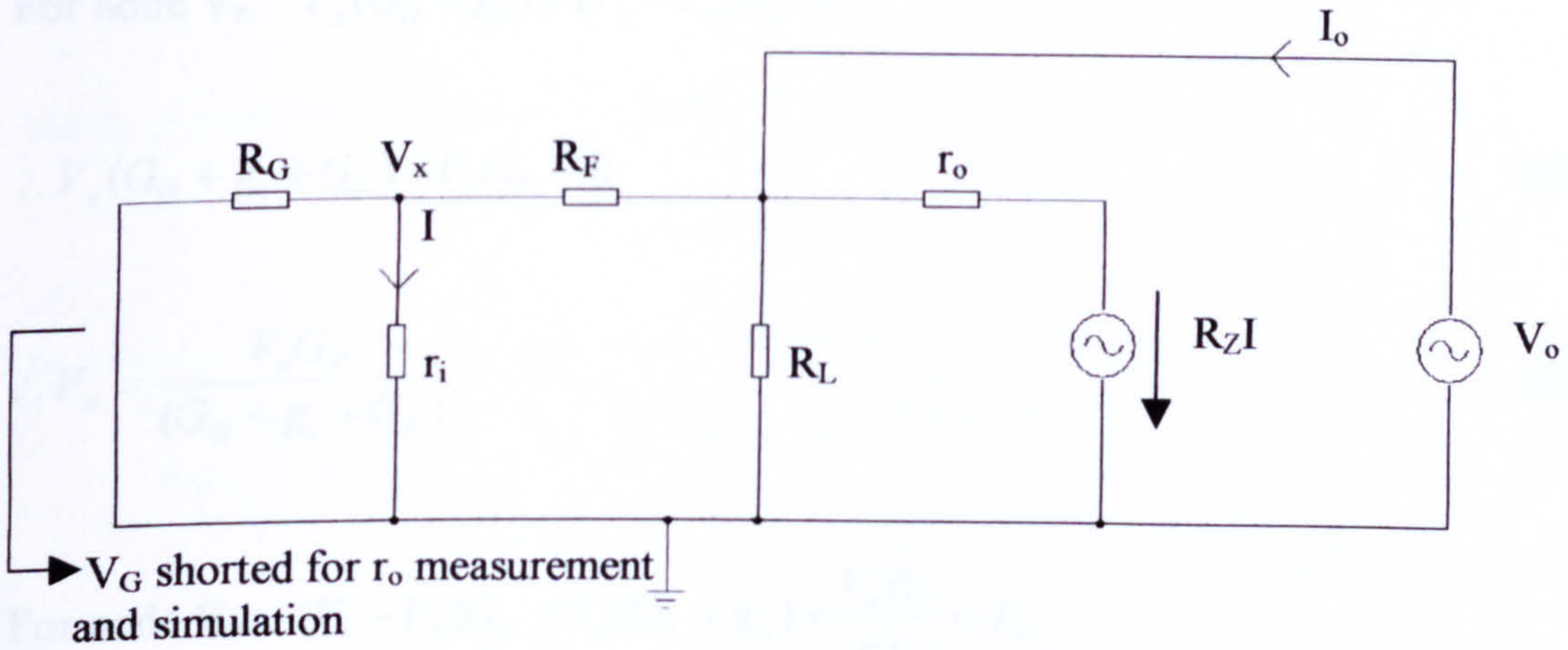


Figure 4.2 The small-signal equivalent circuit for the calculation of CFOA closed-loop output resistance

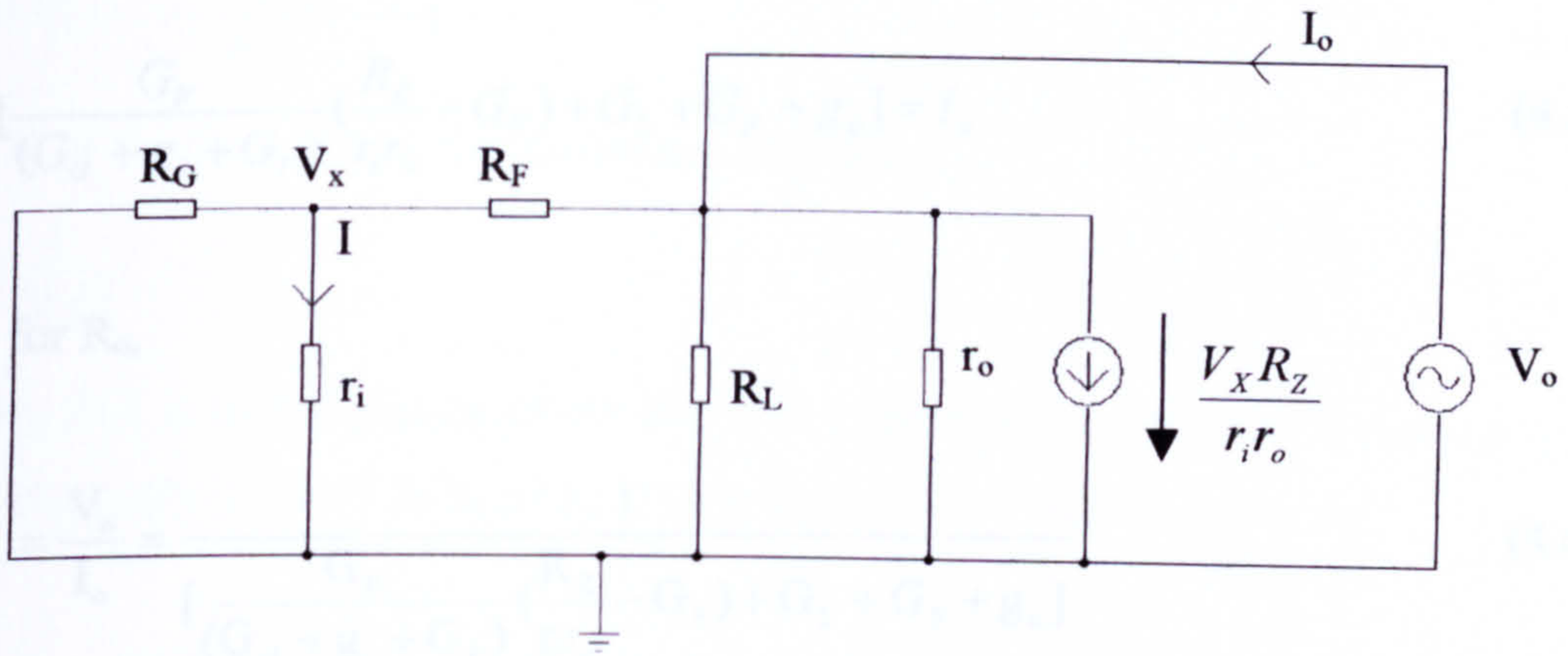


Figure 4.3 Simplified Norton's equivalent for Fig.4.2

Using nodal analysis (to find V_o/I_o) with conductance instead of resistance ($G_G=1/R_G$, etc…)

For node V_x: $V_x(G_G+g_i)+(V_x-V_o)G_F=0$

$$\therefore V_x(G_G+g_i+G_F)-V_oG_F=0 \tag{4.1}$$

$$\therefore V_x=\frac{V_oG_F}{(G_G+g_i+G_F)} \tag{4.2}$$

For node V_o: $(V_o-V_x)G_F+V_o(G_L+g_o)+\frac{V_xR_Z}{r_ir_o}=I_o$

$$\therefore V_x[\frac{R_Z}{r_ir_o}-G_F]+V_o[G_L+G_F+g_o]=I_o \tag{4.3}$$

Substitute equation (4.2) into (4.3), then,

$$\frac{V_o G_F}{(G_G + g_i + G_F)}[\frac{R_Z}{r_i r_o} - G_F] + V_o[G_L + G_F + g_o] = I_o \tag{4.4}$$

$$\therefore V_o[\frac{G_F}{(G_G + g_i + G_F)}(\frac{R_Z}{r_i r_o} - G_F) + G_L + G_F + g_o] = I_o \tag{4.5}$$

Thus for R_o,

$$\therefore R_o = \frac{V_o}{I_o} = \frac{1}{[\frac{G_F}{(G_G + g_i + G_F)}(\frac{R_Z}{r_i r_o} - G_F) + G_L + G_F + g_o]} \tag{4.6}$$

Now rewrite this in terms of resistances instead of conductances to make it easier to follow:

$$R_o = \frac{1}{[\frac{1}{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F})}(\frac{R_Z}{r_i r_o} - \frac{1}{R_F}) + (\frac{1}{R_L} + \frac{1}{R_F} + \frac{1}{r_o})]} \tag{4.7}$$

Since, in practice, $(\frac{R_Z}{r_i r_o}) >> \frac{1}{R_F}$, and

$$R_o \approx \frac{1}{[\frac{1}{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F})}(\frac{R_Z}{r_i r_o})] + (\frac{1}{R_L} + \frac{1}{R_F} + \frac{1}{r_o})} \tag{4.8}$$

From previous simulation, $[\frac{1}{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F})}(\frac{R_Z}{r_i r_o})] >> (\frac{1}{R_L} + \frac{1}{R_F} + \frac{1}{r_o})$, Thus

$$\therefore R_o \approx \frac{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F}) r_i r_o}{R_Z} \tag{4.9}$$

$$R_o \approx r_o[\frac{R_F(1+\frac{r_i}{R_G}+\frac{r_i}{R_F})}{R_Z}] \tag{4.10}$$

This is of the form typical for operational amplifiers,

$$R_o \approx \frac{r_o}{|LG|}$$

where, $|LG|$ is the magnitude of the first-order expression for the low frequency loop gain. Normally $|LG|>>1$ so $R_O<<r_O$. This is borne out by the plot in Fig 4.4:

The slope of Fig 4.4 at a given I_O gives r_O at that I_O. Note that there is normally a small inductive component in the output impedance because of the presence of emitter-followers at the voltage-follower output. This, of course, does not show up in d.c. measurements.

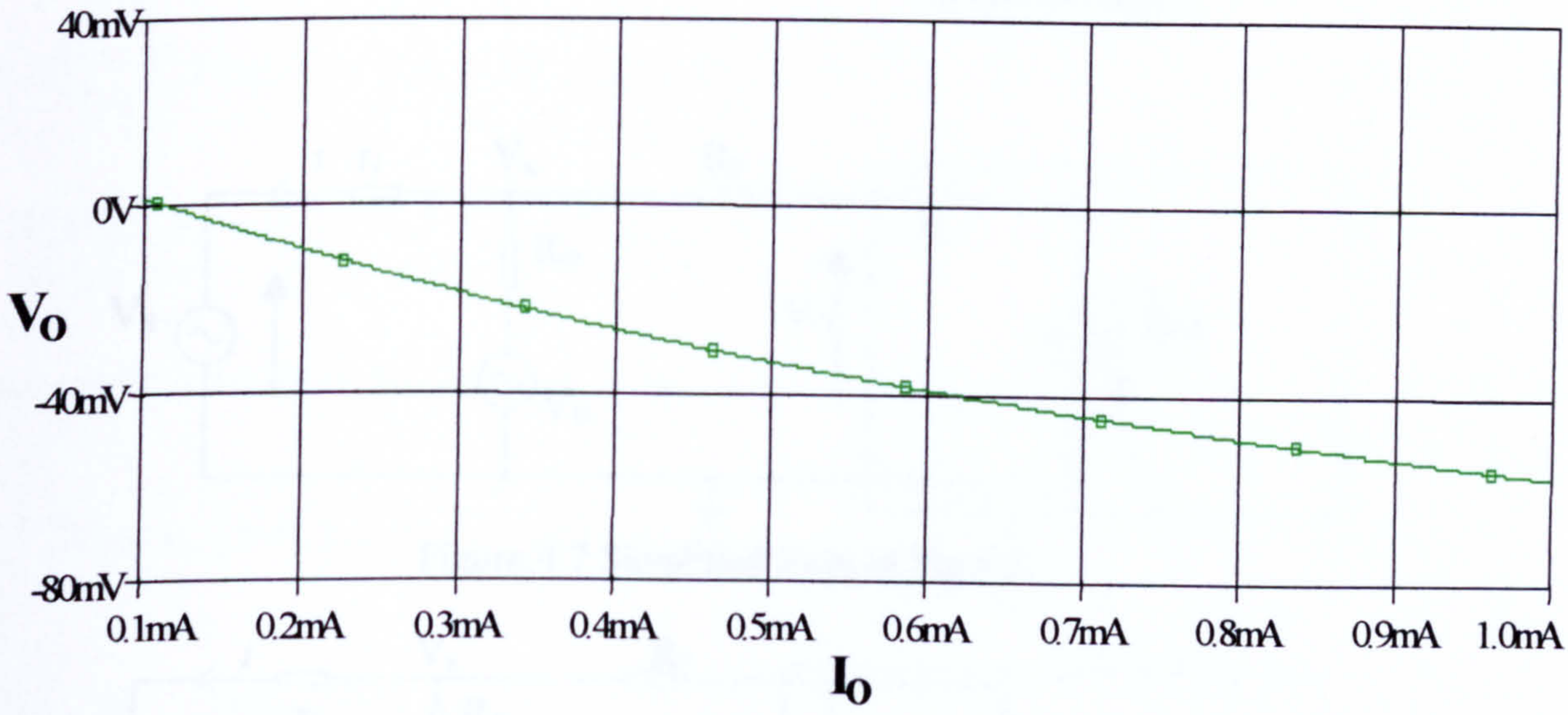


Fig.4.4 The plot of V_O versus I_O for the basic CFOA on closed loop with I_Q=0.1mA

(4.3) Closed-loop low frequency and d.c. behaviour

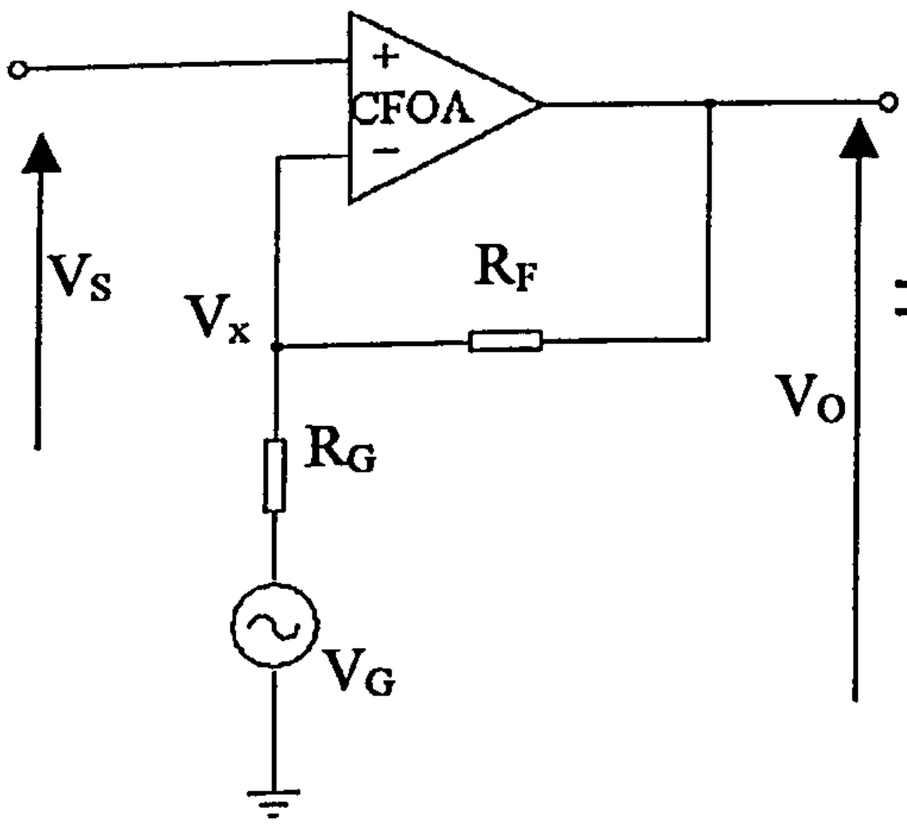


Figure.4.5 General amplifier configuration

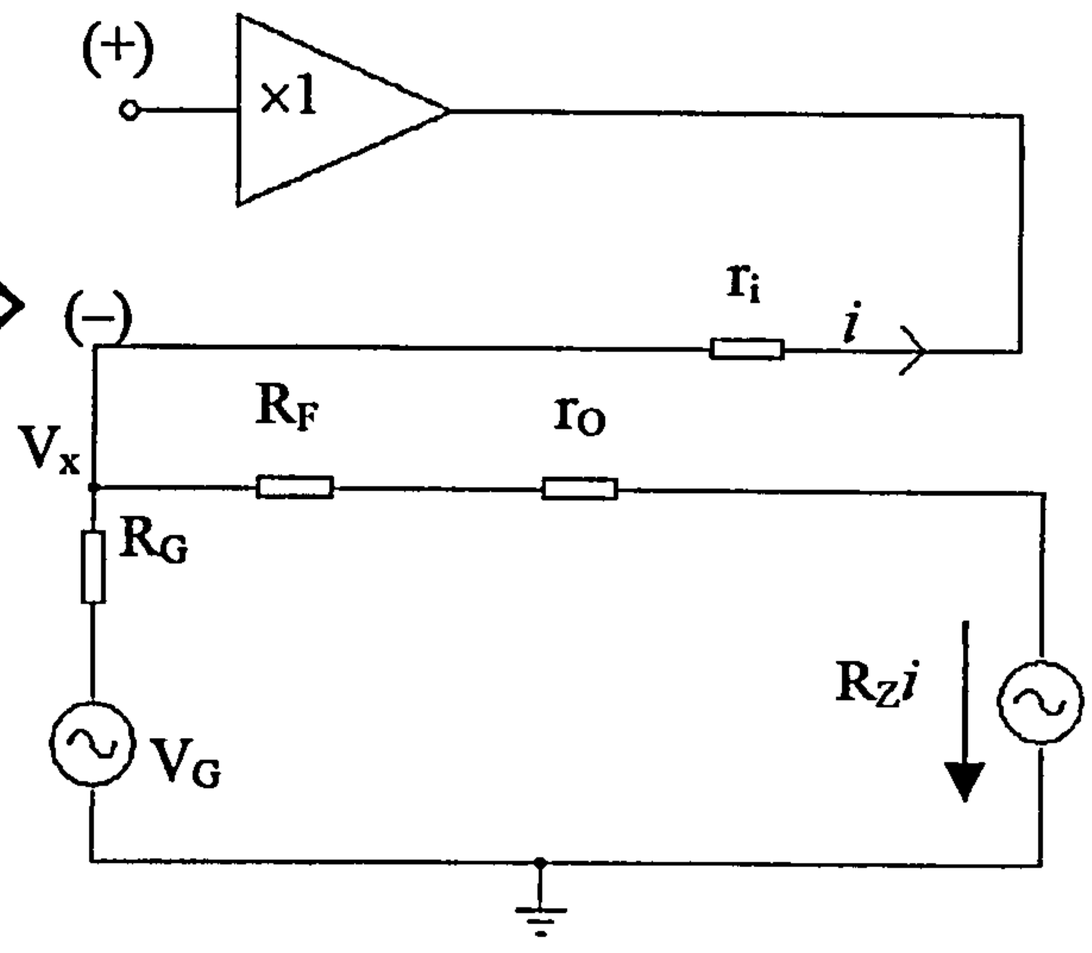


Figure.4.6 Macro-modelling the circuit of Fig.4.5

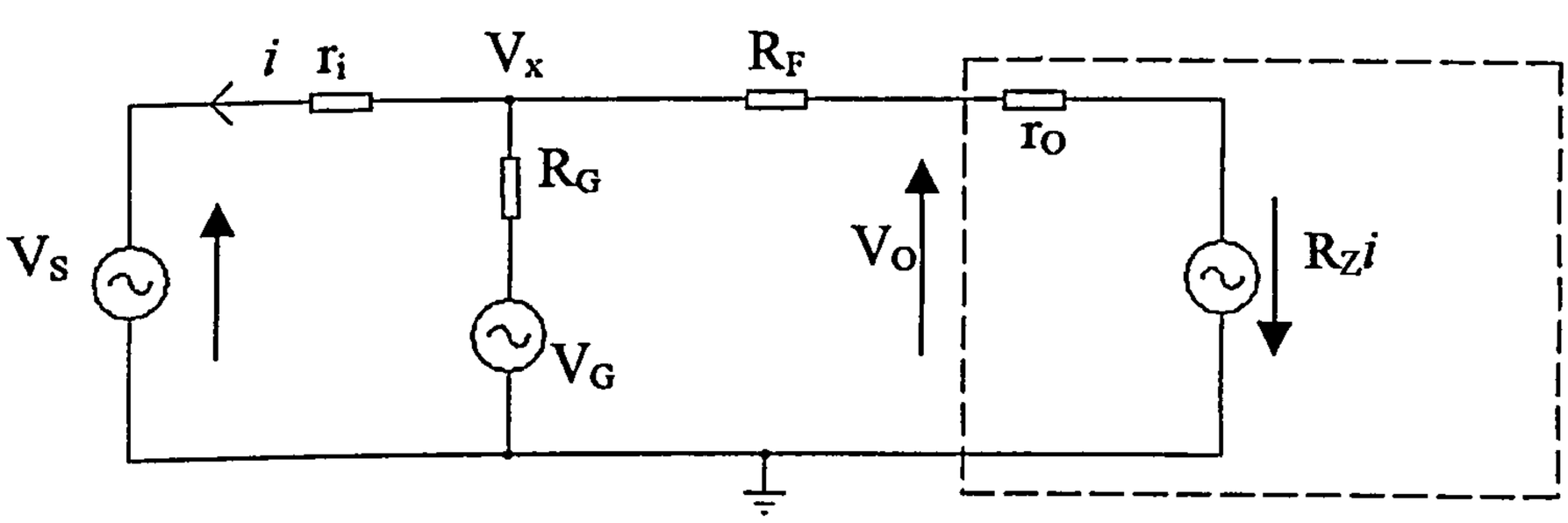


Figure.4.7 Simplified form of Fig.4.6

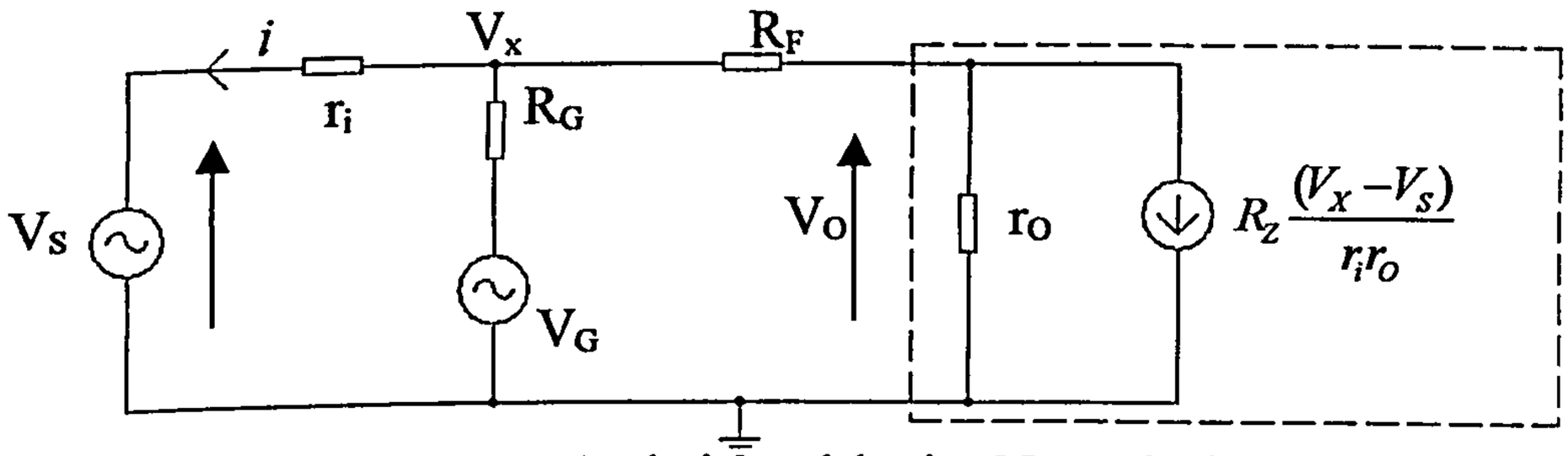


Figure.4.8 Analysis model using Norton's theorem to change ($R_Z i$) to a current generator

Fig.4.5 represents the most general amplifier configuration. Thus:

For V_G=0 it is a non-inverting amplifier, V_S being the input;

for V_S=0 it is an inverting amplifier, V_G being the input;

for $V_S \neq 0$, $V_G \neq 0$ it is a type of differential amplifier;

for V_S=0, $R_G \rightarrow \infty$, $V_G \rightarrow \infty$, but (V_G / R_G) finite, it is an I/V converter;

At node V_x:

$$(V_x - V_S)g_i + (V_x - V_G)g_G + (V_x - V_O)g_F = 0 \qquad (4.11)$$

$$\therefore V_x[g_i + g_G + g_F] = V_O g_F + V_S g_i + V_G g_G \qquad (4.12)$$

At node V_O:

$$g_F(V_O - V_x) + g_O V_O + R_Z g_i g_O (V_x - V_S) = 0 \qquad (4.13)$$

$$\therefore V_x[R_Z g_i g_O - g_F] = R_Z g_i g_O V_S - V_O[g_O + g_F] \qquad (4.14)$$

But, under normal conditions $R_Z g_i g_o >> g_F$

$$\therefore V_x[R_Z g_i g_O] \approx R_Z g_i g_O V_S - V_O[g_O + g_F] \qquad (4.15)$$

$$\therefore V_x = V_S - \frac{V_O[g_O + g_F]}{R_Z g_i g_O} \qquad (4.16)$$

Substitute for V_x from equation (4.16) into equation (4.12).

$$[V_S - \frac{V_O[g_O + g_F]}{R_Z g_i g_O}](g_i + g_G + g_F) = V_O g_F + V_S g_i + V_G g_G \qquad (4.17)$$

$$\therefore -V_O[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)] = -V_S(g_i + g_G + g_F) + V_S g_i + V_G g_G \qquad (4.18)$$

$$\text{or, } V_O[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)] = V_S(g_G + g_F) - V_G g_G \qquad (4.19)$$

$$\therefore V_O = V_S[\frac{(g_G + g_F)}{[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)]}] - V_G[\frac{g_G}{[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)]}] \qquad (4.20)$$

Now by converting into resistance from conductances, then,

$$V_O = V_S[\frac{(\frac{1}{R_G} + \frac{1}{R_F})}{[\frac{1}{R_F} + \frac{(\frac{1}{r_O} + \frac{1}{R_F})}{R_Z} r_i r_O(\frac{1}{r_i} + \frac{1}{R_G} + \frac{1}{R_F})]}] - V_G[\frac{\frac{1}{R_G}}{[\frac{1}{R_F} + \frac{(\frac{1}{r_O} + \frac{1}{R_F})}{R_Z} r_i r_O(\frac{1}{r_i} + \frac{1}{R_G} + \frac{1}{R_F})]}] \qquad (4.21)$$

Multiply the numerator and the denominator by ($R_F R_G$),

$$V_O = V_S[\frac{(R_F + R_G)}{R_G[1 + \frac{(R_F + r_O)}{R_Z}\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\}]}] - V_G[\frac{R_F}{R_G[1 + \frac{(R_F + r_O)}{R_Z}\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\}]}] \qquad (4.22)$$

$$V_O = V_S[\frac{R_F + R_G}{R_G}][\frac{1}{1 + \left|\frac{1}{LG}\right|}] - V_G[\frac{R_F}{R_G}][\frac{1}{1 + \left|\frac{1}{LG}\right|}] \qquad (4.23)$$

where, by analogy with the conventional voltage feedback operational amplifier, $|LG|$ is the magnitude of the loop-gain (but in this case current loop-gain rather than voltage loop-gain)

$$|LG| = \frac{R_Z}{(R_F + r_O)[1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})]} \tag{4.24}$$

Having $r_i \geq 0$ and $r_O \geq 0$ means a reduced loop gain over that assumed in the conventional first-order treatments of the CFOA in which,

$$|LG| = \frac{R_Z}{R_F} \tag{4.25}$$

An interpretation of this is obtained by making V_S=0 and inserting a test current I at the inverting input.

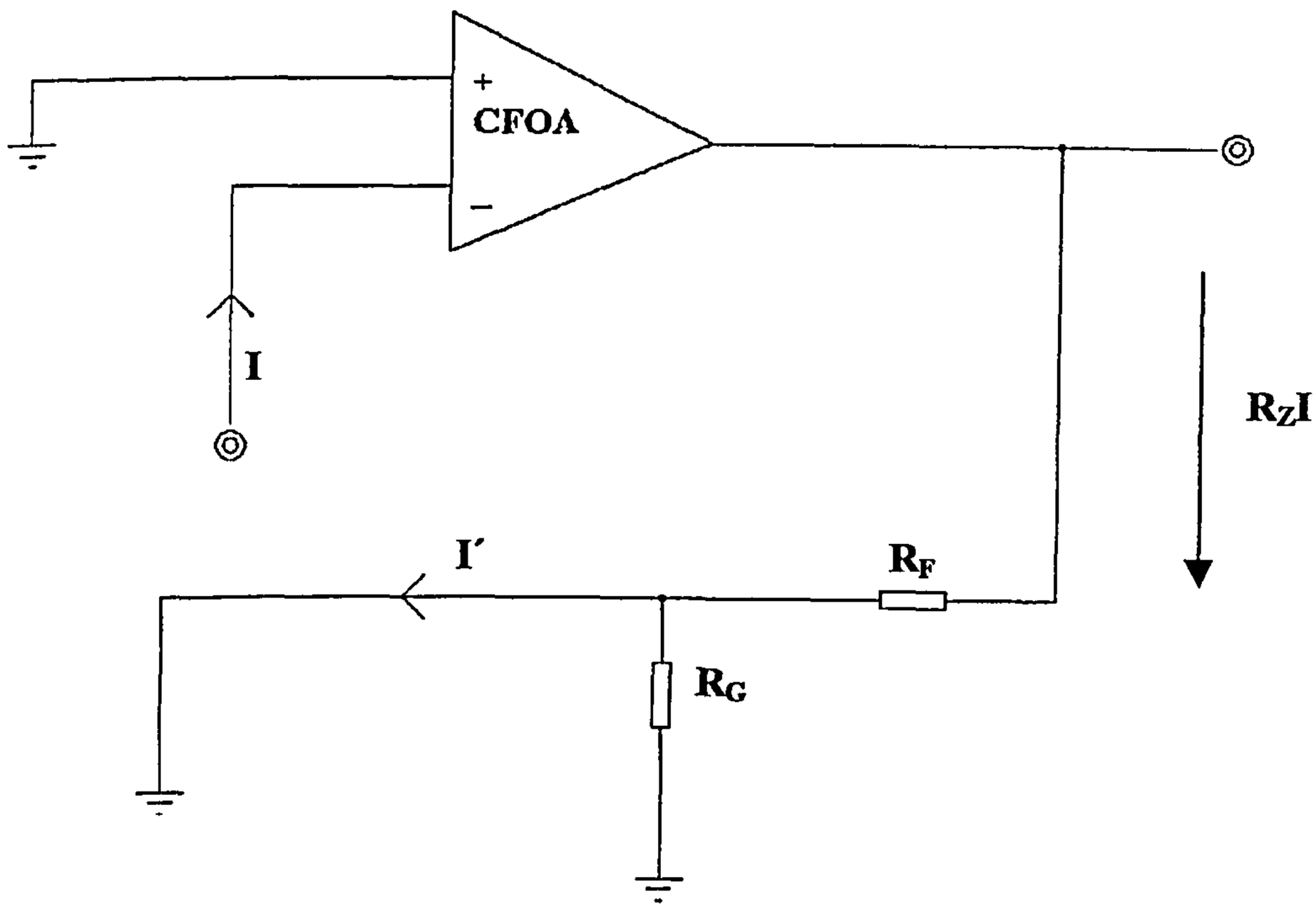


Figure.4.9 Model for CFOA voltage offset

$$|LG| = \left|\frac{I'}{I}\right| = \left|-\frac{IR_Z}{R_F} \cdot \frac{1}{I}\right| = \frac{R_Z}{R_F} \tag{4.26}$$

The analysis so far applies to a.c. inputs but can also apply to d.c. offset voltage. This is taken into account by making V_G=0, and inserting V_S=V_{OS}

Then, $V_O = \pm V_{os}(\frac{R_F + R_G}{R_G})$ (4.27)

The ± signs take with account the uncertainty in the direction of V_{os}. The general equation (4.23), with the assumption $|LG| >> 1$, leads to two familiar results:

1. $V_O = V_S \frac{(R_F + R_G)}{R_G}$ for $V_G=0$ (4.28)

This correspond to the non-inverting mode (Fig.10)

2. $V_O = -V_G \frac{R_F}{R_G}$ for $V_S=0$ (4.29)

This correspond to the inverting mode (Fig.11)

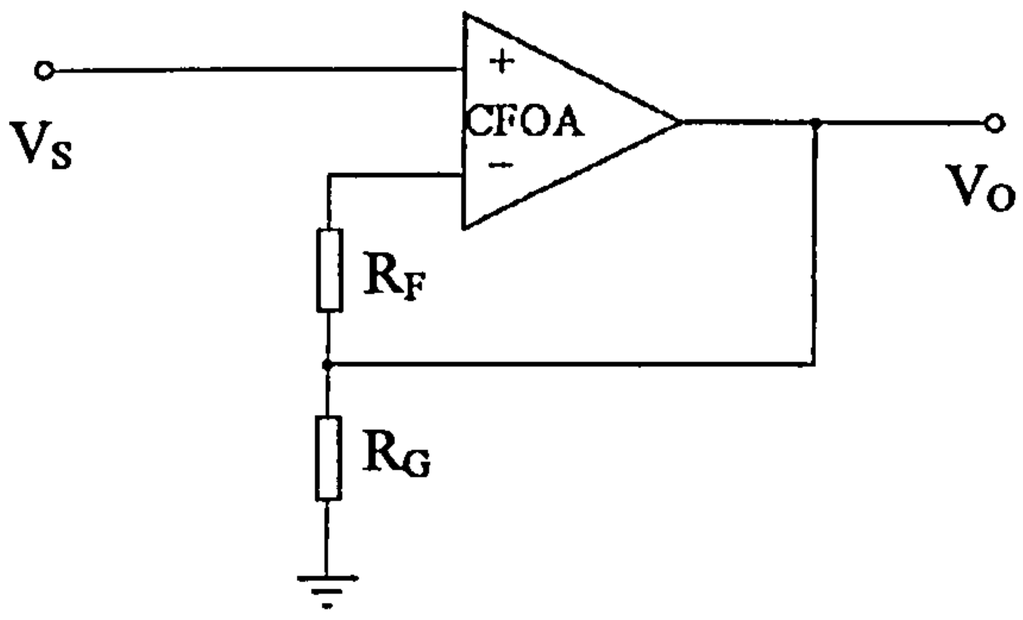


Figure.4.10 Non-inverting configuration representing equation (4.28)

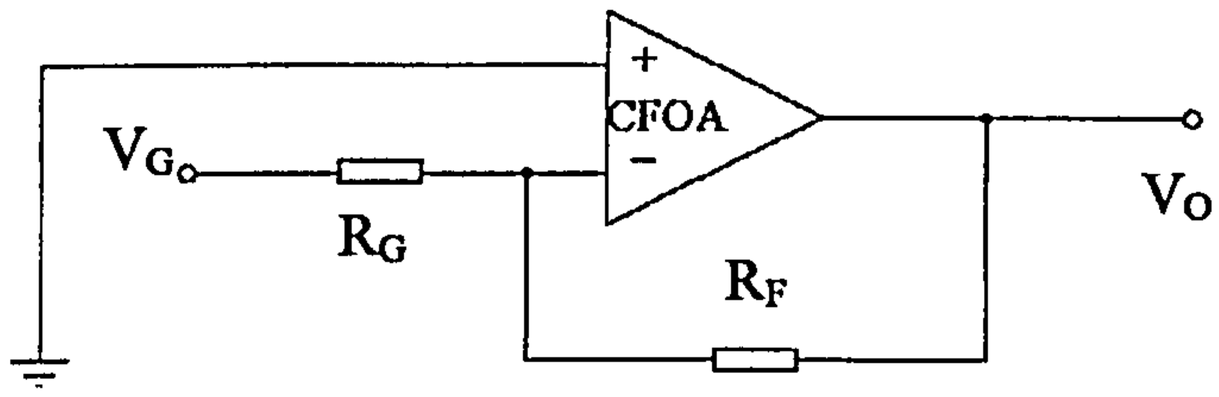


Figure.4.11 Inverting configuration representing equation (4.29)

However, there is also another result which is obtained by putting $V_S=0$, and making V_G and R_G very large, but finite, so $I_{in}=(V_G/R_G)$. Then,

$V_O \approx -I_{in} R_F$ (4.30)

This is the case of the I/V converter.

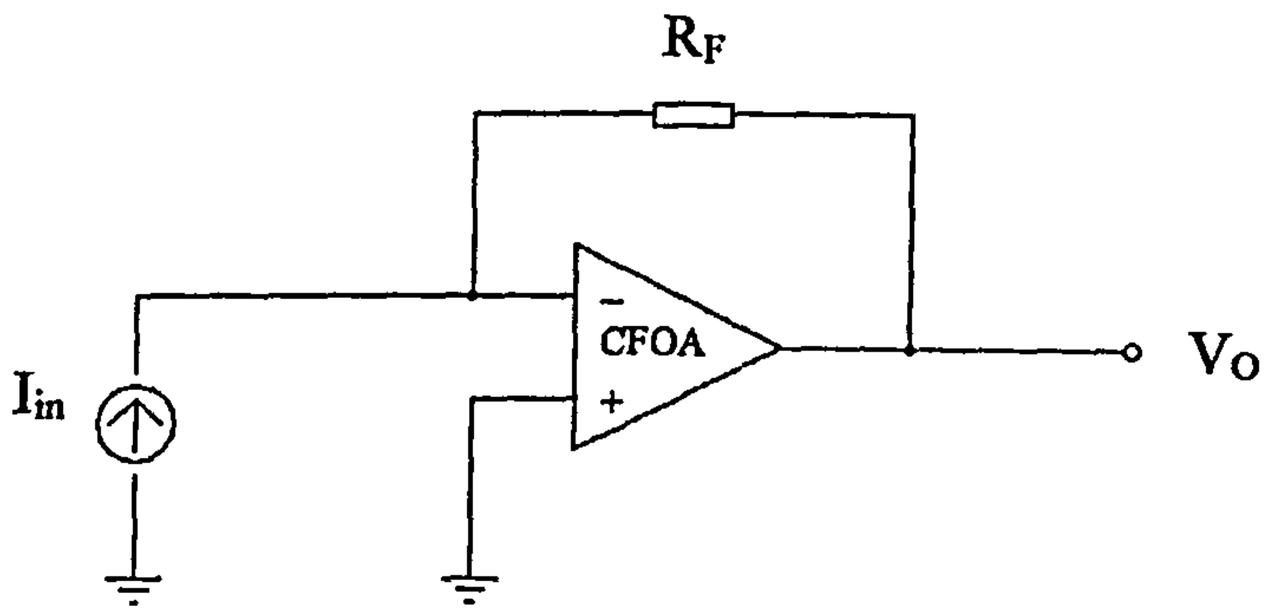


Figure.4.12 (I/V) circuit configuration representing equation (4.30)

(4.4) Closed-loop frequency response

The general expression for CFOA closed-loop amplifier response is,

$$A(o) = \frac{Ideal\ \ gain}{[1 + \frac{(R_F + r_O)}{R_Z}\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}]} \tag{4.31}$$

This is for low frequencies: to determine the frequency response we must replace $(1/R_Z)$ by the $(\frac{1}{R_z} + sC_z)$ where s is the complex frequency variable (this assumes all other parameters are frequency-independent: this assumption is examined, further, later) then, the expression,

$$[1 + \frac{R_F + r_O}{R_Z}\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}] \tag{4.32}$$

becomes,

$$[1 + (R_F + r_O)[\frac{1}{R_Z} + sC_Z]\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}] \tag{4.33}$$

or,

$$[1 + (\frac{R_F + r_O}{R_Z})\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}] + (R_F + r_O)sC_Z\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}] \tag{4.34}$$

Hence,

$$A(s)=\frac{Ideal\ gain}{[1+\frac{R_F+r_O}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]\left[1+\frac{(R_F+r_O)sC_Z[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]}{[1+\frac{R_F+r_O}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]}\right]} \tag{4.35}$$

$$A(s)=\frac{A(o)}{1+\frac{(R_F+r_O)sC_Z[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]}{[1+\frac{R_F+r_O}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]}} \tag{4.36}$$

For the usual case $(R_F+r_O)<<R_Z$ it is legitimate to approximate this to,

$$A(s)=\frac{A(o)}{1+s(R_F+r_O)C_Z[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]} \tag{4.37}$$

or, in the frequency domain,

$$A(j\omega)=\frac{A(o)}{1+j\omega C_Z(R_F+r_O)[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]} \tag{4.38}$$

The (–3dB) cut off frequency occurs when the coefficient of j is unity, i.e. at a frequency f_c given by

$$f_C=\frac{1}{2\pi C_Z(R_F+r_O)[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]} \tag{4.39}$$

For the simplest case, assumed in first order treatments, r_O=0, r_i=0, then,

$$f_C = \frac{1}{2\pi R_F C_Z} \tag{4.40}$$

However this is only an approximation because, even if r_i is neglected (as r_i<<R_G//R_F), r_O cannot be neglected since it may be comparable with R_F for 'low' values of R_F.

$$f_C = \frac{1}{2\pi(R_F + r_O)C_Z} \tag{4.41}$$

The effect of finite r_i is to reduce the bandwidth to f_c'. The amount of reduction depends on R_G (for a fixed R_F)

$$f_C' = \frac{f_C}{[1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})]} \tag{4.42}$$

To investigate the effect of r_O a simulation SPICE test was carried out using the set-up in Fig.4.13, in which R_A is an added resistor and the boxed section now represents the modified CFOA. For this arrangement equation (4.39) should apply with r_O replaced by ($r_O + R_A$).

In the test V_S=100μV (peak) sinusoidal signal. Fig.4.14, 4.15, 4.16, 4.17, show the frequency response for gain magnitude for values of R_A (0, 150Ω, 1KΩ, –150Ω). To discuss these further we can re-write equation (4.39) as,

$$f_C = \frac{K}{(R_F + r_O + R_A)} \tag{4.43}$$

where K is a constant,

The effective value of r_O can be found by substituting data from Fig.4.14 (f_C=17.2MHz, R_A=0) and Fig.4.16 (f_C=9.2MHz, R_A=1KΩ): this gives r_O=0.15KΩ.

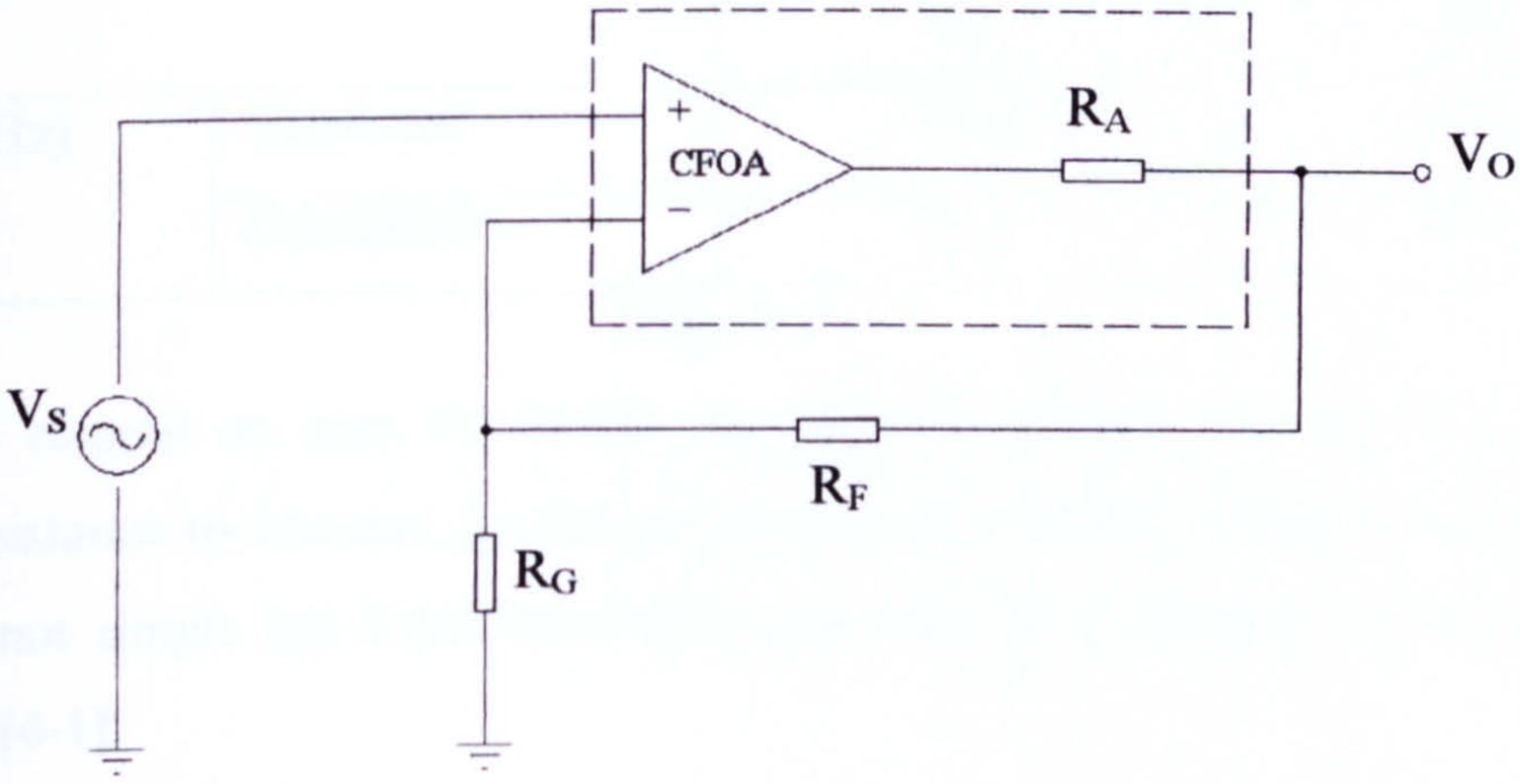


Figure.4.13 Set-up for investigating the effect of r_O on bandwidth

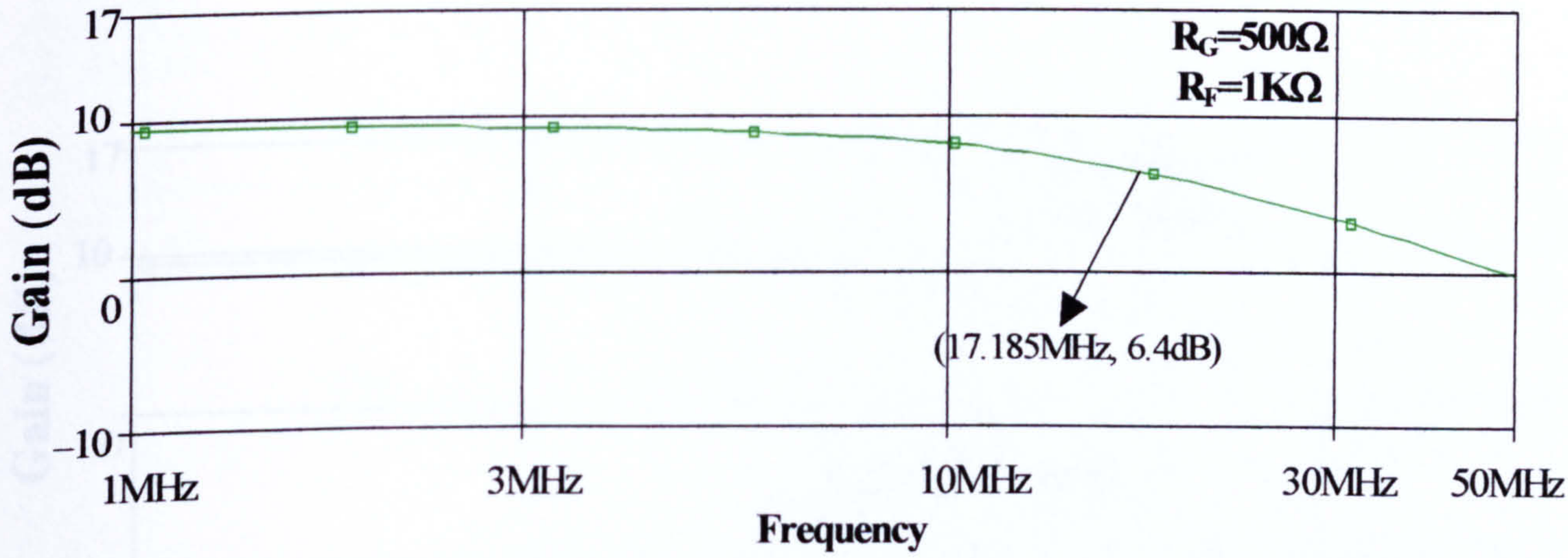


Figure.4.14 CFOA (Bandwidth ~ Frequency) for R_A=0

Using this value of r_O and the f_C, (R_A=0) of Fig.4.17 the f_C was calculated for

a) R_A=150Ω

b) R_A= −150Ω

The calculated results displayed in Table 4.1 are in good agreement with the simulated values.

		$R_A(\Omega)$	
		(a)	(b)
f_C (MHz)	Simulated	15.2	20.6
	Calculated	15.3	19.8

Table 4.1

The results suggest an area for further investigation, namely the use of a floating negative resistance to increase f_C. The production of a floating negative resistance in practice is not simple but it has been done and used in the design of precision V/I conversion **[4-1]**.

Note that R_A has little effect on gain magnitude. This to be expected since r_O in equation (4.39) only affects a small correction term in the expression for gain magnitude (whereas it has a direct effect on f_C)

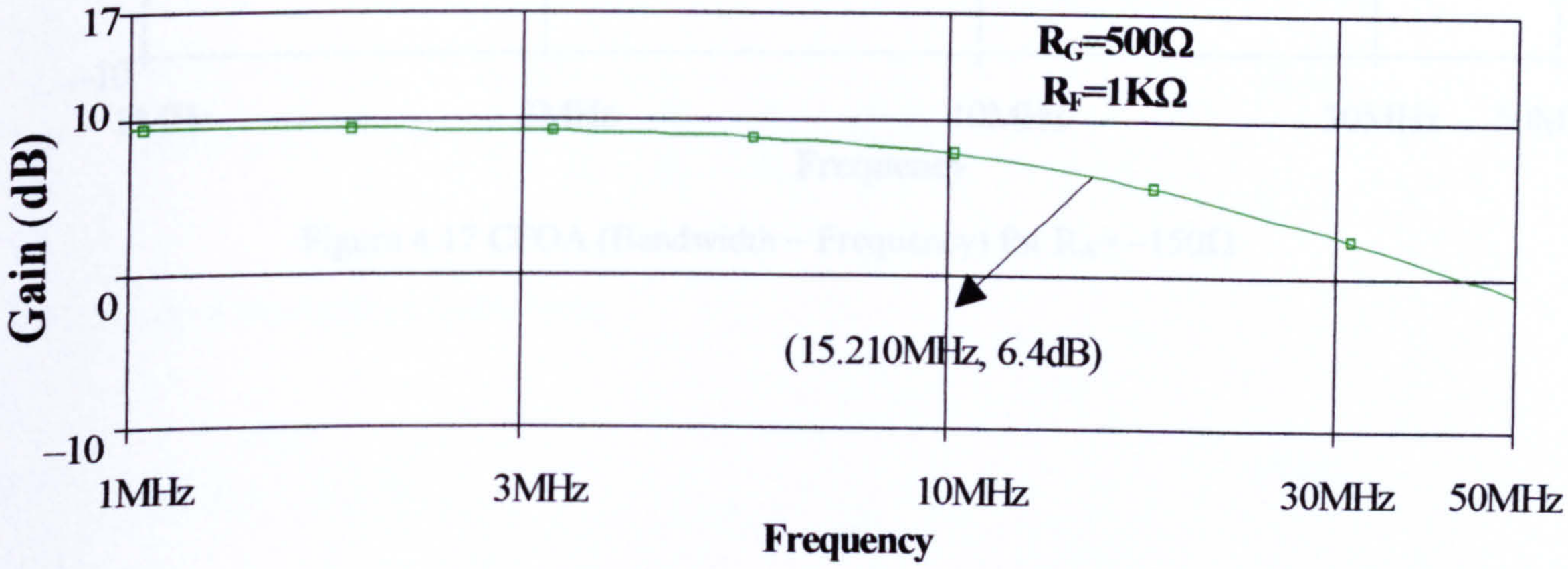


Figure.4.15 CFOA (Bandwidth ~ Frequency) for R_A=150Ω

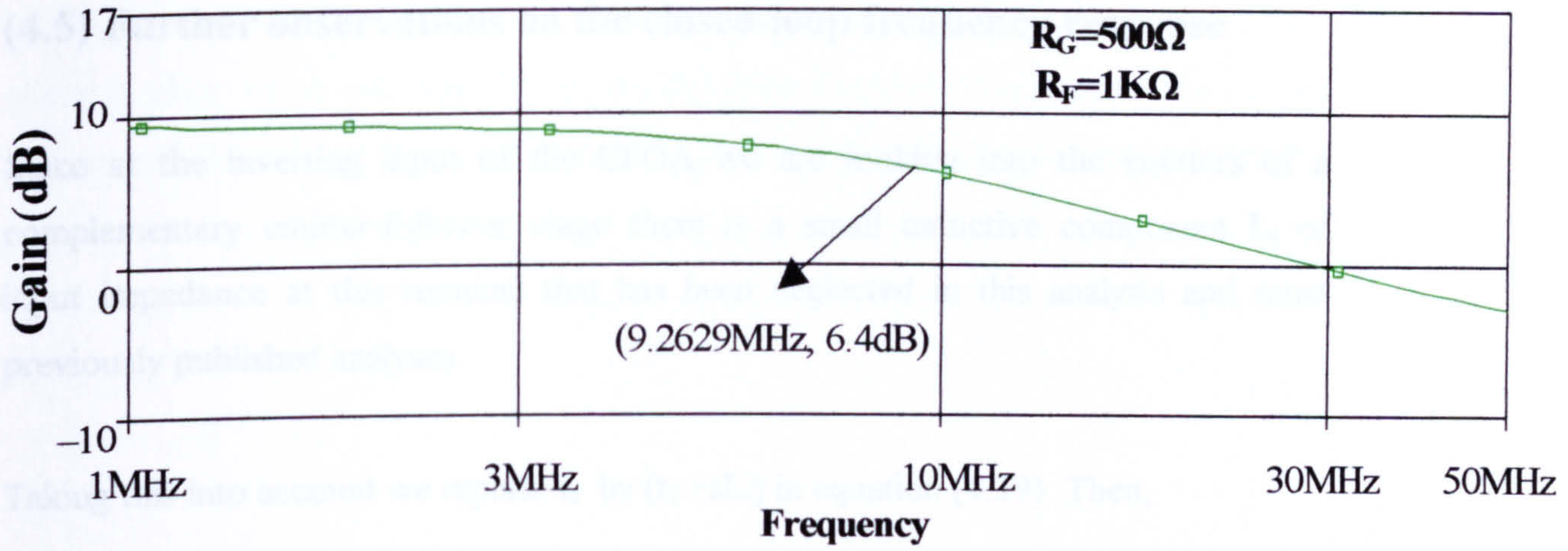


Figure.4.16 CFOA (Bandwidth ~ Frequency) for R_A= R_F=1KΩ

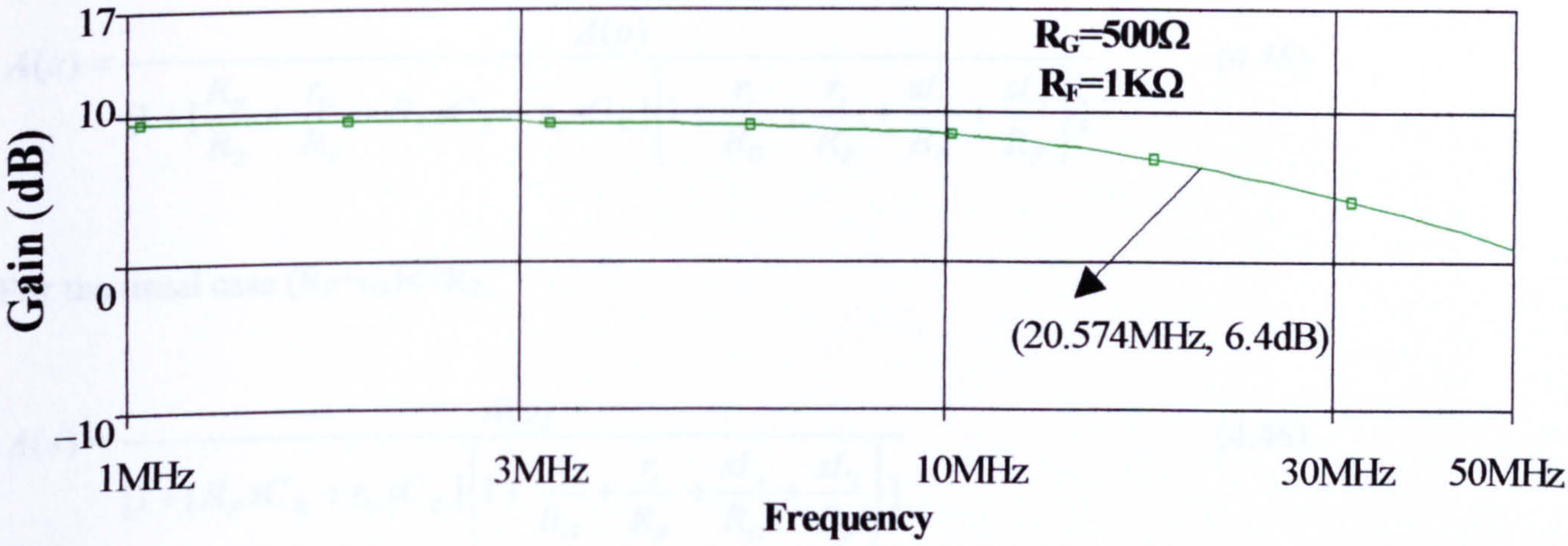


Figure.4.17 CFOA (Bandwidth ~ Frequency) for R_A= –150Ω

(4.5) Further observations on the closed-loop frequency response

Since at the inverting input of the CFOA we are looking into the emitters of a complementary emitter-follower stage there is a small inductive component L_i of input impedance at this terminal that has been neglected in this analysis and most previously published analyses.

Taking this into account we replace r_i by $(r_i + sL_i)$ in equation (4.39). Then,

$$A(s) = \frac{A(o)}{[1 + (R_F + r_O)[\frac{1}{R_Z} + sC_Z]\left\{1 + [r_i + sL_i](\frac{1}{R_G} + \frac{1}{R_F})\right\}]} \tag{4.44}$$

$$A(s) = \frac{A(o)}{[1 + [\frac{R_F}{R_Z} + \frac{r_O}{R_Z} + R_F sC_Z + r_O sC_Z]\left\{1 + \frac{r_i}{R_G} + \frac{r_i}{R_F} + \frac{sL_i}{R_G} + \frac{sL_i}{R_F}\right\}]} \tag{4.45}$$

For the usual case $(R_F + r_O) << R_Z$,

$$A(s) \approx \frac{A(o)}{[1 + [R_F sC_Z + r_O sC_Z]\left\{1 + \frac{r_i}{R_G} + \frac{r_i}{R_F} + \frac{sL_i}{R_G} + \frac{sL_i}{R_F}\right\}]} \tag{4.46}$$

By inspection this reduces to the form,

$$A(s) = \frac{A(o)}{[1 + X_1 s + X_2 s^2]} \tag{4.47}$$

X1, X2 being parameter groupings.

In the frequency domain,

$$A(j\omega) = \frac{A(o)}{[1 + j\omega X_1 + j^2 \omega^2 X_2]} \tag{4.48}$$

It is apparent that the ω^2 term can contribute to peaking in the frequency response which is observed in practice. Of course, the finite frequency response of the current mirrors and the voltage followers, also so far ignored, complicates the matter further.

(4.6) Slew rate

Rise time usually refers to the time it takes for a voltage or current to rise from 10% to 90% of its peak value, and generally this is measured before the onset of large signal limiting due to slew rate. Slew rate limiting is a phenomena generally due to current limitations feeding a key nodal capacitance and is effectively a disconnect between input and output.

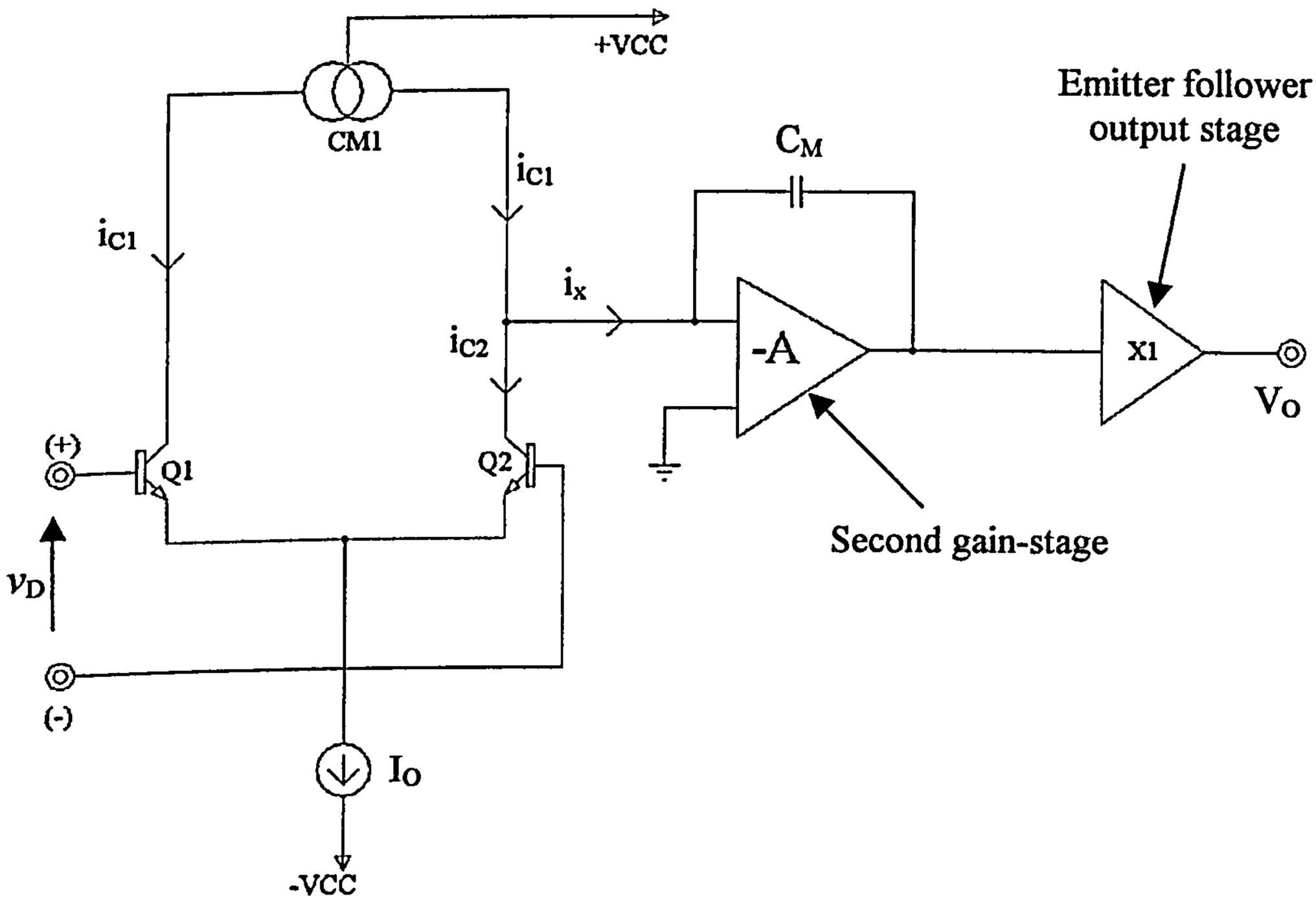


Figure.4.18 Basic architecture of the voltage operational amplifier (VFOA)

The slew rate S, is the maximum rate of change of the output voltage with time when a large-signal step function voltage is applied to the input terminals. The stipulation 'large-signal' inevitably rules out small-signal behaviour. It will be seen that slew rate is limited by the amount of current available to charge a dominant internal node capacitance included to ensure frequency stability under the closed-loop operation.

Consider, first, the case of VFOA shown schematically in Fig.4.18. If v_D is a large positive step-voltage, Q_1 passes the full tail current I_O, so $i_{c1} \approx I_O$ and $i_{c2} \approx 0$. The current mirror CM1 repeats i_{c1}, so the charging current for the Miller capacitance, C_M, included for closed loop frequency stability, is given by, $i_x \approx I_O$.

$$\text{Hence, } S_+ \approx \frac{I_o}{C_M} \tag{4.49}$$

Similarly, if v_D is a large negative going step-voltage,

$$S_- \approx -\frac{I_o}{C_M} \tag{4.50}$$

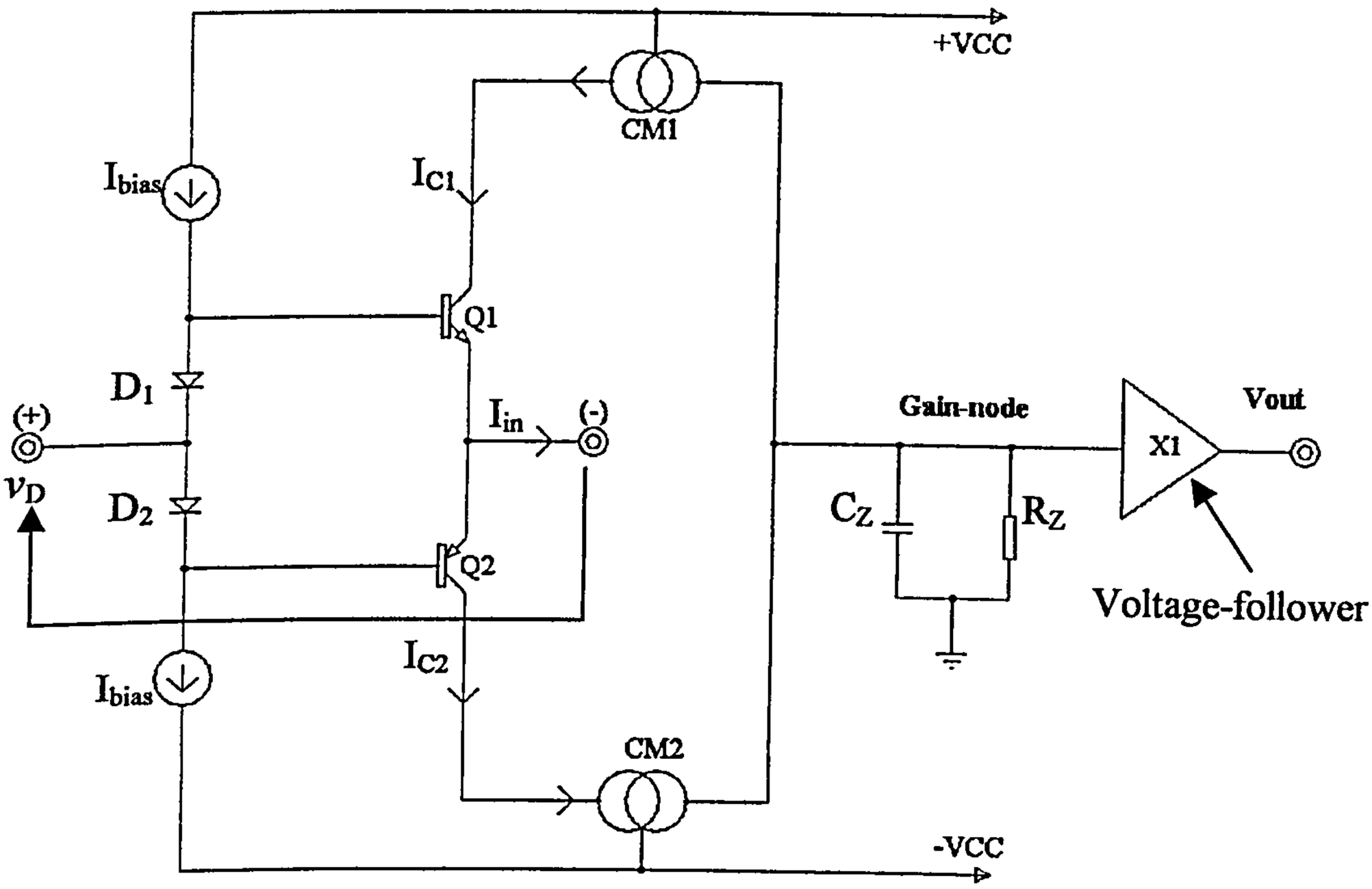


Figure.4.19 CFOA schematic for slew-rate discussion

thus,

$$S \approx S_+ \approx |S_-| \approx \frac{|I_O|}{C_M} \tag{4.51}$$

For the VOA type μA741, $I_O \approx 20\mu A$ and $C \approx 30pF$. The resulting value of S is less than 1V/μs. Consider next the case of the basic CFOA, a schematic diagram of which is shown in Fig. 4.19. The slew rate for this configuration is sometimes quoted as being virtually infinite but definite limits for this do exist as the following brief discussion shows. D_1, D_2 in Fig.4.19 model the input emitter followers. When a large differential voltage v_D is applied, in the direction shown, D_1 and Q_2 tend to cut off and the equivalent circuit for discussing slew rate S is that of Fig.4.20.

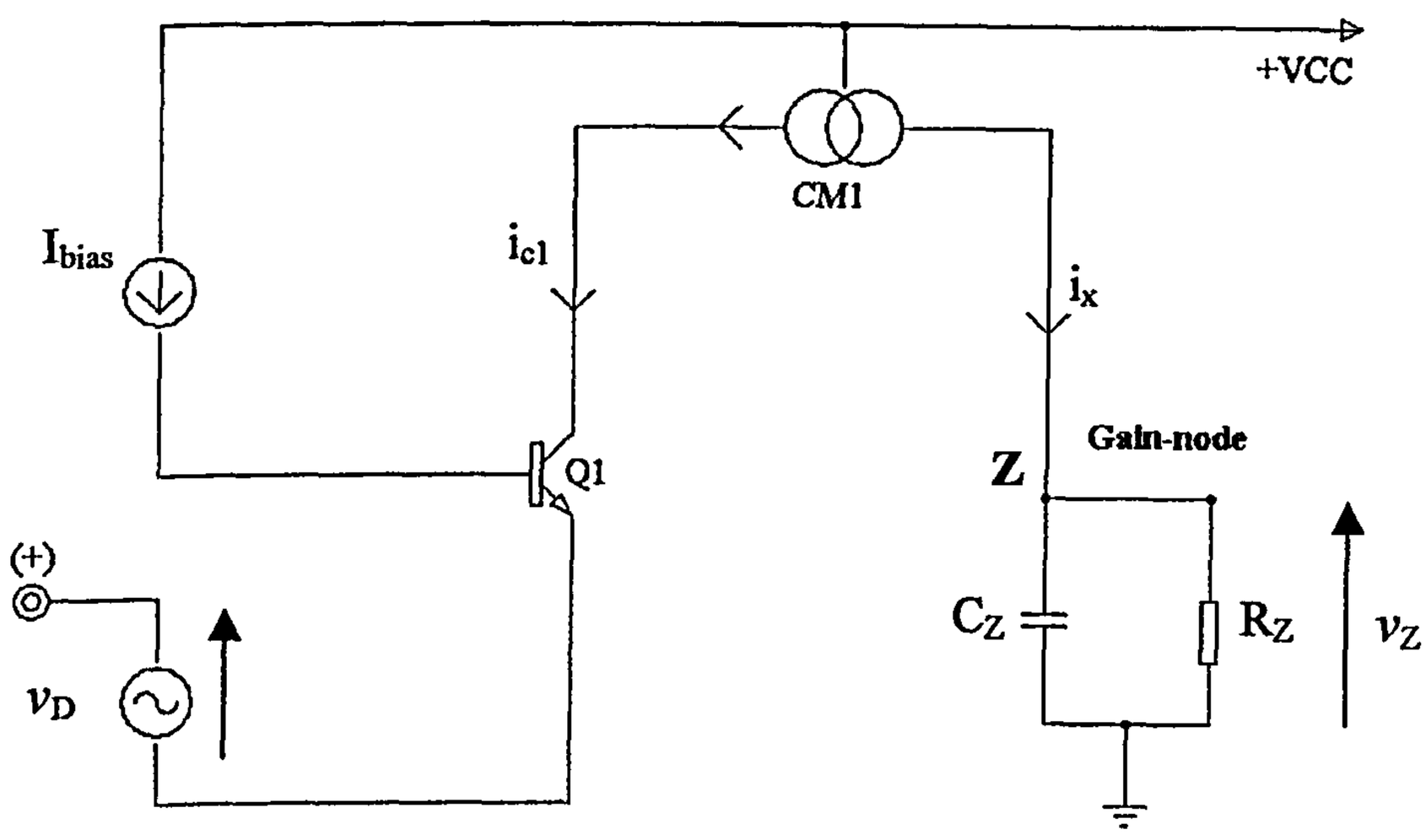


Figure.4.20 Reduced schematic from Fig.4.19 for a large v_D

Q_1 is supplied with a step of base current, I_{bias}, that provides a collector current i_{c1}, which can be estimated using transistor charge-control theory **[4-2]**.

$$i_{c1} \approx \beta_n I_{bias}[1-\exp(-\frac{t}{\beta_n \tau_F})] \tag{4.52}$$

in which: β_n=c.e. current gain of Q_1 at low frequencies; τ_F is a transistor time-constant dependent on its geometry and doping levels. Actually $\tau_F \approx 1/\omega_T$, ω_T being the characteristic BJT frequency at which $|\beta_n|=1$.

The current i_{c1} is repeated by the current-mirror CM1 but i_x is time-related to it. The equation for the voltage rise at point Z is,

$$C_Z \frac{dv_Z}{dt} + \frac{v_Z}{R_Z} \approx \beta_n I_{bias}[1 - \exp(-\frac{t}{\beta_n \tau_F})] \qquad (4.53)$$

A limit to slew rate is achieved by setting $\tau_F = 0$ and ignoring R_Z.

$$\text{Then, } S_+ \approx \beta_n \frac{I_{bias}}{C_Z} \qquad (4.54)$$

The same result is achieved for a large negative value of v_D, in which case D_2 and Q_1 tend to cut off. Clearly, for the same operating current ($I_{bias}=I_O$) and capacitor, S is much greater for the CFOA than the VOA. Typical values for the CFOA normally exceed 200V/μs.

The maximum value of the slew rate is obviously achieved with the maximum i_x and highest ω_T, so any improvement over that obtained for the basic CFOA must take these into account, as they are in improved designs, considered in later chapters. Ultimately the current available from the supplies limits the slew rate and this depends on supply-lead inductance and resistance.

Summary

This chapter continued the work of Chapter Three in making a general investigation and critical review into CFOA closed-loop characteristics.

An op-amp that has a non-linear effect can cause an input referred noise and slew rate performance degradation. This chapter looked at the theoretical study of the slew rate and evaluation of the architectural differences between the conventional VOA, and the conventional CFOA in order to fully understand how op-amps behave dynamically. In the VOA, when a sinusoidal waveform is applied to the input, the output is expected to be a reproduction of the shape of the input signal.

Unfortunately this is not the case due mainly to the fact that the VOA architecture provides inherent limitations in the slew rate. The design of the input stage of the VOA is a transconductance block with a classical long-tail pair input. The VOA topology shows a compensation capacitor C_Z, and high impedance node where the voltage gain is produced. Now the transconductance of the VOA is slew-rate limited due to the current available to charge or discharge C_Z which is the bias current (I_{bais}=Io) of this stage. The transconductance of the VOA will obviously provide an output saturation level, which causes limited slew-rate capability. As a result, an output waveform is distorted by this effect, and the amplitude will be reduced.

The theoretical absence of slew-rate limiting is one of the CFOA's attractive features. This arises from the fact that the maximum current, I_O, available to charge the internal capacitance, C_Z, at the onset of a step is proportional to the step regardless of its size. The time constant ($\tau \approx C_Z R_F$) must be constant. The slew rate of a current back op-amp will only be finally limited by the maximum value of the current drive into the base of the transistors which is set by (I_{bias}) current value. A high slew rate is obtained as a result of using the current, as a feedback error signal. Slew-rate limiting is a major cause of high-frequency distortion in high frequency amplifiers that are handling the output signal levels.

In this chapter, the theoretical study indicates that in the CFOA, the non-saturation transconductance (g_m) provides a theoretically unlimited slew-rate capability so that the CFOA gives low distortion for large amplitude, high frequency inputs. In practice, the slew-rate is governed by the power-supply's ability to deliver sufficient current to the class-AB complementary pair, and by power dissipation in the circuit.

The CFOA exhibits an almost constant closed-loop bandwidth for closed-loop voltage gains. The critical study in this chapter shows that it is necessary to set both the closed-loop bandwidth R_F and to set the gain R_G. A typical value for R_F would be between (750 Ω to 2.5 KΩ), as CFOA manufacturers have recommended. The results again show the unique feature of the CFOA design, which has made the bandwidth remain constant as a function of the closed-loop gain. In CFOA, the designer must be careful in deciding how to use a reactive feedback element (such as in the case of the integrator operation), because the closed loop pole must be lower in frequency than any reactive component poles when it is connected directly from the input to the output, in order to insure stability in the closed-loop operation for all gain settings. Otherwise, if the designers are not careful, the domain pole can be shifted too close to the secondary pole and oscillation might occur as a result.

These characteristics are due to the asymmetric class-AB input stage and make the CFOA a very suitable amplifier for video signal processing. The theoretical performance of the CFOA in terms of bandwidth has been looked at and the author has suggested that the effect of the output impedance on the bandwidth can be further investigated by future researchers.

(4.7) References for Chapter 4

[4-1] Seevinck, E, Wassenaar, R.F, Leeuwen, M.G.van, Boom, G, Holle, E and Wal, R.Vande, 'Wide band voltage to current converter circuit', Dig. Tech. Papers European Solid State Conference. (ESSCIRC, Toulouse, France), Sept. 1985, pp. 108-112.

[4-2] Introduction to Electronics; Gray. P. E., John Wiley, New York 1967, Chapter 5, pp. 183-195.

CHAPTER 5

New Input Stages For Current Feedback Operational Amplifiers

(5.1) Introduction

This chapter considers the trade-offs involved in the design of new input stages intended to improve the performance of a CFOA, over that possible using an established input circuit configuration, with respect to three major characteristics, *viz.*, Common-mode rejection ratio (CMRR), Offset Voltage (V_{OS}) and Slew-Rate (SR).

For convenience in comparison, a schematic circuit of the established CFOA, considered in Chapter 3, is repeated in Fig 5.1 **[5-1]**.

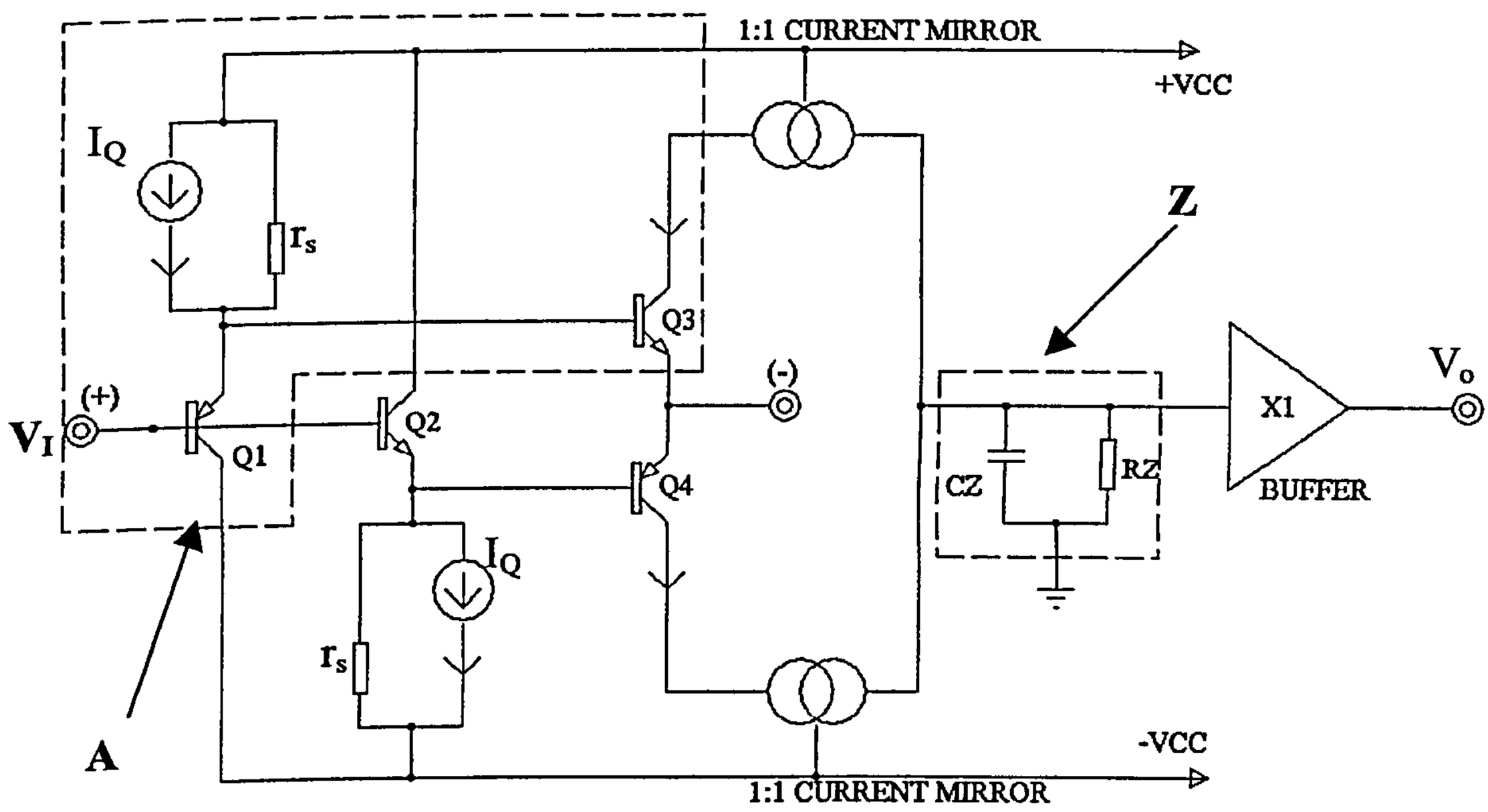


Figure. 5.1 Schematic of established CFOA circuit

Within the contour A, Q_1 together with its emitter load (bias current source I_Q and Q_3 may be considered to comprise an input 'half-circuit' (A) and it is this which is considered further. The other 'half- circuit', comprising Q_2 and its emitter load and Q_3, behaves in an identical, complementary, manner. The next section explores the 'half-circuit' concept in some detail and the following sections deals with the current-mirrors used in the half-circuit design.

(5.2) The 'Half-Circuit' concept explored

The essential feature of the 'Half-circuit' concept is that in new designs there is mirror-symmetry about an imaginary horizontal line joining the (+) and (–) terminals in Fig 5.1. This means that the base-emitter voltage of similar polarity devices are balanced rather than the base-emitter voltage of opposite polarity devices, so there is a reduced-offset voltage.

In the replacement for A (of Fig.5.1) in the circuits that follow, the effect of V_{AP} is minimized by having I_Q supplied by a cascode source referenced to the rail supplies, and the effect of V_{AN} is made to appear smaller by employing a bootstrapped cascode transistor Q_5 in the collector circuit of Q_3. Both these procedures help to increase the CMRR. The slew rate is improved by supplying more base current to the base of Q_3 via the inclusion of an emitter-follower.

The bootstrapping technique typifies the configuration. Type 1 circuits are exemplified in Figs 5.2, 5.3, 5.4. In these the base of Q_5 is bootstrapped to the inverting input, which follows the non-inverting input in normal CFOA operation: a suggested name for this is 'reverse bootstrapping'. The output resistance at the collector of Q_5 is approximately equal to $\beta_N V_{AN}/I_Q$ (β being the common emitter current gain of Q_5): the output resistance of the source supplying I_Q is $\beta_P V_{AP}/I_Q$ so the common-mode rejection ratio is increased by a factor $\beta_P\beta_N$.

The offset-voltage V_{os}, however, is poor in half-circuit B because of practical mismatch in the V_{BE} of Q_1 and Q_3. This is reduced in half-circuit C, in which Q1 is now an NPN transistor, diode-strapped. In half-circuit D, the diode-strapped transistor of Fig.5.3 now functions as a normal transistor and the emitter-follower Q_8 makes possible an increase in the slew rate by making more current available at the base of Q_3.

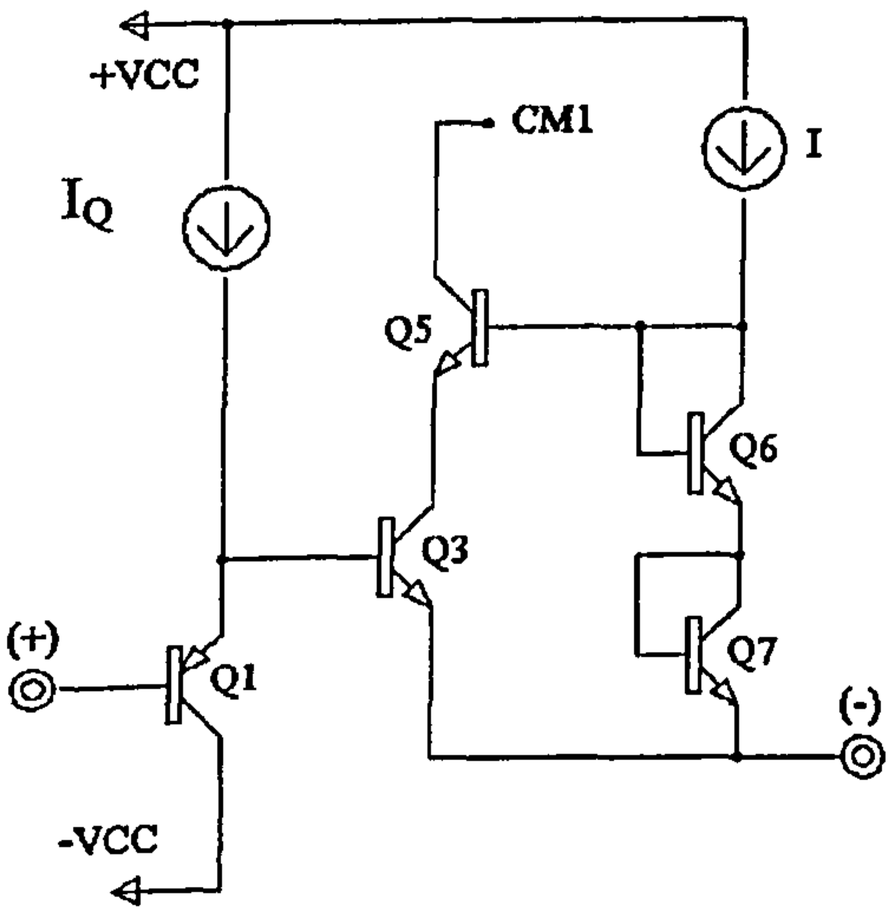


Figure.5.2. Half-circuit B

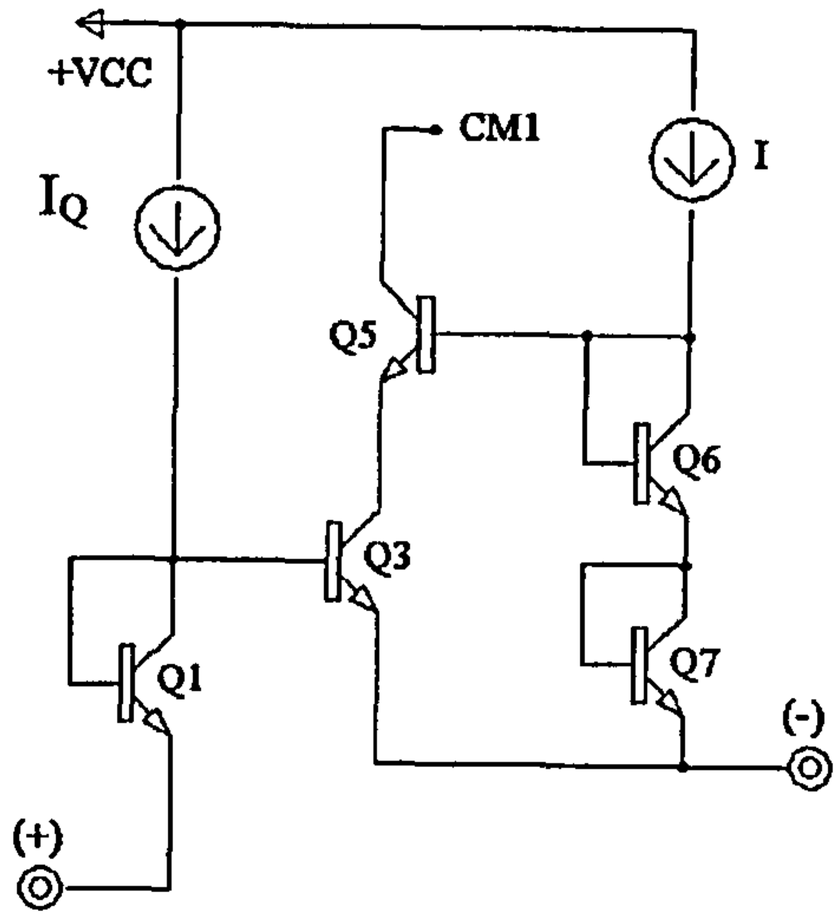


Figure.5.3. Half-circuit C

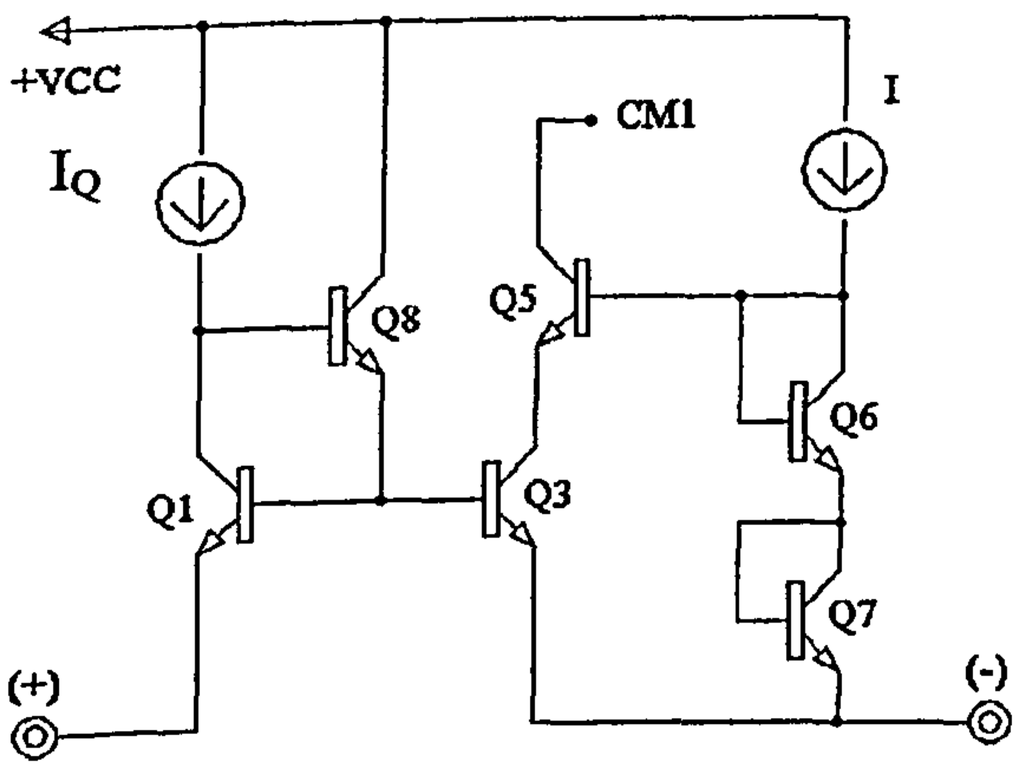


Figure.5.4. Half-circuit D

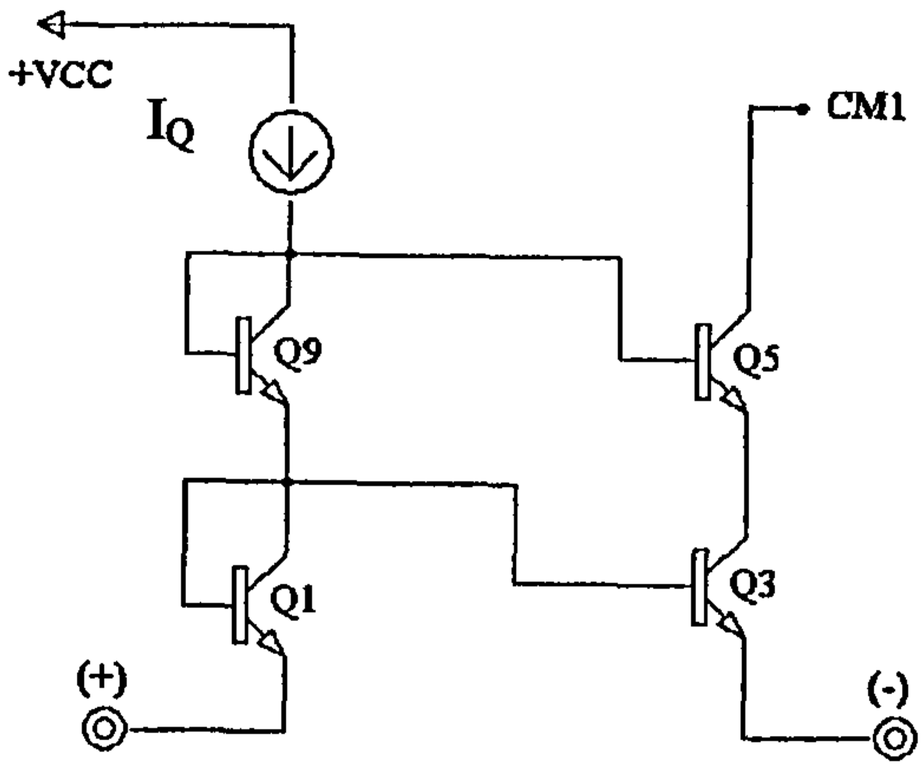


Figure.5.5. Half-circuit E

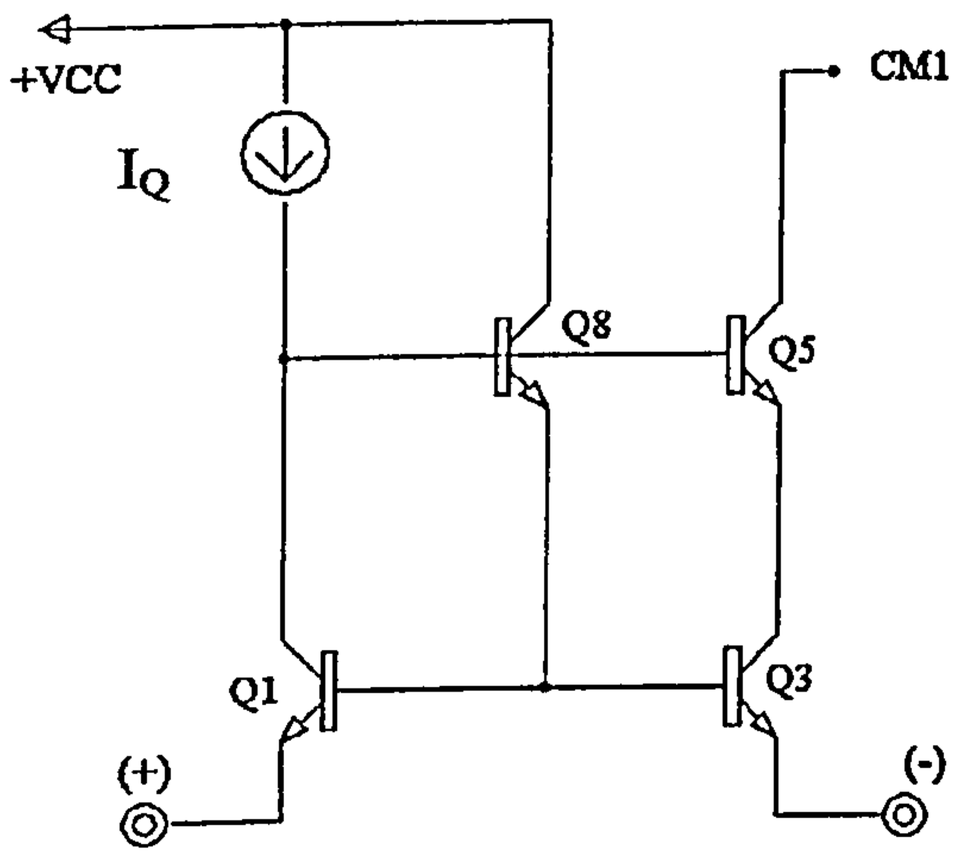


Figure.5.6. Half-circuit F

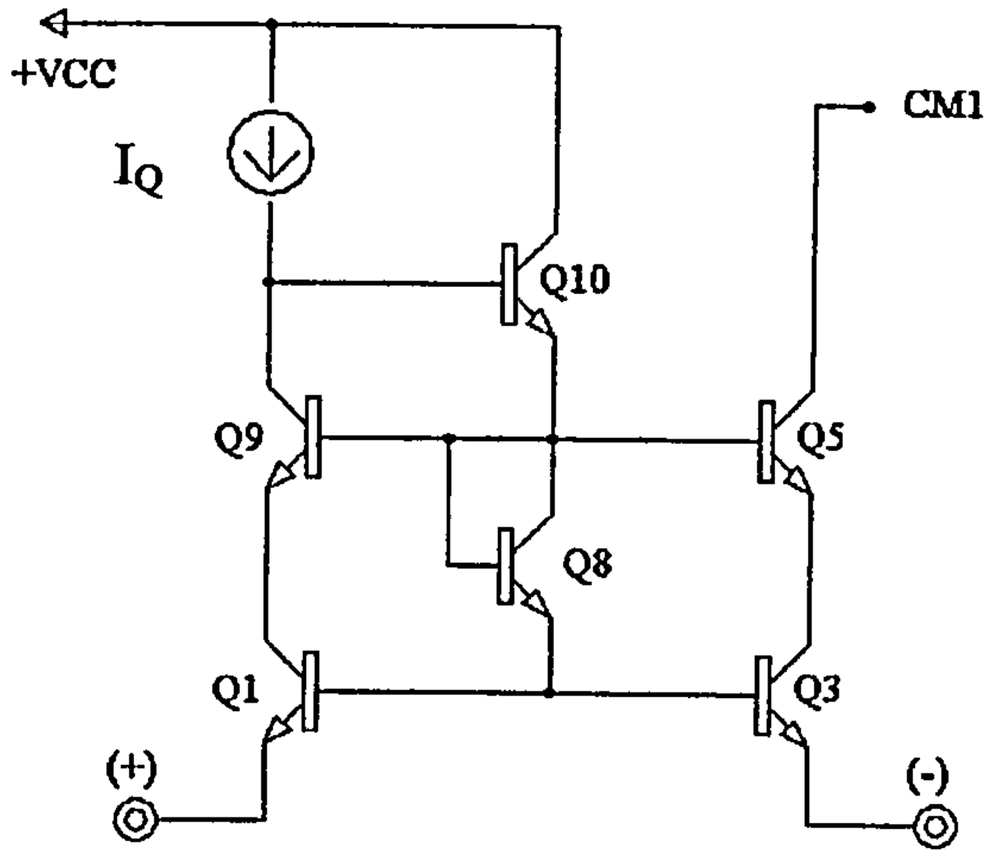


Figure.5.7. Half-circuit G

Type 2 circuits are-exemplified in Figs 5.5, 5.6, 5.7, in which the base of Q_5 is driven from the non-inverting input ('forward-bootstrapping'). Figs 5.6, 5.7, like Fig.5.5, employ emitter-followers to drive the base of Q_3 for an increased slew rate.

In Fig.5.7 **[5-2]**, Q_1 and Q_3 both operate at the same V_{CB} ($\approx$0), as well as the same collector current, to ensure a low V_{os}.

(5.3) Common-base characteristics

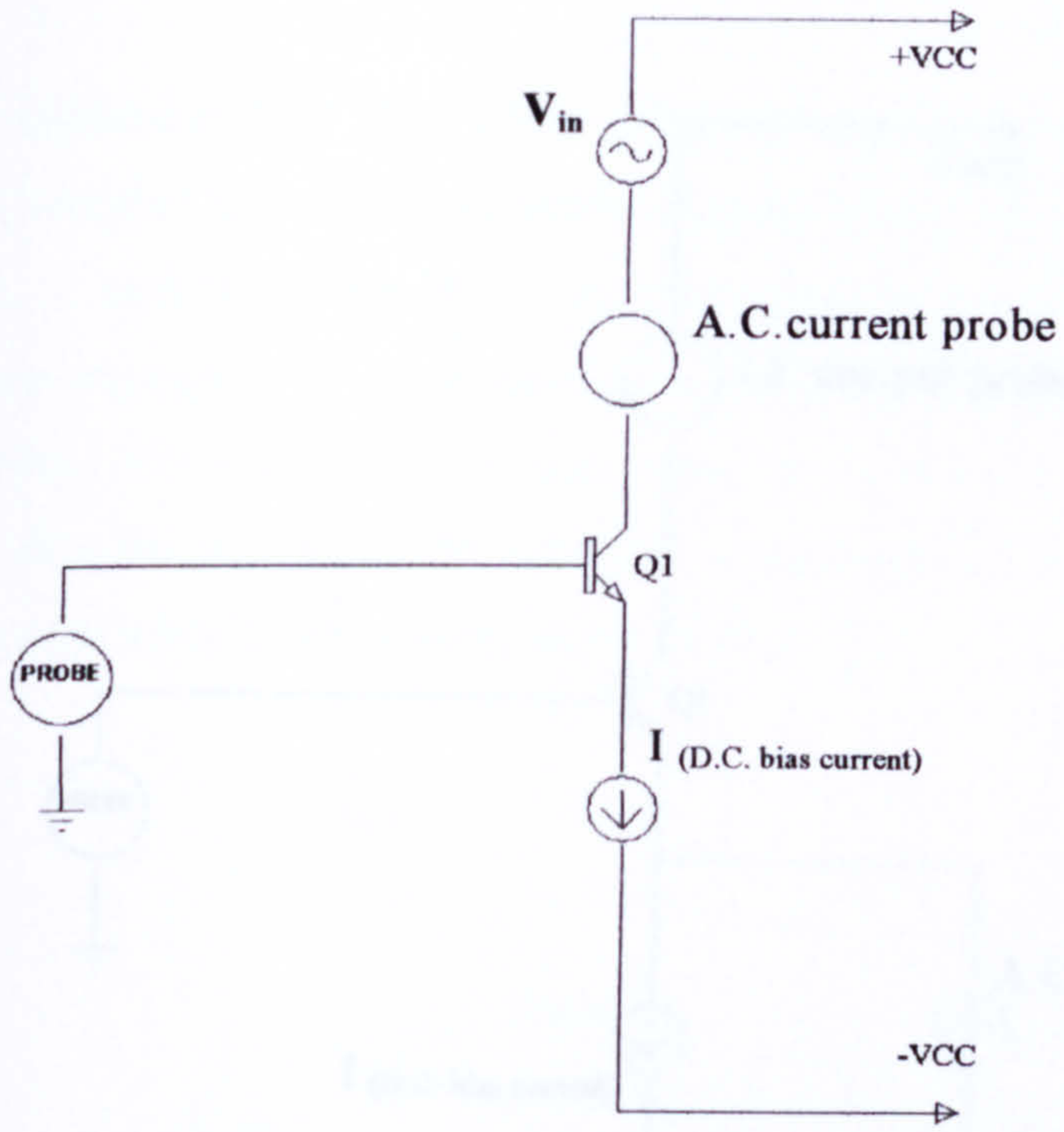


Figure.5.8. A Common-base amplifier stage for measuring the output impedance

Fig.5.8 shows a common-base stage, which is useful in impedance transformation. The measurements presented here give an indication of the actual β of the BJT under circuit operating conditions because R_O with a constant current emitter load is $(\beta_N + 1)\frac{V_{AN}}{I_Q}$. Furthermore, the frequency response for the c-b current gain gives a good indication of the f_T of the BJT at the I_C and V_{CB} used.

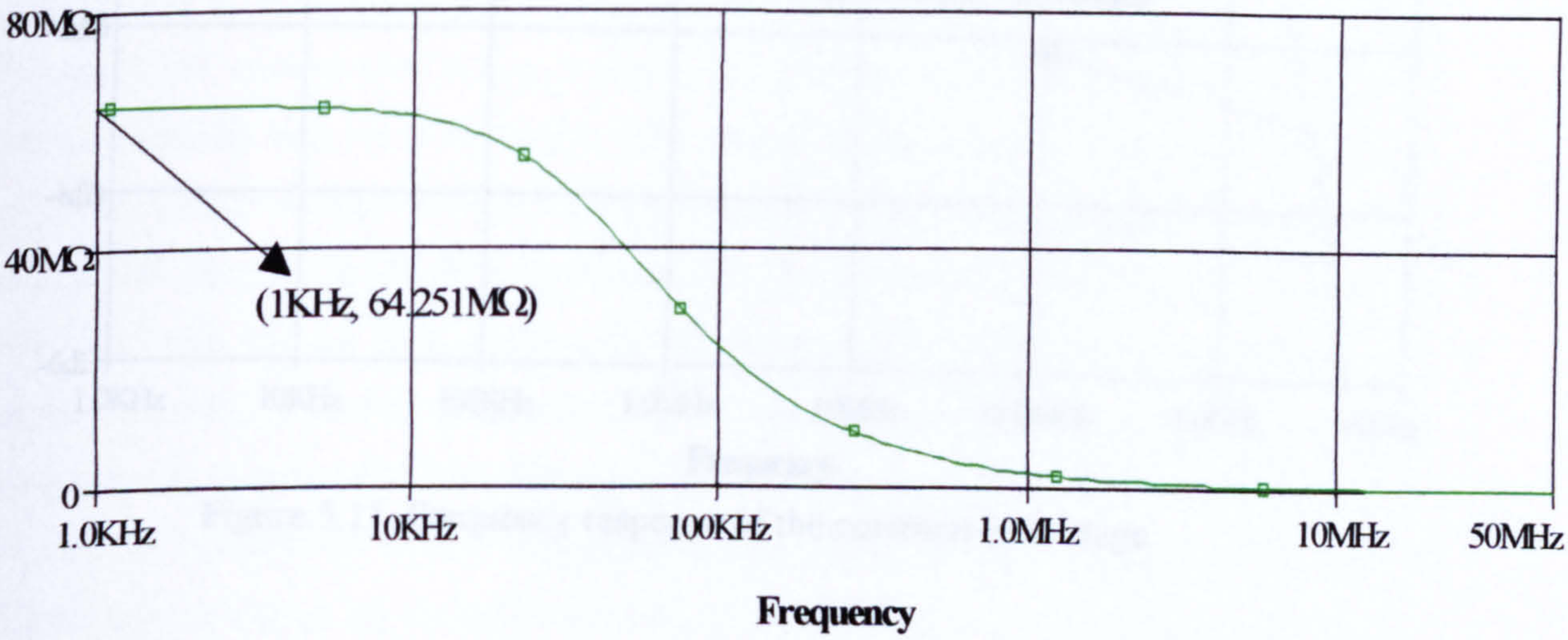


Figure.5.9. The output impedance of the common-base transistor for I=0.1mA

From Fig.5.9 we deduce that $\beta_N \approx 70$ since $V_{AN} \approx 90V$ and $I_C = 0.1mA$: from Fig.5.11, $f_T \approx 3GHz$.

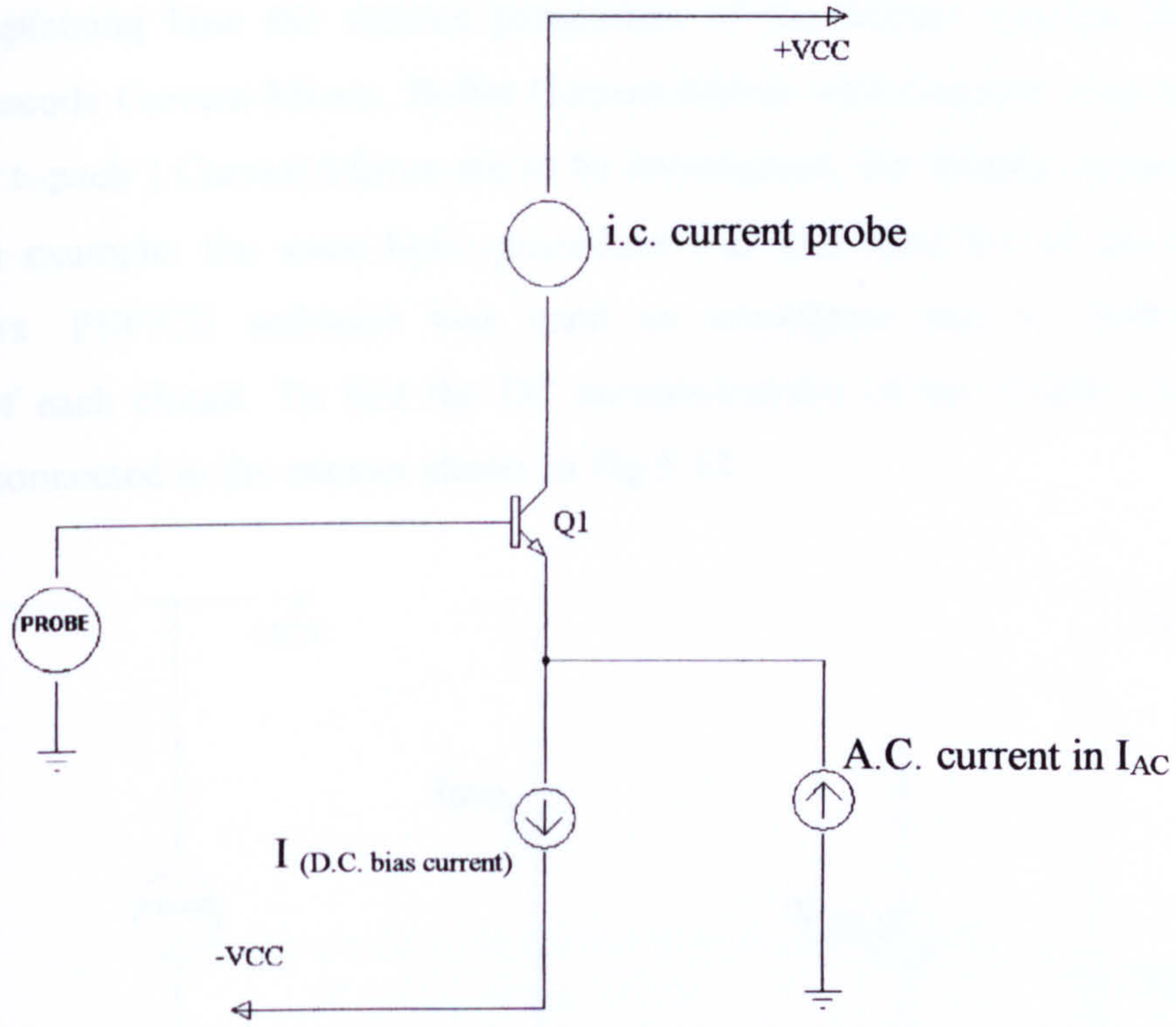


Figure.5.10. A Common-base amplifier stage for measuring the bandwidth

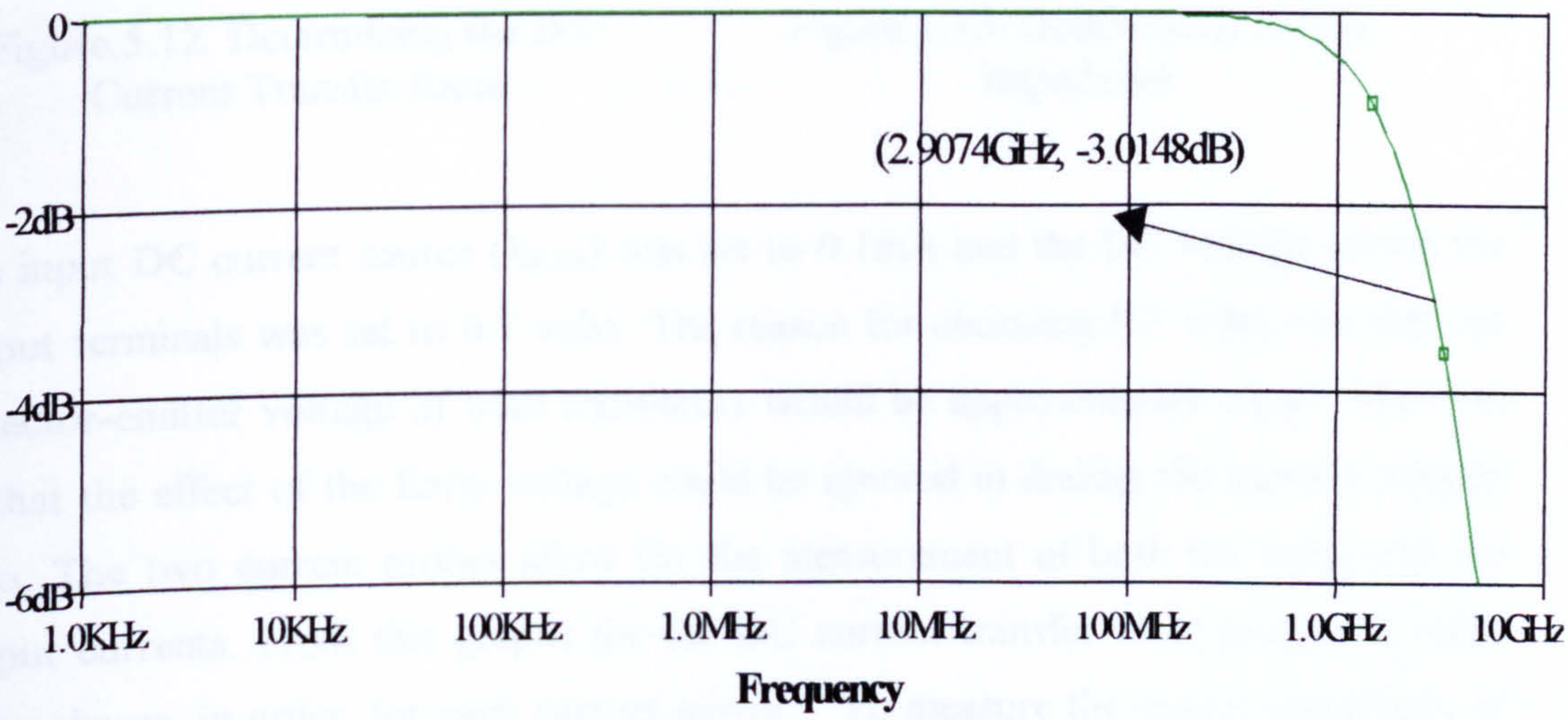


Figure.5.11. Frequency response of the common-base stage

(5.4) Current-mirror performance

By way of explaining how the various parameters of the Simple Current-Mirror, Wilson and Cascode Current-Mirror, Buffer Current-Mirror with Cascode output, and Precision (or, '6-pack') Current-Mirror are to be investigated, the Simple current will be used as an example: the same basic procedure was also used for all the other current mirrors. PSPICE software was used to investigate and to study the performance of each circuit. To find the DC current-transfer of the Simple Current Mirror it was connected in the manner shown in Fig.5.12.

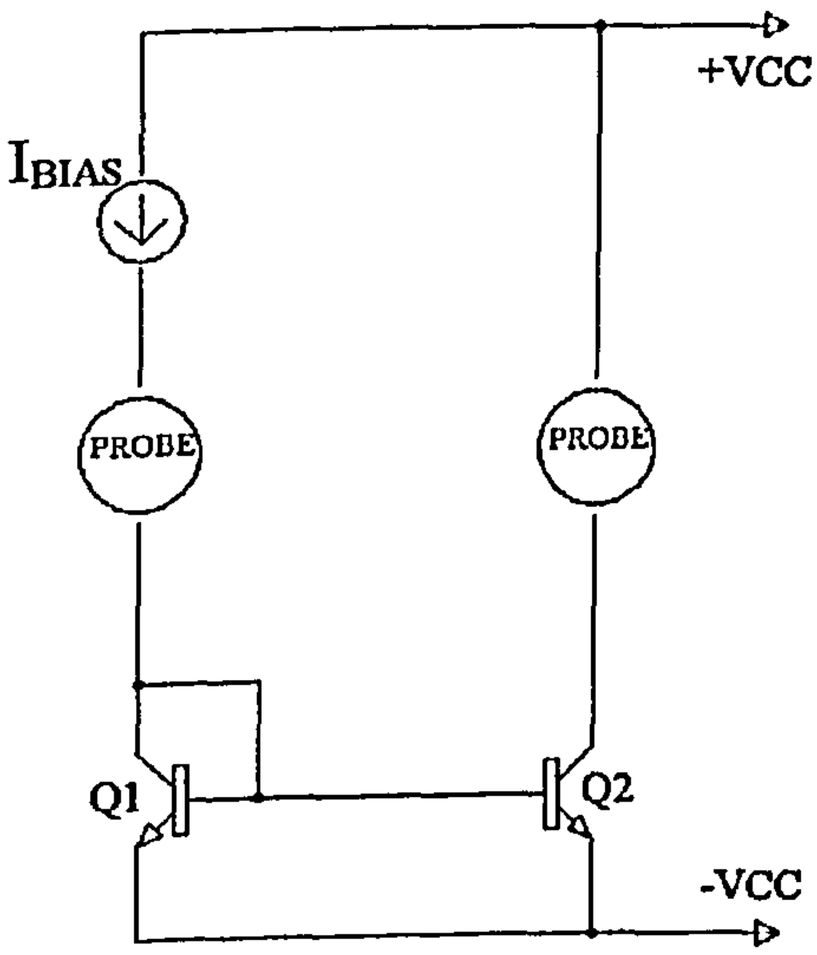


Figure.5.12. Determining the D.C Current Transfer Ratio

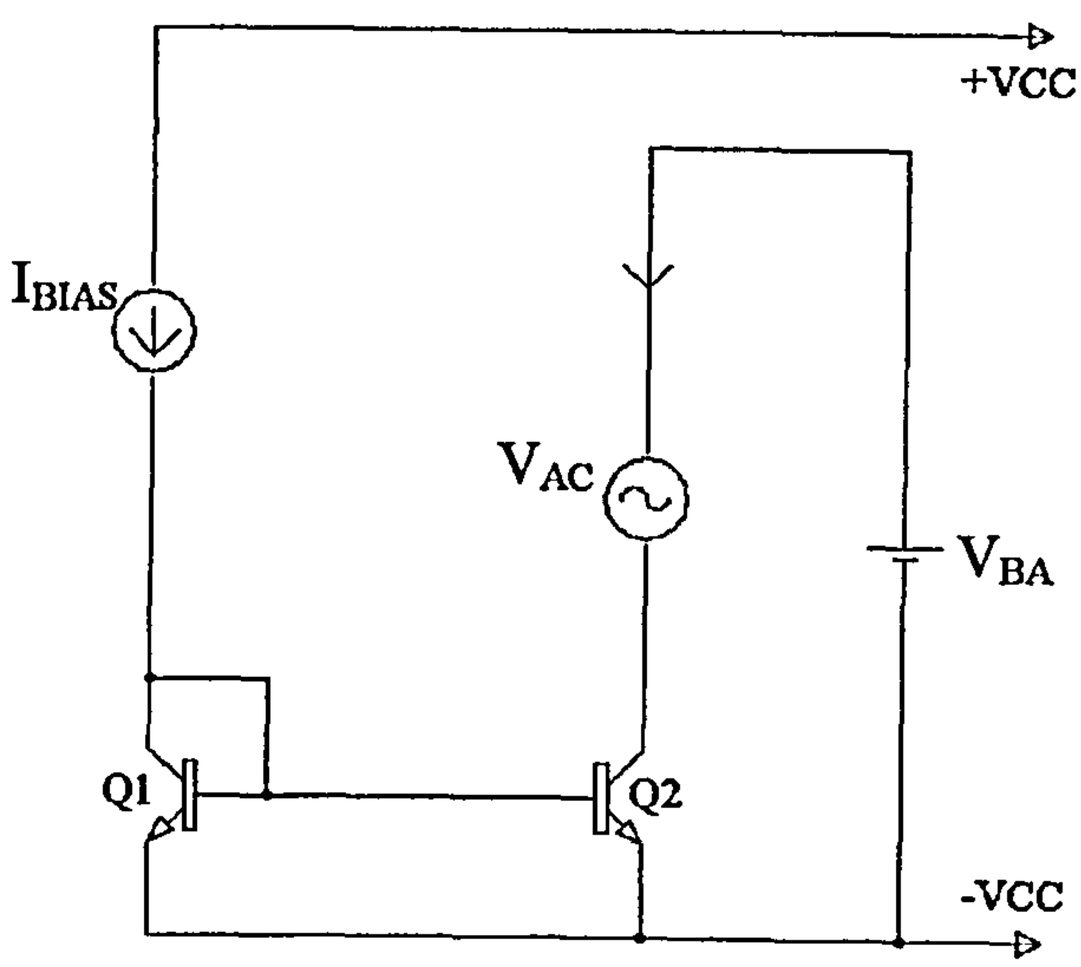


Figure.5.13. Determining output impedance

The input DC current source (I_{BIAS}) was set to 0.1mA and the DC voltage across the output terminals was set to 0.7 volts: The reason for choosing 0.7 volts was that the collector-emitter voltage of both transistors would be approximately equal. This was so that the effect of the Early voltage could be ignored in finding the current transfer ratio. The two current probes allow for the measurement of both the input and the output currents. From this graphs for the DC current transfer were produced, these being shown, in order, for each current mirror. To measure the output impedance of the current mirrors the circuit was modified, as shown in Fig.5.13. Again, the DC current source (I_{BIAS}) on the input was set to 0.1mA, and AC voltage source (V_{AC}) was connected at into the output of the current mirror. Also a DC voltage (V_{BA}) was

connected in series to the output to insure that the voltage across the collector–emitter is set to 1V in the case of the Simple, and Buffered Current-Mirror. With the rest of the current-mirrors the DC voltage (V_{BA}) was set to 5 volts.

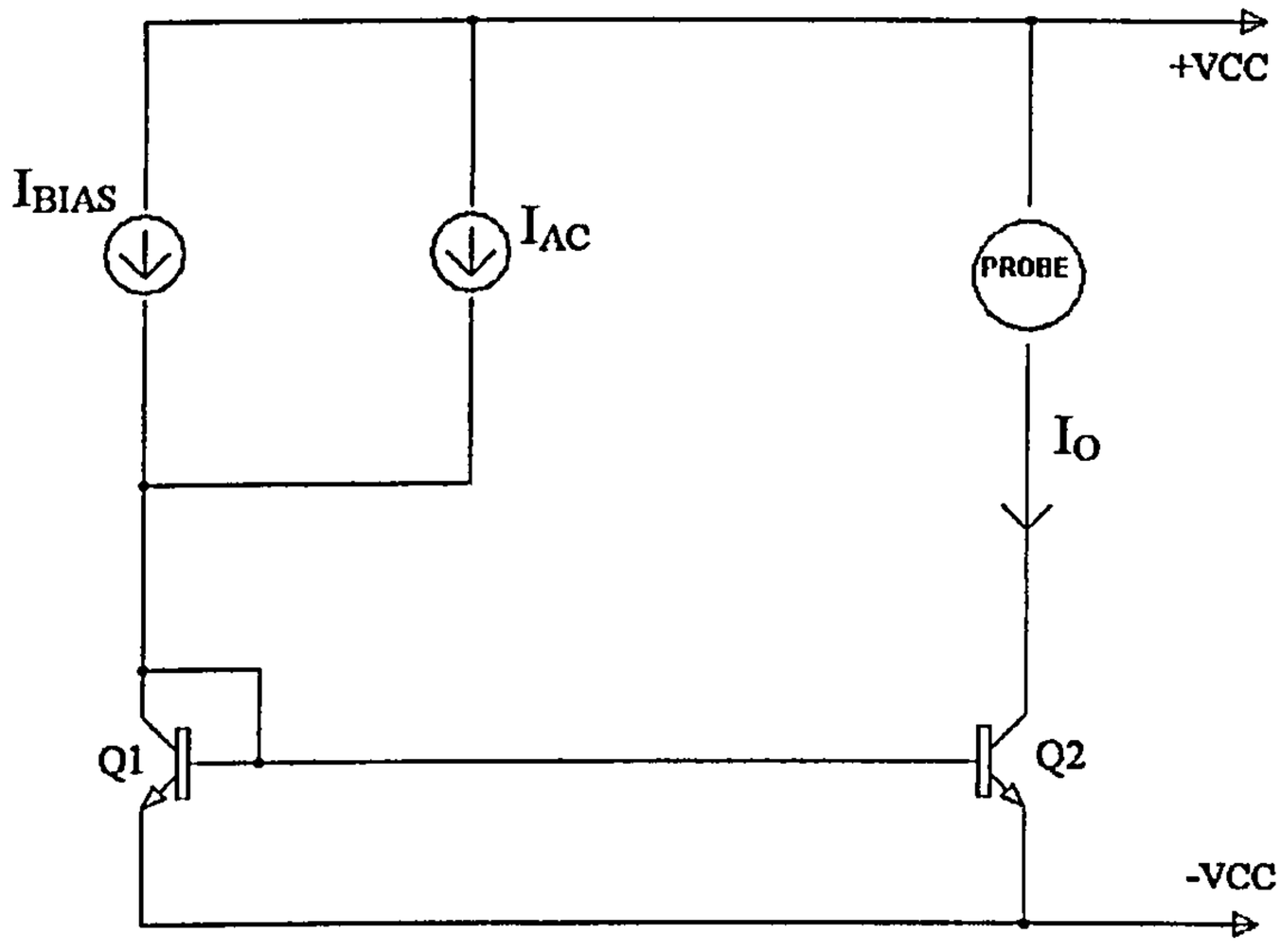


Figure.5.14. Determining the frequency response of the Simple Current Mirror

To measure the frequency response the circuit was modified, as shown in Fig.5.14. A low level AC current source (I_{AC}) was added to the circuit in parallel with the bias current of 0.1mA. This was set with an amplitude of 10μA (which is 1/10 of I_{BIAS}) and its frequency swept from 1KHz to 3GHz. All measurements refer to the transistor types mentioned in Chapter Three, and Four.

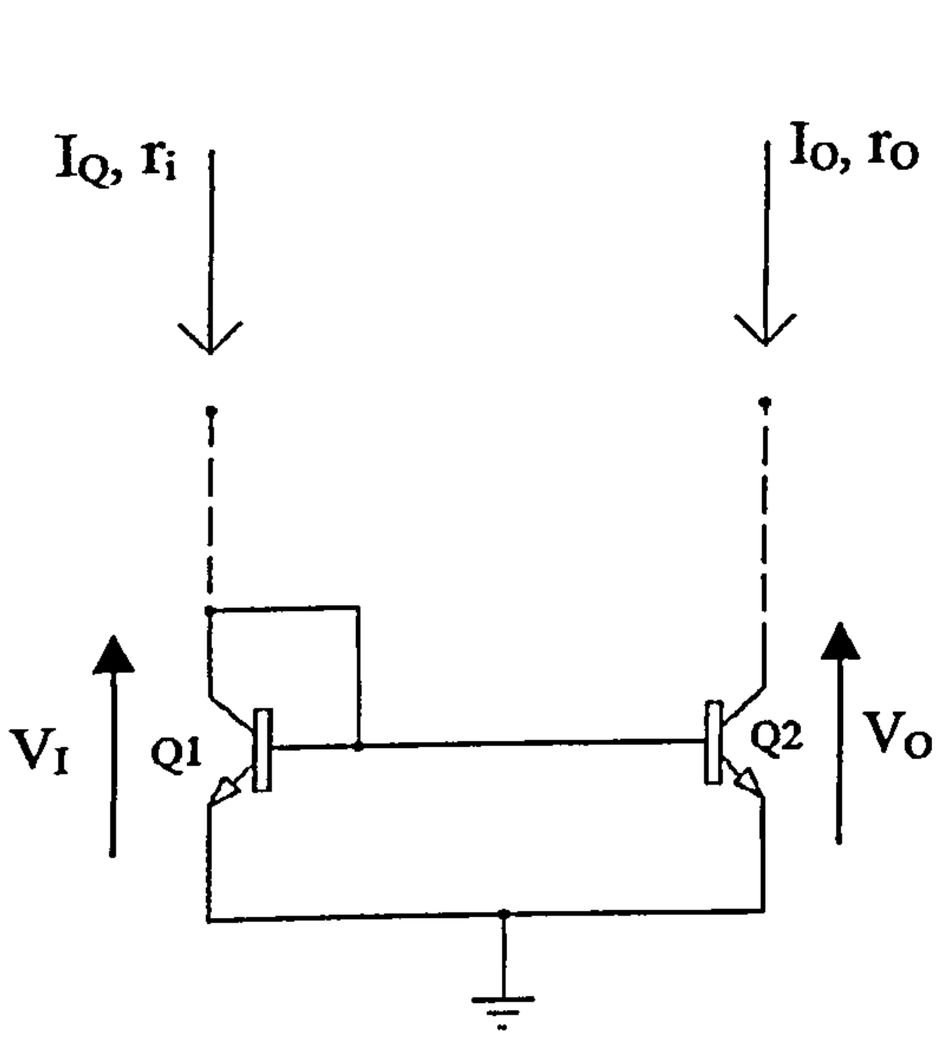


Figure.5.15. Simple Current-Mirror

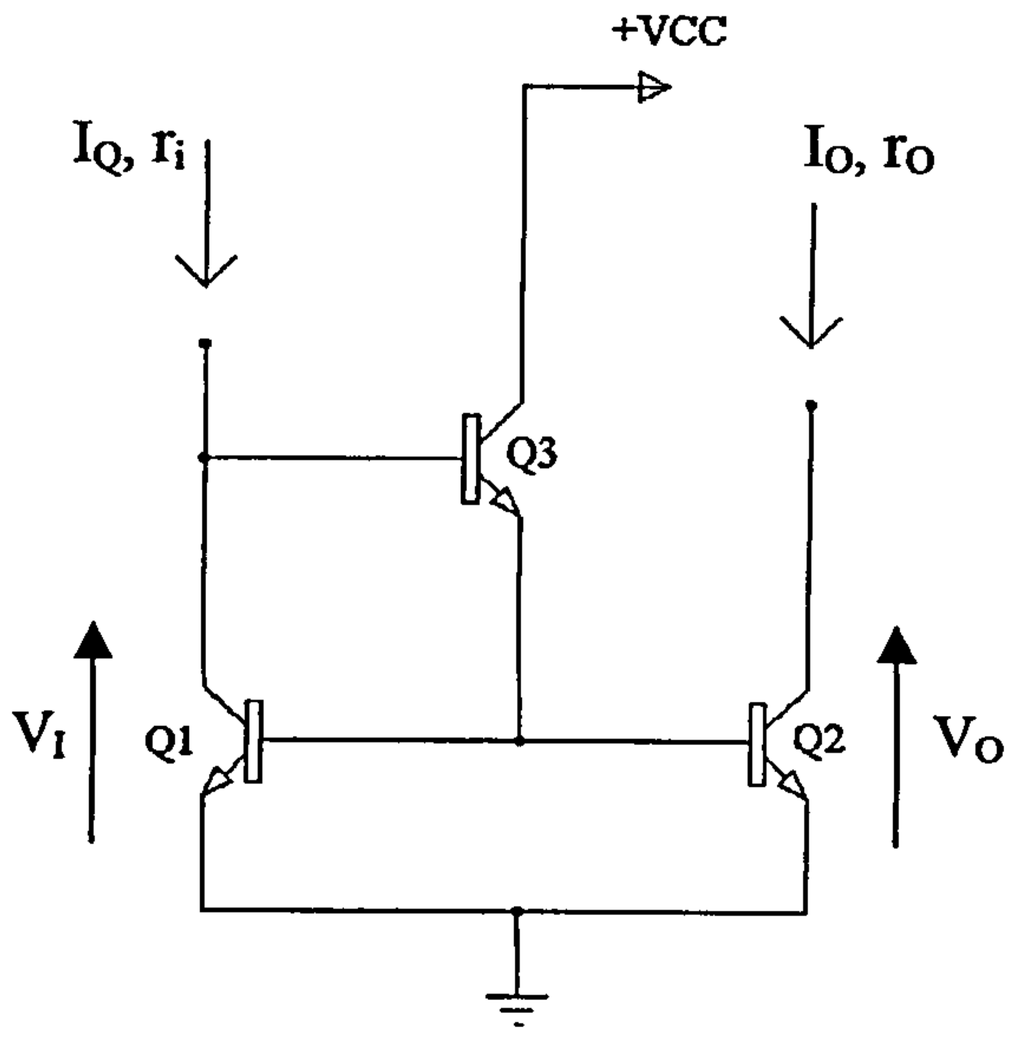


Figure.5.16. Buffered Current-Mirror

	Simple current-mirror **[5-3], [5-4]** (Fig.5.15)	Buffered current-mirror **[5-3], [5-4]** (Fig.5.16)
λ	$\frac{\beta}{(\beta+2)} \pm \frac{V_{Os}}{V_T}$	$\frac{1}{(1+\frac{2}{\beta^2})} \pm \frac{V_{OS}}{V_T}$
V_I (Min)	V_{BE}	$2V_{BE}$
V_O (Min)	V_{BE}	V_{BE}
r_O	$\frac{V_{AN}}{I_Q}$	$\frac{V_{AN}}{I_Q}$

Table 5.1 Characteristics of a simple and Buffered Current-Mirror

* Here and in the subsequent Tables in this Chapter, V_{OS} refers to the V_{BE} mismatch between Q_1 and Q_2: see, also, Appendix 5.1.

Note that r_μ is neglected in the expressions for r_O. It is also neglected in Tables 5.2, 5.3, later.

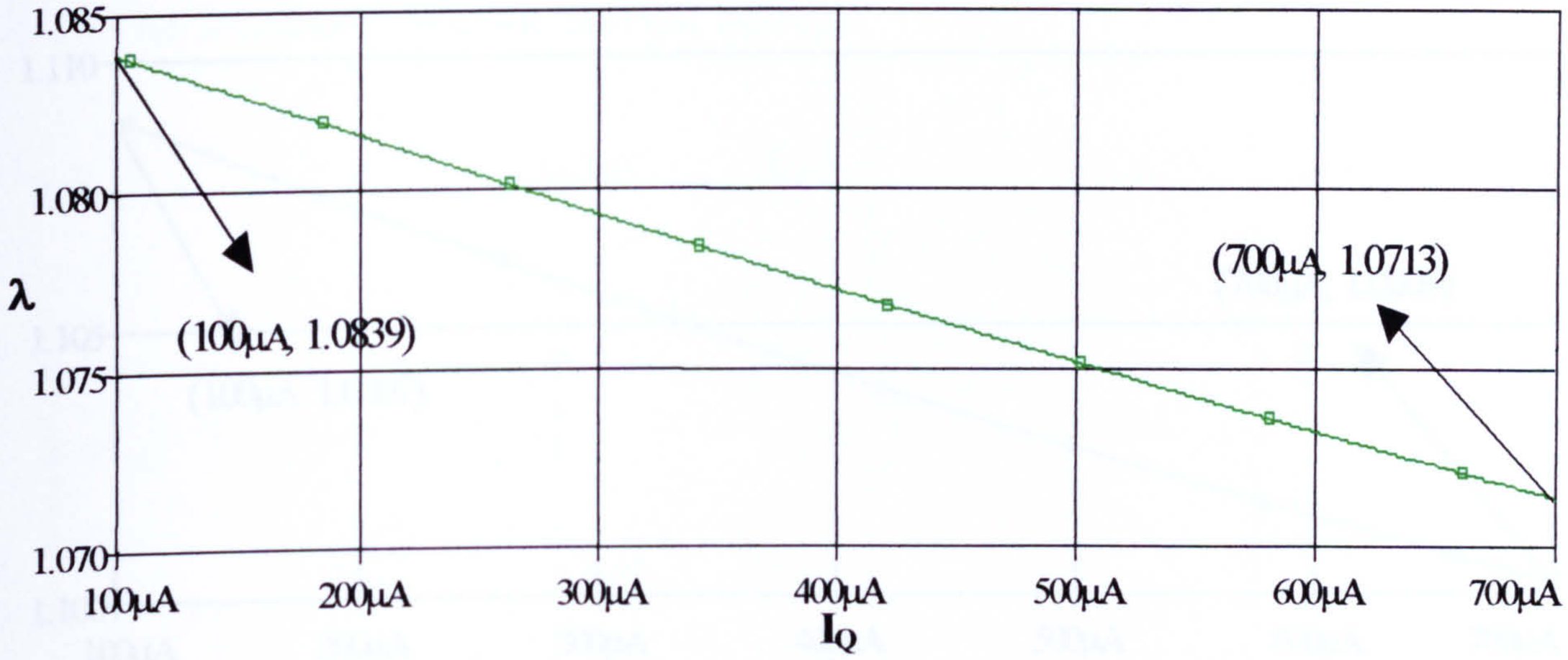


Figure.5.17. D.C. Current transfer ratio, λ, as a function of I_C for a simple Current-Mirror

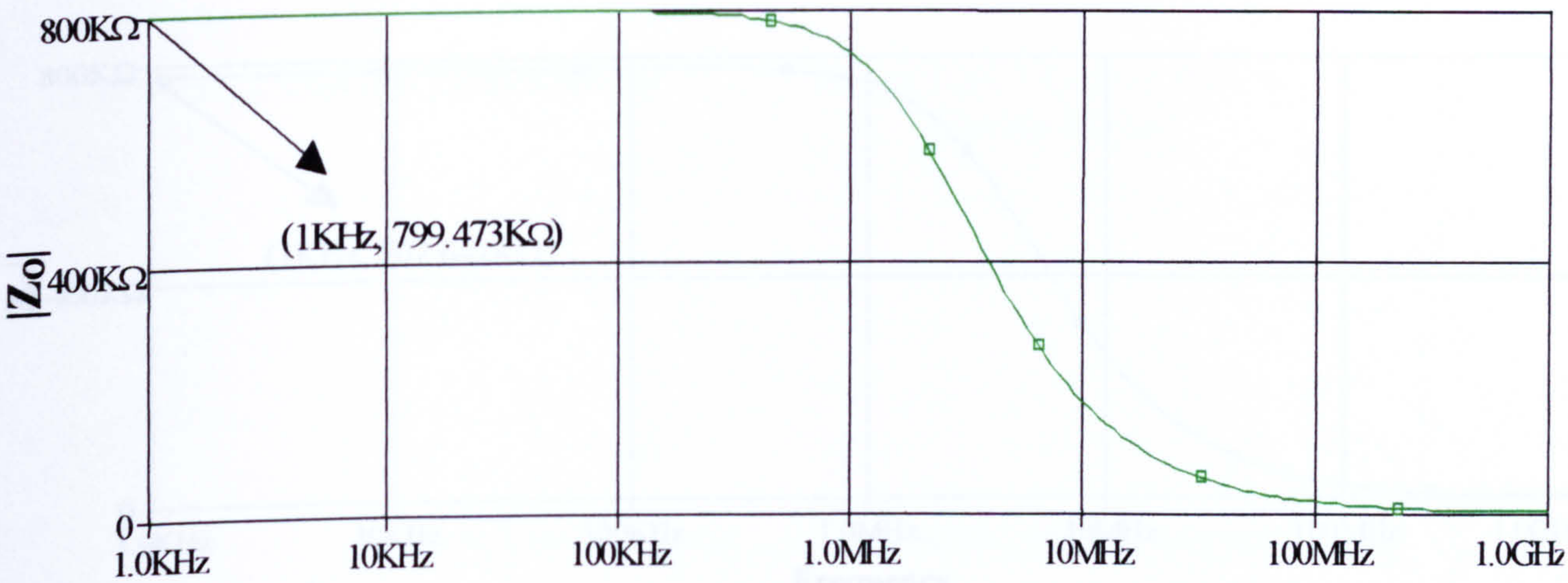


Figure.5.18. The output impedance of the simple Current-Mirror

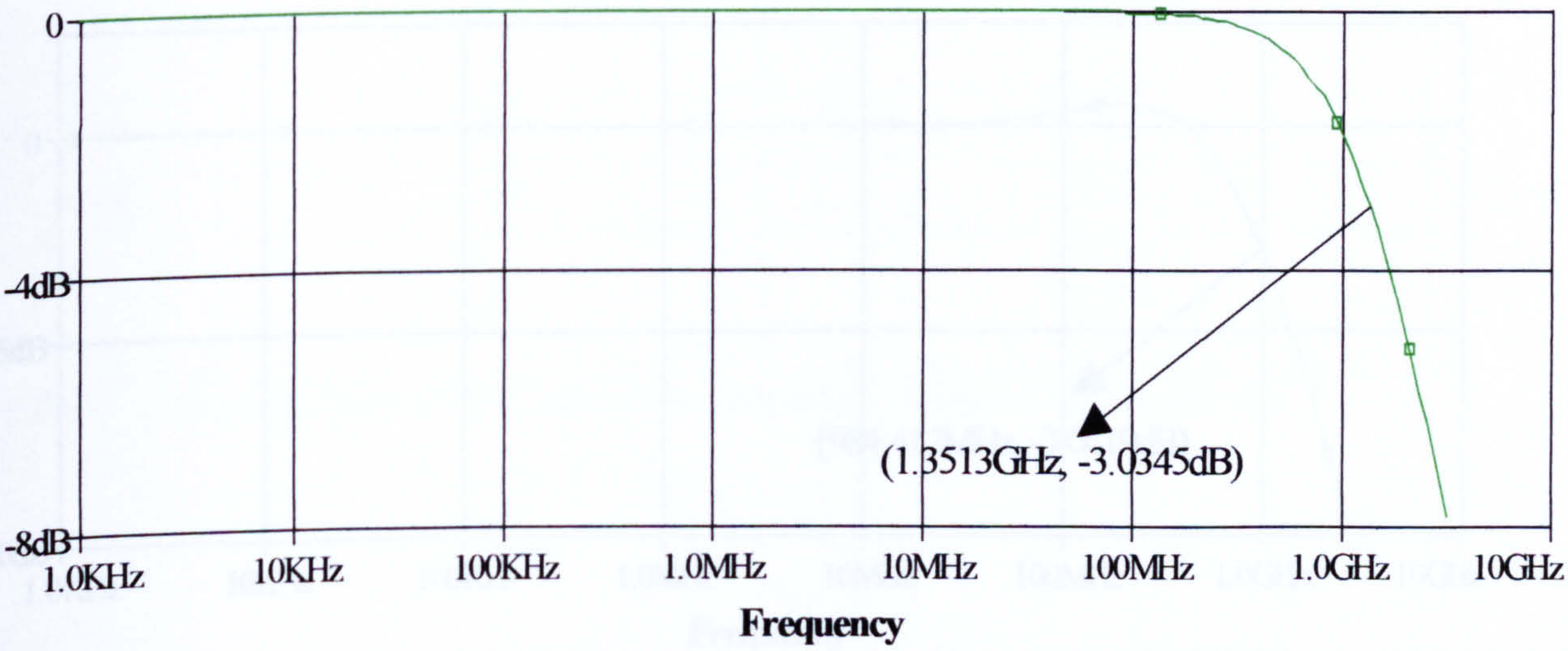


Figure.5.19. Frequency response of the simple Current-Mirror

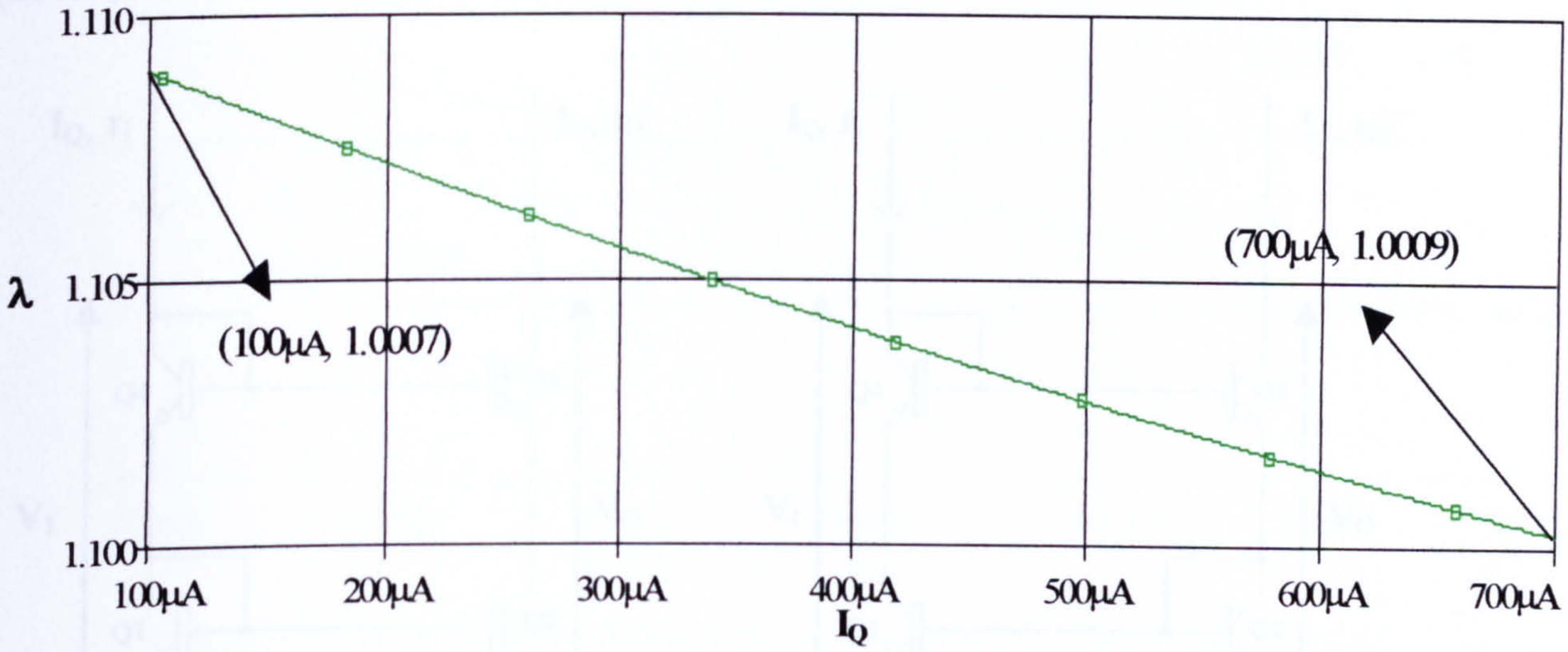


Figure. 5.20. D.C. Current transfer ratio, λ, as a function I_C for a Buffered Current-Mirror

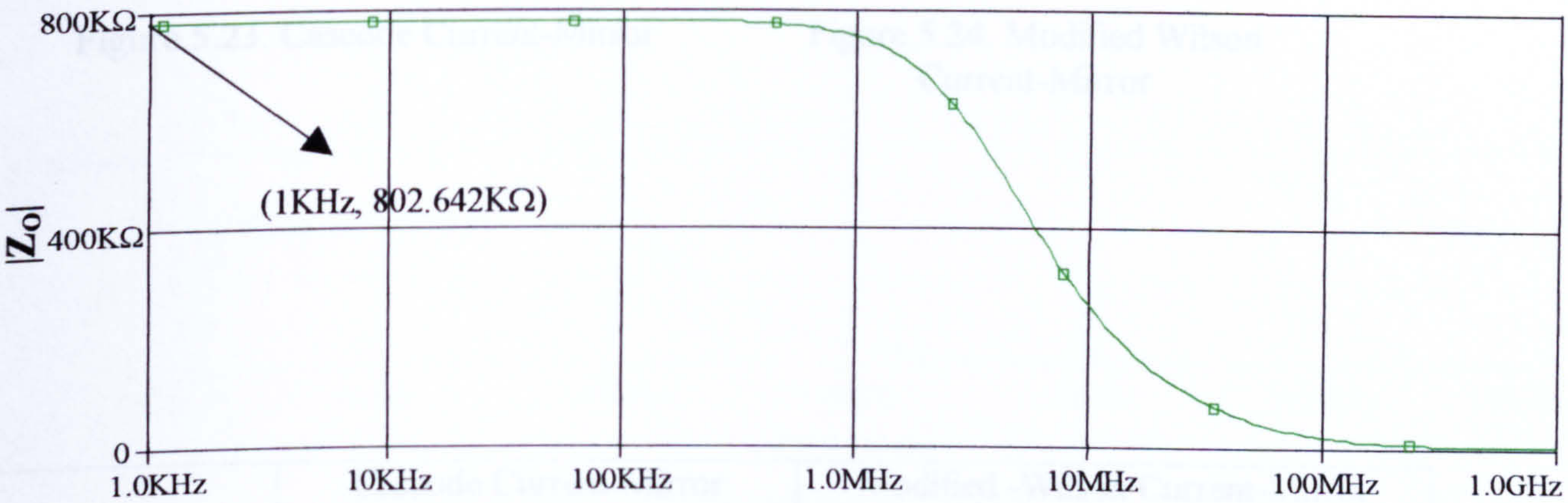


Figure.5.21. The output impedance of the Buffered Current-Mirror (compare with Fig.5.18)

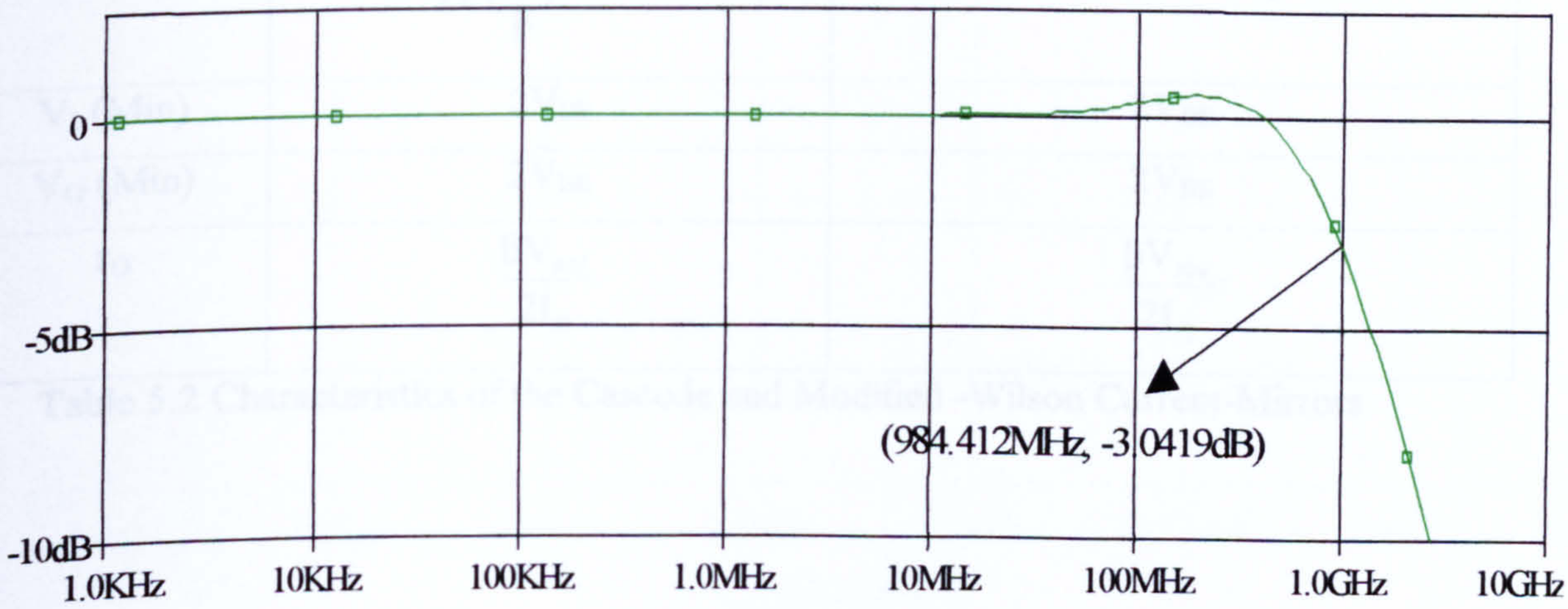


Figure.5.22. Frequency response of the Buffered Current-Mirror

(5.4.1) The Modified Wilson current mirror

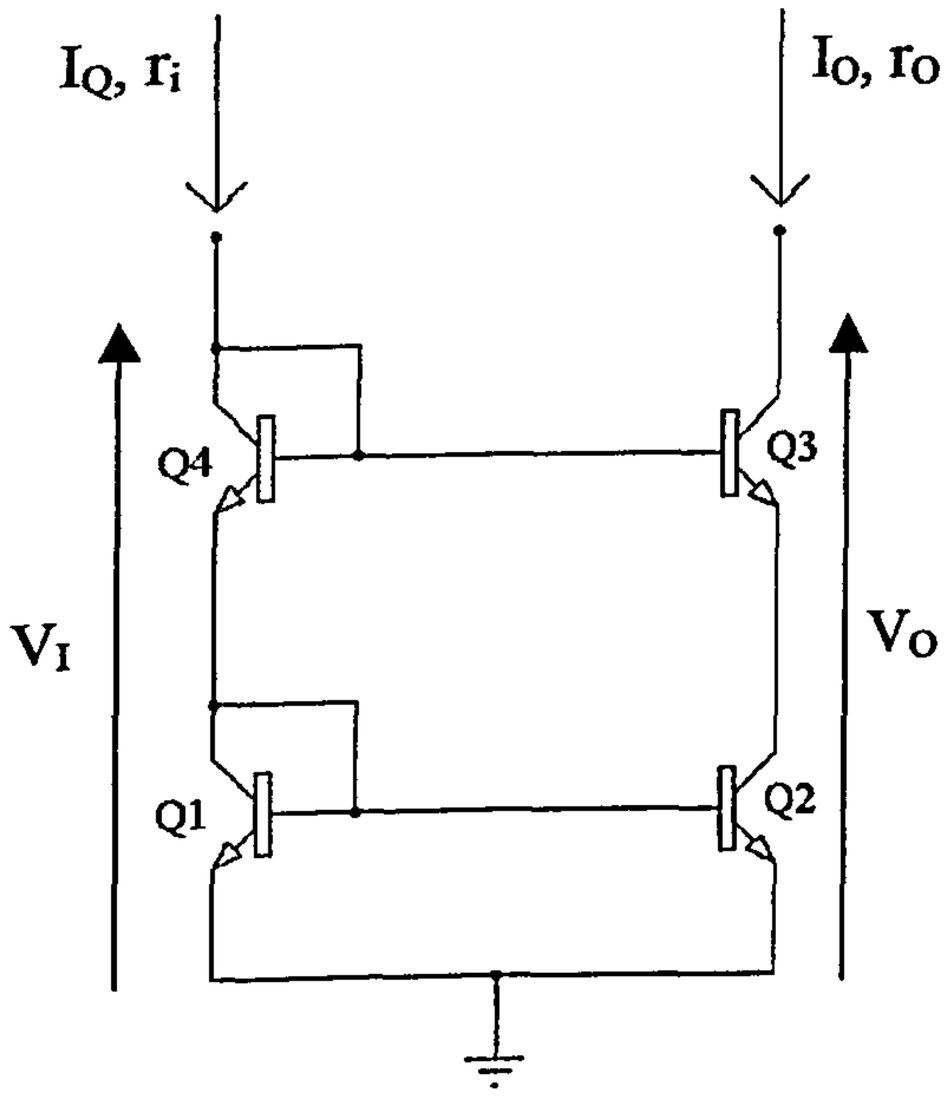


Figure.5.23. Cascode Current-Mirror

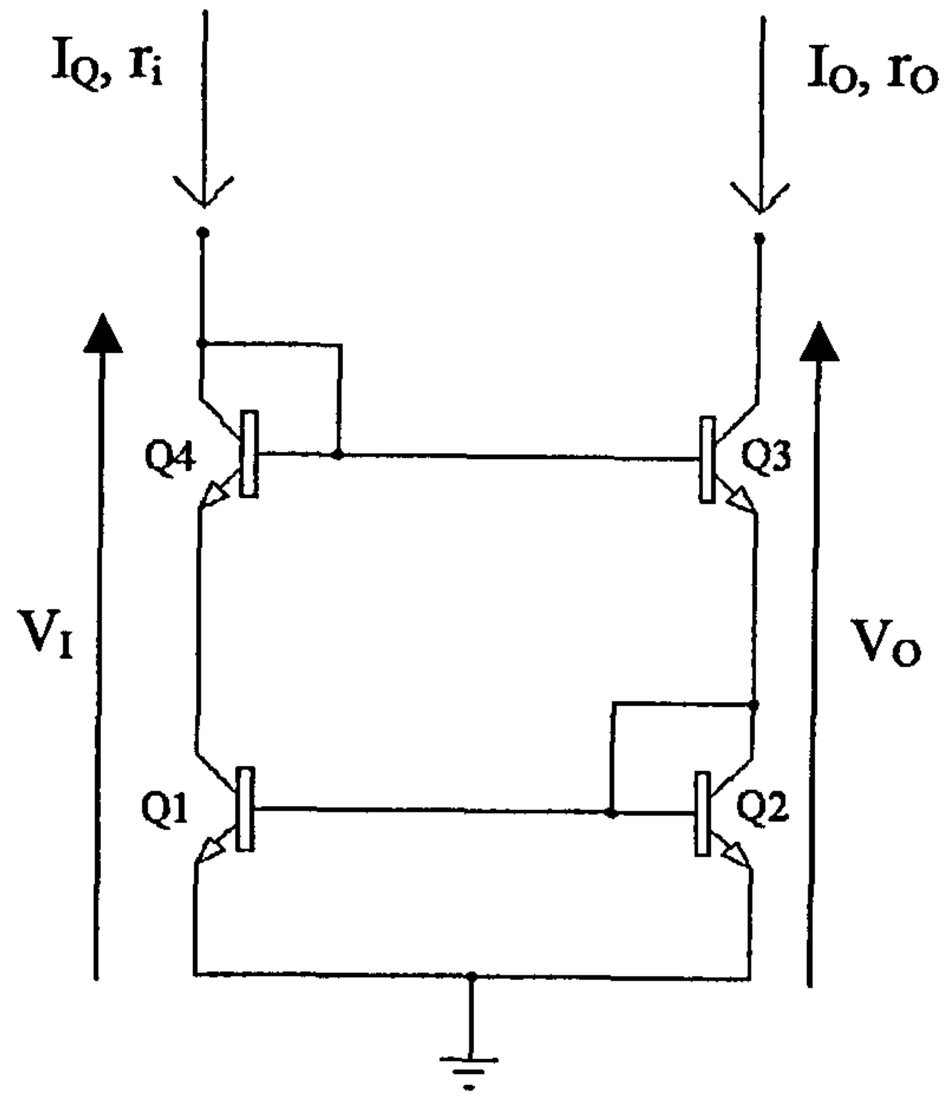


Figure.5.24. Modified Wilson Current-Mirror

	Cascode Current-Mirror **[5-3], [5-4]** (Fig.5.23)	Modified -Wilson Current-Mirror **[5-3], [5-4]** (Fig.5.24)
λ	$\frac{1}{(1+\frac{4}{\beta})} \pm \frac{V_{OS}}{V_T}$	$(1-\frac{2}{\beta^2}) \pm \frac{V_{OS}}{V_T}$
V_I (Min)	$2V_{BE}$	$2V_{BE}$
V_O (Min)	$2V_{BE}$	$2V_{BE}$
r_O	$\frac{\beta V_{AN}}{2I_Q}$	$\frac{\beta V_{AN}}{2I_Q}$

Table 5.2 Characteristics of the Cascode and Modified -Wilson Current-Mirrors

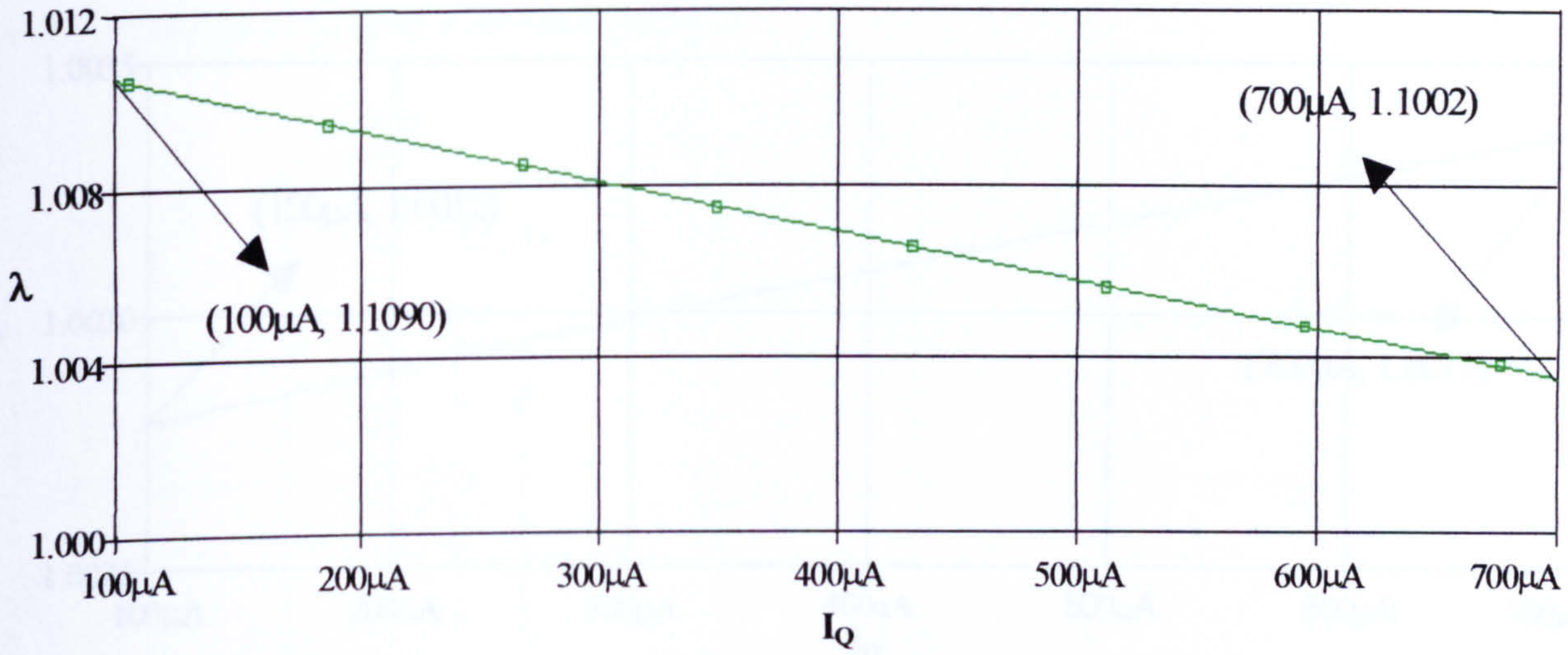


Figure.5.25. D.C.Current transfer ratio, λ, as a function of I_C for the Cascode Current-Mirror

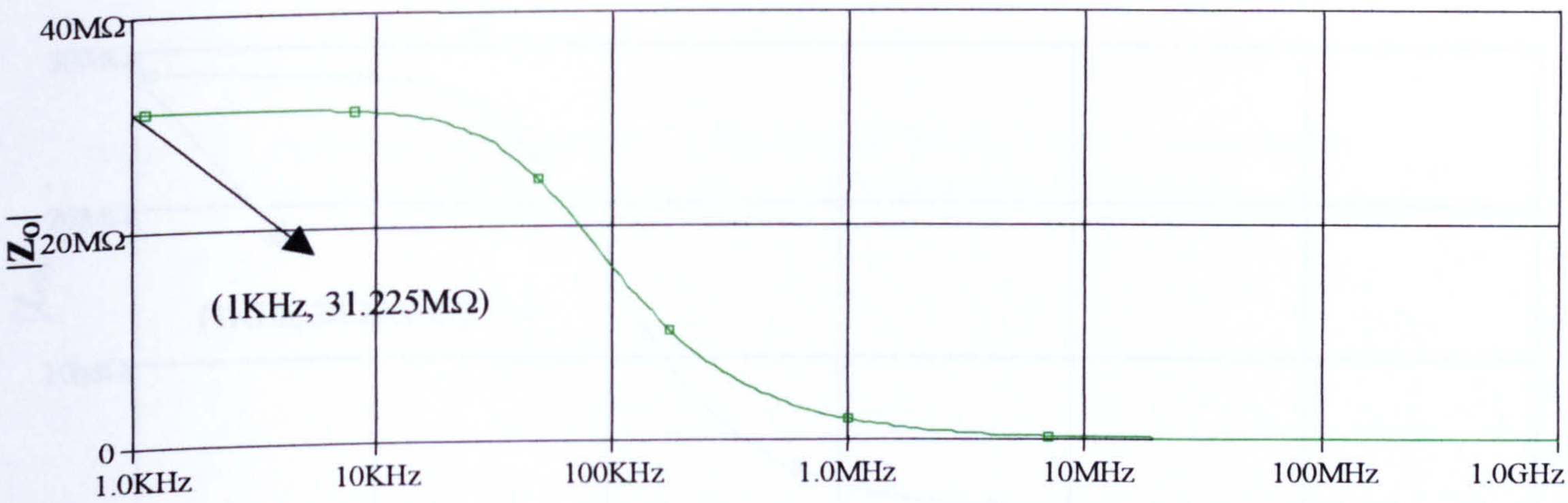


Figure.5.26. The output impedance of the Cascode Current-Mirror

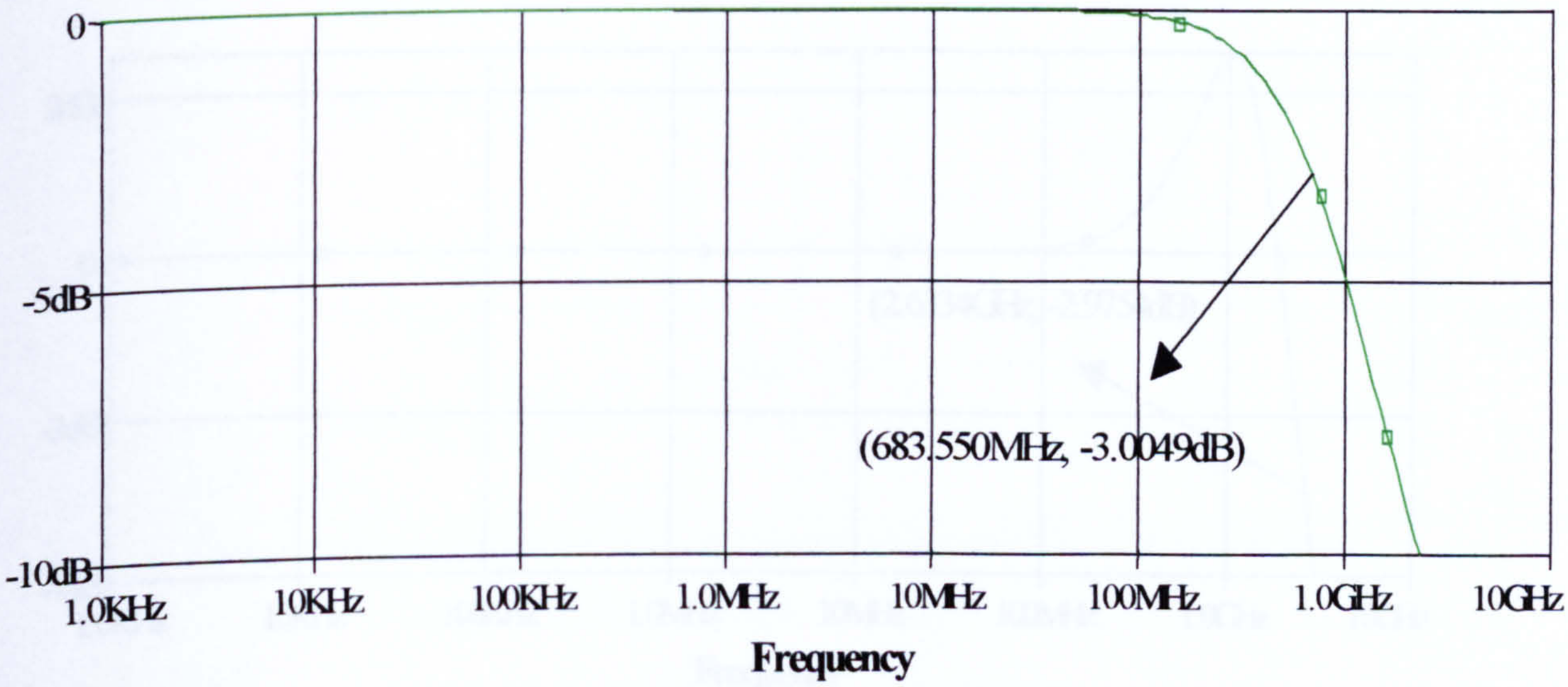


Figure.5.27. Frequency response of the Cascode Current-Mirror

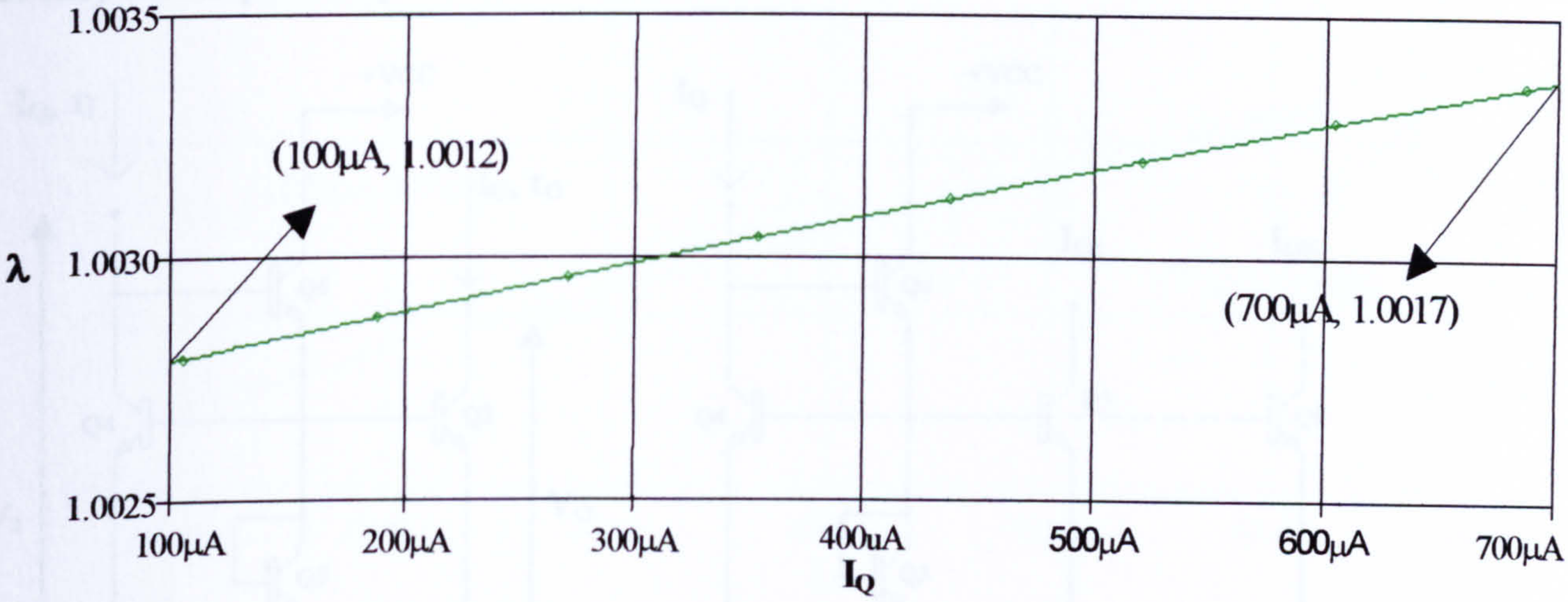


Figure. 5.28. D.C. Current transfer ratio, λ, as a function of I_C for the Modified-Wilson Current-Mirror

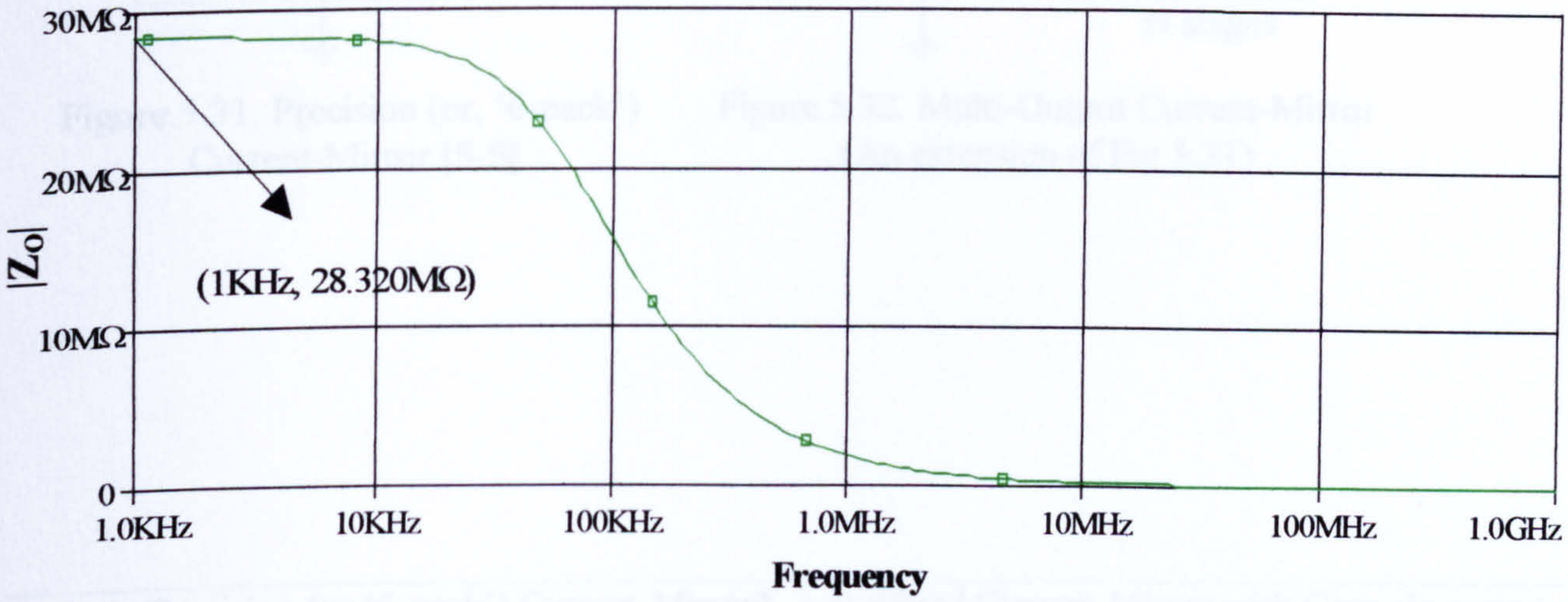


Figure.5.29. The output impedance of the Modified-Wilson Current-Mirror

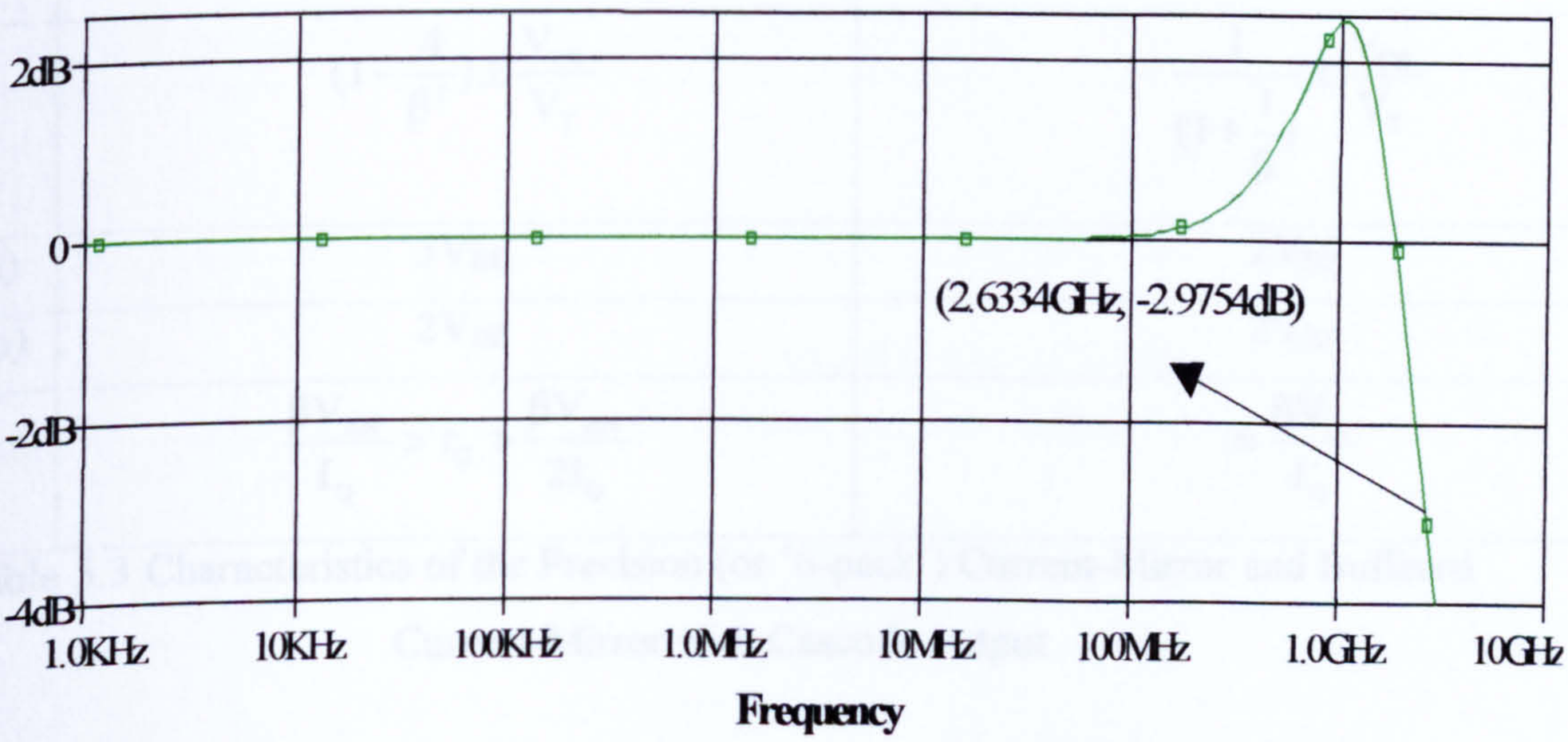


Figure.5.30. Frequency response of the Modified-Wilson Current-Mirror

(5.4.2) Multiple-output current mirror

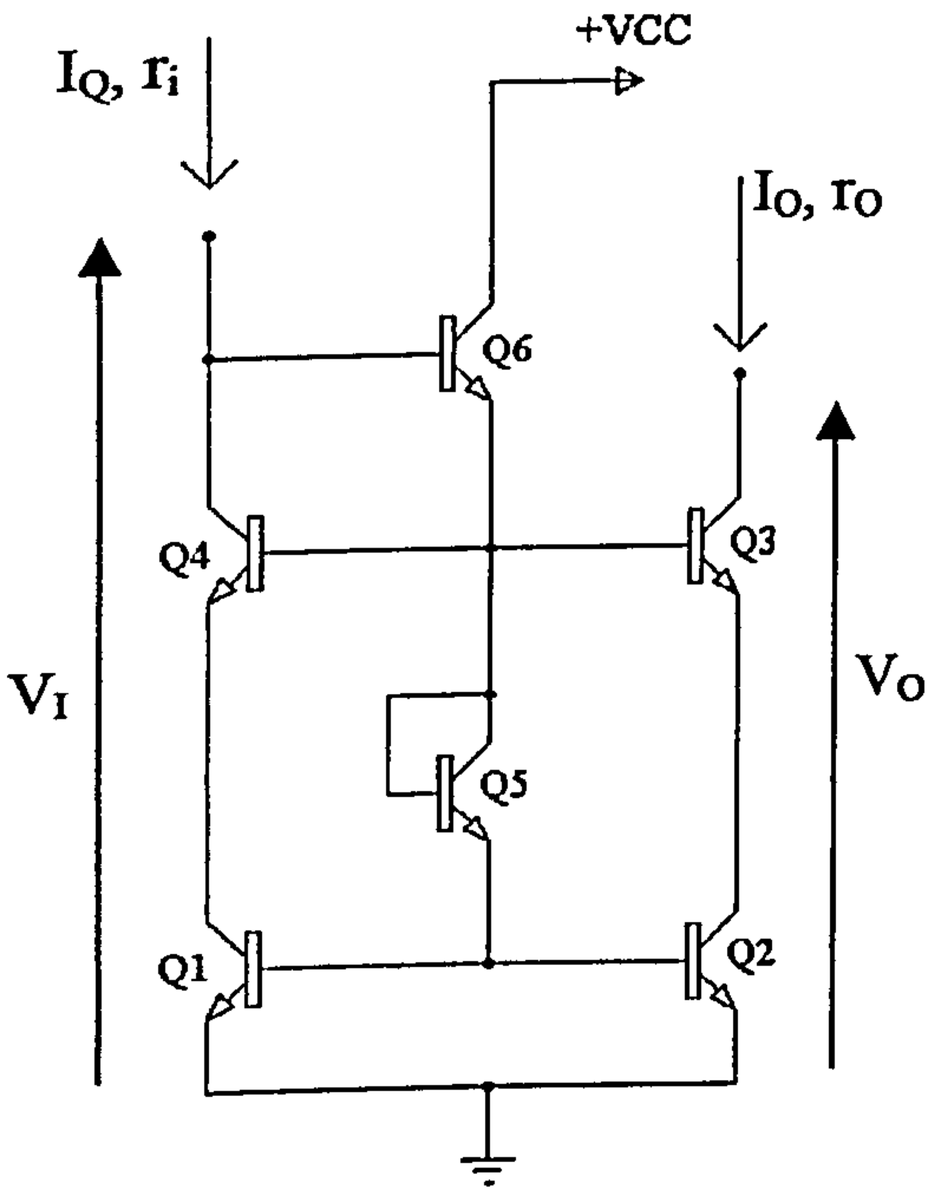


Figure.5.31. Precision (or, '6-pack') Current-Mirror **[5-5]**

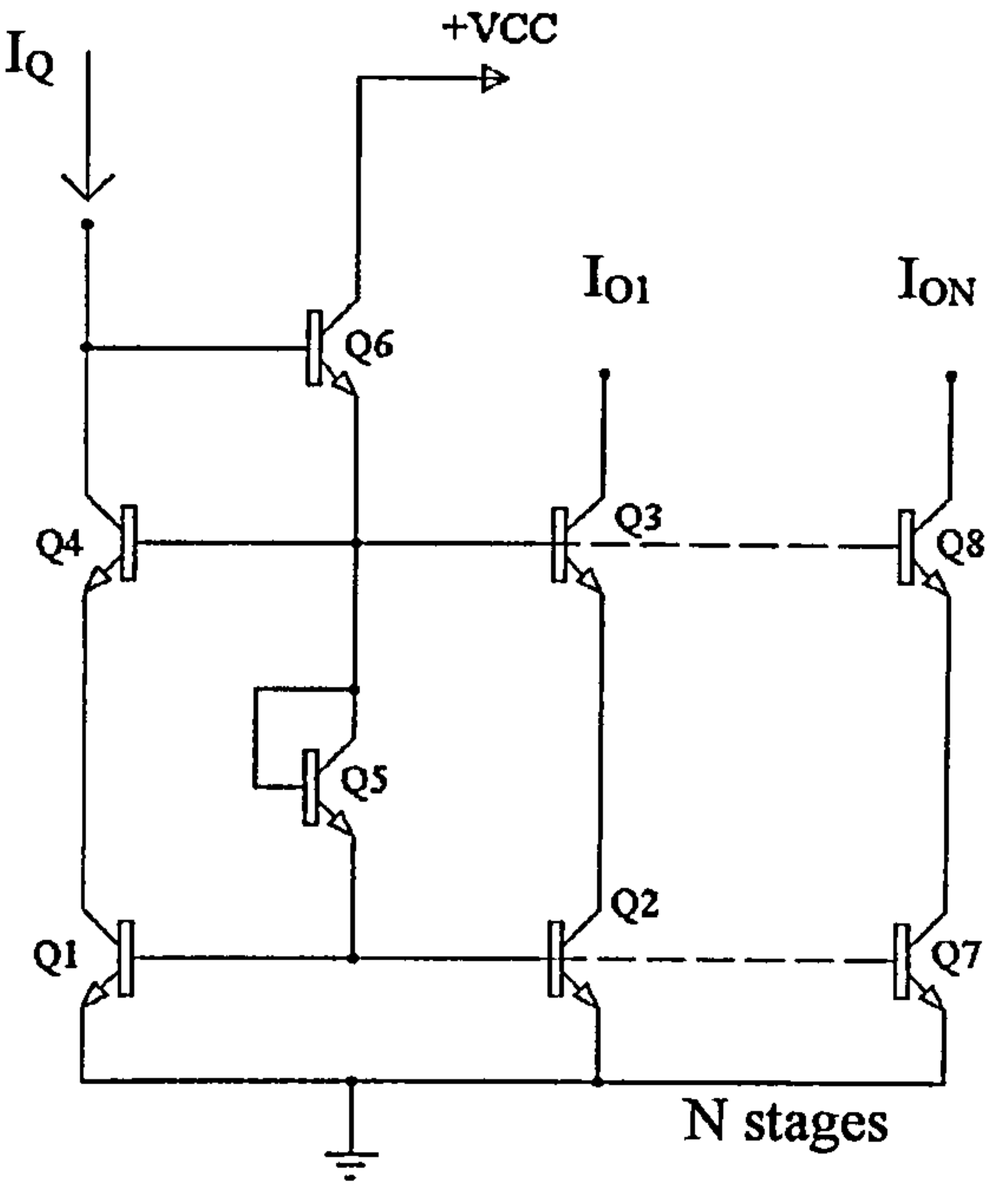


Figure.5.32. Multi-Output Current-Mirror (An extension of Fig.5.31)

	Precision (or '6-pack') Current-Mirror* (Fig.5.31) **[5-5]**	Buffered Current-Mirror with Cascode output (Fig.5.36)
λ	$(1-\frac{4}{\beta^2})\pm\frac{V_{OS}}{V_T}$	$\frac{1}{(1+\frac{1}{\beta})}\pm\frac{V_{OS}}{V_T}$
V_I (Min)	$3V_{BE}$	$2V_{BE}$
V_O (Min)	$2V_{BE}$	$2V_{BE}$
r_O	$\frac{\beta V_{AN}}{I_Q} > r_O > \frac{\beta V_{AN}}{2I_Q}$	$\approx\frac{\beta V_A}{I_Q}$

Table 5.3 Characteristics of the Precision (or '6-pack') Current-Mirror and Buffered Current-Mirror with Cascode output

* See Appendix 5.1 for derivation of λ.

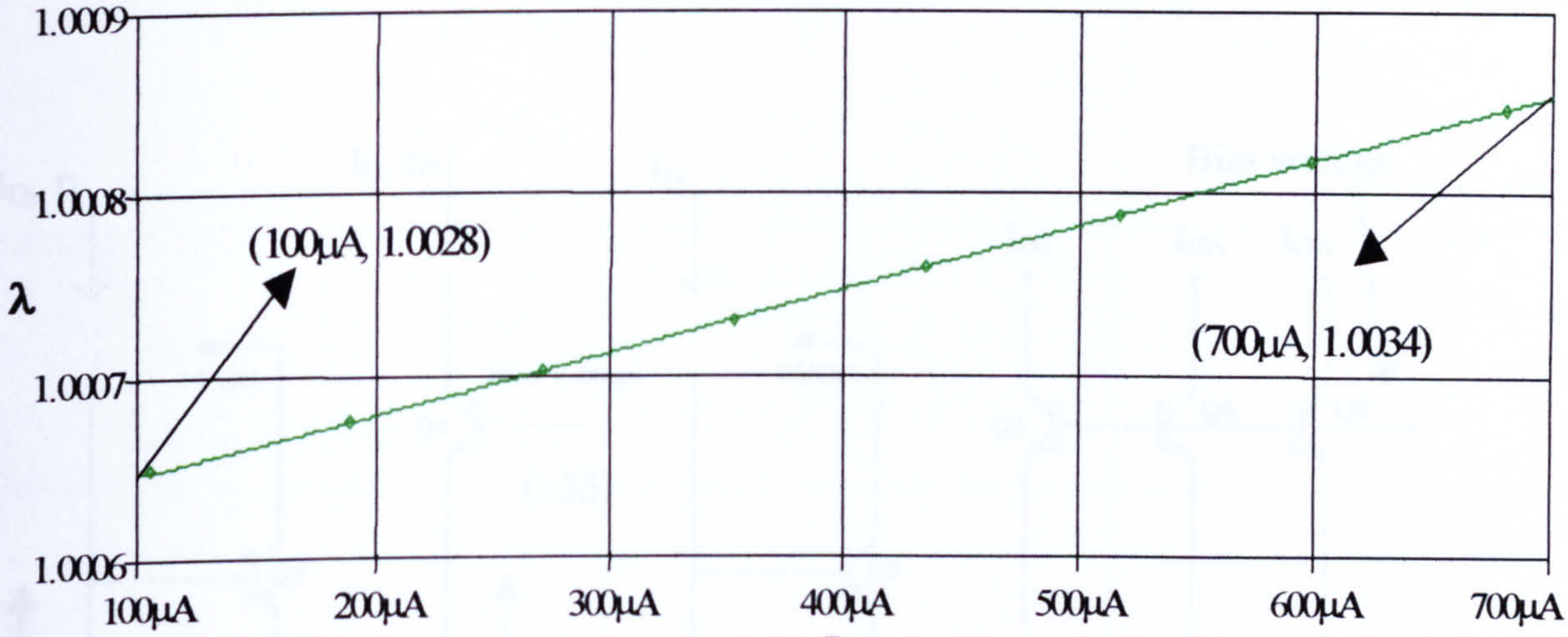


Figure. 5.33. D.C. Current transfer ratio, λ, as a function of I_C for the Precision Current-Mirror

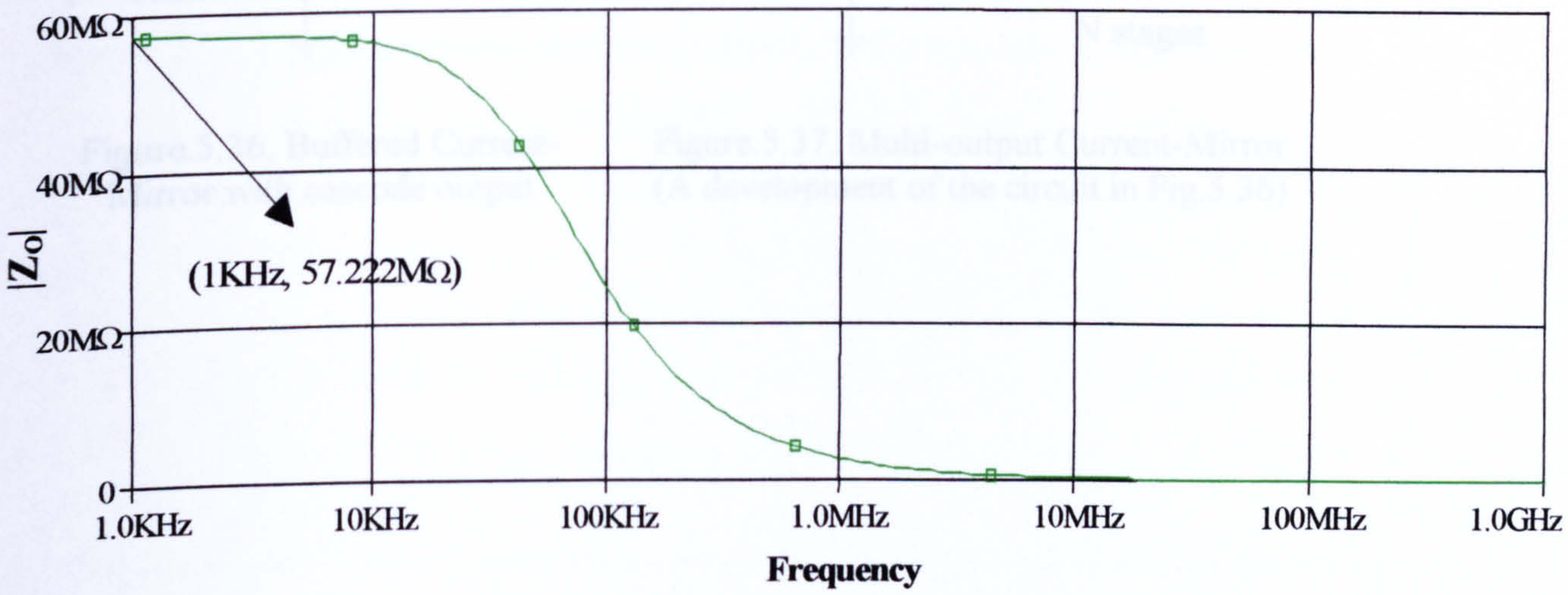


Figure.5.34. The output impedance of the Precision Current-Mirror

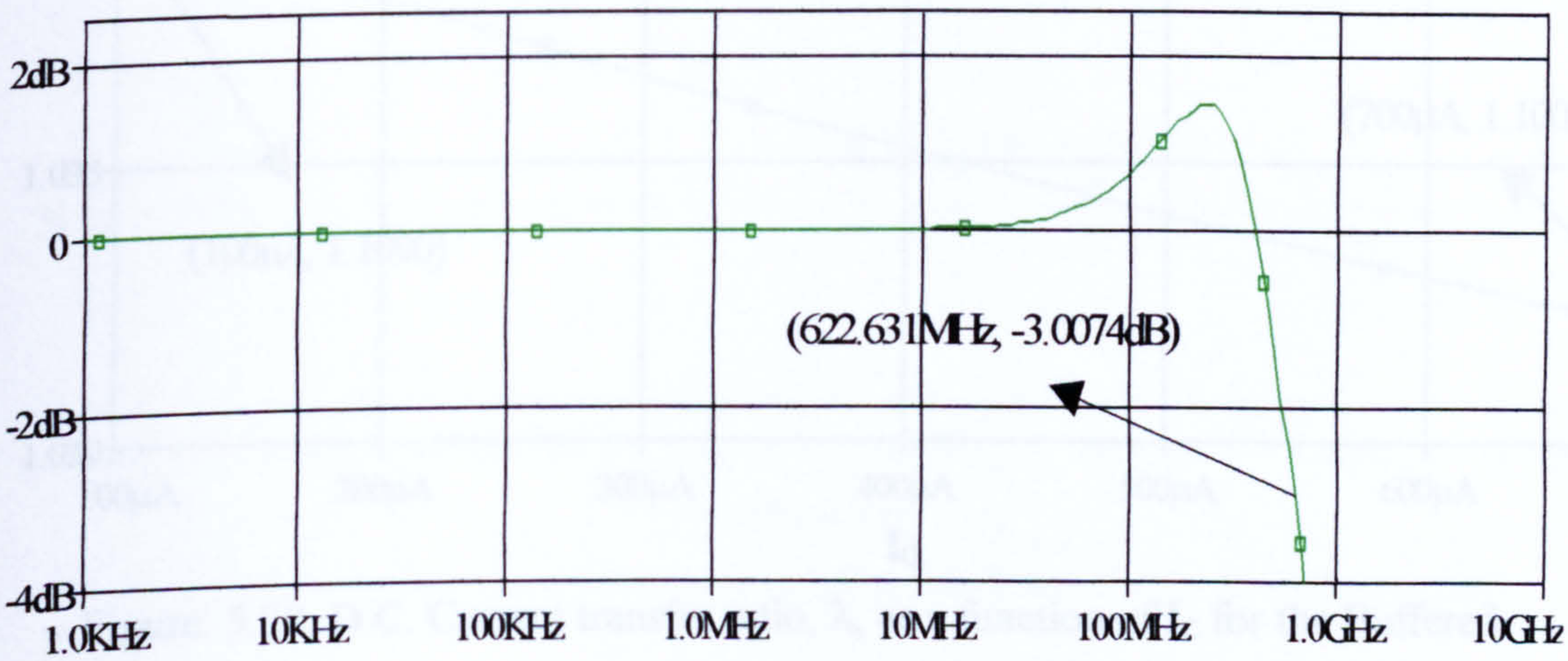


Figure.5.35. Frequency response of the Precision Current-Mirror

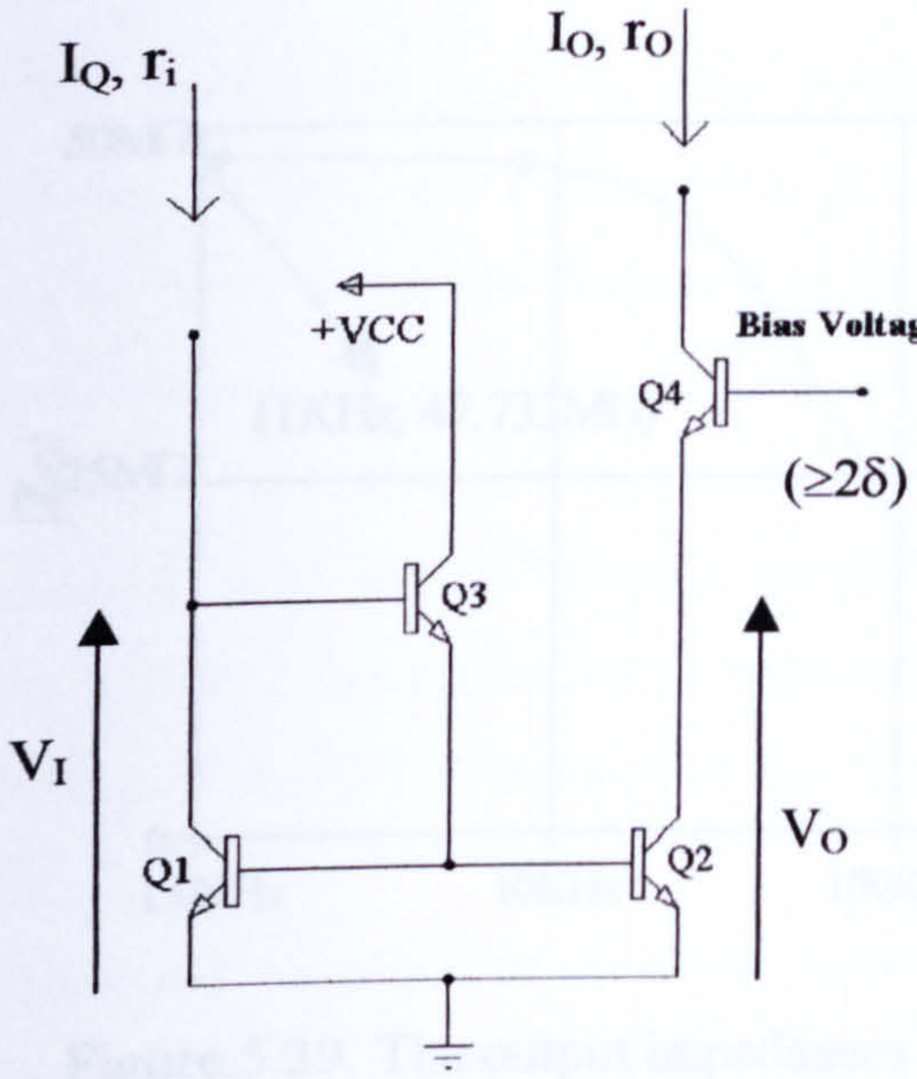


Figure.5.36. Buffered Current-Mirror with cascode output

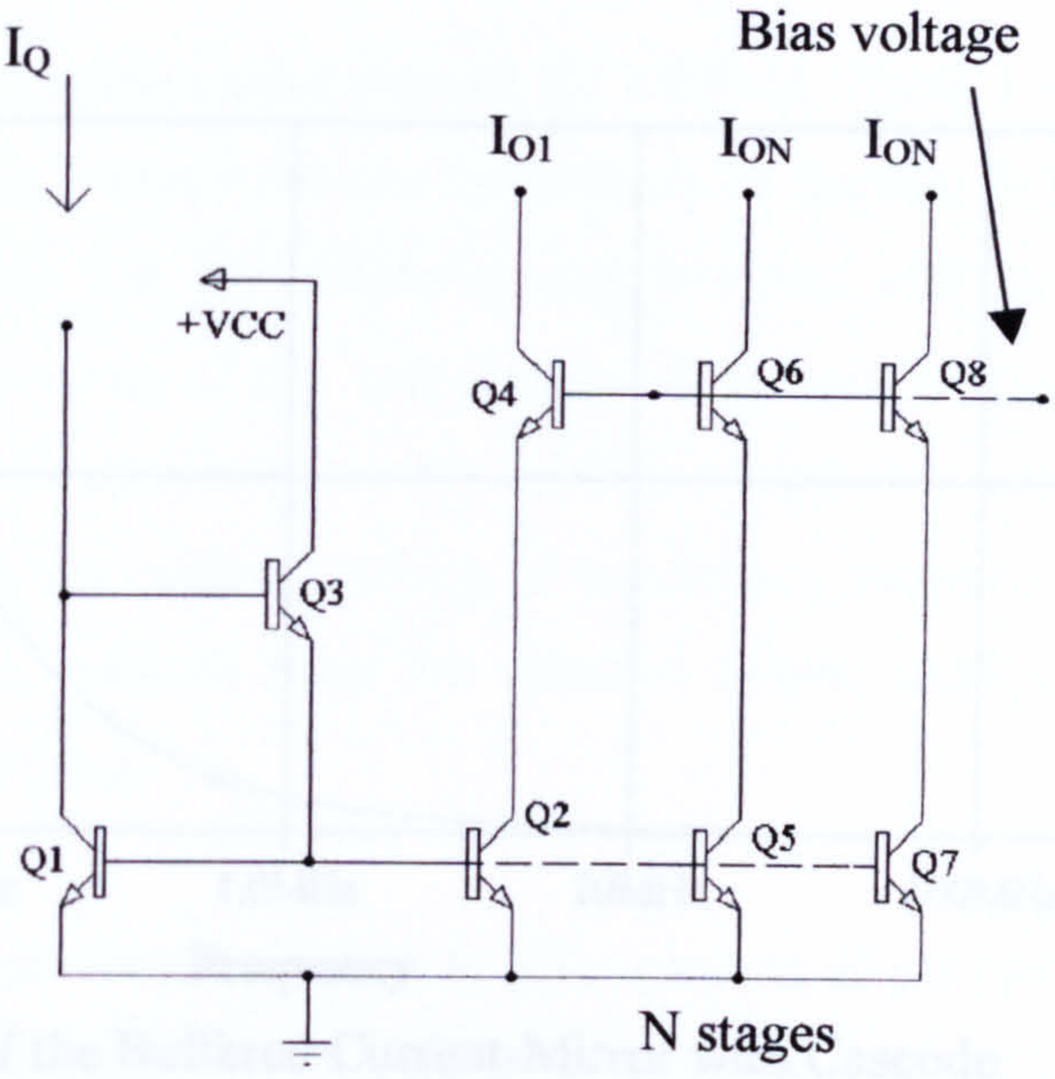


Figure.5.37. Multi-output Current-Mirror (A development of the circuit in Fig.5.36)

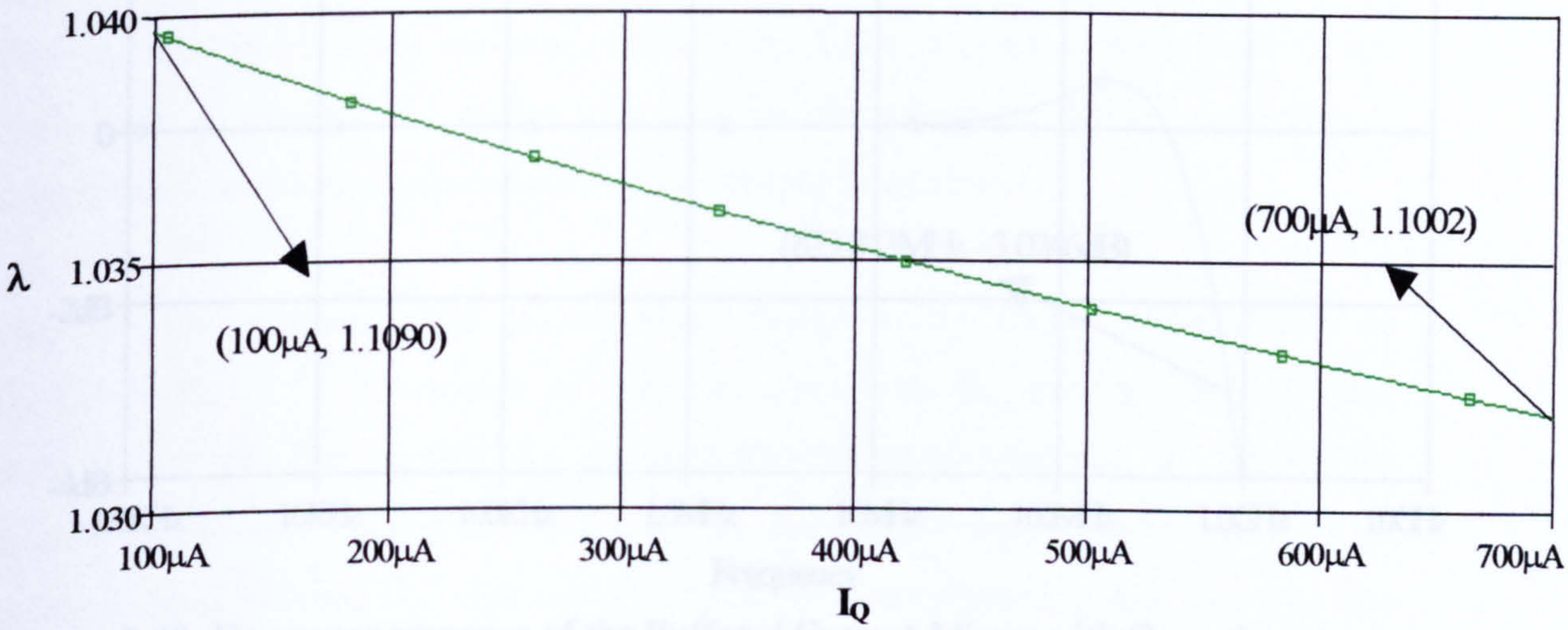


Figure. 5.38. D.C. Current transfer ratio, λ, as a function of I_C for the Buffered Current-Mirror with Cascode output

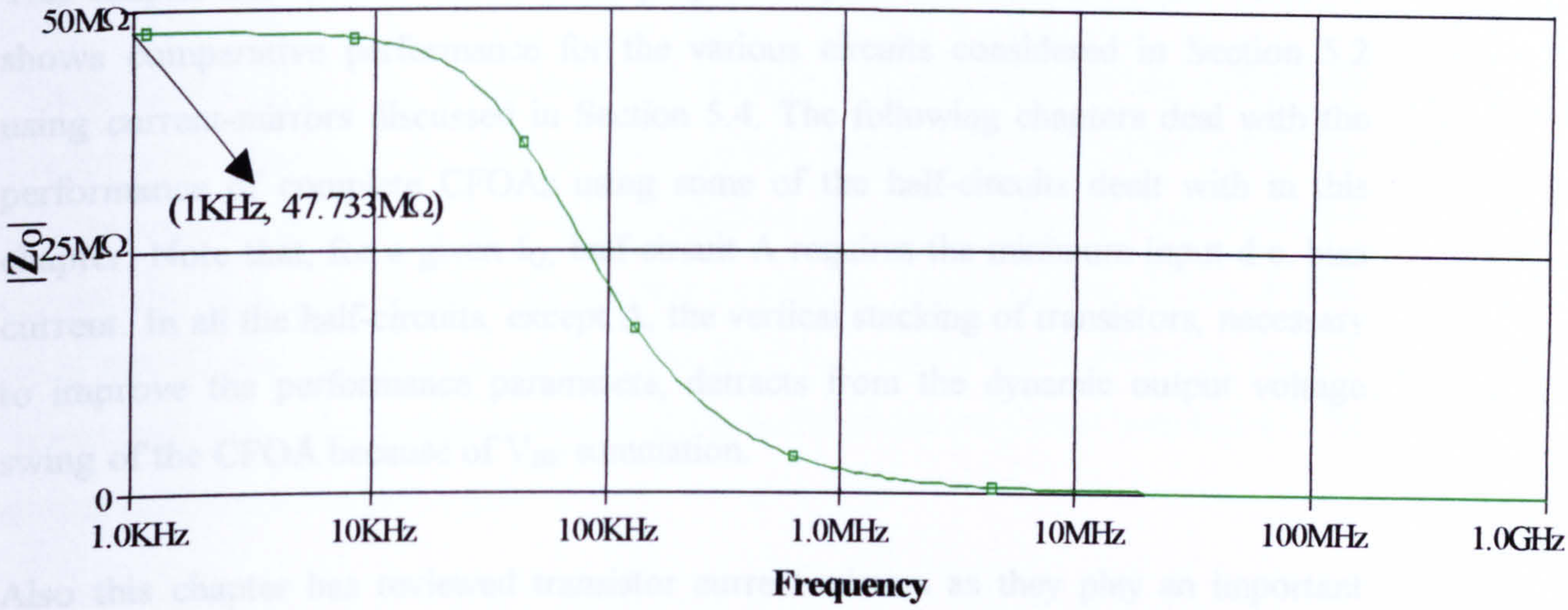


Figure.5.39. The output impedances of the Buffered Current-Mirror with Cascode output

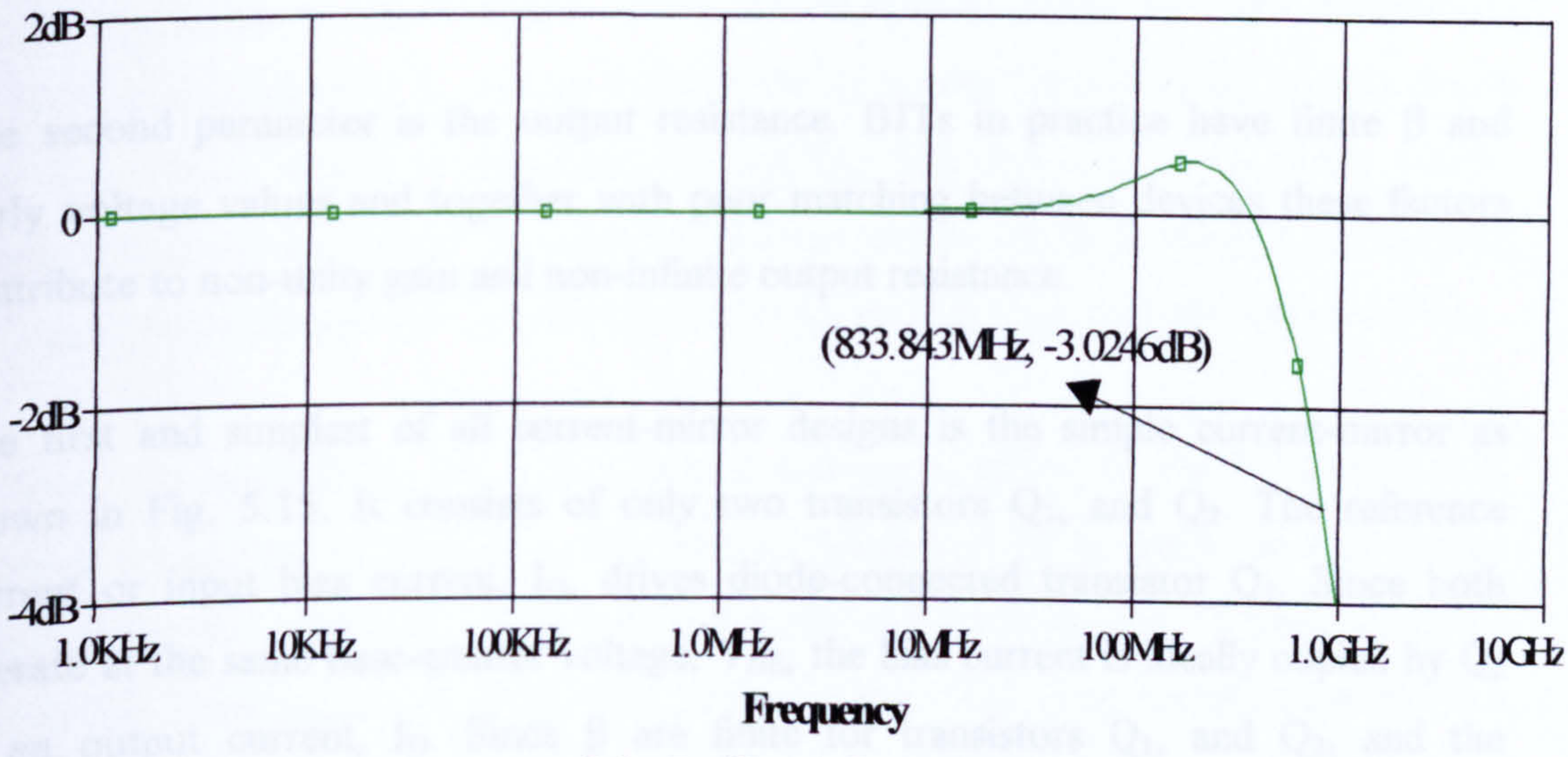


Figure.5.40. Frequency response of the Buffered Current-Mirror with Cascode output

Summary

This chapter has reviewed some newly proposed input circuits for a CFOA. Table 5.4 shows comparative performance for the various circuits considered in Section 5.2 using current-mirrors discussed in Section 5.4. The following chapters deal with the performance of complete CFOAs using some of the half-circuits dealt with in this chapter. Note that, for a given I_Q, half-circuit A requires the minimum input d.c. bias current. In all the half-circuits, except A, the vertical stacking of transistors, necessary to improve the performance parameters, detracts from the dynamic output voltage swing of the CFOA because of V_{BE} summation.

Also this chapter has reviewed transistor current-mirrors as they play an important part in CFOA designs by providing current bias, and current from the input stage of a the CFOA to a high impedance gain-node (Z). The importance of current-mirrors is recognised in this chapter, most popular current-mirrors designs being compared for their current-mirroring accuracy, and output impedance. As far as CFOA designs are concerned there are two essential parameters of current-mirrors that improve the CFOA with respect to CMRR, voltage offset, and slew rate. One of these parameters is the ratio, λ, between the output current, I_{out}, and the input reference current, I_{in}, for ideal current-mirrors λ is unity.

The second parameter is the output resistance. BJTs in practice have finite β and Early voltage values and together with poor matching between devices these factors contribute to non-unity gain and non-infinite output resistance.

The first and simplest of all current-mirror designs is the simple current-mirror as shown in Fig. 5.15. It consists of only two transistors Q_1, and Q_2. The reference current or input bias current, I_Q, drives diode-connected transistor Q_1. Since both operate at the same base-emitter voltage, V_{BE}, the bias current is ideally copied by Q_2 as an output current, I_O. Since β are finite for transistors Q_1, and Q_2, and the transistors are not well matched, the value of, λ, of the simple current-mirror is not closely defined and could be either greater than, or less than, unity. In the PSPICE simulation graph of Fig. 5.17, λ, is shown to be greater than unity. A PSPICE graph

of the simple current-mirror, gave an output resistance of 800 kΩ for a drive current of 0.1 mA. This compares with a theoretical value of 900 kΩ given by the r_{ce} (= 90 V early voltage/0.1 mA collector current) of Q_2.

This design in Fig. 5.16 is an improved version of the simple current-mirror and incorporates a transistor Q_3, whose emitter current supplies the base current of Q_1 and Q_2. The emitter current of Q_3 is then divided by (β +1), yielding to a much smaller current that has to be supplied by the bias current I_Q. Thus by using Q_3 as a buffer, transistor Q_1 now conducts a collector current (i.e., output) that is closer to the bias current value, I_Q. The output resistance of the buffered current-mirror was 802 kΩ for an input drive current of 0.1 mA.

The cascode current-mirror (Fig. 5.23) consists of two simple current-mirrors stacked one on top of the other. Fig. 5.25 shows the PSPICE simulation graph of, λ, the transfer function. It is not as close to unity as those of the simple, and Buffered current-mirrors. Despite the cascading of the two transistors, the output impedance result, $\frac{\beta \times r_{ce}}{2}$, of the circuit is not an improvement over that of the Wilson-mirror.

The circuit shown in Fig. 5.24 is known, as the Modified Wilson current-mirror. It is a simple but ingenious modification of the Wilson current-mirror and was designed by B. Hart, and R. Barker. It uses an extra diode connected transistor, Q_4, to help match the V_{CB} voltage values of transistors Q_1 and Q_2. The inclusion of Q_4 in the current input path does not change the negative feedback action of the circuit but by matching its V_{BE} drop to that across Q_3 both transistors Q_1 and Q_2 must operate with zero V_{CB}.

In terms of maximising the λ and output resistance, either of the Wilson current-mirrors appear to be a good design choice. However, to improve on this design, without simply using better matched transistors, the Precision (or, '6-pack') current-mirror has been conceived **[5-5]**, This shown in Fig. 5.31. The current transfer ratio, λ, transfer function is given in Appendix 5.1 but the result, shown in Table 5.3, presents an interesting situation. The transistors Q_1 and Q_2 should match so that I_{s1} copies I_{s2} and the reciprocal of the β values β_3 and β_4 should ideally cancel. Although

complete cancellation is unlikely at least their β values should be closely matched for given current input. The PSPICE simulation graph for the output resistance is shown in Fig. 5.33 as almost 60 MΩ, which is closer to βr_{CE} than $\beta(r_{CE}/2)$.

The Buffered current-mirror with cascode output shown in Fig. 5.36 is the last of the popular current mirror architectures to be discussed. This is a development of the Buffered current-mirror. The output resistance of the Buffered current-mirror with cascode output is not that of a single transistor collector impedance, r_{ce} like that of the simple and Buffered current-mirrors. The PSPICE simulation graph of the output resistance is shown in Fig. 5.39 as almost a 50 MΩ, which is larger than that of the Wilson, Cascode, and Modified Wilson current-mirrors.

In conclusion, Table 5.4 compares the performance of the various half circuit, using the current-mirrors, with respect to CMRR, offset voltage and slew-rate.

	IMPROVED PARAMETER		
Half-circuit	**CMRR (ρ)**	**V_{os}**	**SR or S**
B	✓		
C	✓	✓	
D	✓	✓	✓
E	✓	✓	
F	✓	✓	✓
G	✓	✓	✓

Table 5.4. Half-circuit performance comparison

(5.5) References

[5-1] S. Franco, 'Design with Operational Amplifiers and Analog ICs,' McGraw Hill, 3rd Edition, Chapter 6, pp. 294, 2002.

[5-2] Vere Hunt, M. A., Charles, K. 'Design and development of a high slew-rate operational amplifier.' Ph.D Thesis. Oxford Brookes University, 1992. pp. 33–55.

[5-3] Sedra, A. S., and Smith K. C., 1998, 'Microelectronic Circuits', Oxford University Press, 4th Edition, pp. 485–631.

[5-4] Gray, P. R., and Meyer R. G., 1993, 'Analysis and Design of Analog Integrated Circuits', Wiley, 3rd Edition, pp. 269–353.

[5-5] Vere Hunt M.A, 'Design and development of high slew-rate operational amplifier', PhD thesis, Oxford Brookes University, 1992, pp 45–46.

APPENDIX 5

APP 5.1 The d.c. current transfer-ratio, λ, of the '6-pack' of Current-Mirror

Fig.A.5.1 is a redrawn and relabelled of Fig.5.31.

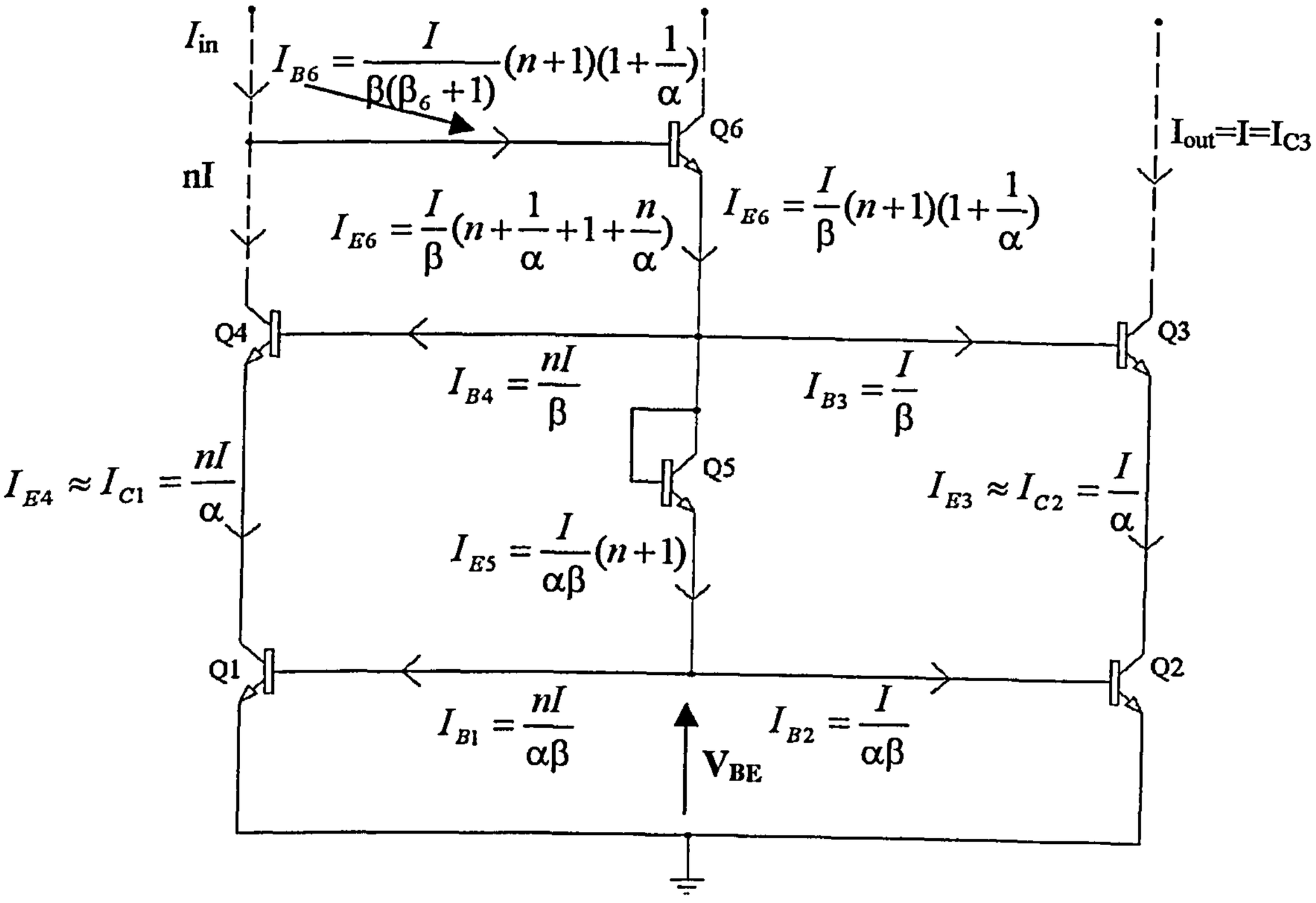


Figure A 5.1

I_{C1} (of transistor Q_1) = I_{S1} exp (V_{BE}/V_T)

I_{C2} (of transistor Q_2) = I_{S2} exp (V_{BE}/V_T)

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}}, \qquad \text{Therefore } I_{C1} = (\frac{I_{S1}}{I_{S2}}) \cdot I_{C2}$$

$$\text{Let} \quad (\frac{I_{S1}}{I_{S2}}) = n$$

$$\therefore I_{C1} = n \cdot I_{C2} \qquad : \qquad I_{out} = I = I_{C3}$$

$$I_{in} = nI + \frac{I}{\beta(\beta_6 + 1)}(1+n)(1+\frac{1}{\alpha}),$$ by Kirchoff's Current Law

But, $(1+\frac{1}{\alpha}) = [1+\frac{\beta+1}{\beta}] = (2+\frac{1}{\beta})$

Therefore, $I_{in} = nI + \frac{I}{\beta(\beta_6 + 1)}(1+n)(2+\frac{1}{\beta})$

Since $I_{out} = I$,

$$\therefore \frac{I_{out}}{I_{in}} = \frac{I}{nI + \frac{I}{\beta(\beta_6 + 1)}(1+n)(2+\frac{1}{\beta})}$$

$$\frac{I_{out}}{I_{in}} = \frac{1}{n + \frac{(1+n)(2+\frac{1}{\beta})}{\beta(\beta_6 + 1)}}$$

Assuming $(\beta_6+1) \approx \beta_6$ and $\beta >> 1$,

$$\therefore \frac{I_{out}}{I_{in}} \approx \frac{1}{n}[\frac{1}{1 + \frac{2(1+n)}{\beta\beta_6}}]$$

The term in the denominator is small compared with unity; at this stage we can use the binomial expansion and retain the first two terms only.

$$\therefore \lambda = \frac{I_{out}}{I_{in}} \approx \frac{1}{n}[1 - \frac{2(1+n)}{\beta\beta_6}]$$

If $n = 1$ (precisely) the equation mentioned above gives

$$\lambda = \frac{I_{out}}{I_{in}} \approx [1 - \frac{4}{\beta\beta_6}]$$

This equation can be further reduced to,

$$\lambda = \frac{I_{out}}{I_{in}} \approx \frac{1}{n}[1 - \frac{2(1+n)}{\beta^2}]$$

for $n \neq 1$, but $\beta_6 = \beta$,

We can now express n in terms of the offset voltage. This is the difference in V_{BES} when the devices are operated at the same collector currents I_R.

$$V_{BE1} = V_T \log_e \frac{I_R}{I_{S1}}$$

and, $V_{BE2} = V_T \log_e \frac{I_R}{I_{S2}}$

Therefore, $(V_{BE1} - V_{BE2}) = V_{OS} = V_T \log_e \frac{I_{S2}}{I_{S1}}$

Or, in another words, $(\frac{I_{S2}}{I_{S1}}) = \exp(\frac{V_{OS}}{V_T})$

If $(\frac{I_{S2}}{I_{S1}}) = (\frac{1}{n})$, Then $(\frac{1}{n}) = \exp(\frac{V_{OS}}{V_T})$

For n=1 (precisely), then V_{OS}=zero: for n close to unity, $V_{OS} << V_T$. Hence, we can expand the exponential, and use only for the first two terms.

$$(\frac{1}{n}) \approx [1 + (\frac{V_{OS}}{V_T})]$$

However, since in n we can have n<1 or n>1, we should write it as:

$$(\frac{1}{n}) \approx [1 \pm (\frac{V_{OS}}{V_T})]$$

Note that V_{OS} is expressed as a magnitude only in data sheets.

$$\therefore \lambda \approx (1 \pm \frac{V_{OS}}{V_T})[1 - \frac{4}{\beta\beta_6}]$$

Multiplying out and keeping only about the first two terms, gives,

$$\lambda \approx \left[(1 \pm \frac{V_{OS}}{V_T}) - \frac{4}{\beta\beta_6} \right]$$

Or, in the case of $\beta_6=\beta$,

$$\lambda \approx \left[(1 \pm \frac{V_{OS}}{V_T}) - \frac{4}{\beta^2} \right]$$

APP 5.2 The BJT model used

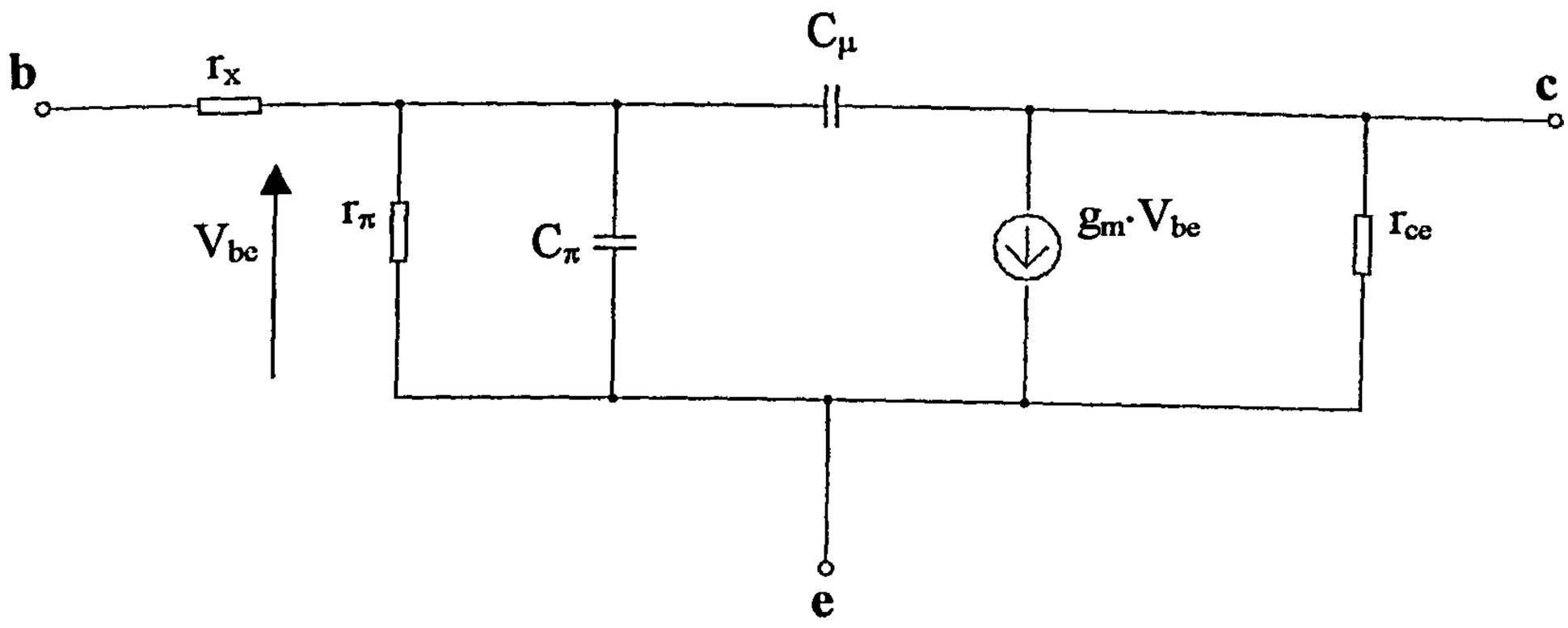


Figure A 5.2

This is a hybrid (π) small-signal model for the BJT

C_π= sum of depletion and diffusion capacitances associated with the emitter-base junction (~2pF)

C_μ= depletion capacitance of reverse biased C-B junction (~0.2pF→3pF)

r_x= base bulk resistance (usually 50Ω→300Ω)

C_π, C_μ, and r_x have almost no effect on the amplification at low frequencies but reduce gain as the frequency rises

$$r_{be} = \frac{V_{be}}{i_b} = \frac{\beta}{g_m} \quad ; \quad g_m = \frac{I_{CQ}}{V_T} \quad ; \quad r_{ce} = \frac{V_A}{I_{CQ}}$$

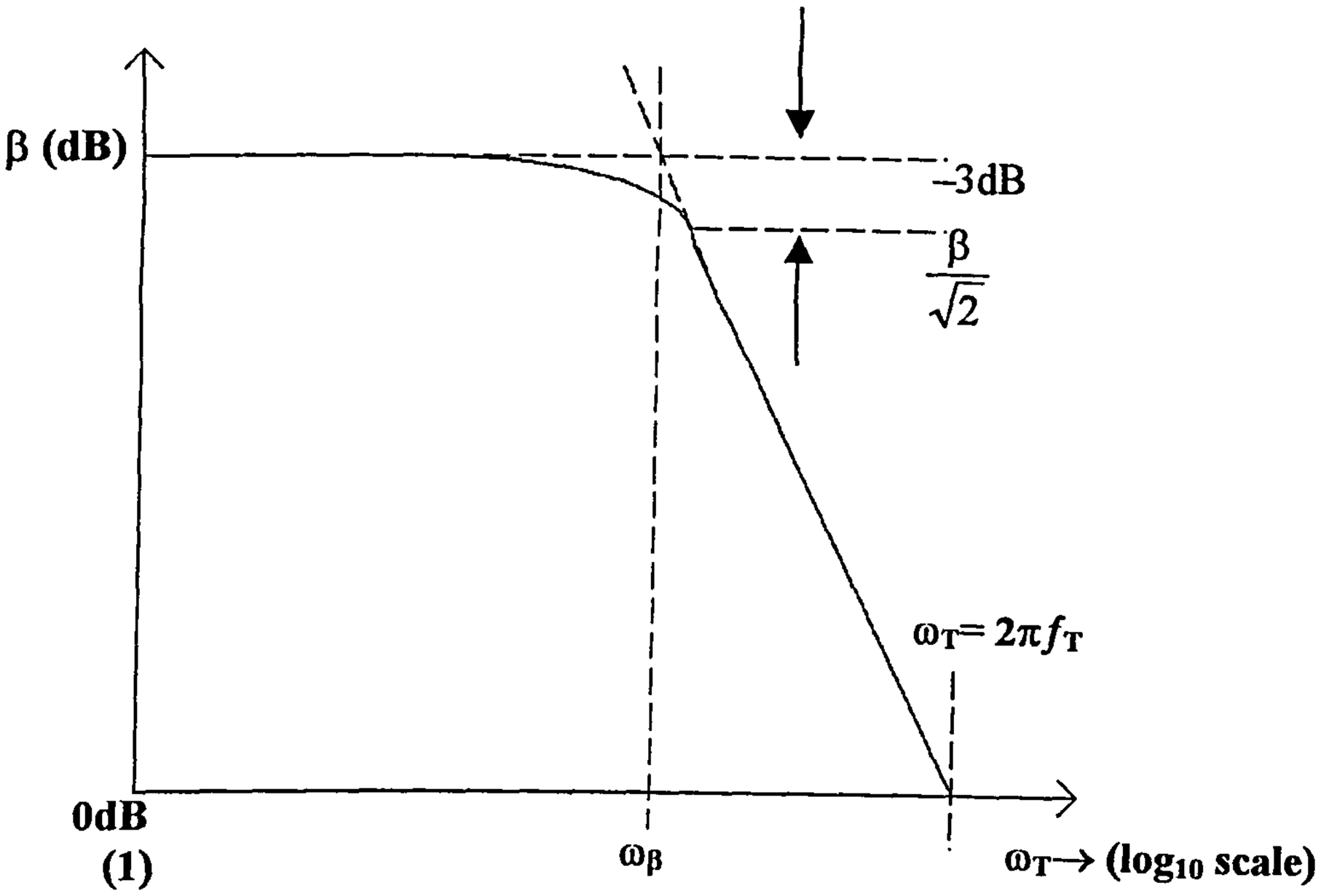


Figure A 5.3

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

For the complementary bipolar XFCB PSpice model

BJT Type	NPN	PNP
CJC=C_μ	7×10^{-14}F	7×10^{-14}F
CJE=C_π	5.7×10^{-14}F	4.8×10^{-14}F
V_A(V)	90	23

Table 5.5 XFCB main PSpice parameter model

CHAPTER 6

Current feedback operation amplifier designs using bootstrapping

(6.1) Introduction

This chapter considers the design of CFOAs that incorporate new input circuits. The first six of these were introduced in Chapter Five; those that follow are variations of them.

The new CFOA designs exhibit a low DC offset-voltage, wide bandwidth, high CMRR and improved gain accuracy, enabling them to be used in applications requiring variable closed-loop gains with constant bandwidth, such as in automatic-gain-control, video, graphics and multimedia applications.

The performance of each new CFOA is compared with that of the basic one shown in Fig.3.1. OrCAD PSpice was used to verify the operation and performance of the circuits. The technology used in the simulation was the complementary bipolar XFCB process of Analog Devices, Santa Clara, California.

In all the new designs, unless otherwise indicated, the main current biasing circuitry is the same as that used in Fig 6.1: Furthermore, all simulation measurements refer to I_Q=0.2mA, V_{CC}= ±5V, at room temperature (27°C).

(6.2) Reverse bootstrapping

(6.2.1) Performance with half-circuit B

In Fig.6.1, the buffered current mirrors, (Q_7+Q_8+Q_9+Q_{17}+Q_{21}) and (Q_5+Q_6+Q_{10}+Q_{18}+Q_{26}) are supplied with a common input current, I_Q, via the resistor R_Q. Since the section of the two buffered mirrors is the same, only one is considered here, (Q_7+Q_8+Q_5+Q_{17}+Q_{21}). The output from Q_7 supplies the cascode transistor Q_{11} with the emitter current for Q_1. The base bias voltage for Q_{11} is provided by the voltage drop across the series connected and diode-strapped transistors Q_{15}, Q_{13} the biasing current for which is supplied by an output of Q_{18} in the other buffered current-mirror. The cascading of Q_7 ensures greater constancy in the emitter current of Q_1 as the input voltage changes: it results in a better CMRR and less variation of incremental input resistance over the input voltage range. The output from Q_{17} supplies current for the bias circuitry of cascode transistor Q_{12} and the output from Q_{21} supplies biasing current for Q_{22}, Q_{23} connected to the base of cascode transistor Q_{19} in the reverse-bootstrapping scheme **[6-1]**.

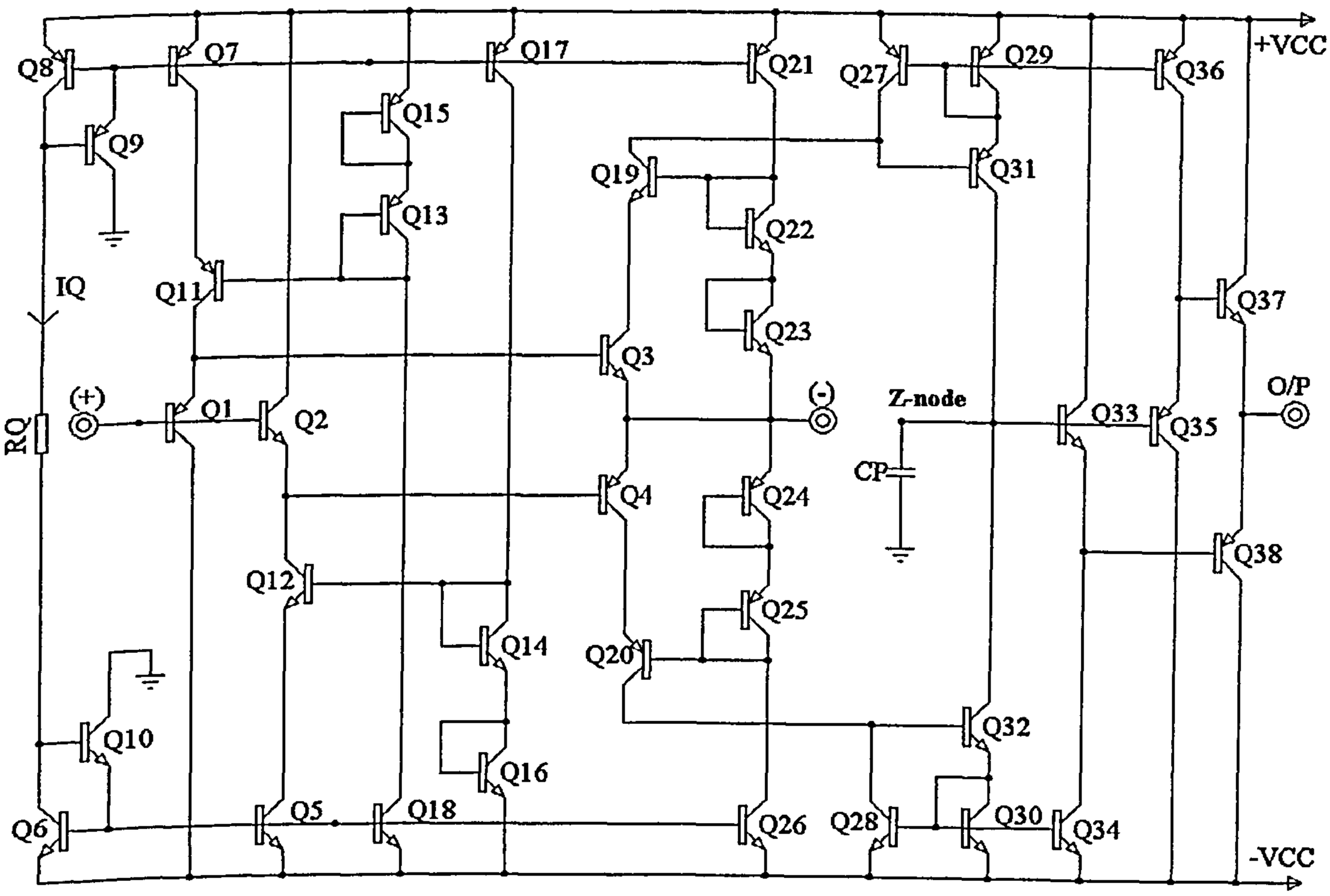


Figure 6.1 Circuit diagram of a CFOA with half-circuit B

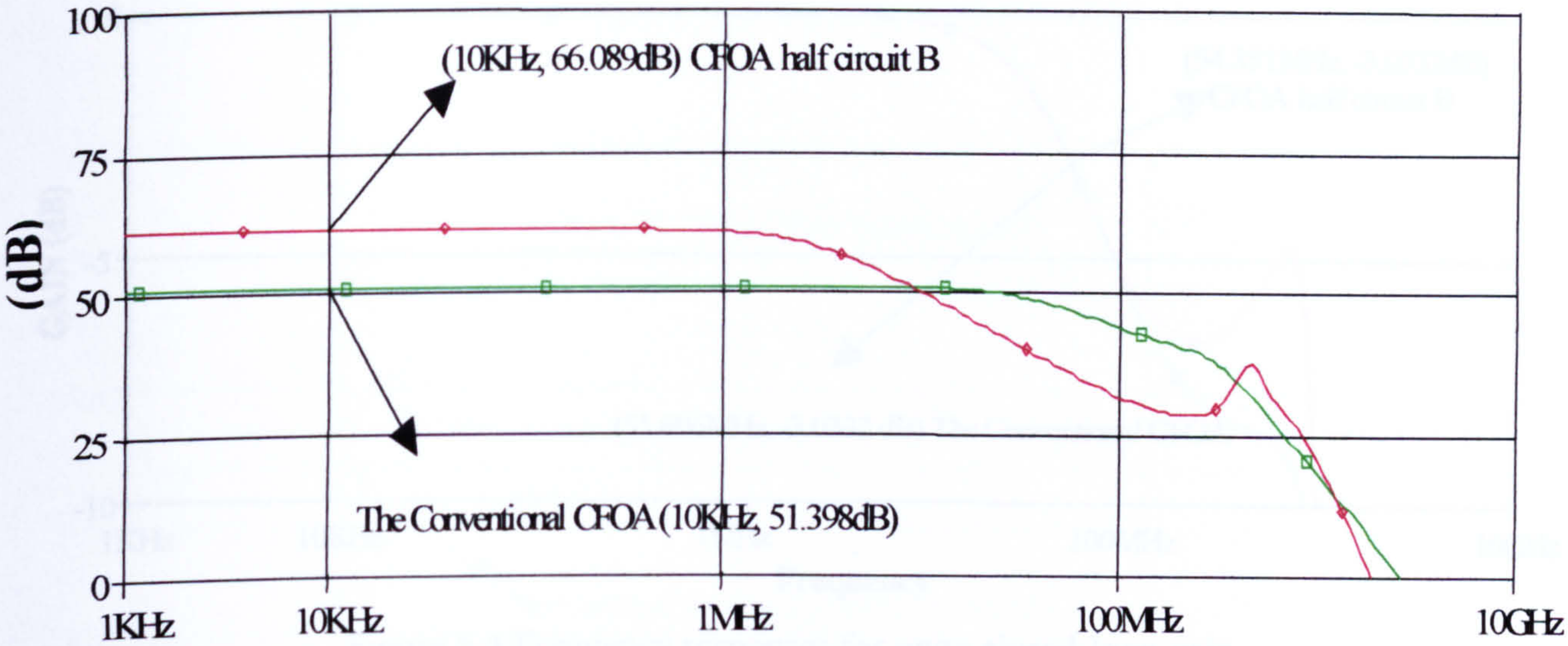


Figure 6.2 CMRR~Frequency

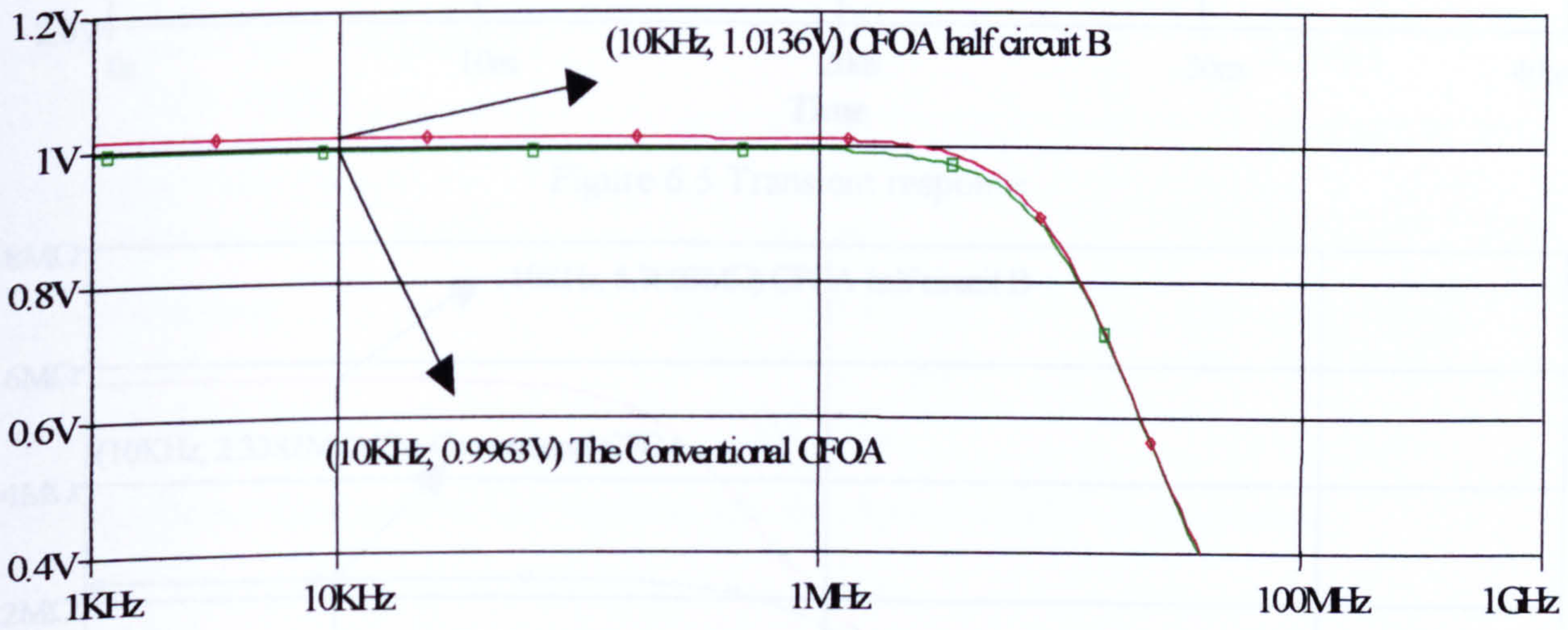


Figure 6.3 AC gain accuracy ~ Frequency

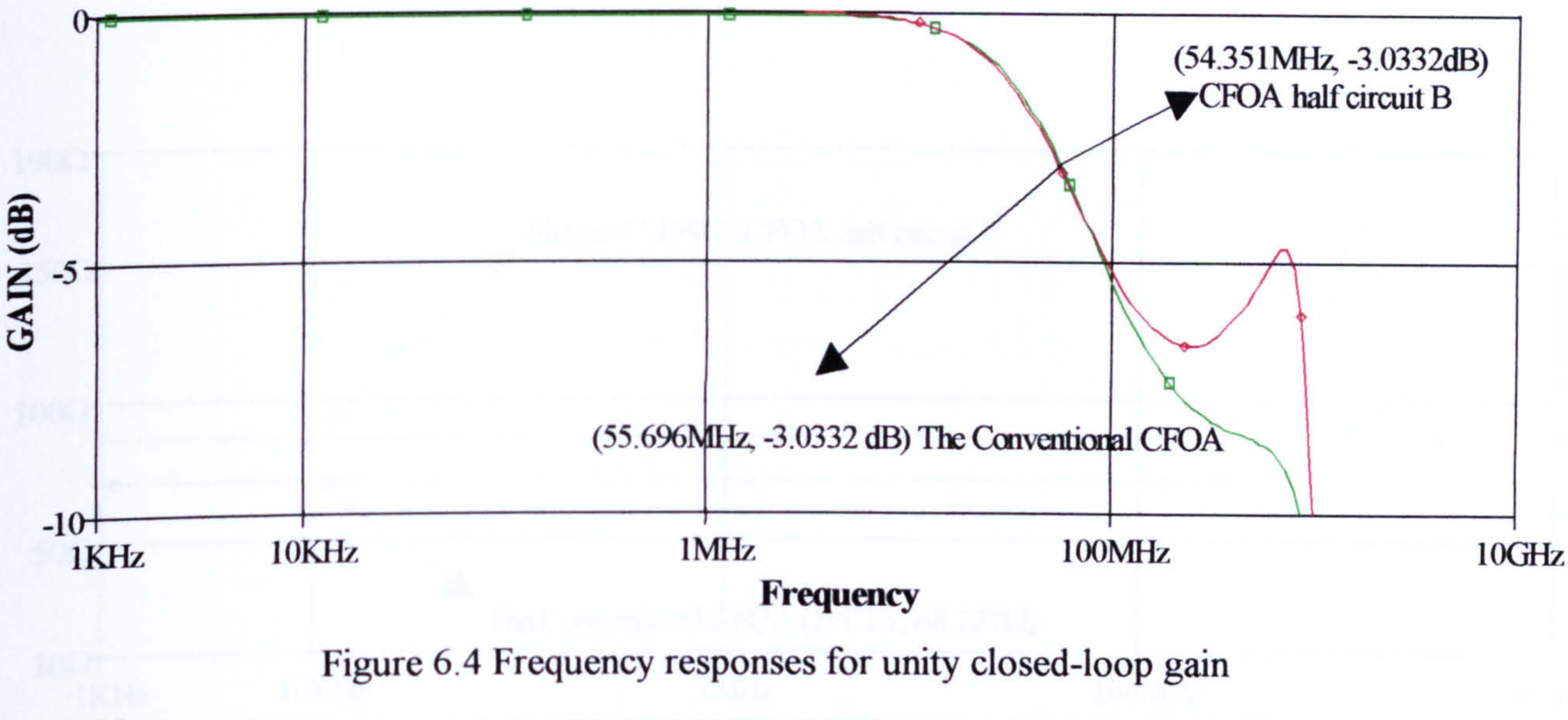


Figure 6.4 Frequency responses for unity closed-loop gain

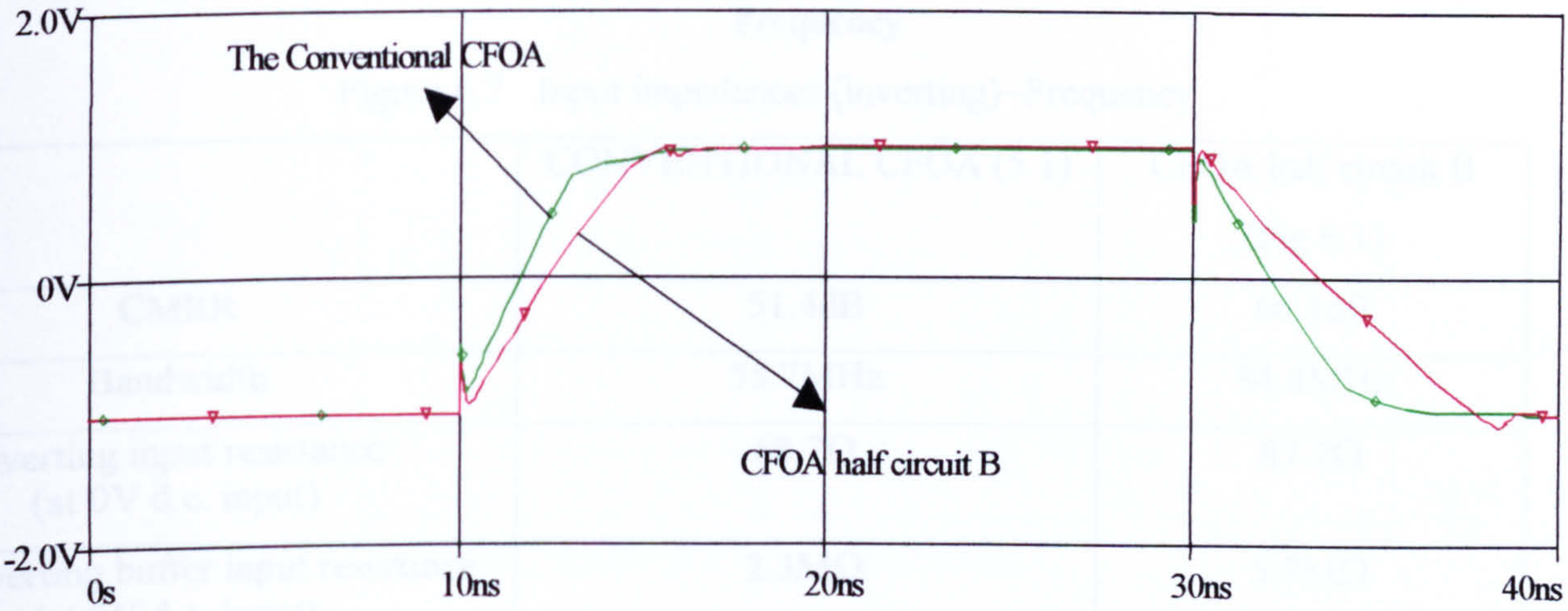


Figure 6.5 Transient response

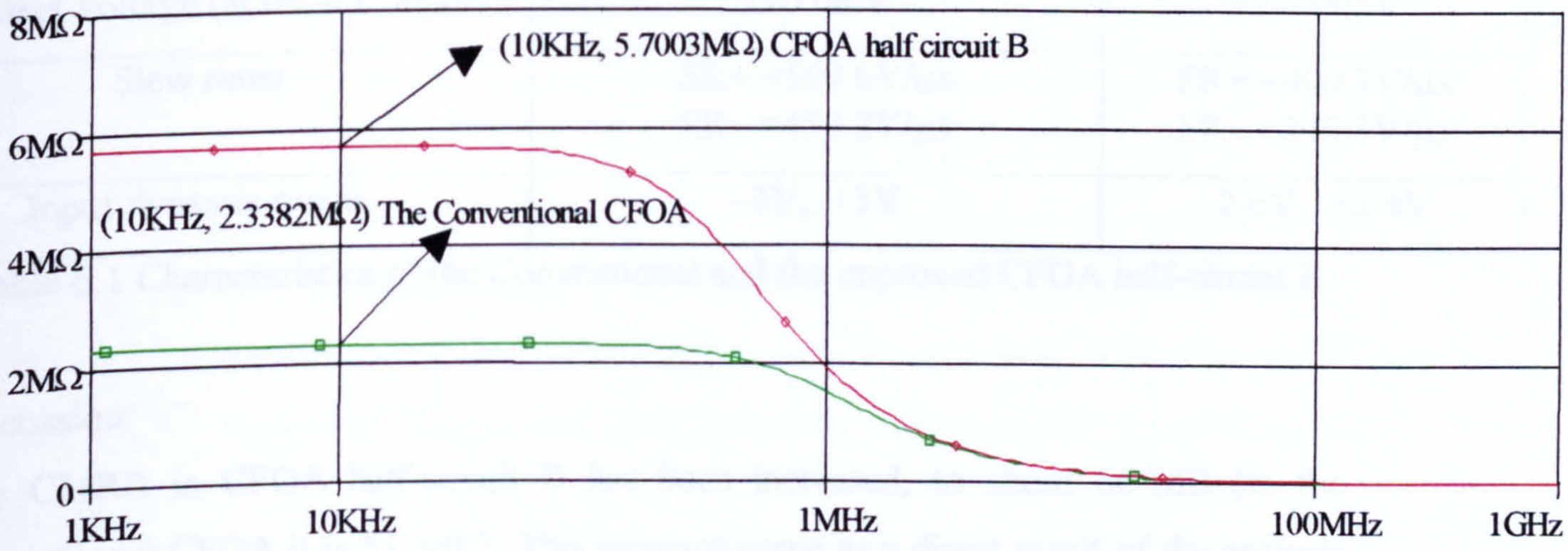


Figure 6.6 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

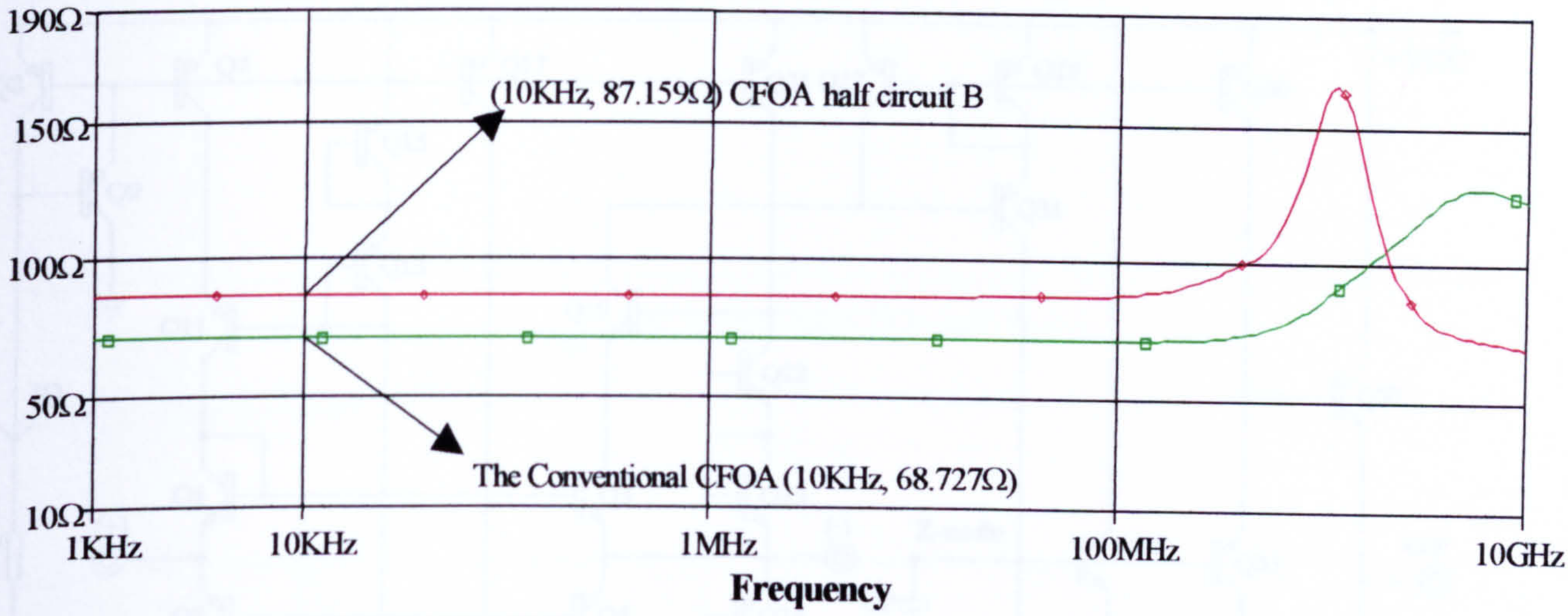


Figure 6.7 Input impedances (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	CFOA half circuit B (Fig 6.1)
CMRR	51.4dB	66.1dB
Bandwidth	55.7MHz	54.4MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	87.2Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	5.7MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	13.6mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±24.45mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =400.7V/μs SR– =245.3V/μs
Input dynamic range	–3V, +3V	–2.6V, +2.4V

Table 6.1 Characteristics of the Conventional and the improved CFOA half-circuit B

Discussion:

The CMRR in CFOA half-circuit B has been increased, to about 66.1dB (in the conventional CFOA it is 51.4dB). This increase come as a direct result of the analysis in Chapter Three (section 3.7). However the improvement in the CMRR has been achieved at the expense of a reduction in slew-rate performance and input dynamic range.

(6.2.2) Performance with half-circuit C

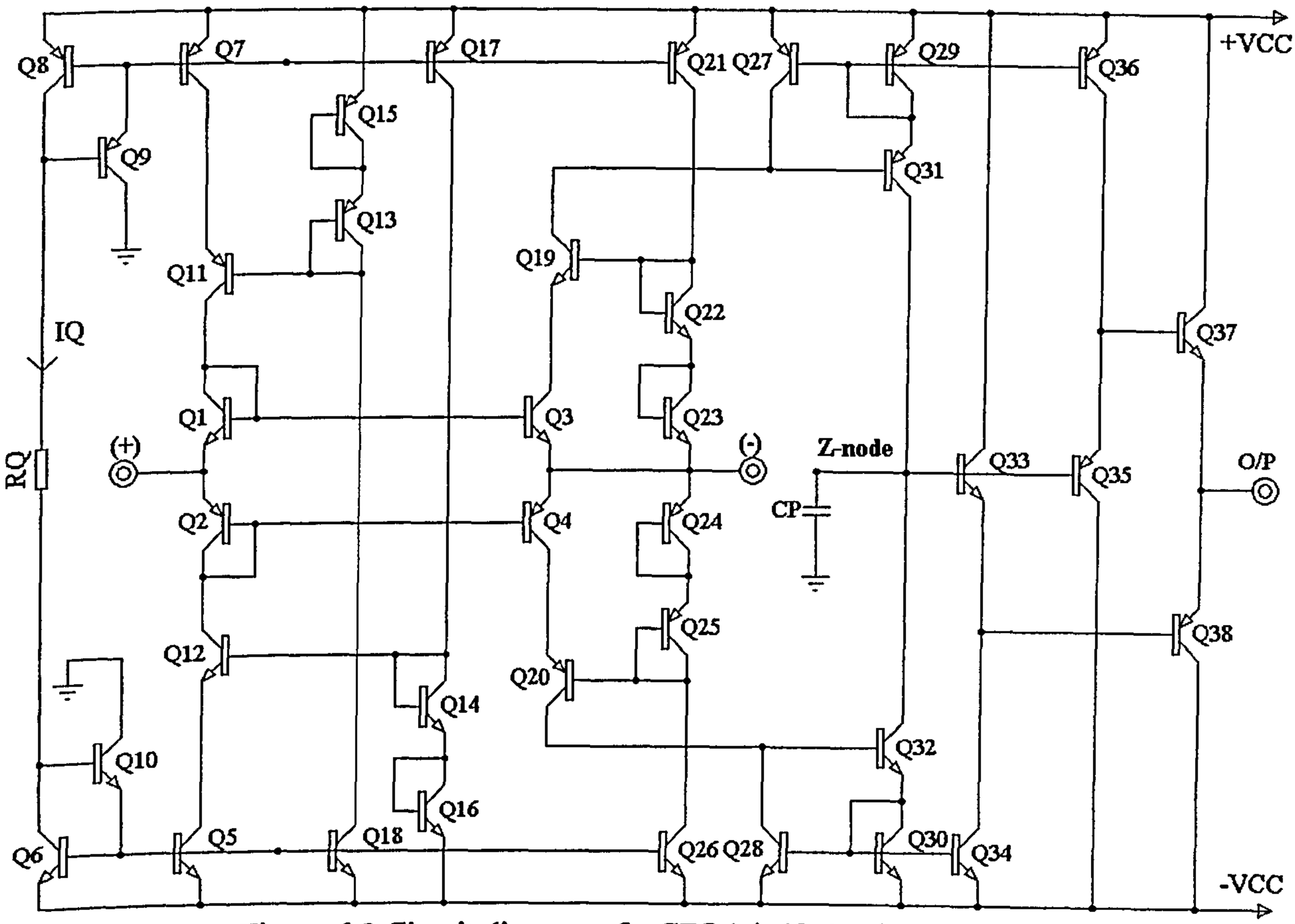


Figure 6.8 Circuit diagram of a CFOA half-circuit C

The circuit diagram of CFOA half-circuit C is shown in Fig.6.8, and should be compared with the half-circuit B shown in Fig.6.1. A significant difference between the two input circuits of the CFOAs are the use of NPN transistors for both Q_1 and Q_3, and the application of the input signal to the emitter of Q_1 rather than its base. Similarly, Q_2, Q_4 are both PNP transistors and the input applied to the emitter of Q_2 rather than its base. Furthermore, Q_1, Q_2 are now strapped to operate as diodes. From Fig.6.8, it follows that the DC voltage difference from the (+) to (-) is first increased (decreased) by V_{BEQ1} (by V_{BEQ2}), and then decreased (increased) by V_{BEQ3} (V_{BEQ4}) **[6-2]**, that is

$$V_{os}=| V_{BEQ1}- V_{BEQ3}|=| V_{BEQ2}- V_{BEQ4}| \qquad (6.1)$$

Because the matching between the same-type transistors (NPN or PNP) is good, a better V_{OS} can be achieved.

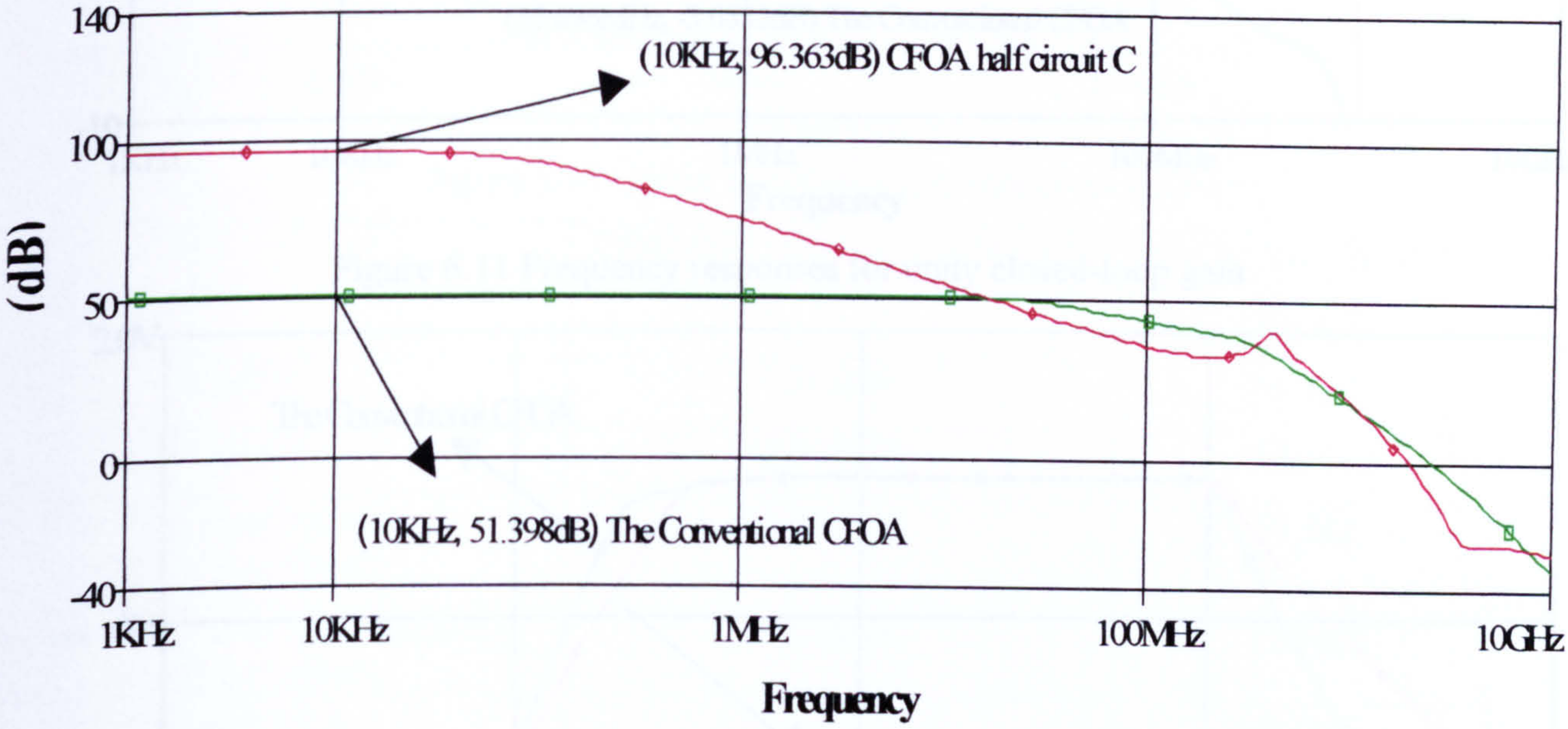


Figure 6.9 CMRR~Frequency

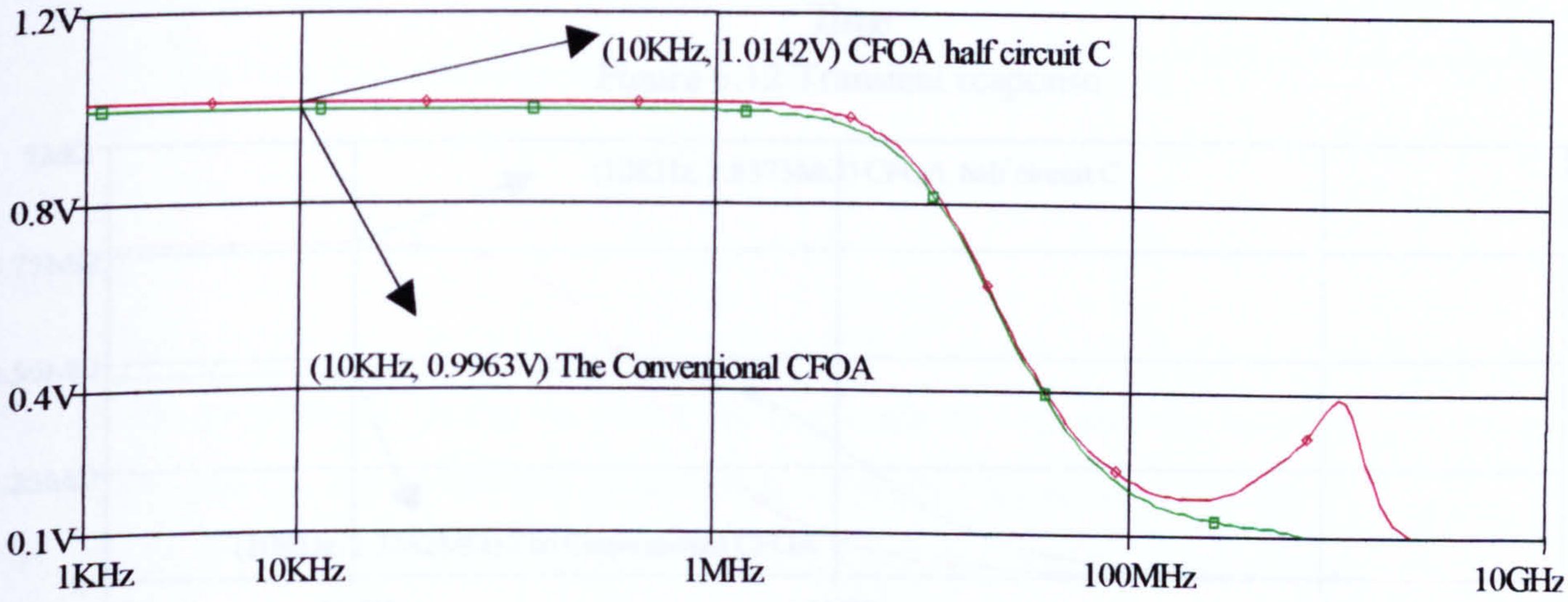


Figure 6.10 AC gain accuracy ~ Frequency

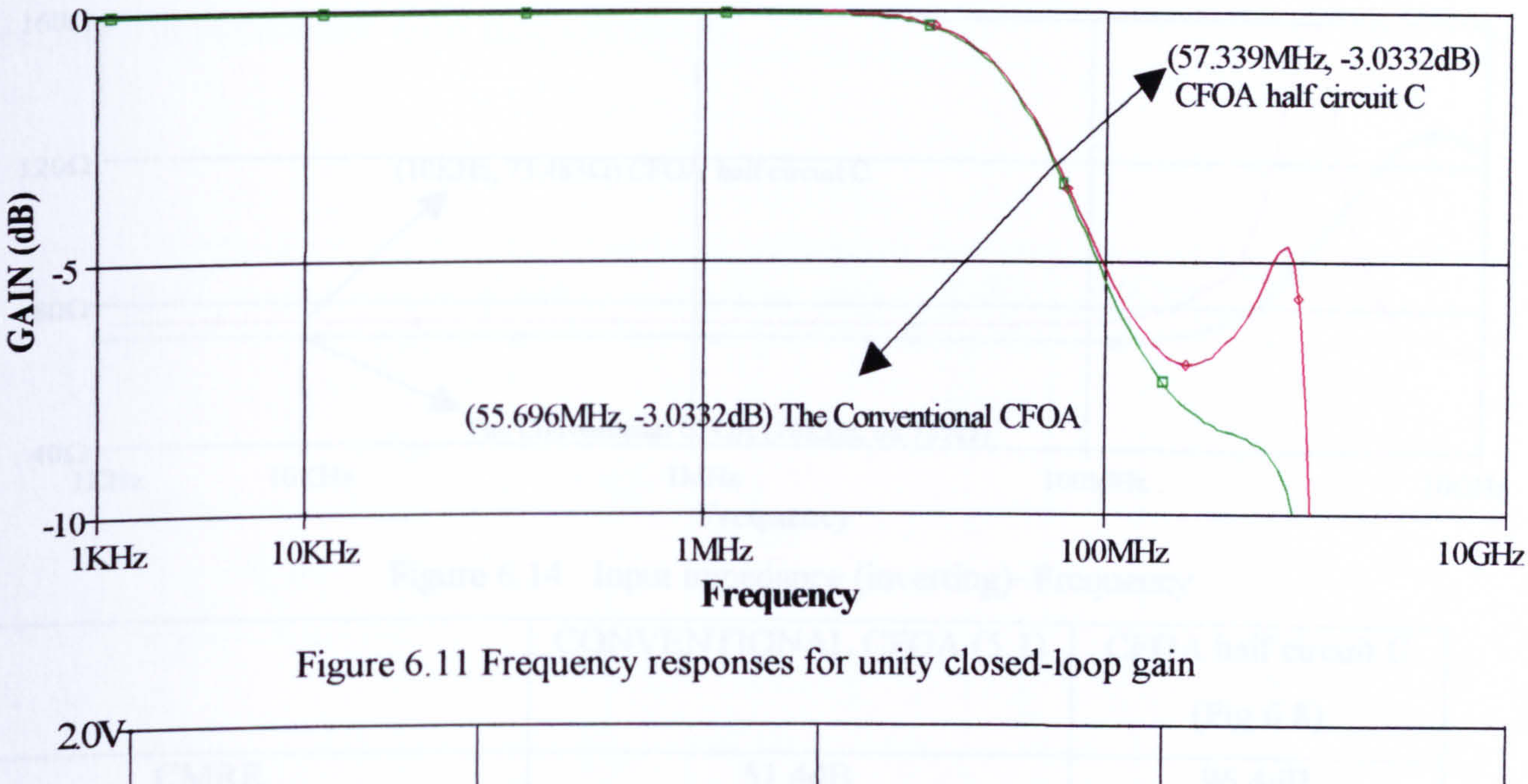


Figure 6.11 Frequency responses for unity closed-loop gain

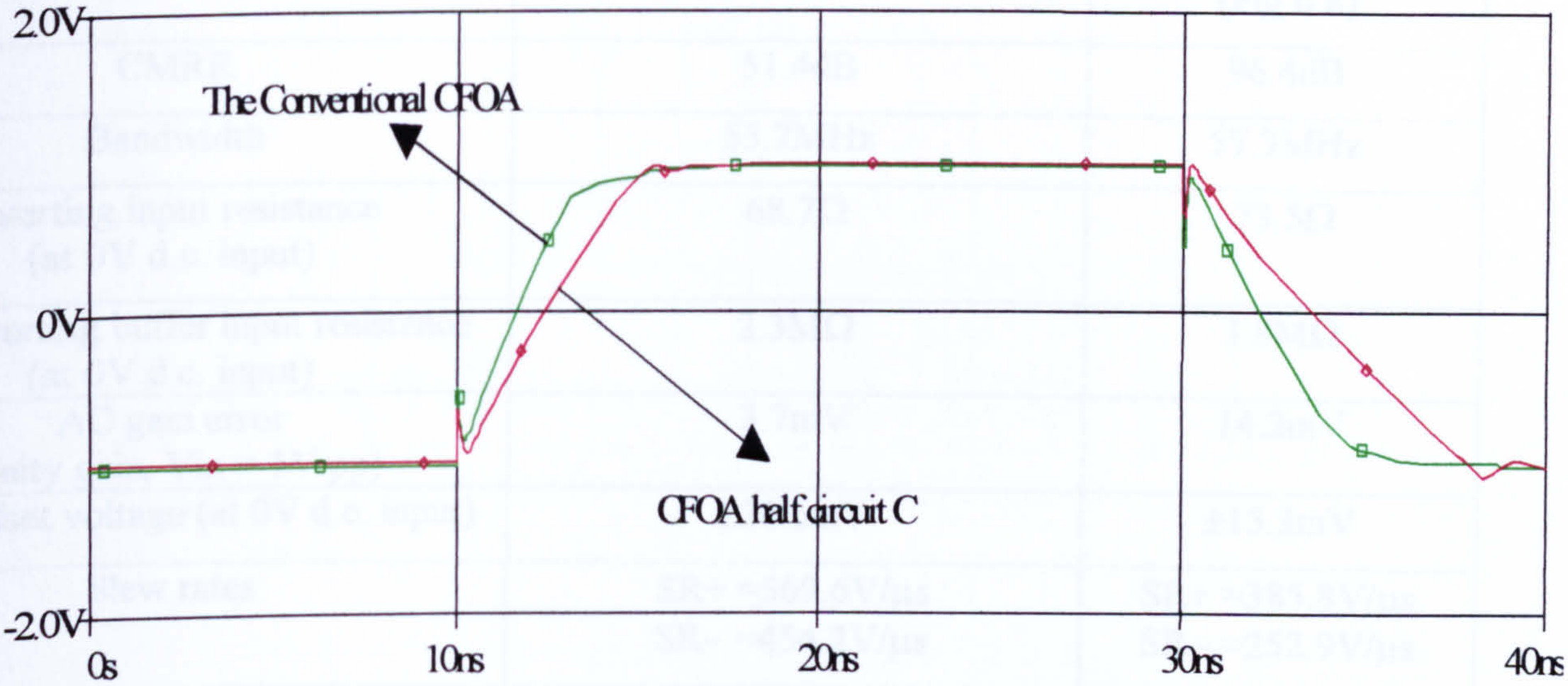


Figure 6.12 Transient response

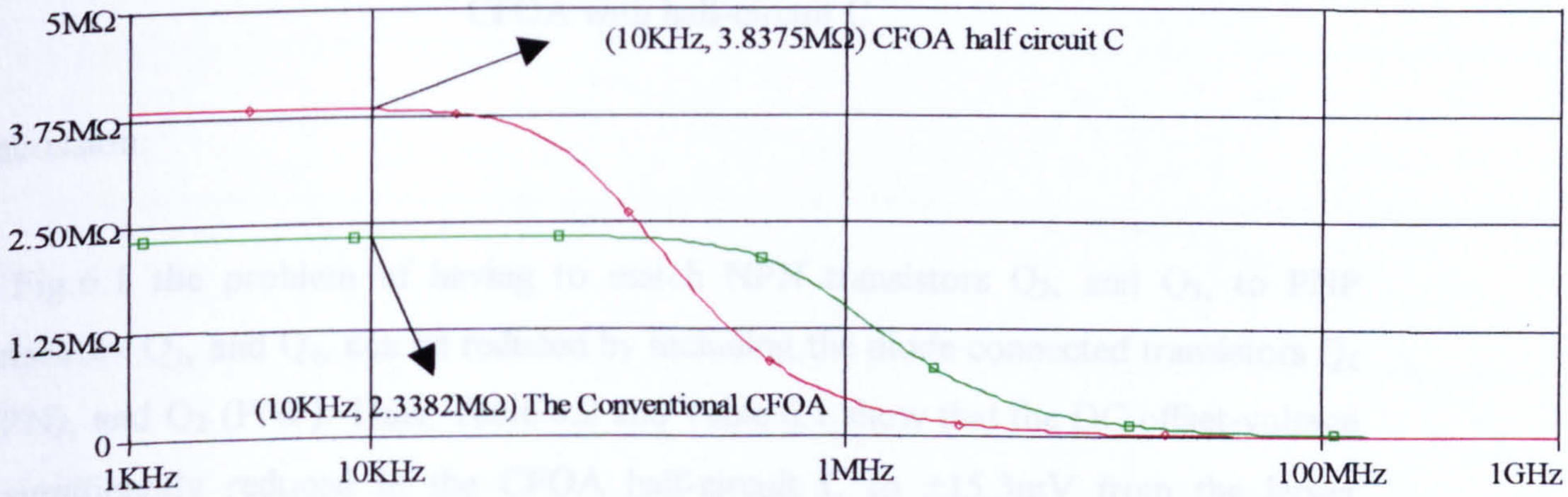


Figure 6.13 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

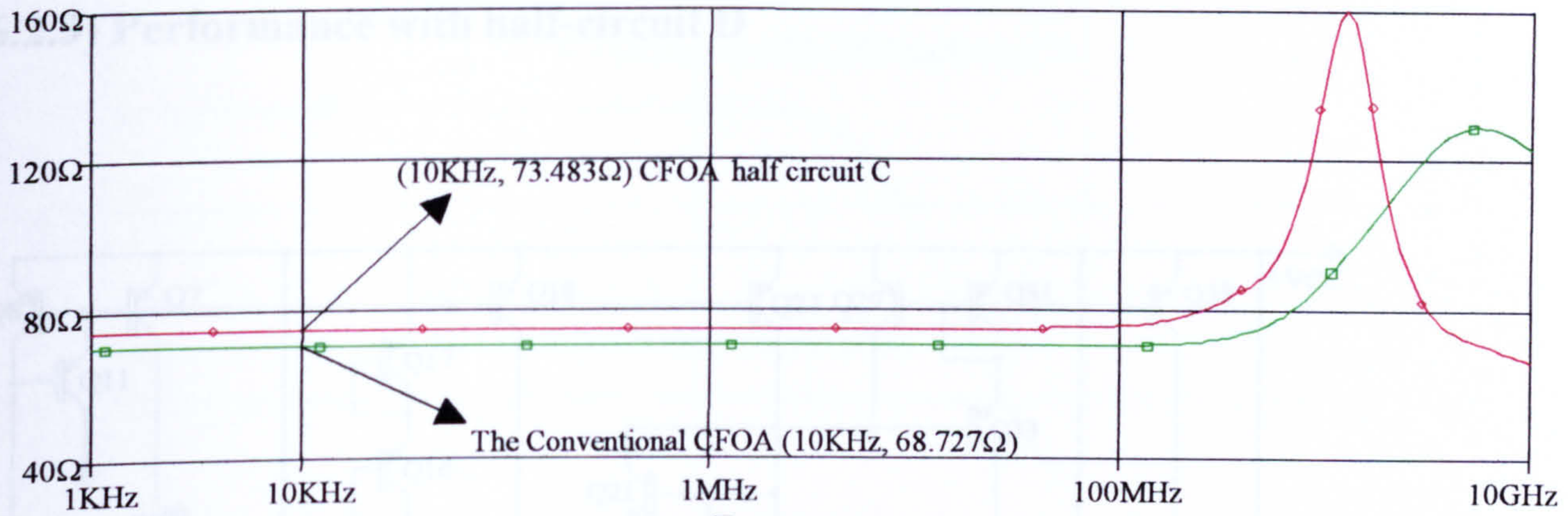


Figure 6.14 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	CFOA half circuit C (Fig 6.8)
CMRR	51.4dB	96.4dB
Bandwidth	55.7MHz	57.3MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	73.5Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3.8MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	14.2mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±15.3mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =385.8V/μs SR– =252.9V/μs
Input dynamic range	–3V, +3V	–2.4V, +2.3V

Table 6.2 Characteristics of the Conventional and the improved CFOA with half-circuit C

Discussion:

In Fig.6.1 the problem of having to match NPN transistors Q_2, and Q_3, to PNP transistors Q_1, and Q_4, can be reduced by including the diode connected transistors Q_1 (NPN), and Q_2 (PNP). Thus, Table 6.2 and Table 6.1 show that the DC offset-voltage is significantly reduced in the CFOA half-circuit C to ±15.3mV from the larger ±24.45mV, ±20.6mV of the CFOA half-circuit B, and the conventional CFOA, respectively. However, of greater importance is the dramatic increase in CMRR.

(6.2.3) Performance with half-circuit D

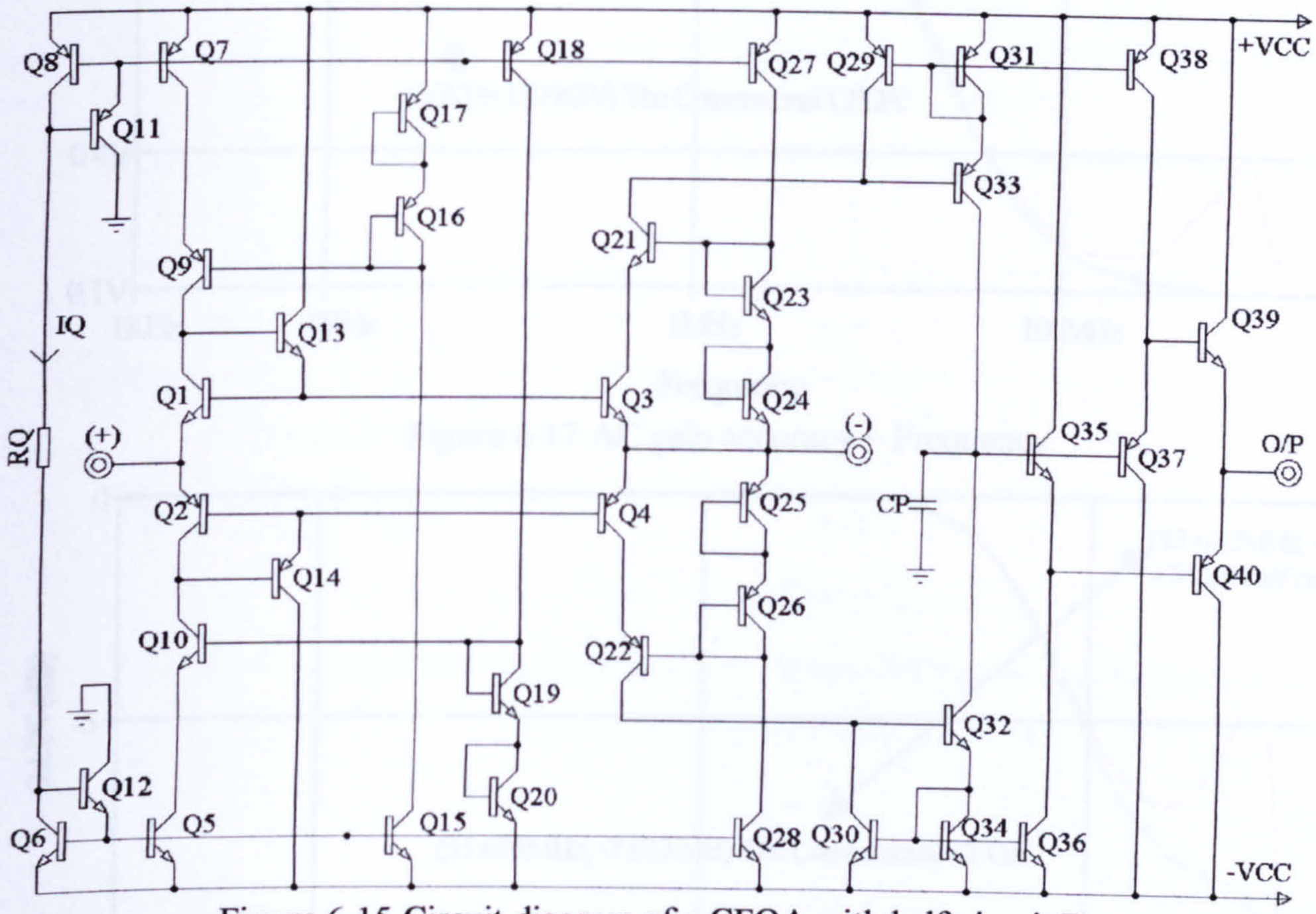


Figure 6.15 Circuit diagram of a CFOA with half-circuit D

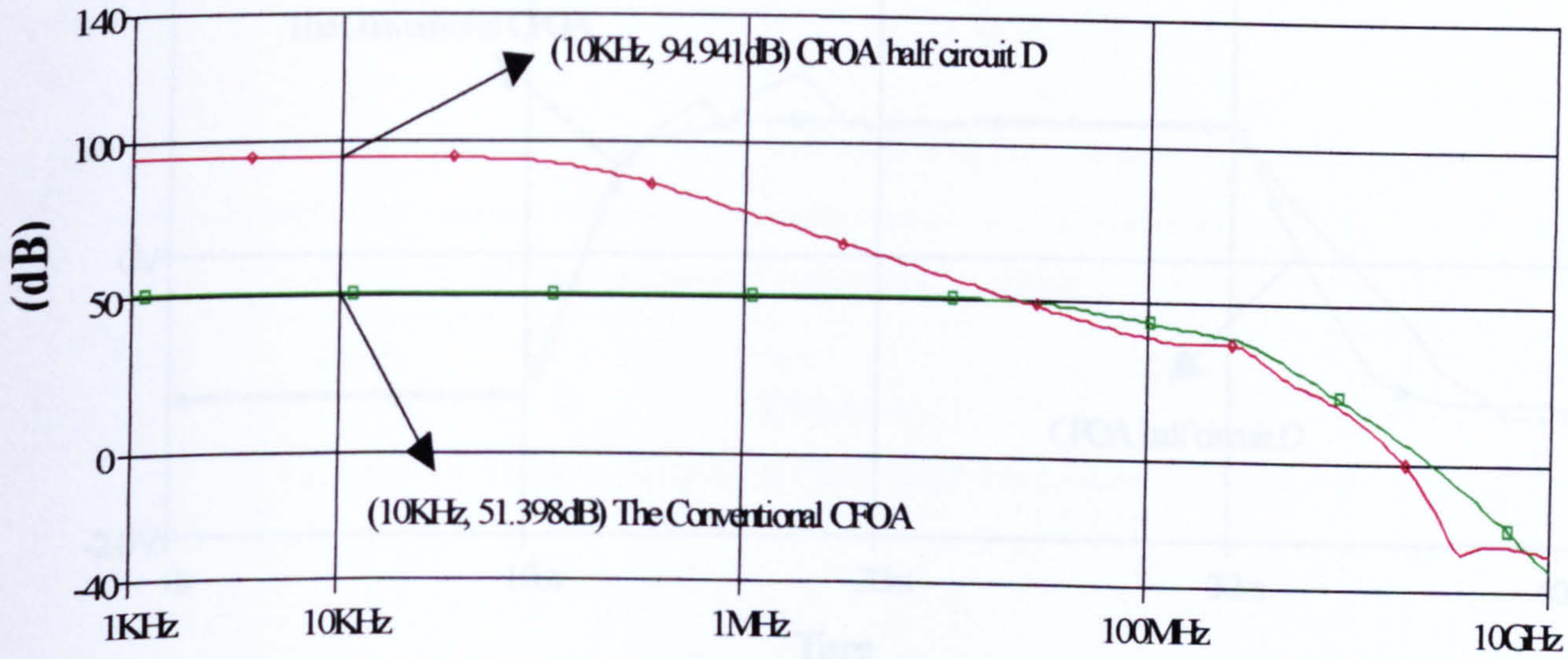


Figure 6.16 CMRR~Frequency

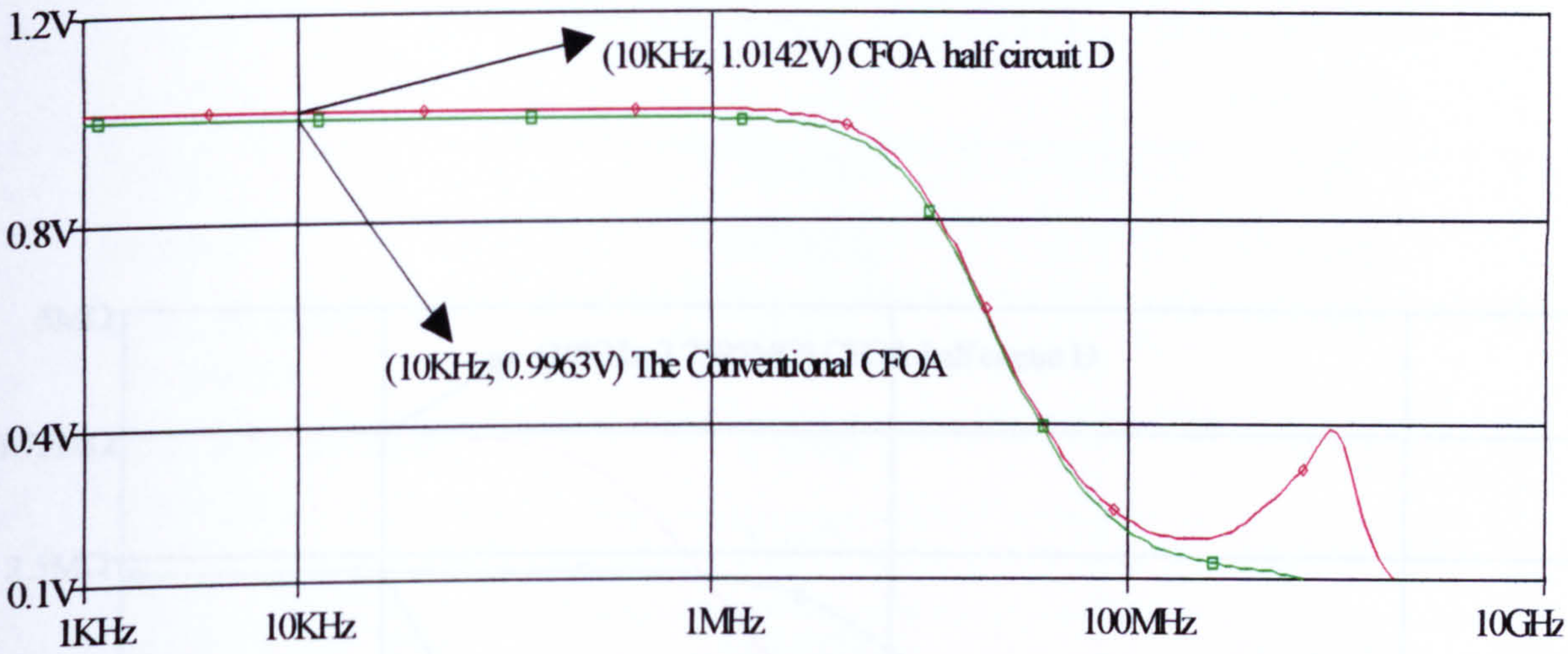


Figure 6.17 AC gain accuracy ~ Frequency

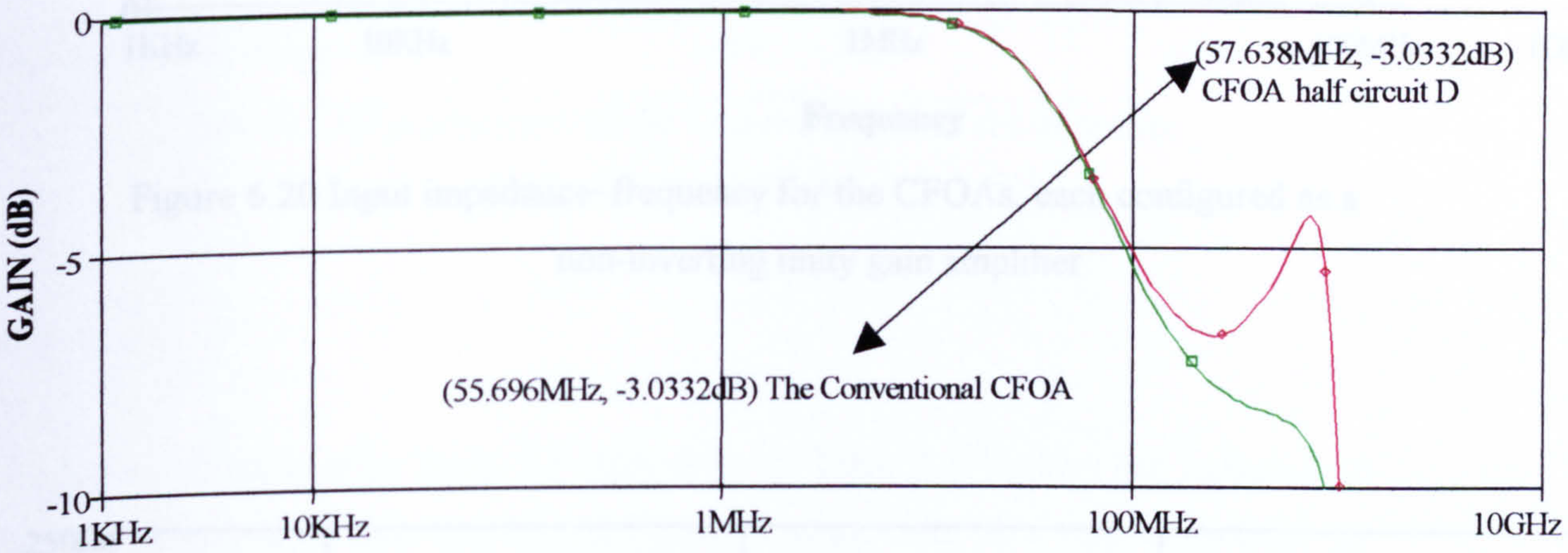


Figure 6.18 Frequency responses for unity closed-loop gain

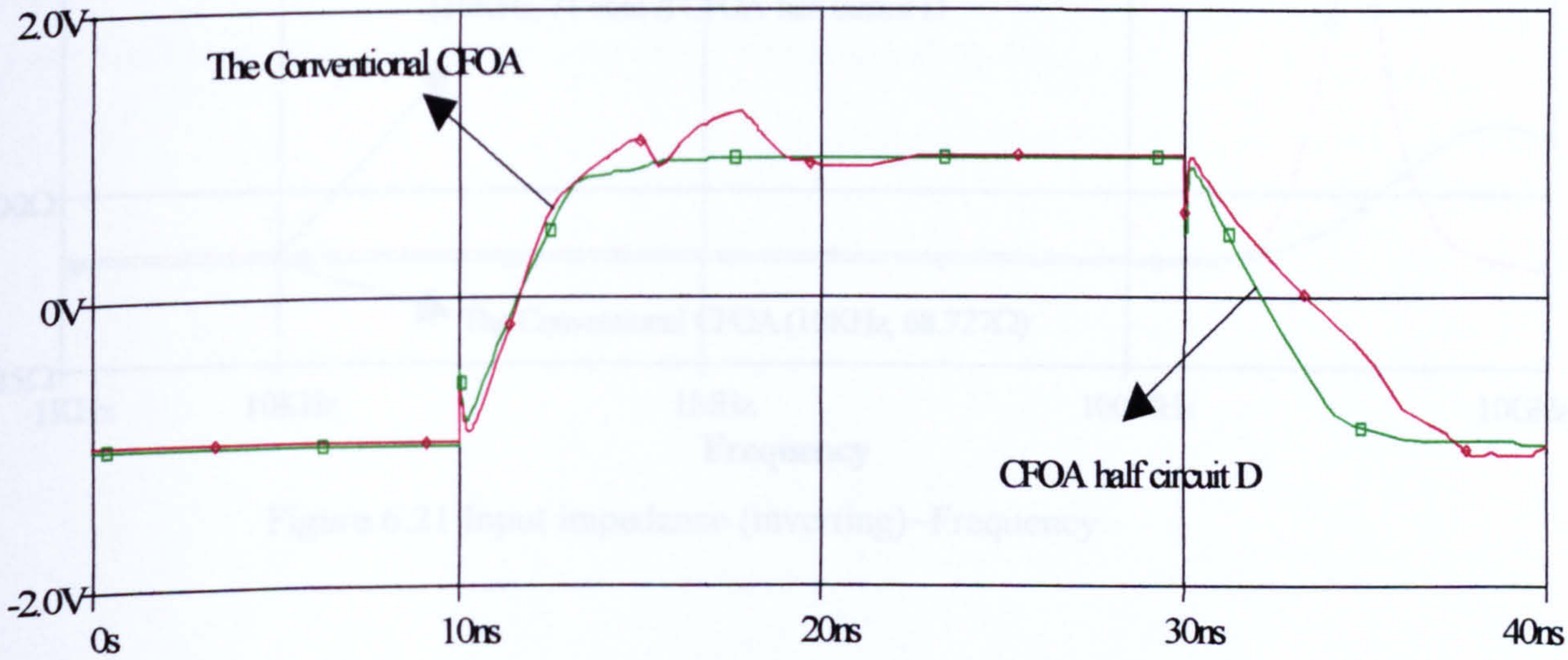


Figure 6.19 Transient response

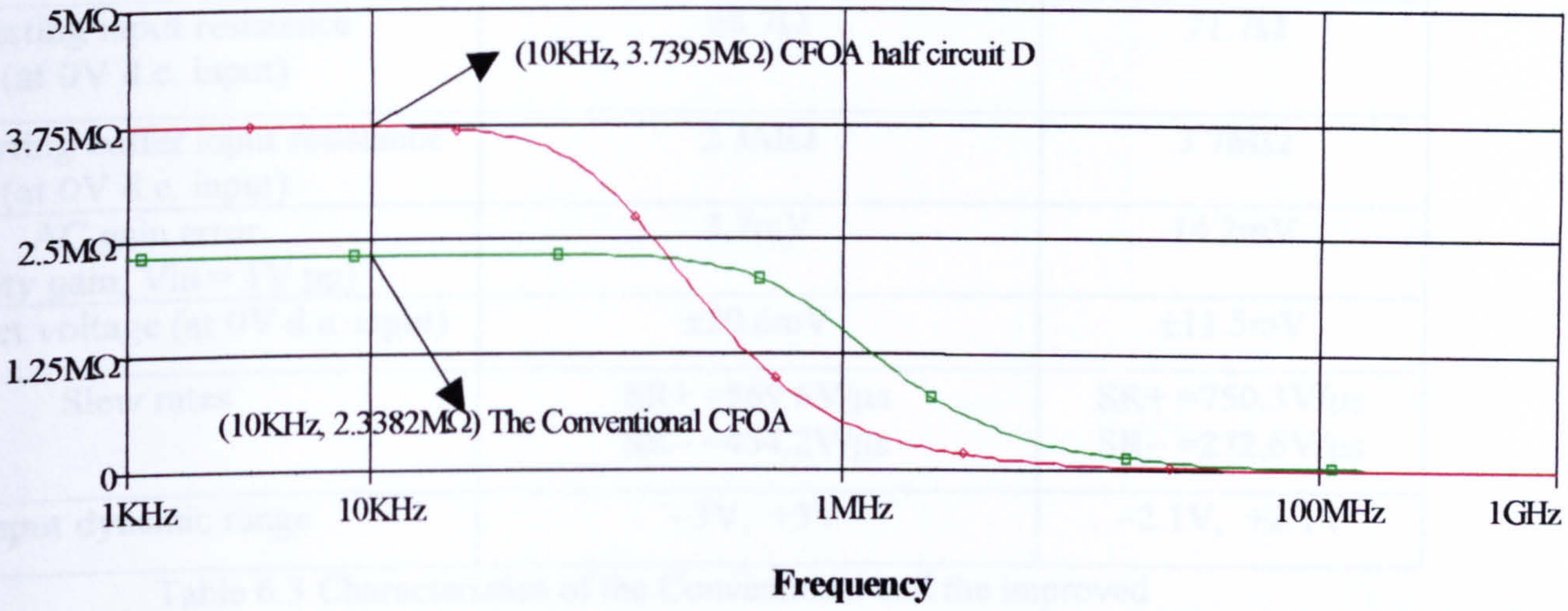


Figure 6.20 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

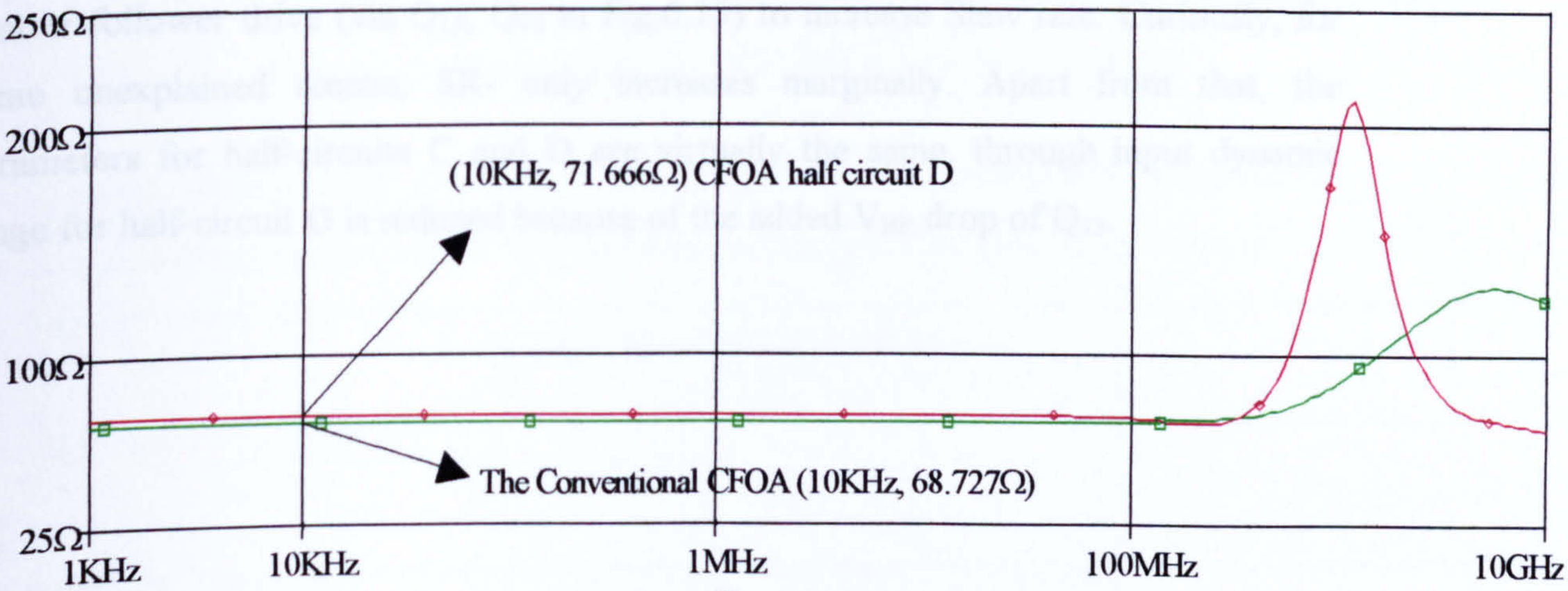


Figure 6.21 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	CFOA half circuit D (Fig 6.15)
CMRR	51.4dB	95dB
Bandwidth	55.7MHz	57.6MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	71.7Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3.7MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	14.2mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±11.5mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =750.3V/μs SR– =272.6V/μs
Input dynamic range	–3V, +3V	–2.1V, +2.1V

Table 6.3 Characteristics of the Conventional and the improved CFOA with half-circuit D

Discussion:

Comparing the entries in Table 6.3 with these in Table 6.2 justifies the inclusion of emitter-follower drive (via Q_{13}, Q_{14} in Fig.6.15) to increase Slew rate. Curiously, for some unexplained reason, SR- only increases marginally. Apart from that, the parameters for half-circuits C and D are virtually the same, through input dynamic range for half-circuit D is reduced because of the added V_{BE} drop of Q_{13}.

(6.3) Forward bootstrapping

(6.3.1) Performance with half-circuit E

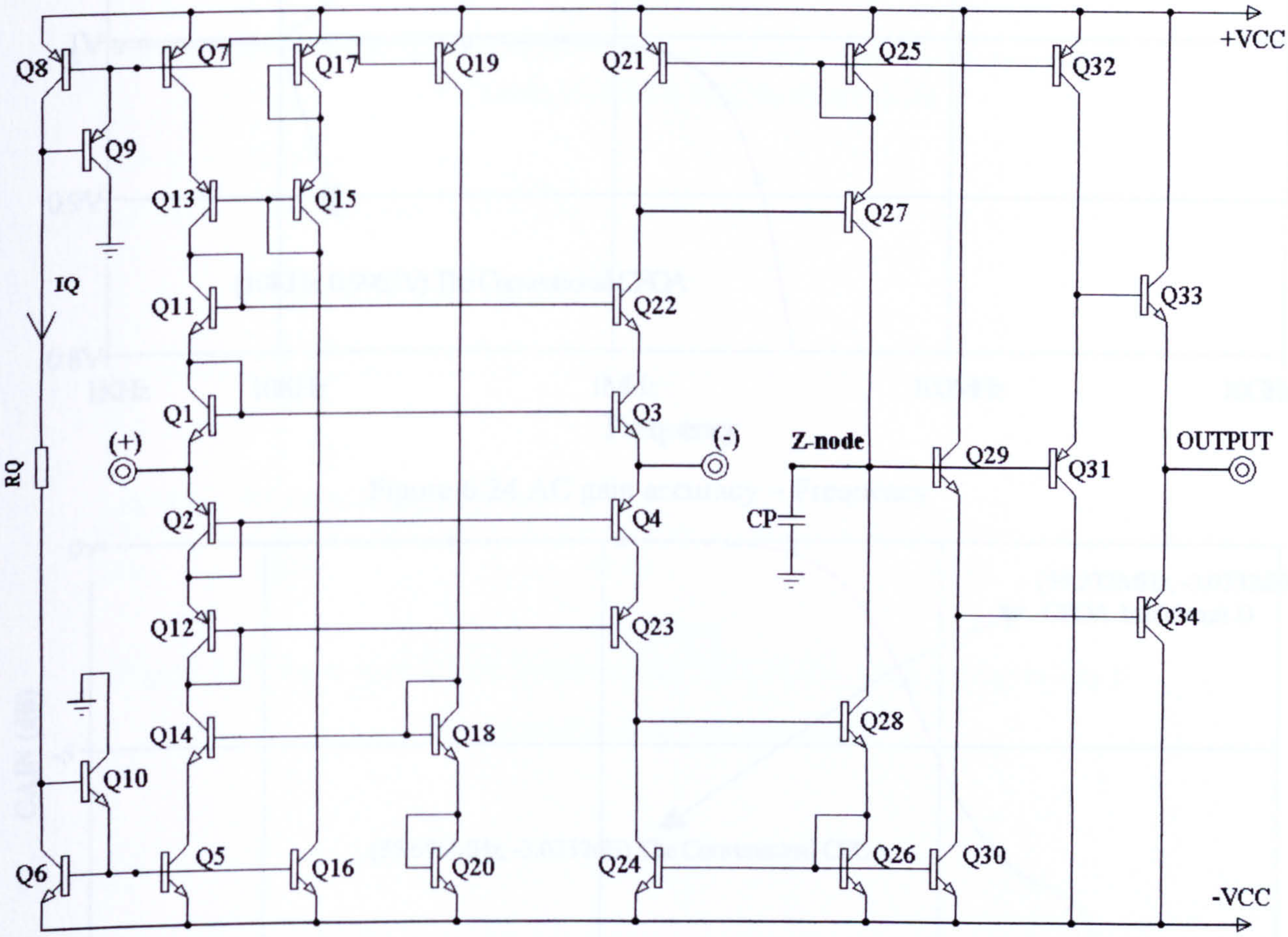


Figure 6.22 Circuit diagram of a CFOA with half-circuit E

The biasing scheme in that used in previous designs but the cascode transistors for Q_3, Q_4 do not, of course, require the bias currents necessary for reverse bootstrapping.

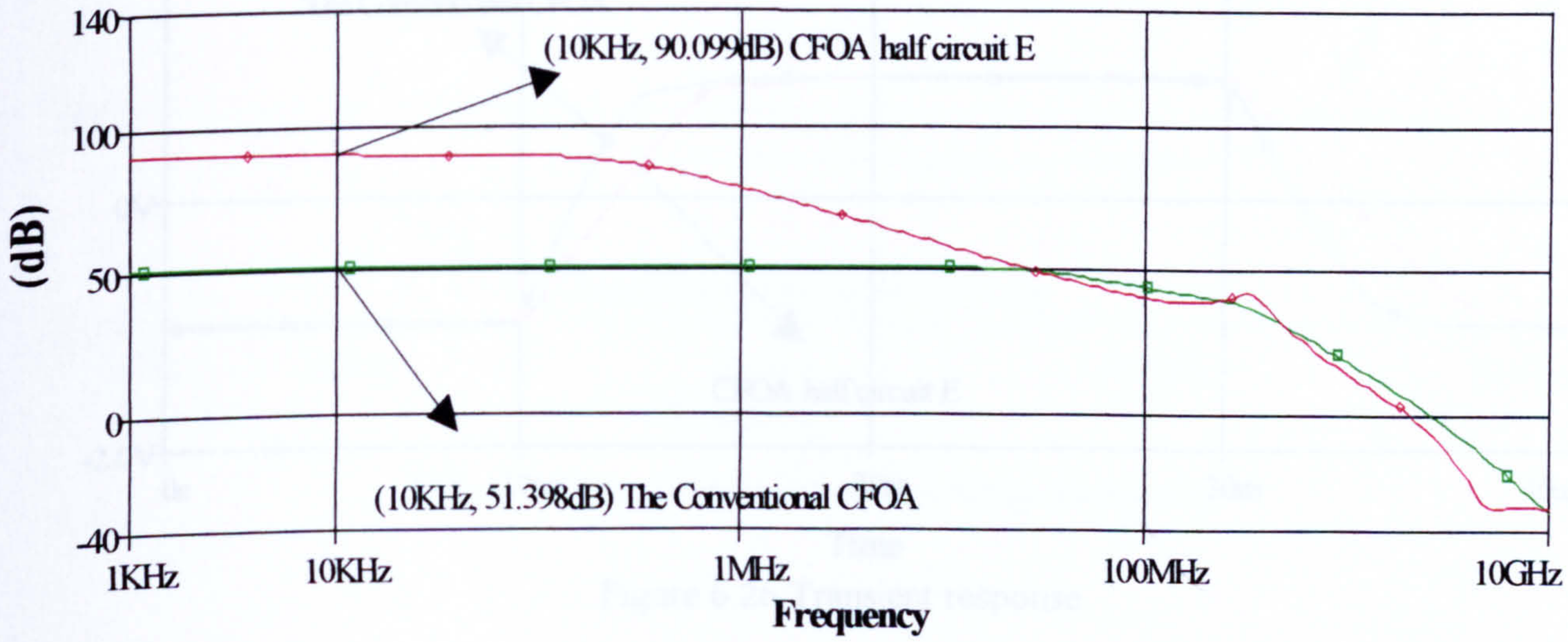


Figure 6.23 CMRR~Frequency

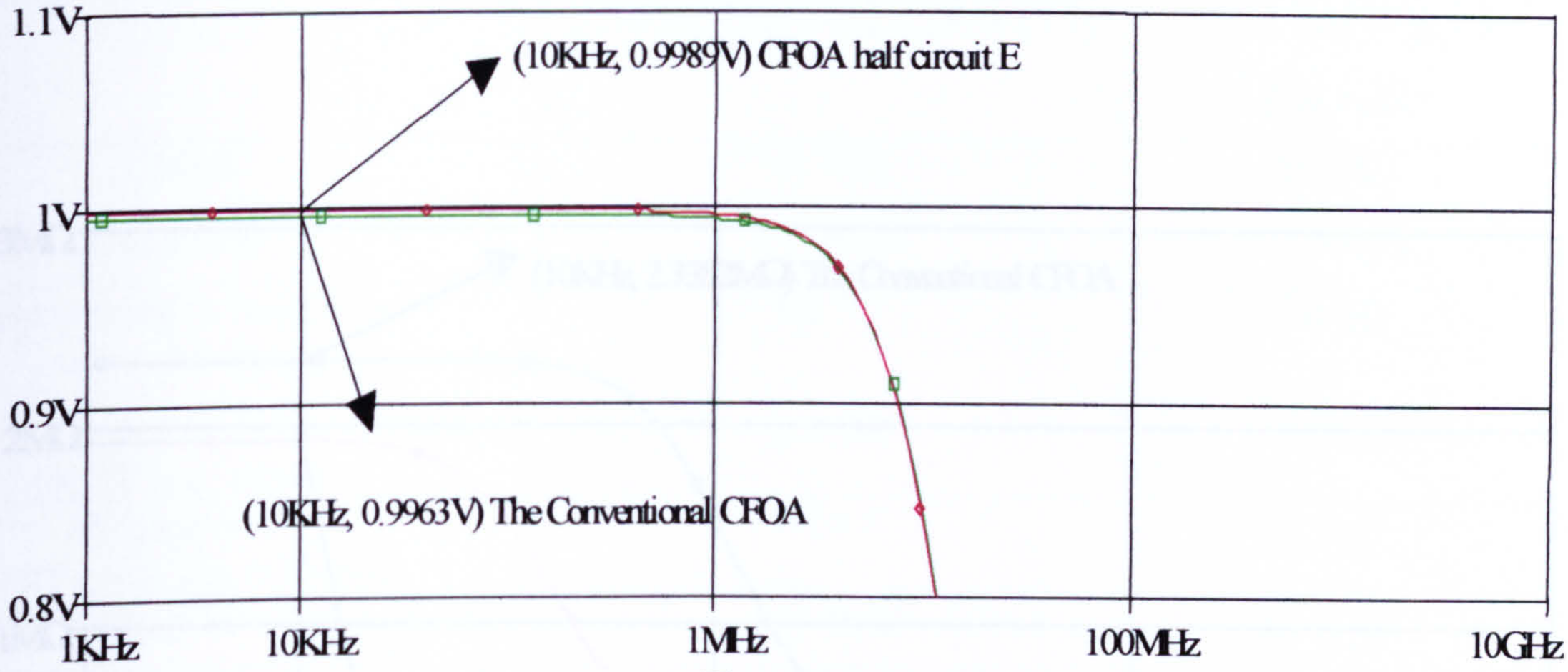


Figure 6.24 AC gain accuracy ~ Frequency

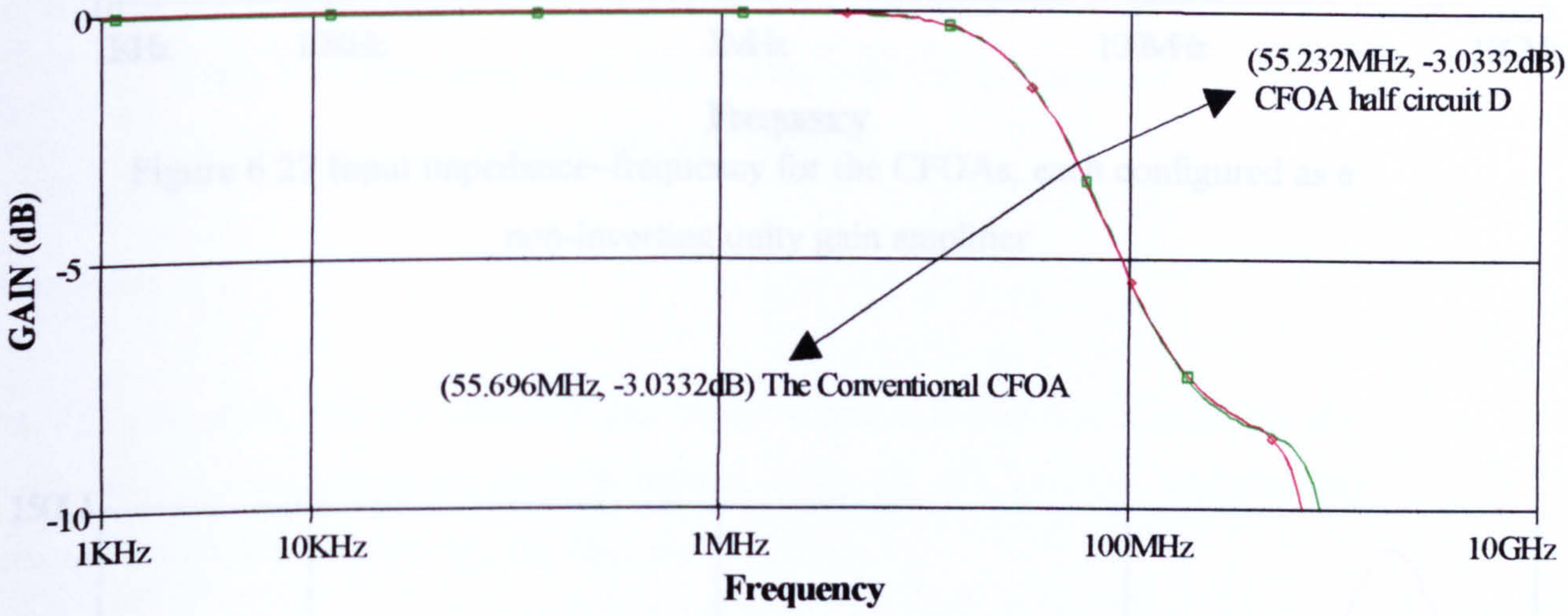


Figure 6.25 Frequency responses for unity closed-loop gain

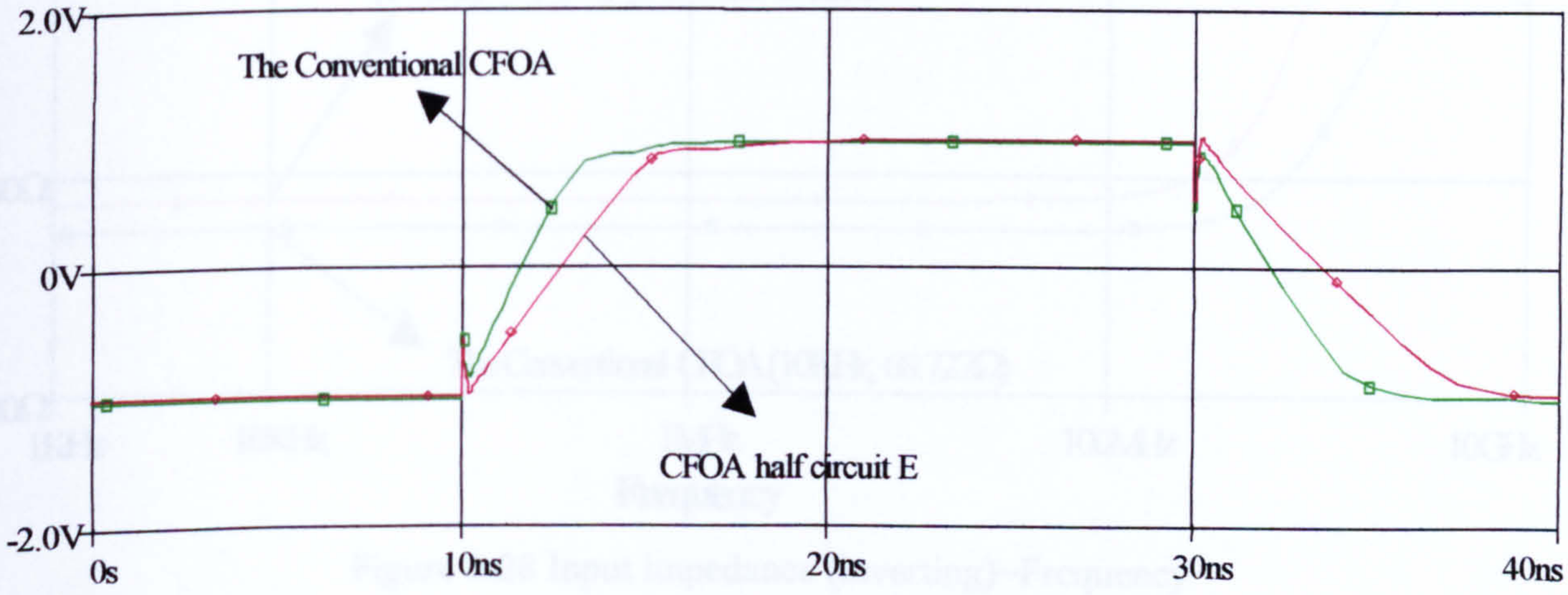


Figure 6.26 Transient response

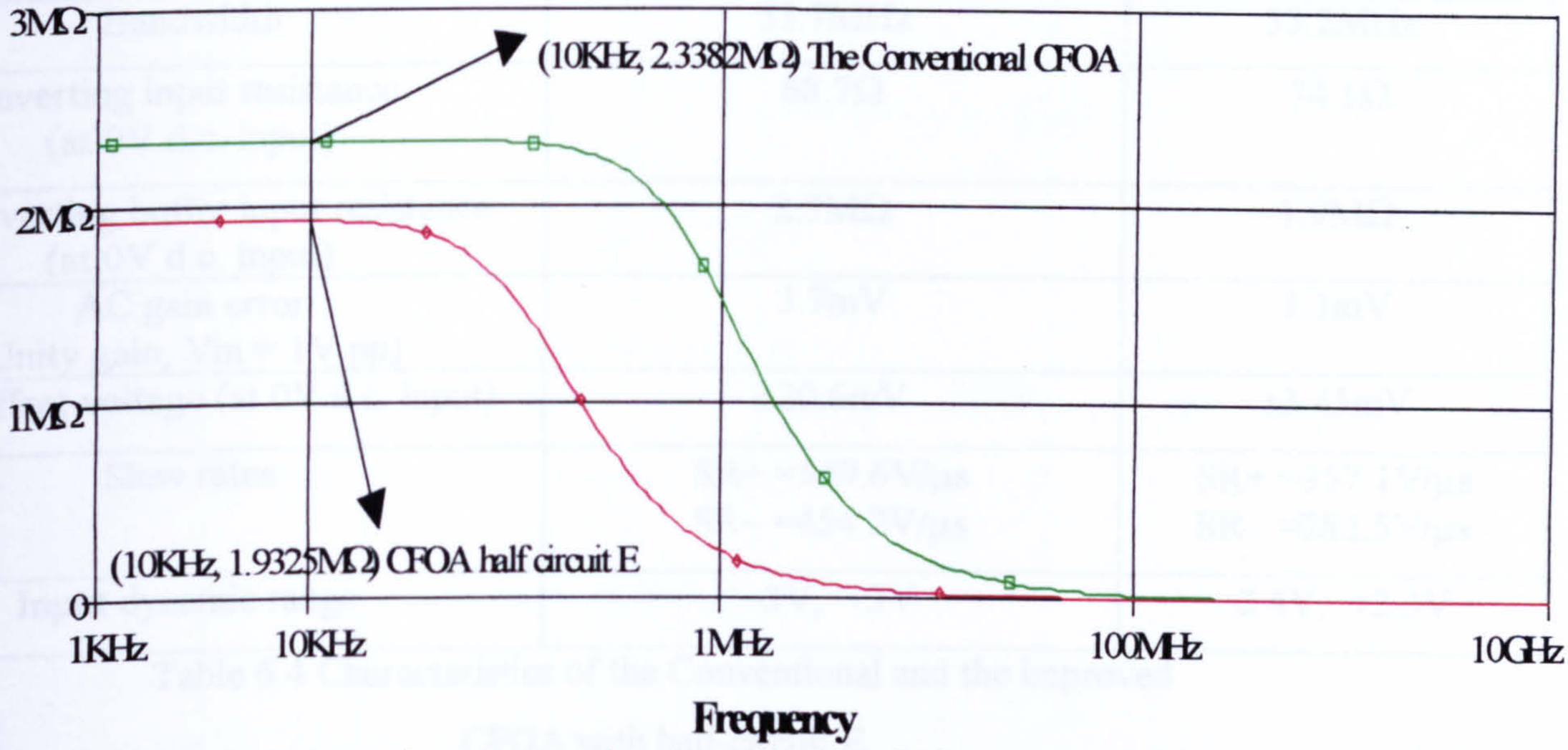


Figure 6.27 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

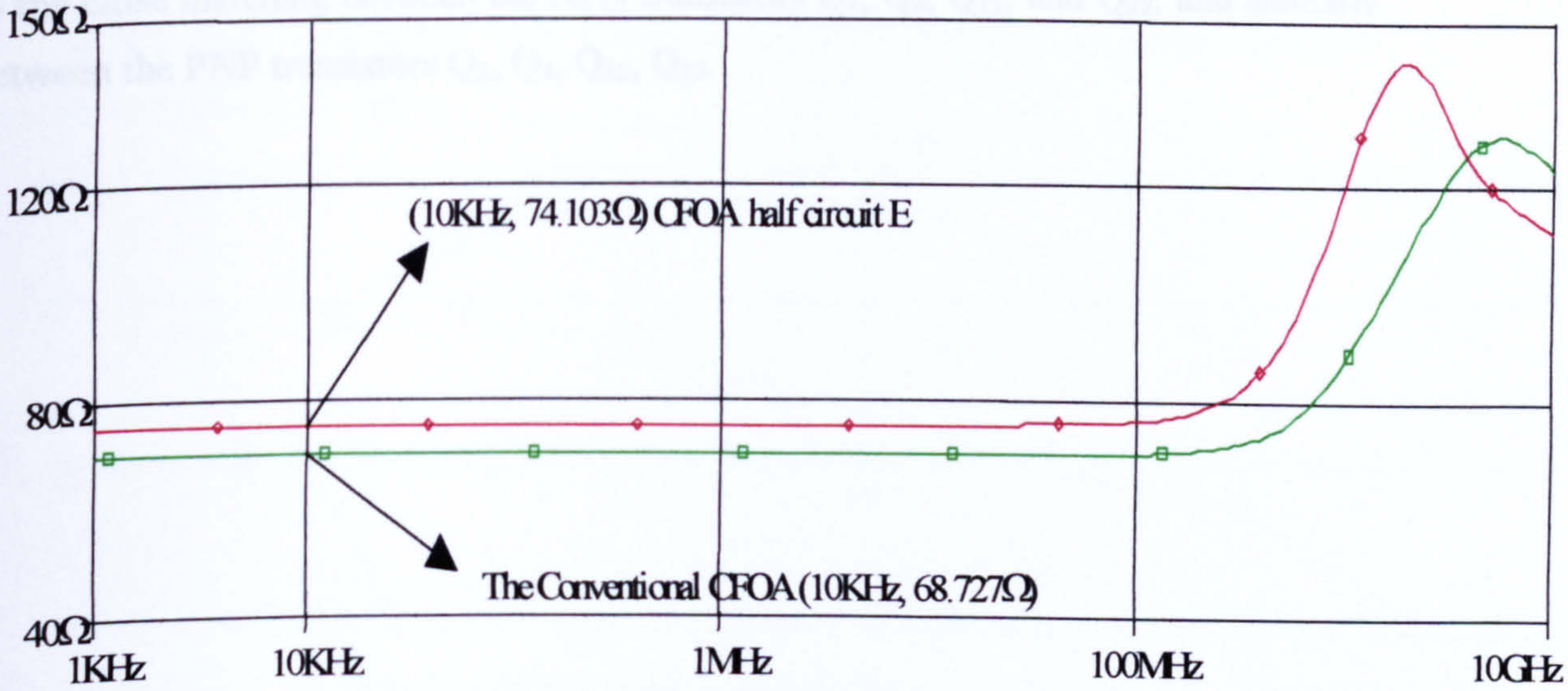


Figure 6.28 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	CFOA half circuit E (Fig 6.22)
CMRR	51.4dB	90.1dB
Bandwidth	55.7MHz	55.2MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	74.1Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	1.9MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	1.1mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±3.45mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =357.1V/μs SR– =282.5V/μs
Input dynamic range	–3V, +3V	–2.4V, +2.3V

Table 6.4 Characteristics of the Conventional and the improved CFOA with half-circuit E

Discussion:

The AC gain-error, and the offset-voltage improvement in half-circuit E is mainly due to the close matching between the NPN transistors Q_1, Q_3, Q_{11}, and Q_{22}, and similarly between the PNP transistors Q_2, Q_4, Q_{12}, Q_{23}.

(6.3.2) Performance with half-circuit F

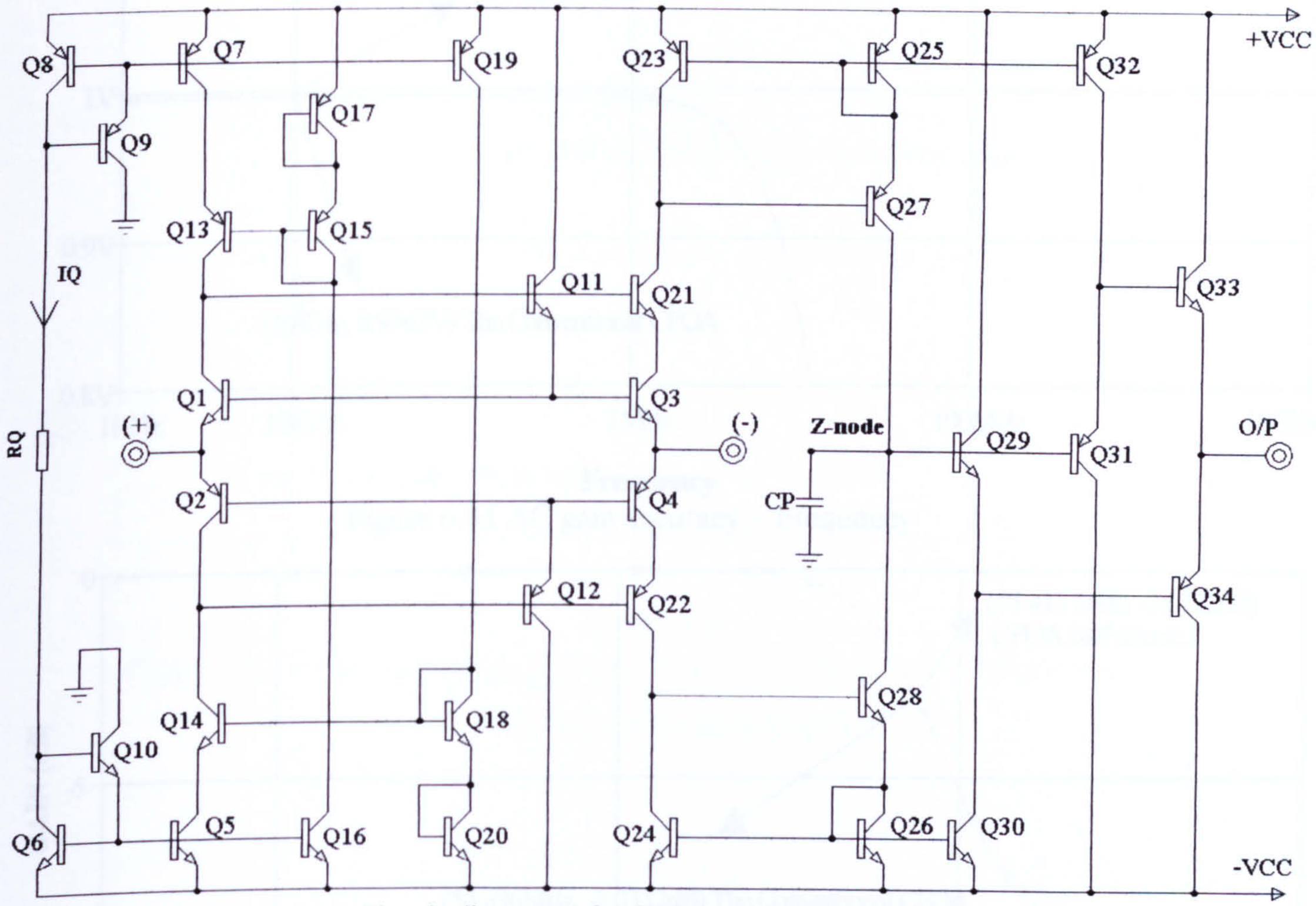


Figure 6.29 Circuit diagram of a CFOA with half-circuit F

This differs from half-circuit E in that Q_{11}, Q_{12} now function as emitter-follower transistors rather than diodes

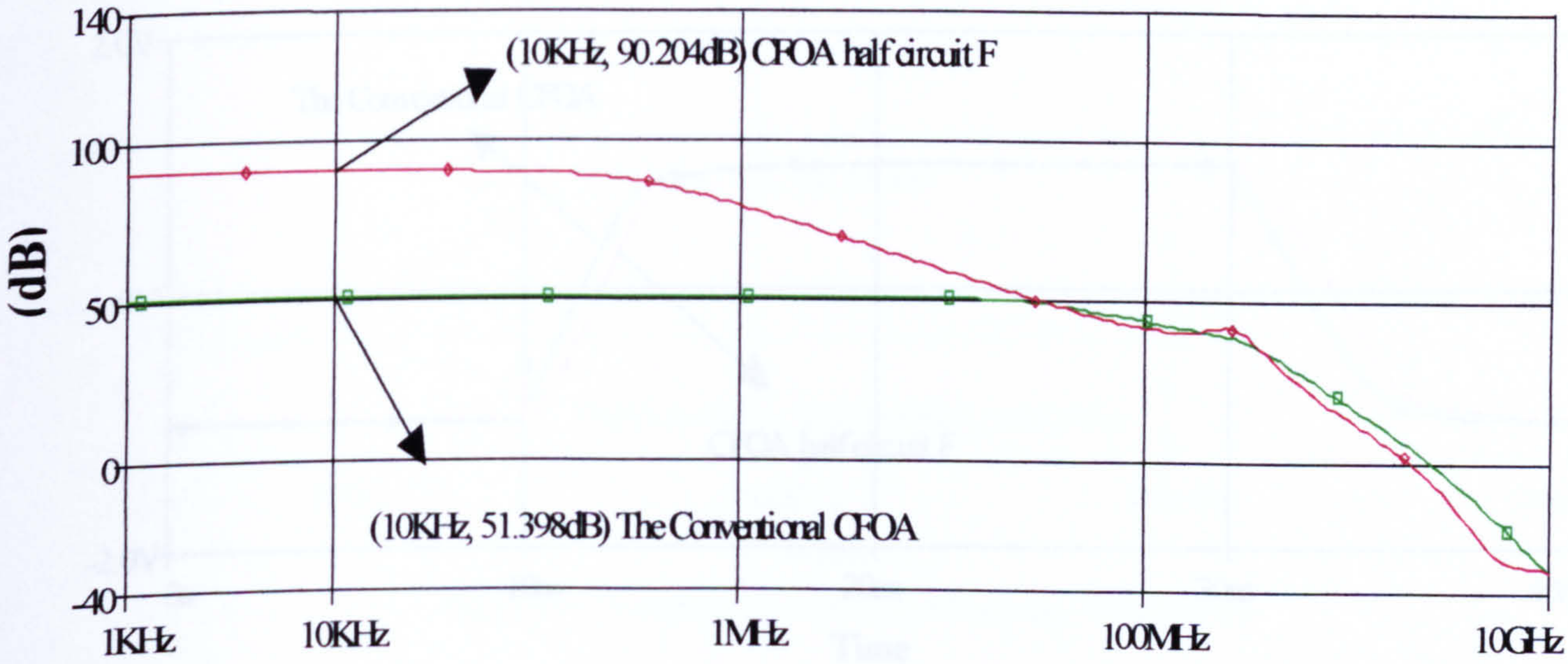


Figure 6.30 CMRR~Frequency

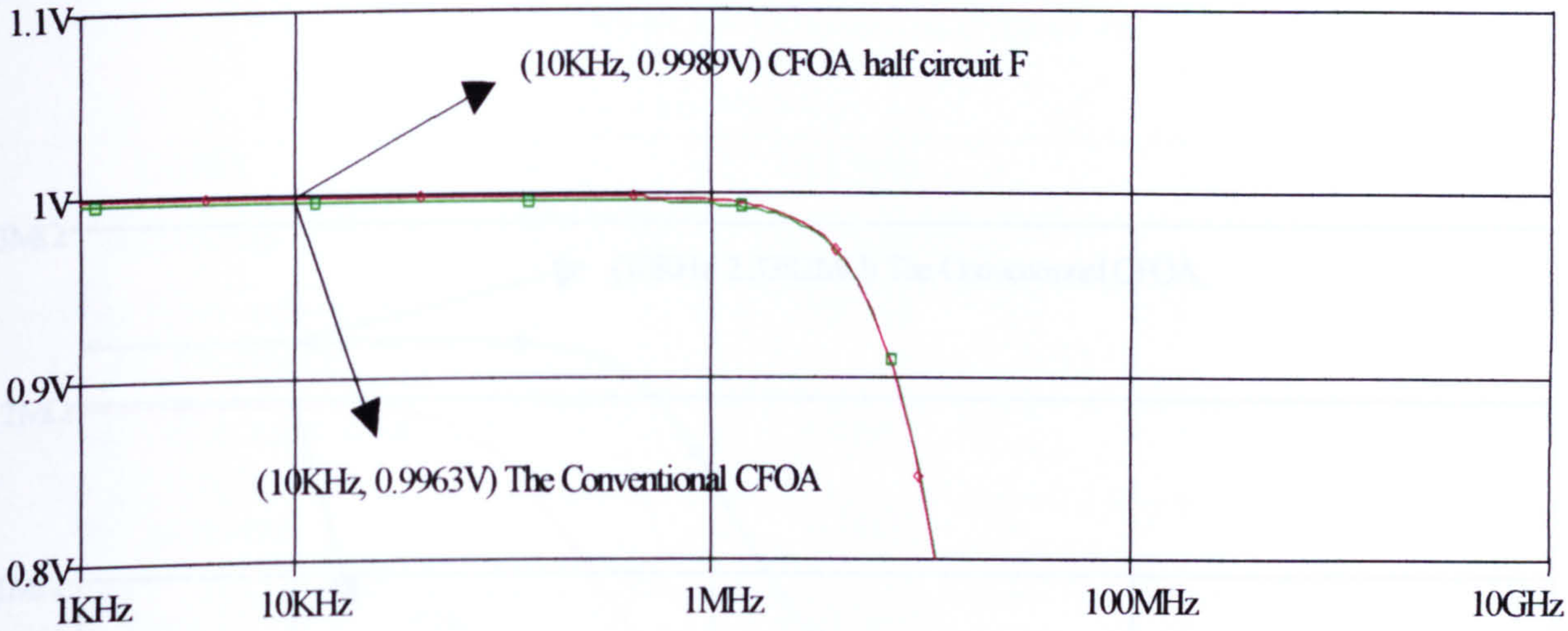


Figure 6.31 AC gain accuracy ~ Frequency

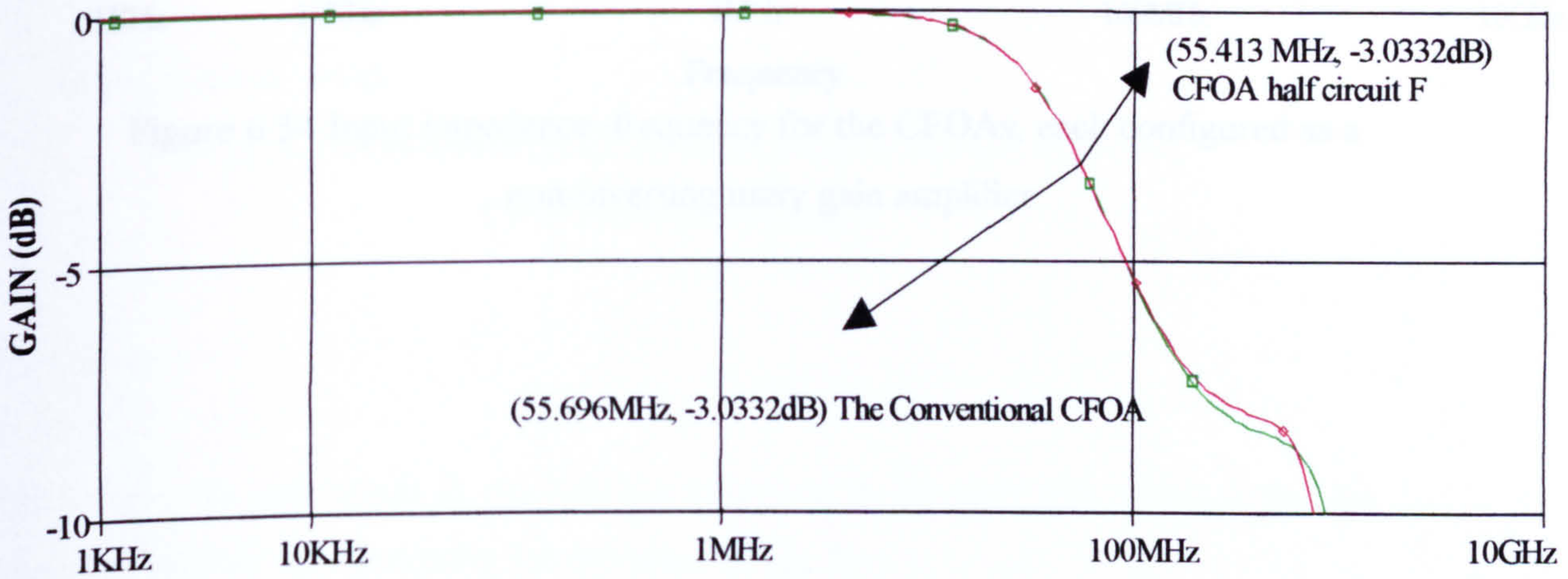


Figure 6.32 Frequency responses for unity closed-loop gain

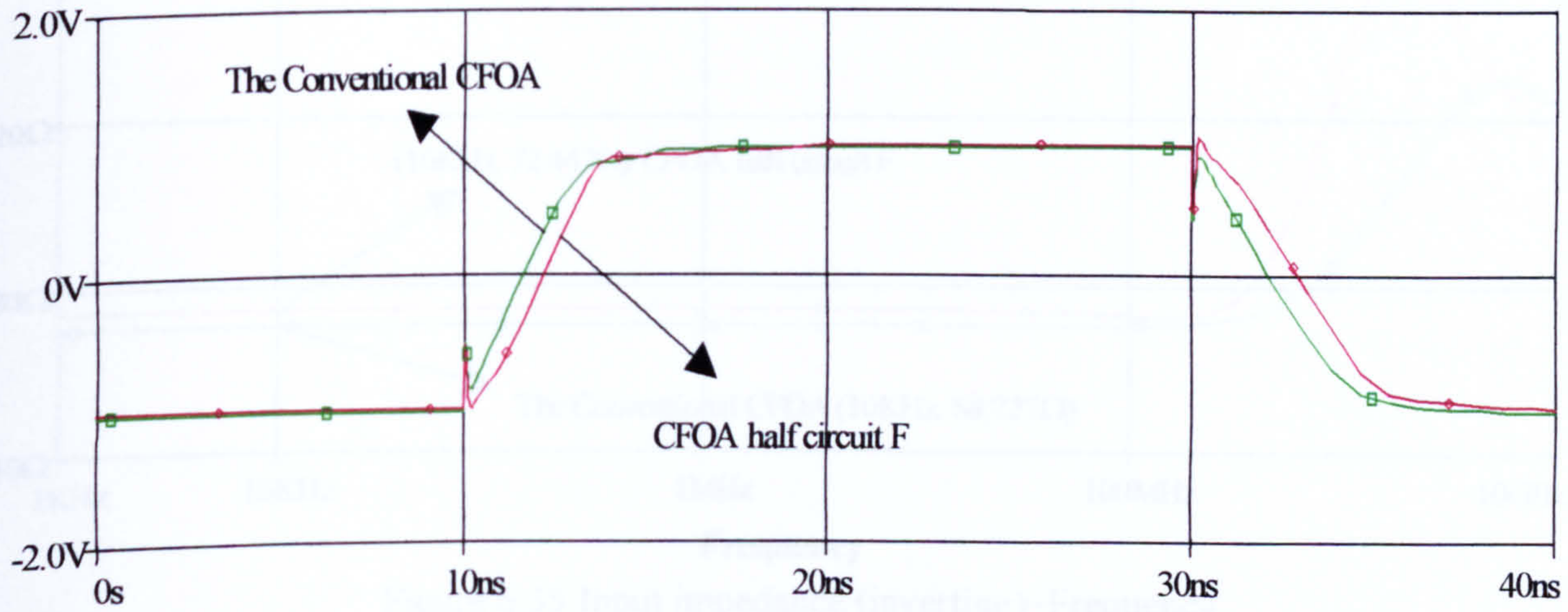


Figure 6.33 Transient response

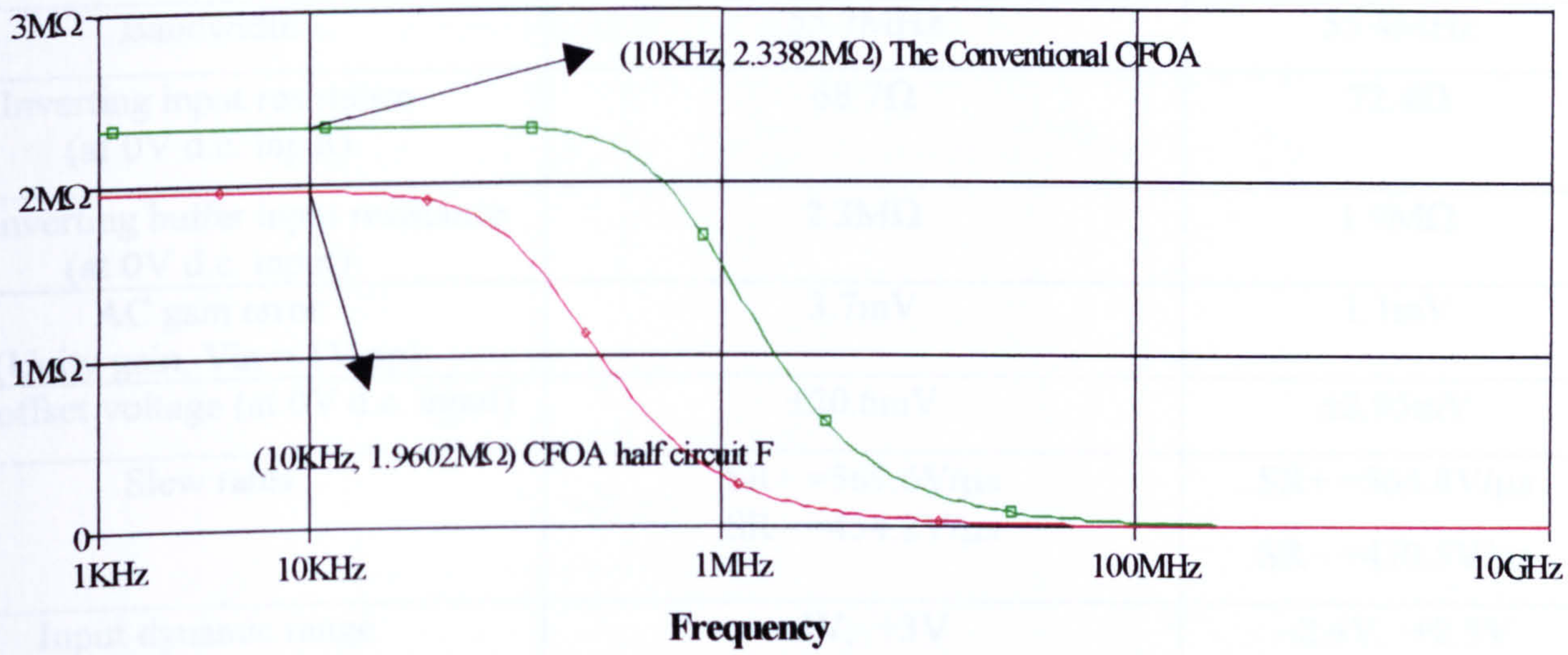


Figure 6.34 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

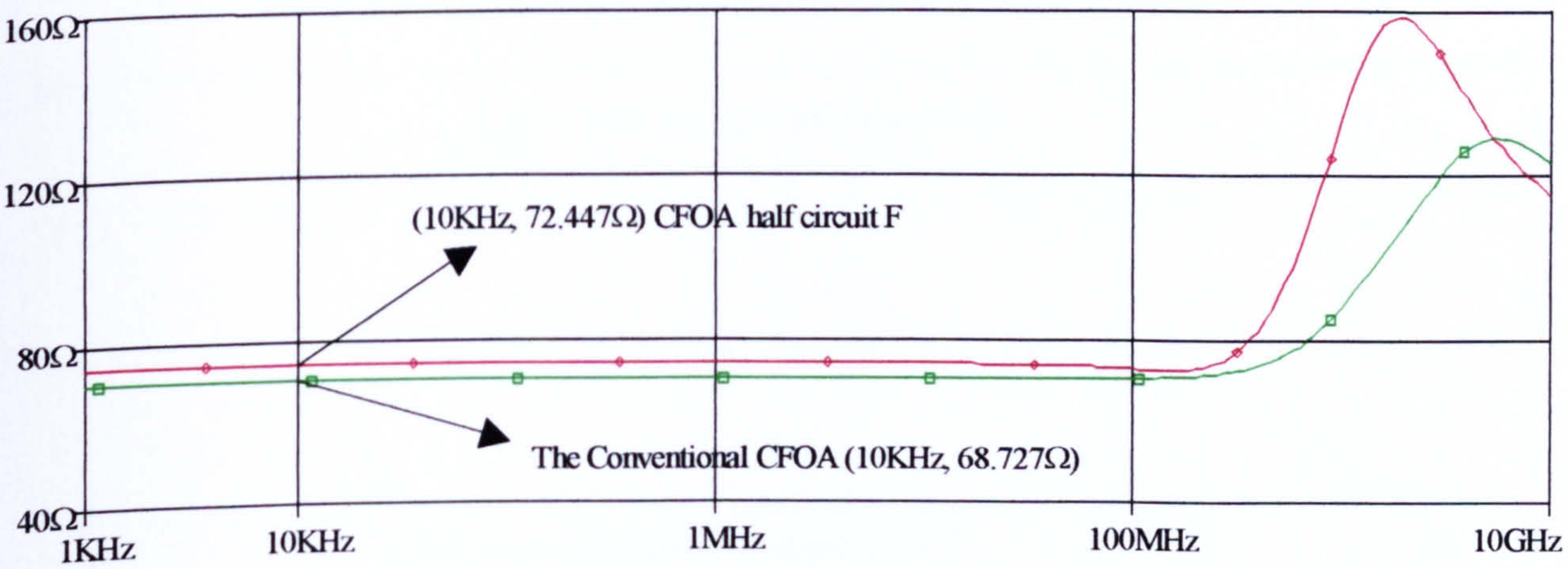


Figure 6.35 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (6.1)	CFOA half circuit F (Fig 6.29)
CMRR	51.4dB	90.2dB
Bandwidth	55.7MHz	55.4MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	72.4Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	1.9MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	1.1mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±2.95mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =564.8V/μs SR– =430.5V/μs
Input dynamic range	–3V, +3V	–2.4V, +2.3V

Table 6.5 Characteristics of the Conventional and the improved CFOA with half-circuit F

Discussion:

Compared with half-circuit E, all that has improved is the slew rate which is due to the use of emitter-follower drive for the bases of Q_3, Q_4.

(6.3.3) Performance with half-circuit G

(6.3.3.A) Performance with half-circuit G (I)

Circuit biasing is the same as used previously for half-circuit E, F.

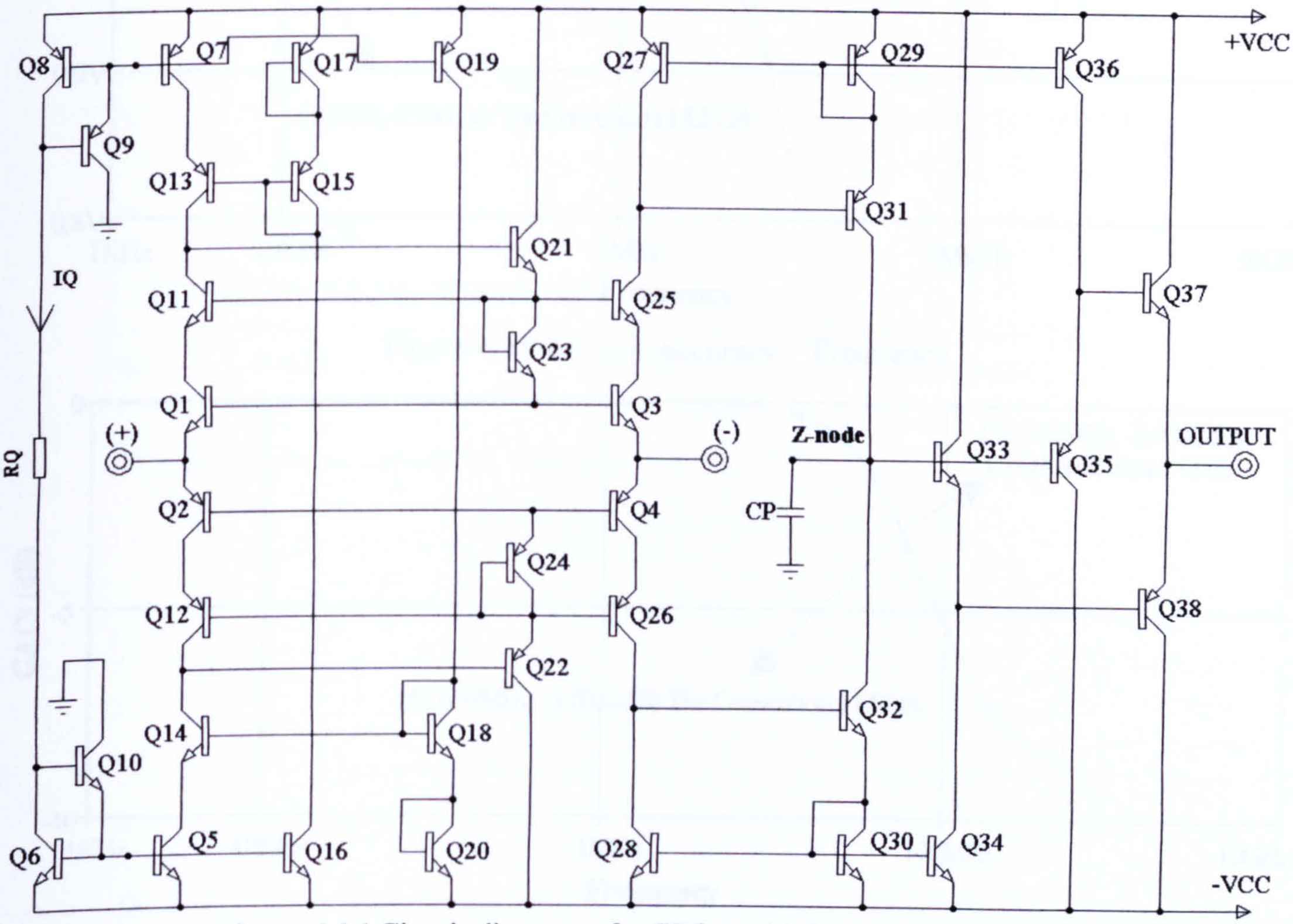


Figure 6.36 Circuit diagram of a CFOA with half-circuit G (I)

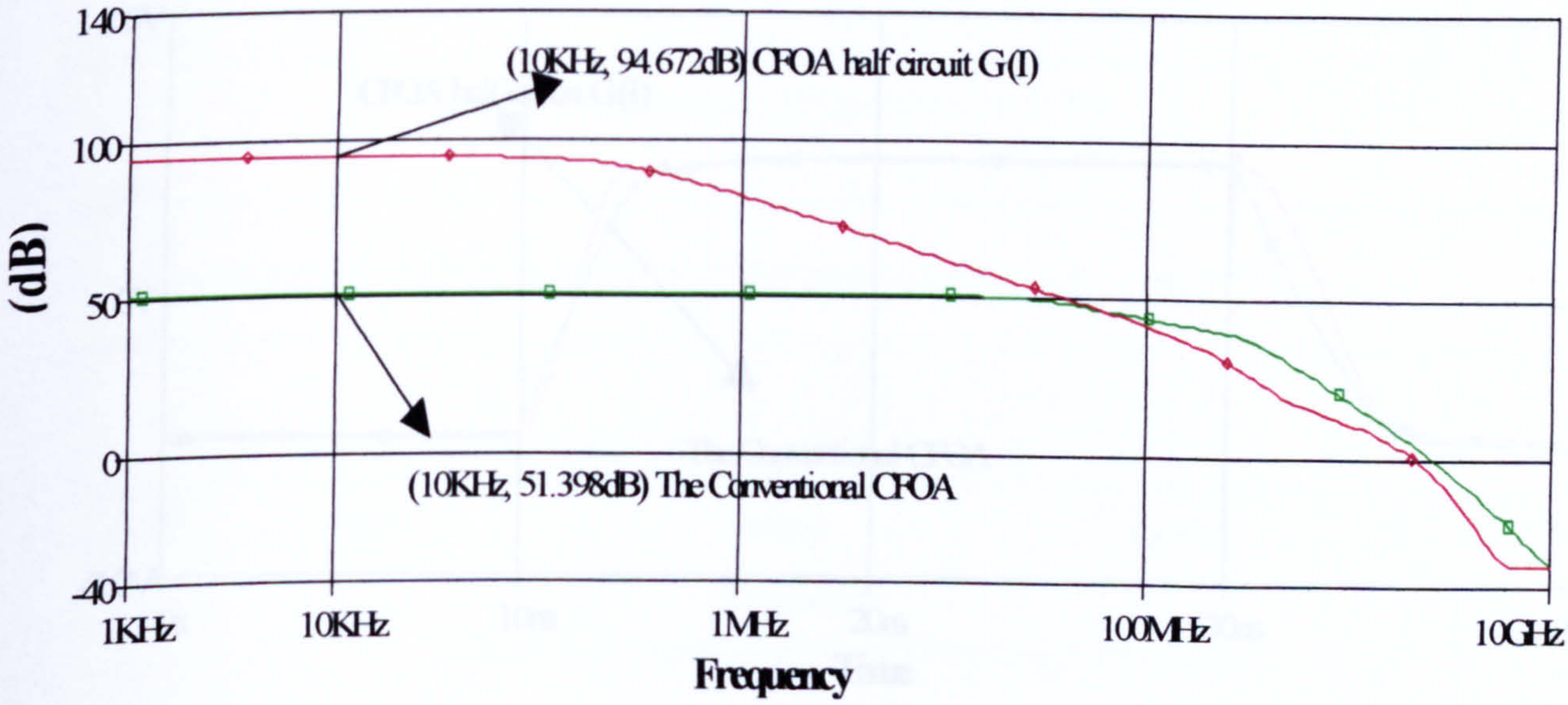


Figure 6.37 CMRR~Frequency

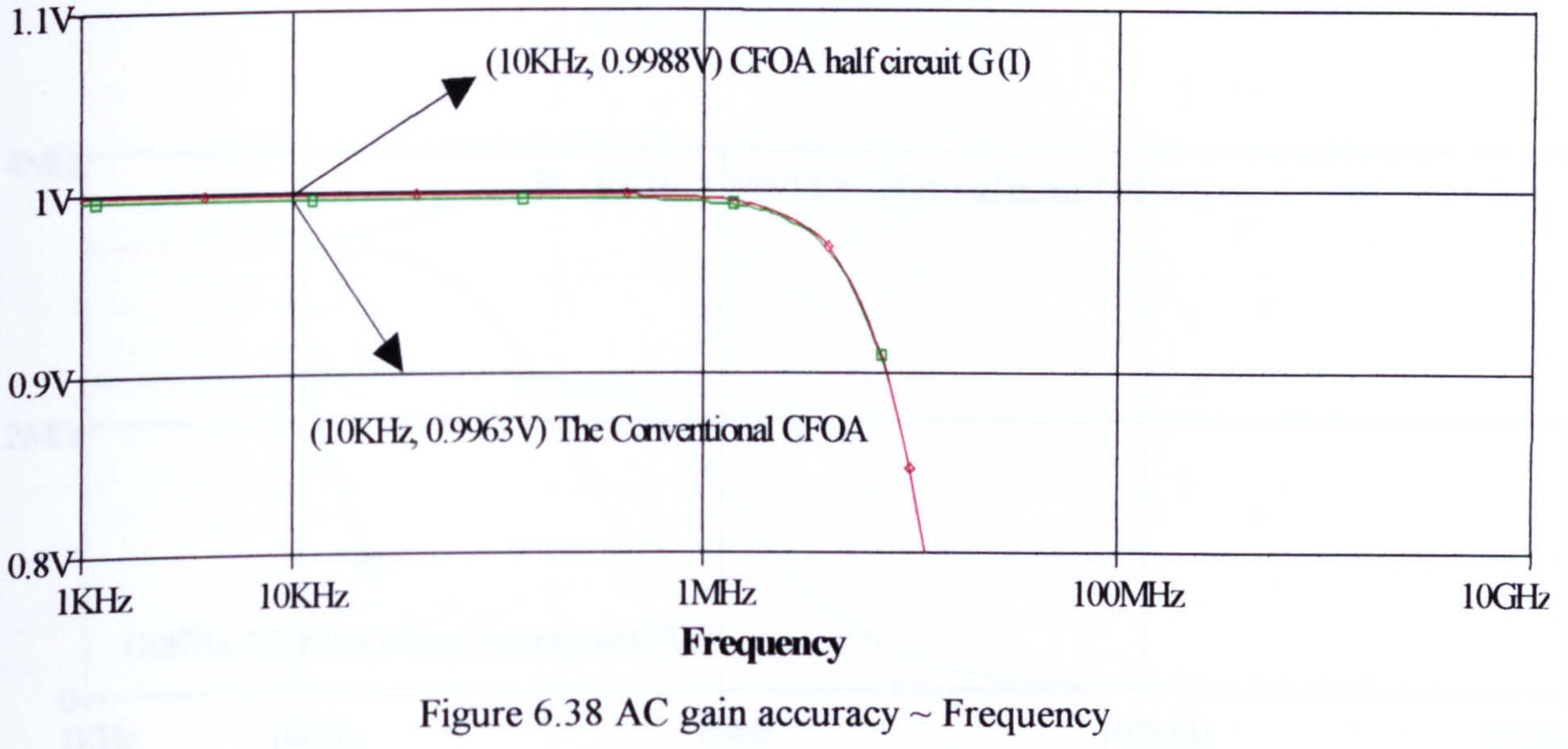


Figure 6.38 AC gain accuracy ~ Frequency

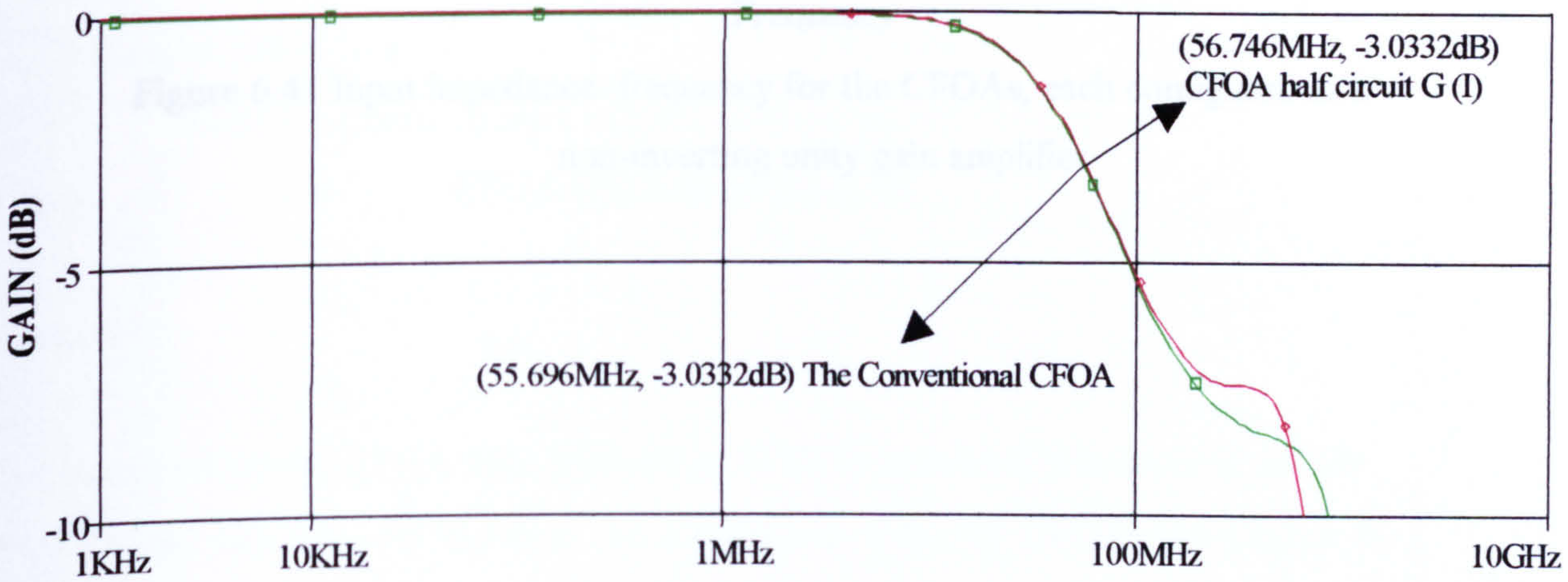


Figure 6.39 Frequency responses for unity closed-loop gain

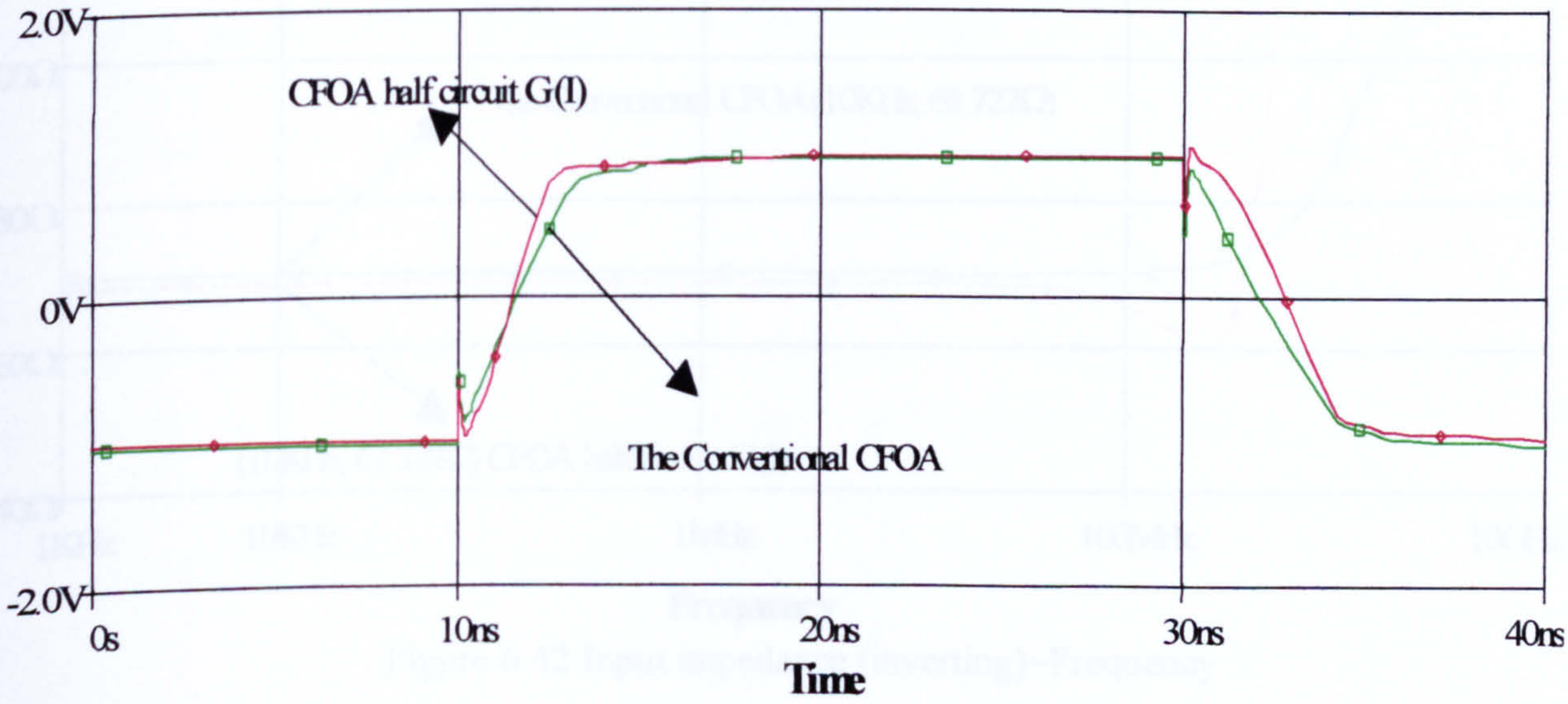


Figure 6.40 Transient response

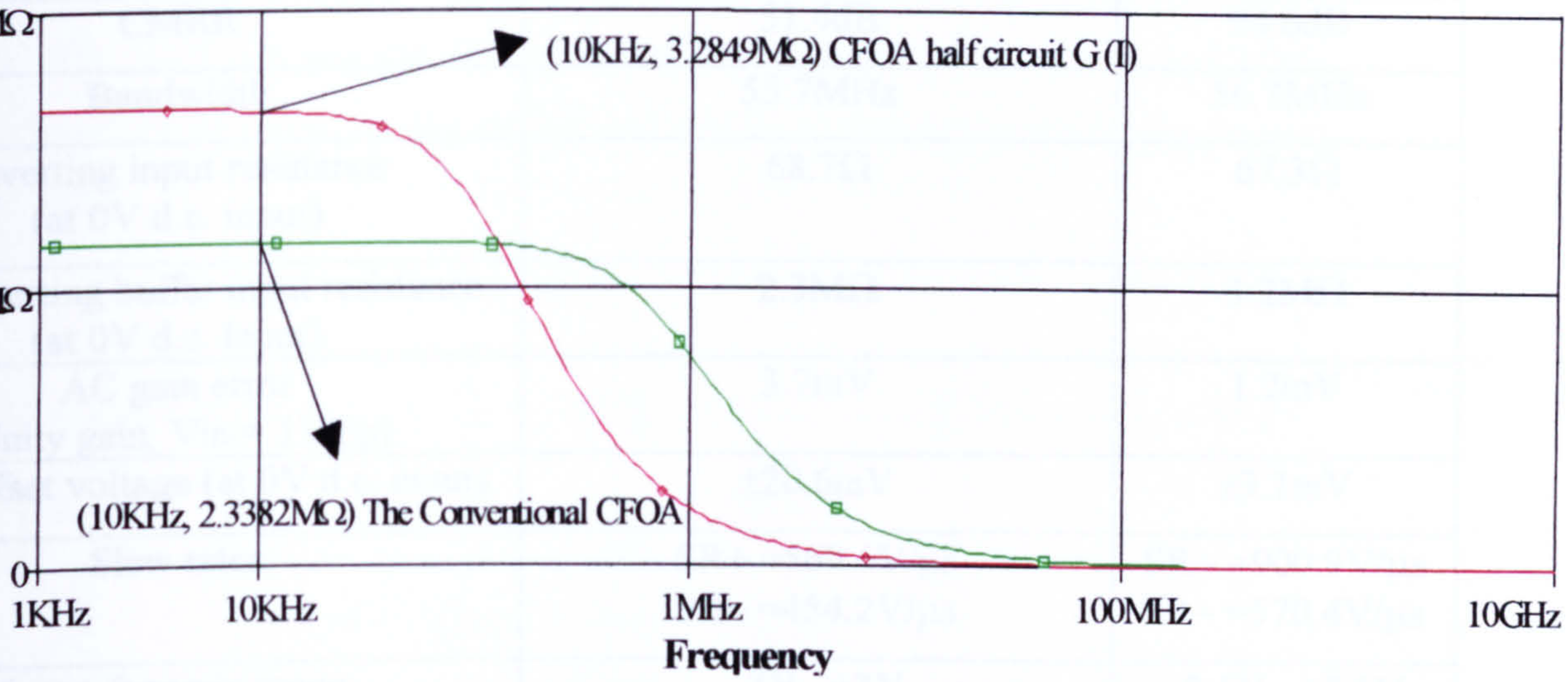


Figure 6.41 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

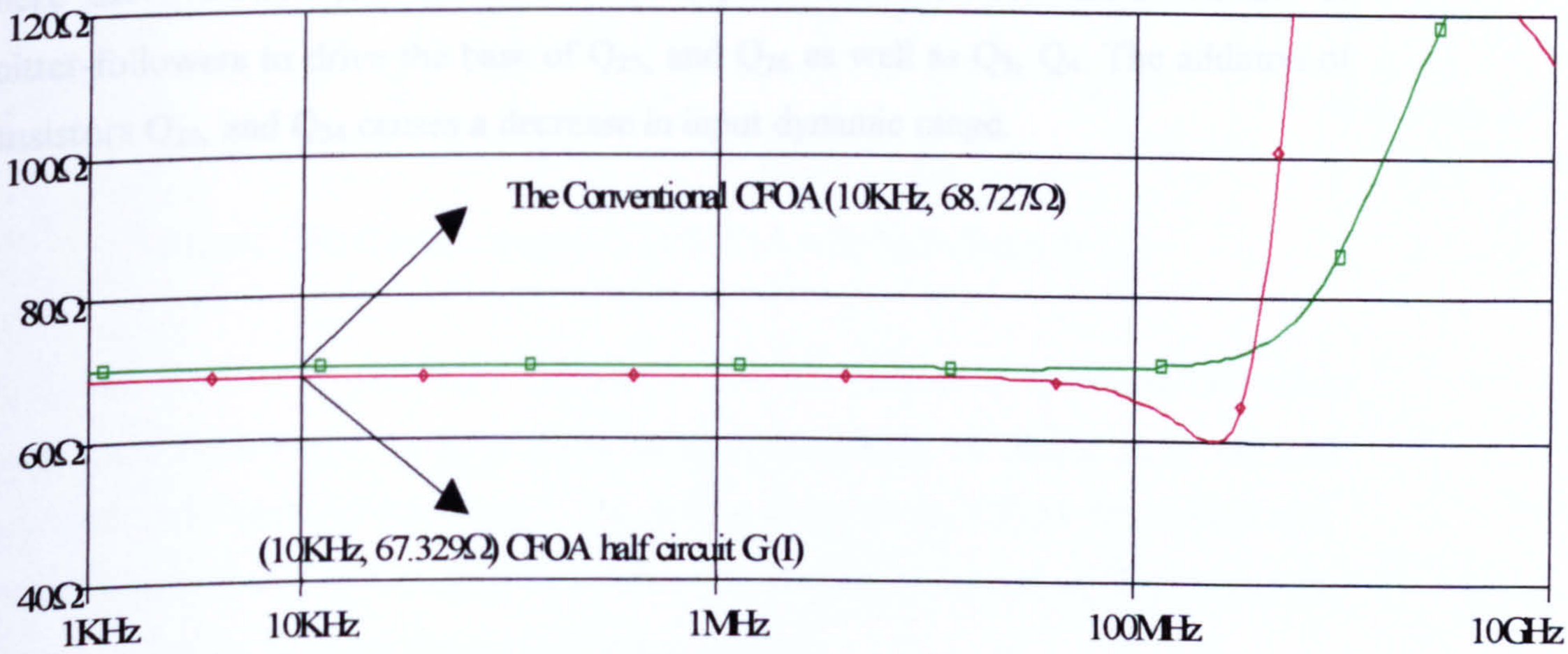


Figure 6.42 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA [6.1]	CFOA half circuit G (I) (Fig 6.36)
CMRR	51.4dB	94.6dB
Bandwidth	55.7MHz	56.7MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	67.3Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3.2MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	1.2mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±3.1mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =900.9V/μs SR– =570.4V/μs
Input dynamic range	–3V, +3V	–2.1V, +2.1V

Table 6.6 Characteristics of the Conventional and the improved CFOA with half-circuit G (I)

Discussion:

The slew rate of the CFOA with half-circuit G (I) is increased dramatically to SR+ =900.9V/μs, and SR– =570.4V/μs, in comparison with the CFOA half-Circuit F where SR+ =564.8V/μs, and SR– =430.5V/μs. The reason for this is the use of emitter-followers to drive the base of Q_{25}, and Q_{26} as well as Q_3, Q_4. The addition of transistors Q_{23}, and Q_{24} causes a decrease in input dynamic range.

(6.3.3.B) Performance with half-circuit G (II)

This scheme does not use the biasing arrangement described for pervious CFOAs. The architecture is based on the design and use in a repeated pattern of a current-transfer cell.

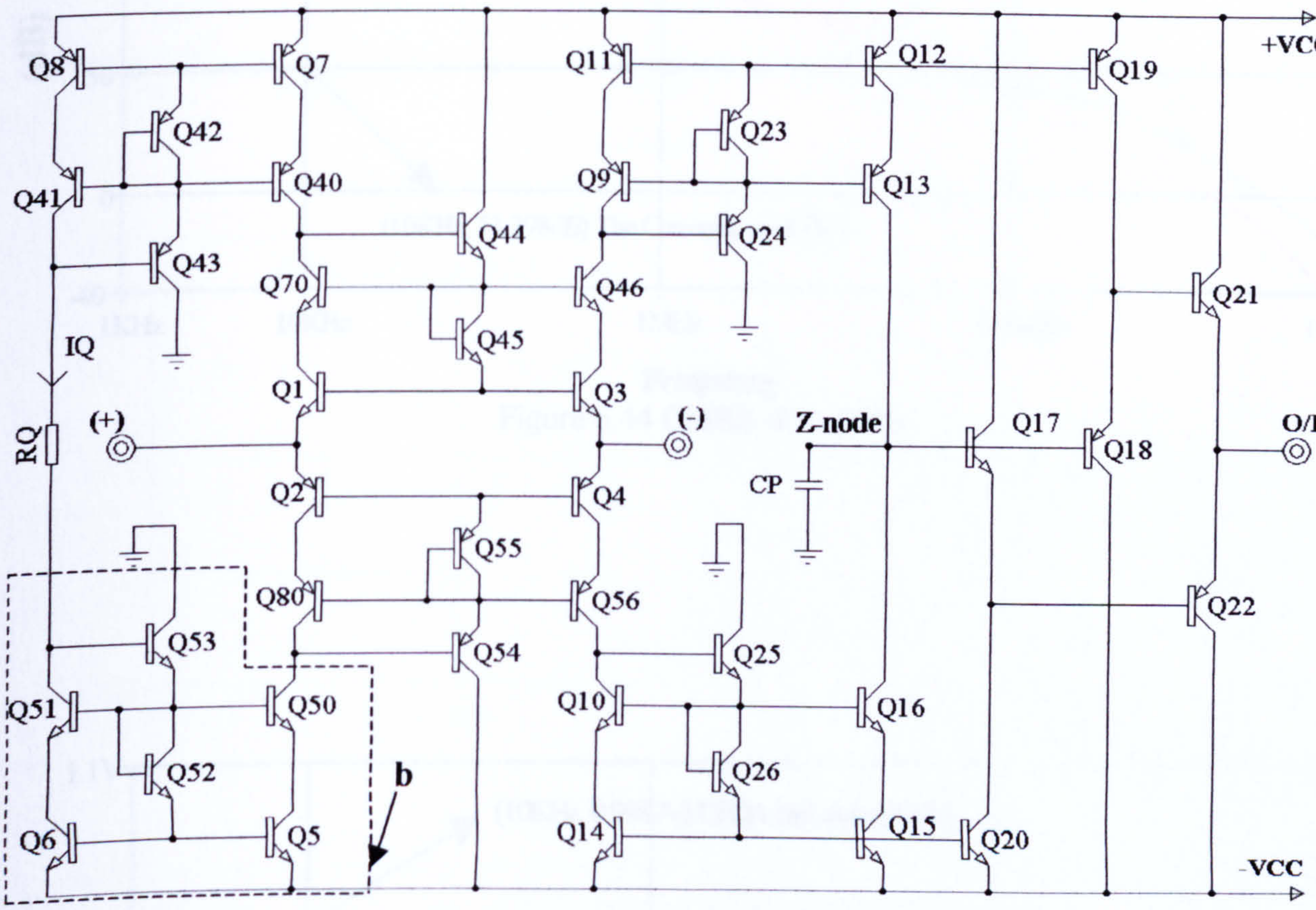


Figure 6.43 Circuit diagram of a CFOA with half-circuit G (II)

The dotted contour, b, encloses a current-transfer cell (described in Chapter 5) which is replicated three times, in NPN form, in the input stage. A similar PNP cell also replicated three times in the design. The output stage of the CFOA is conventional. The mirror-symmetry of the input stage about an imaginary horizontal line joining the '+', and '–' inputs helps promote a low offset voltage.

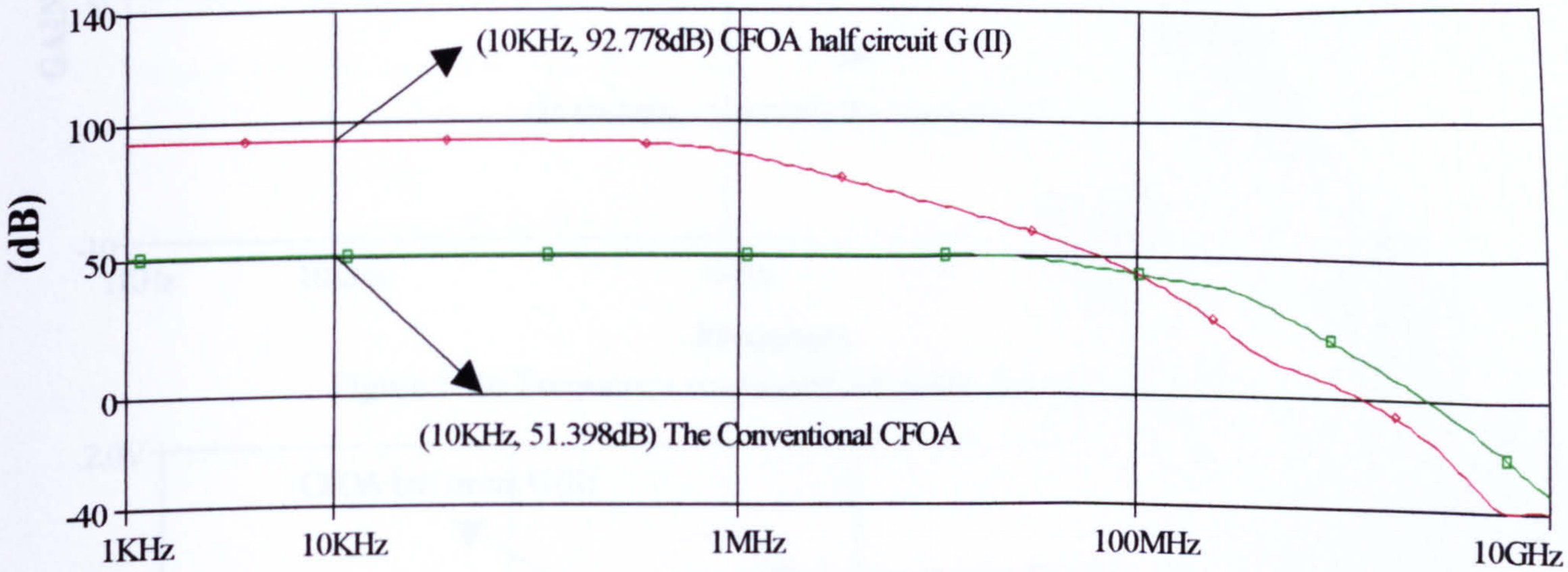


Figure 6.44 CMRR~Frequency

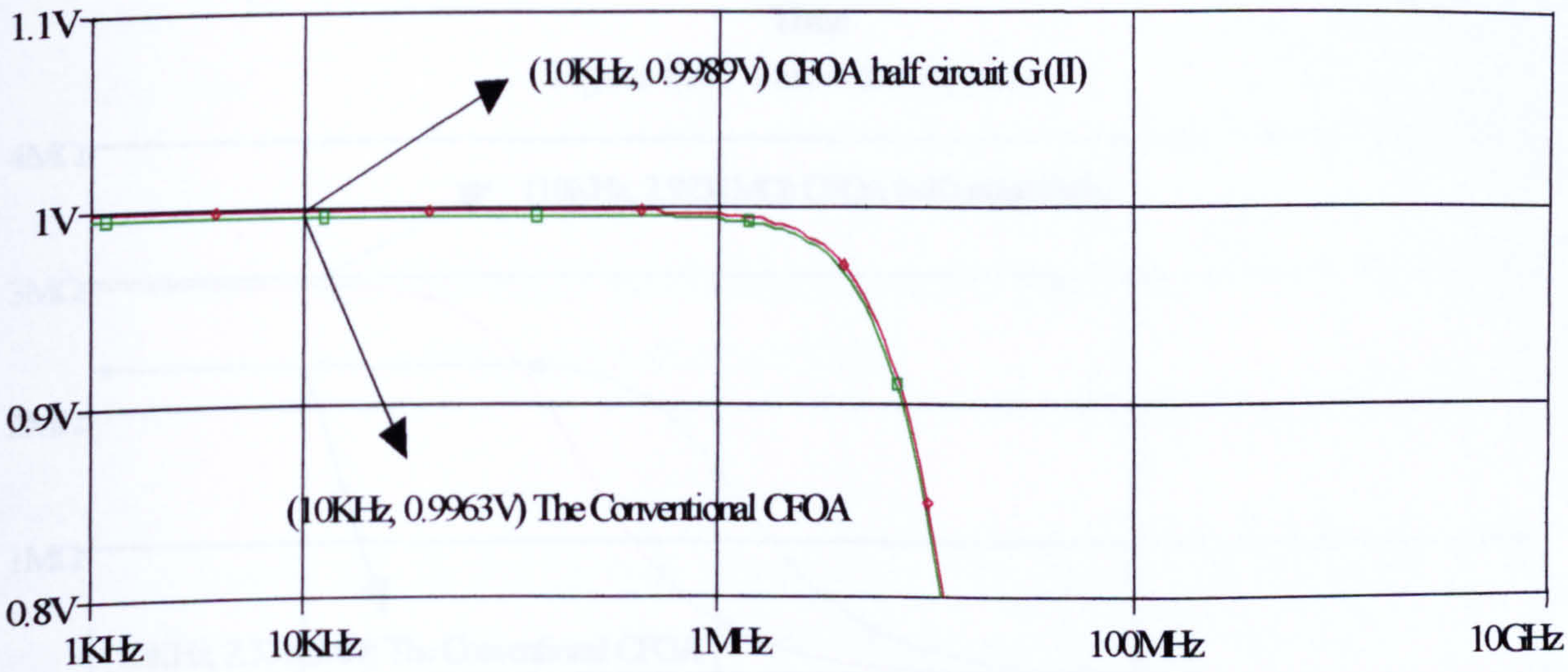


Figure 6.45 AC gain accuracy ~ Frequency

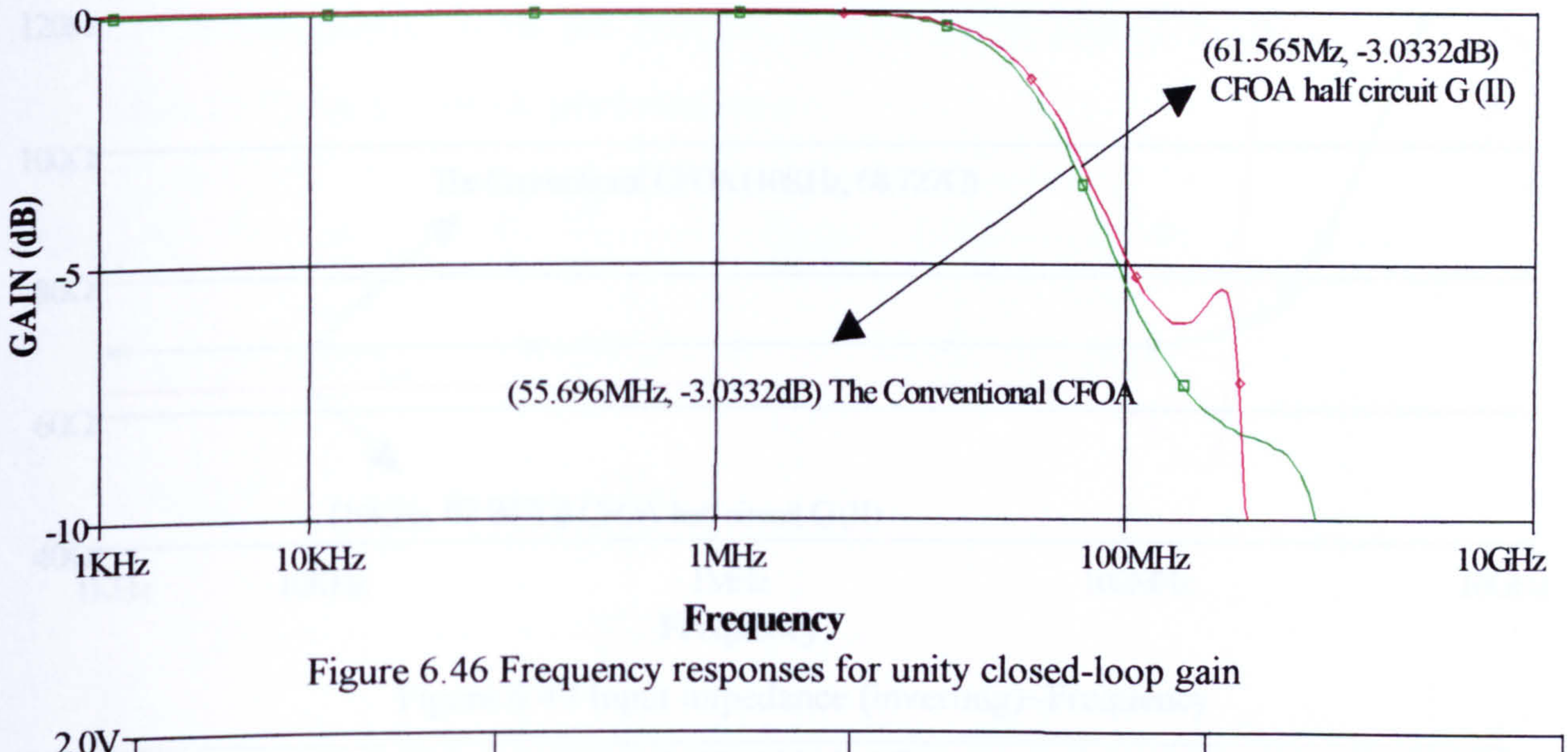


Figure 6.46 Frequency responses for unity closed-loop gain

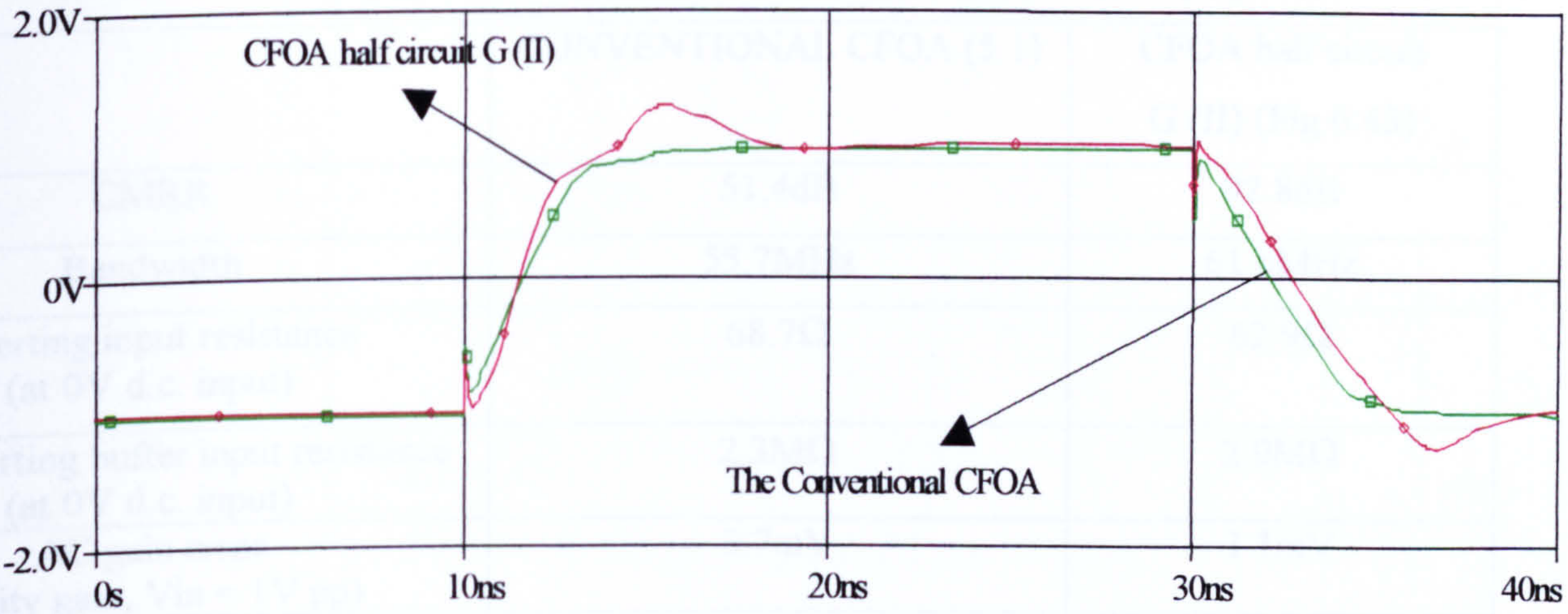


Figure 6.47 transient response

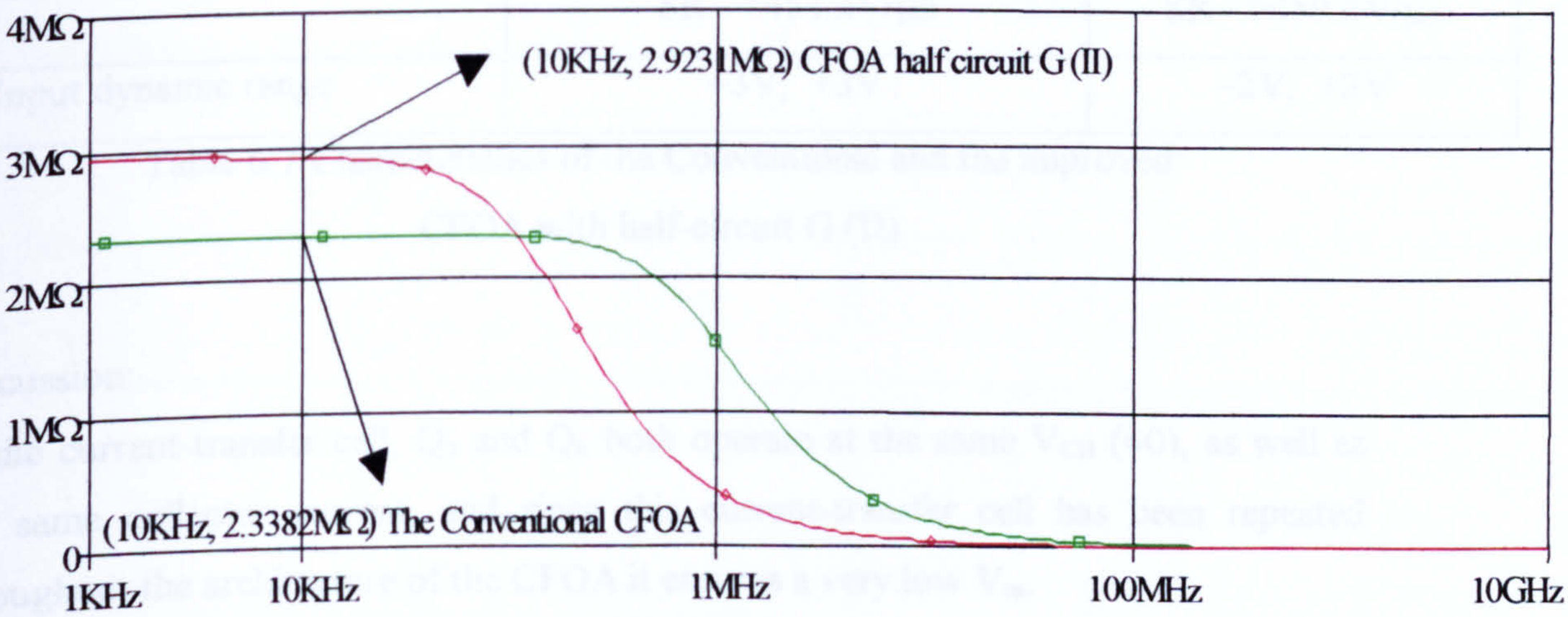


Figure 6.48 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

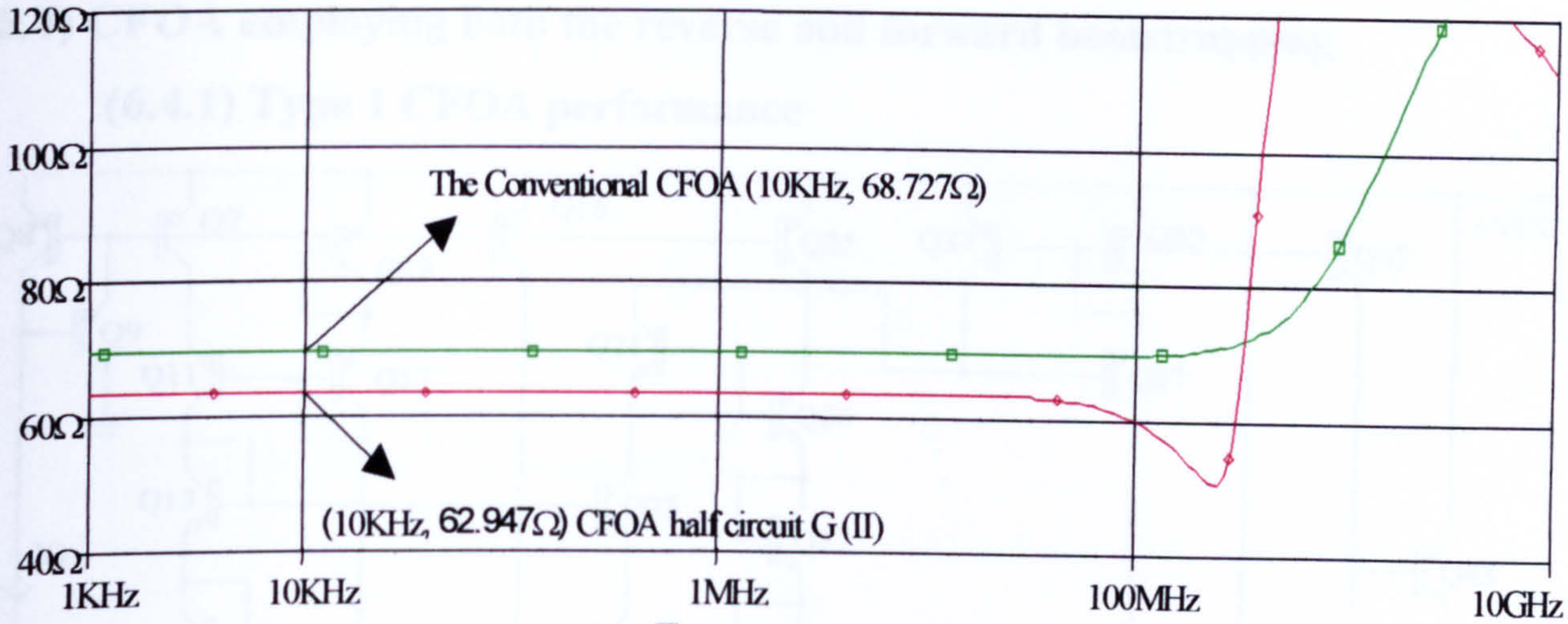


Figure 6.49 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	CFOA half circuit G (II) (Fig 6.43)
CMRR	51.4dB	92.8dB
Bandwidth	55.7MHz	61.6MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	62.9Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	2.9MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	1.1mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±0.75mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =950.6V/μs SR– =459.4V/μs
Input dynamic range	–3V, +3V	–2V, +2V

Table 6.7 Characteristics of the Conventional and the improved CFOA with half-circuit G (II)

Discussion:

In the current-transfer cell, Q_5 and Q_6 both operate at the same V_{CB} ($\approx$0), as well as the same collector current, and since this current-transfer cell has been repeated throughout the architecture of the CFOA it ensures a very low V_{os}.

(6.4) CFOA employing both the reverse and forward bootstrapping

(6.4.1) Type 1 CFOA performance

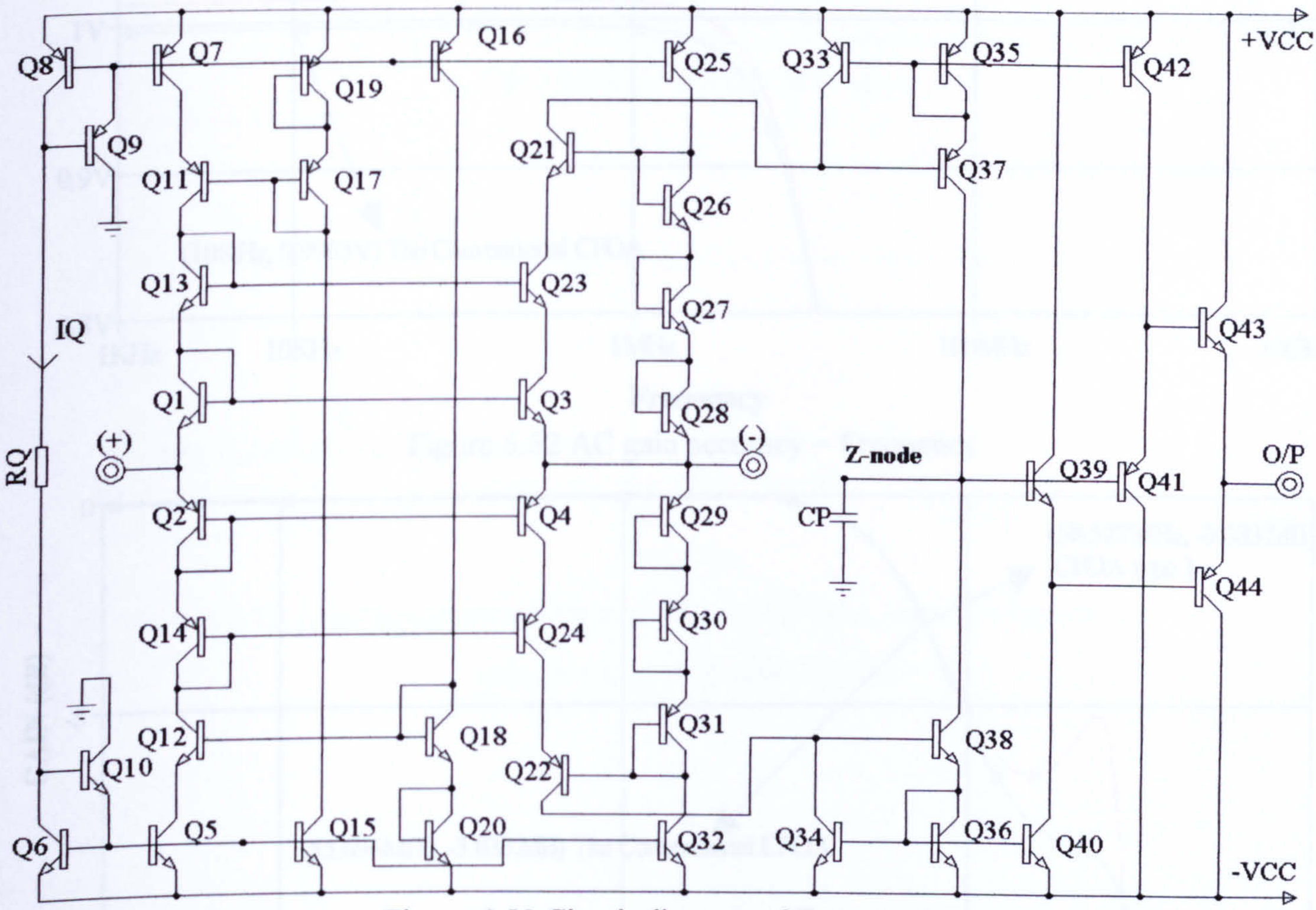


Figure 6.50 Circuit diagram of Type 1 CFOA

The new type of CFOA, shown in Fig.6.50, combines the high CMRR feature of circuit C, in Fig.6.8, with the high bandwidth feature of the circuit G (II) in Fig.6.43. The input circuit is that of half-circuit E.

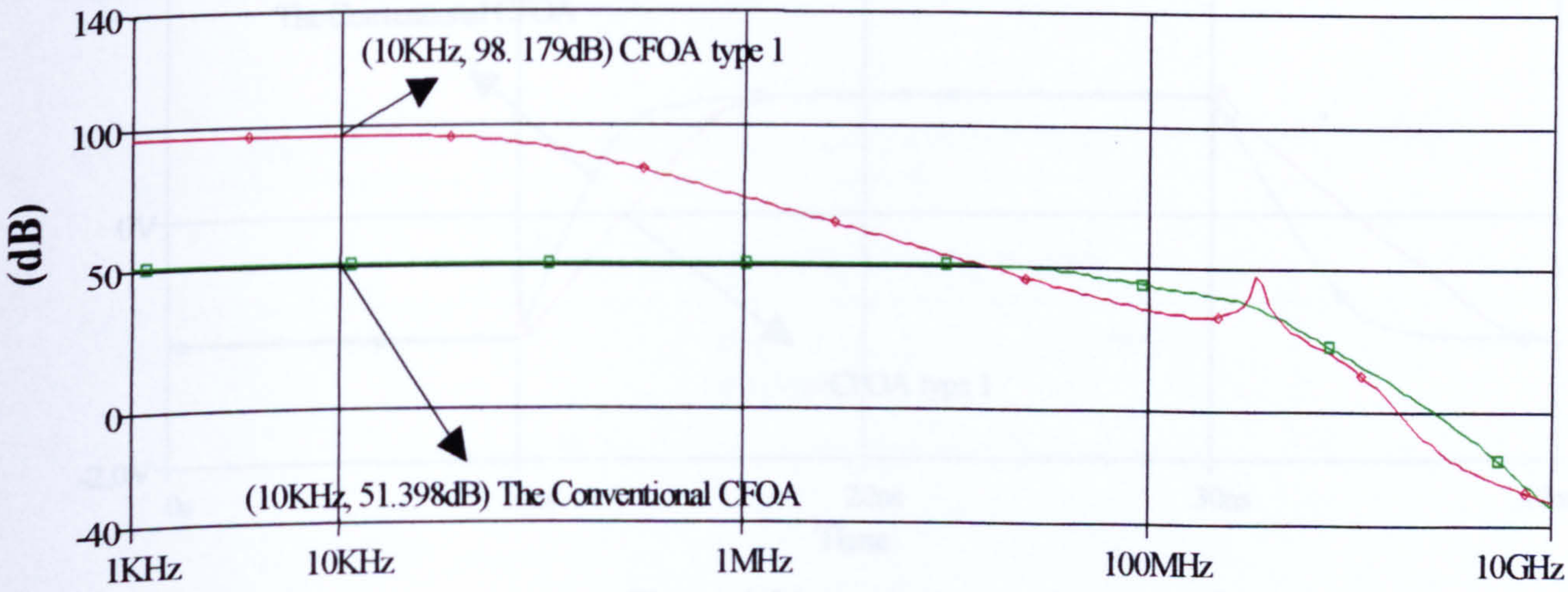


Figure 6.51 CMRR~Frequency

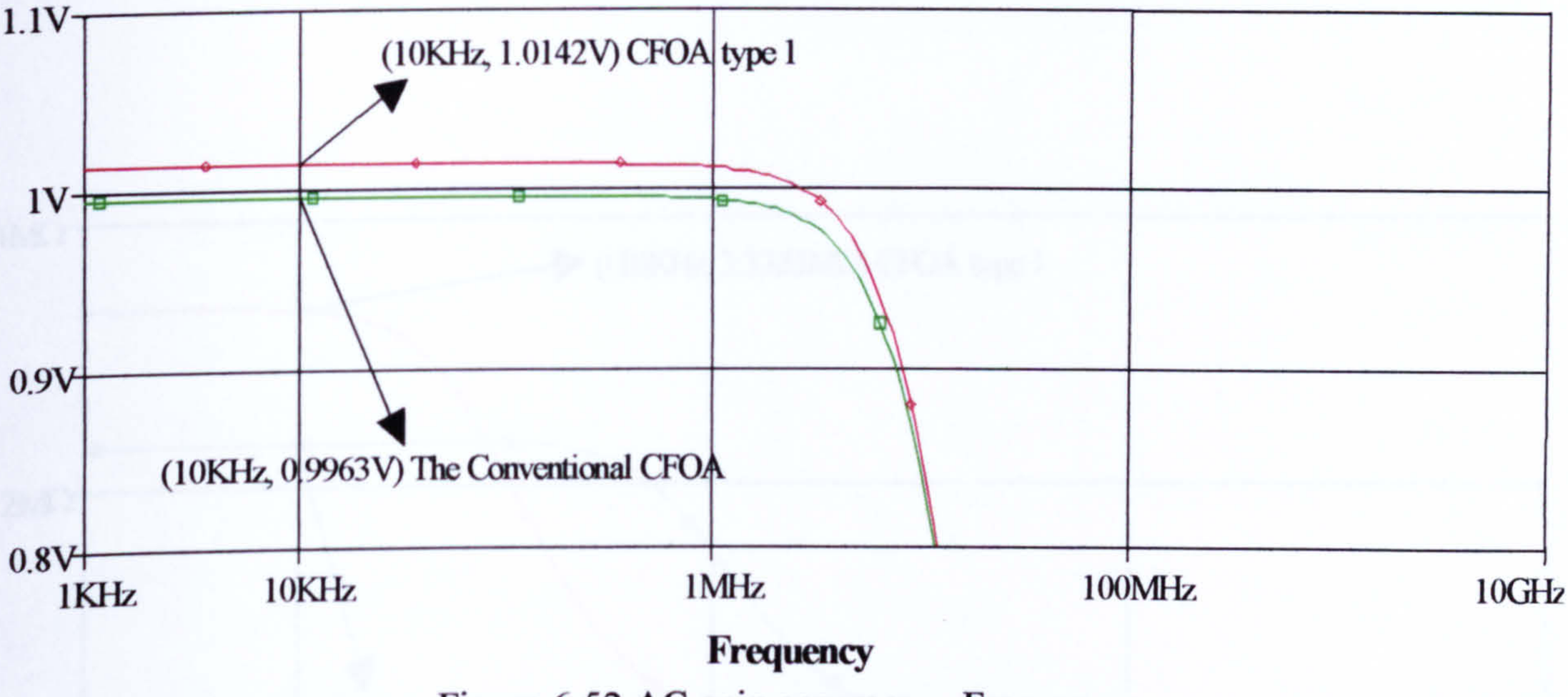


Figure 6.52 AC gain accuracy ~ Frequency

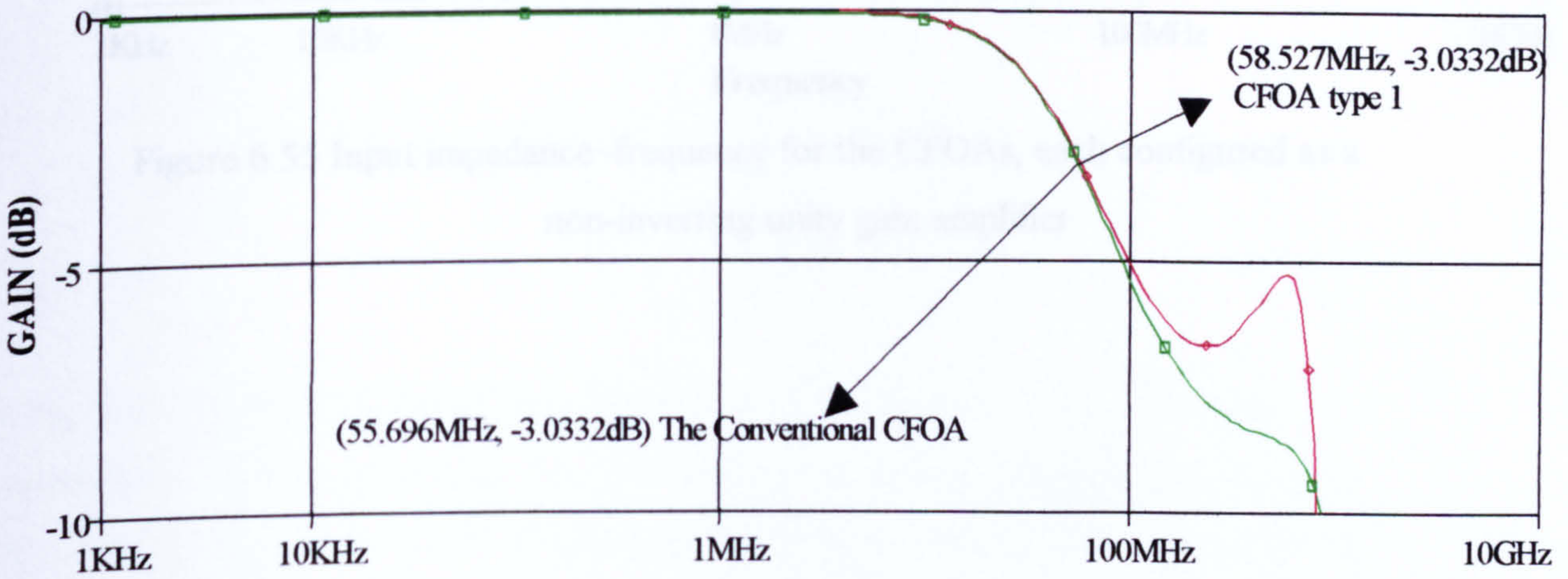


Figure 6.53 Frequency responses for unity closed-loop gain

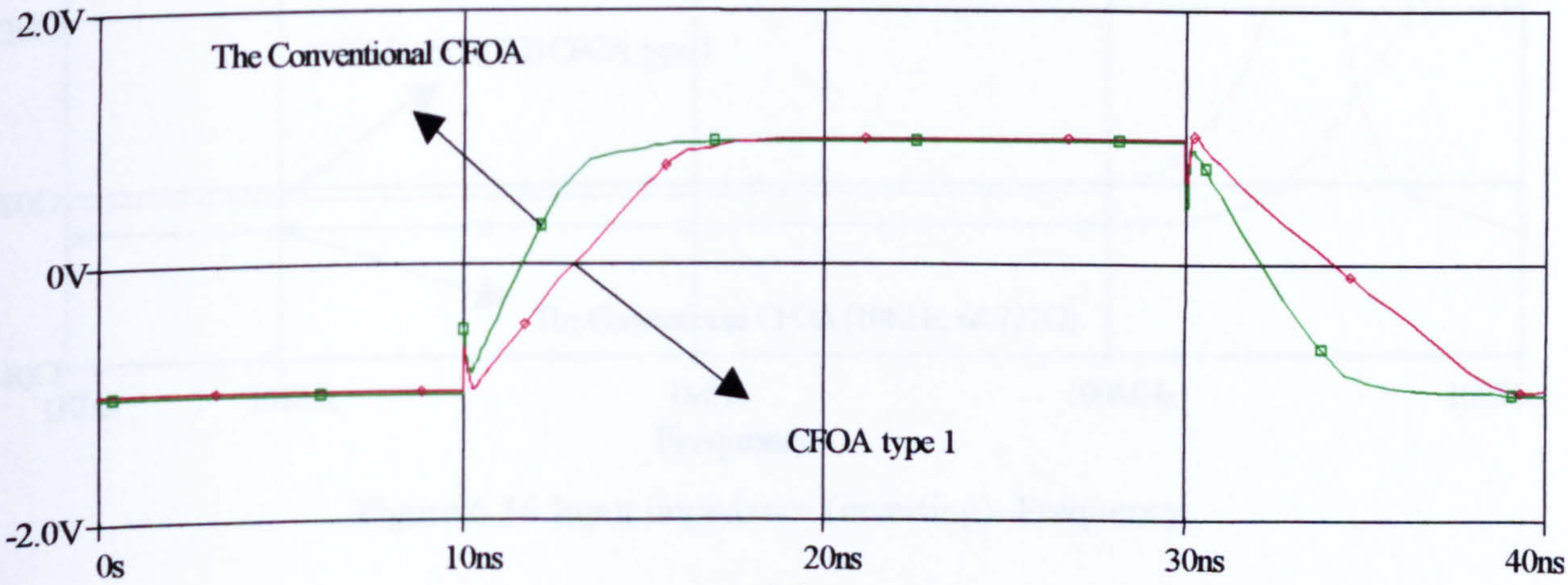


Figure 6.54 transient response

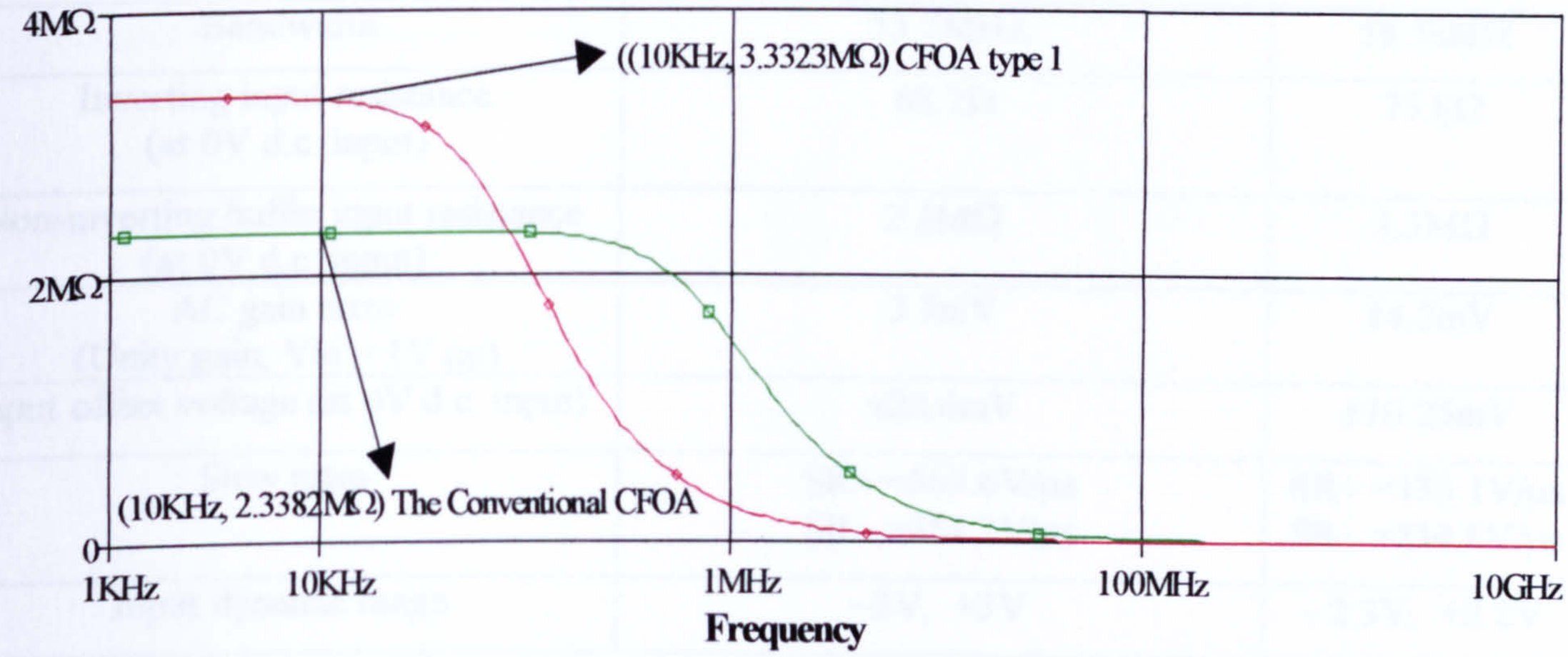


Figure 6.55 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

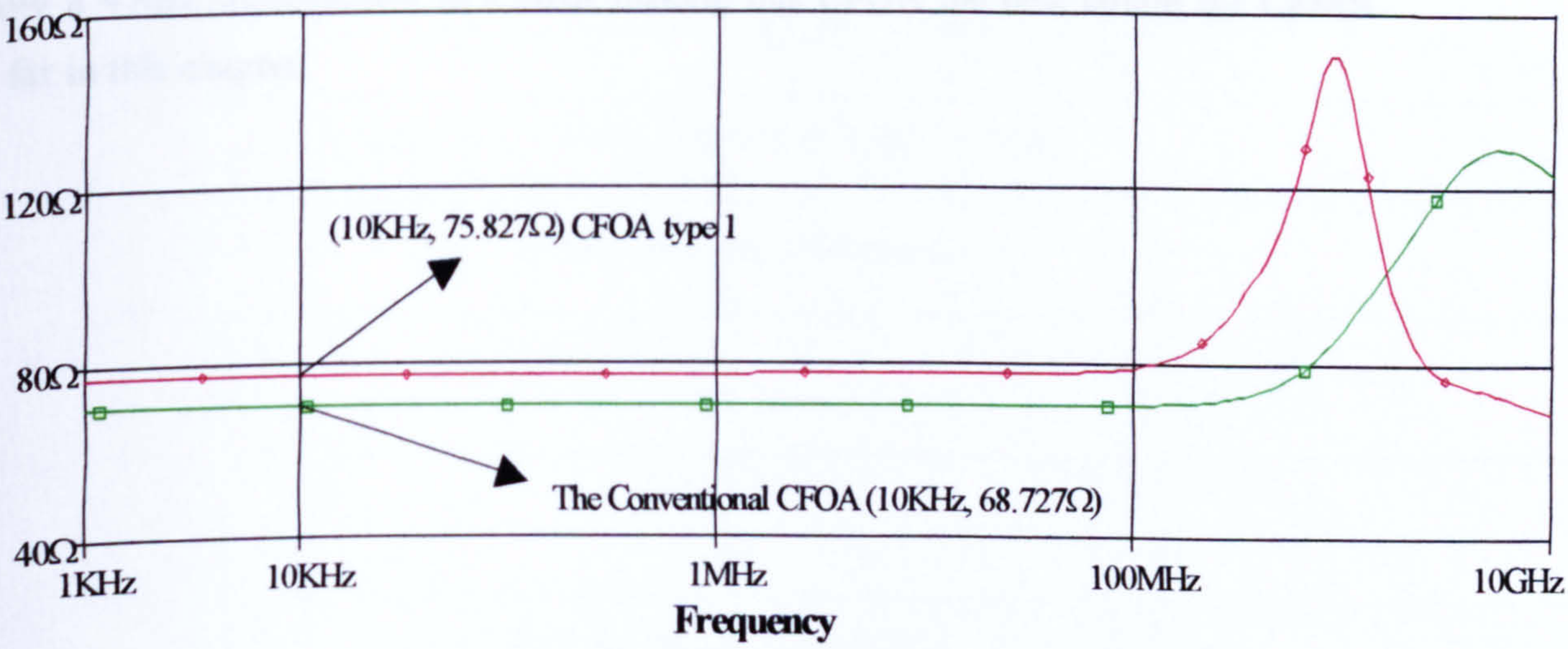


Figure 6.56 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	Type 1 CFOA (Fig 6.50)
CMRR	51.4dB	98.1dB
Bandwidth	55.7MHz	58.5MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	75.8Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3.3MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	14.2mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±10.25mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =335.1V/μs SR– =234.8V/μs
Input dynamic range	–3V, +3V	–2.3V, +2.2V

Table 6.8 Characteristics of the Conventional and Type 1 CFOA

Discussion:

In Fig.6.50, the Type 1 CFOA illustrates a new architecture for the CFOA based on a combination of two previously reported designs described earlier in this Chapter. Comparative simulation results (Table 6.8) for the conventional and Type 1 CFOA, show a 47dB improvement in CMRR making this CFOA the best circuit for CMRR so far in this chapter.

(6.4.2) Type 2 CFOA performance

This resembles the CFOA with half-circuit E, but the input biasing is different and two forms of bootstrapping are re-employed.

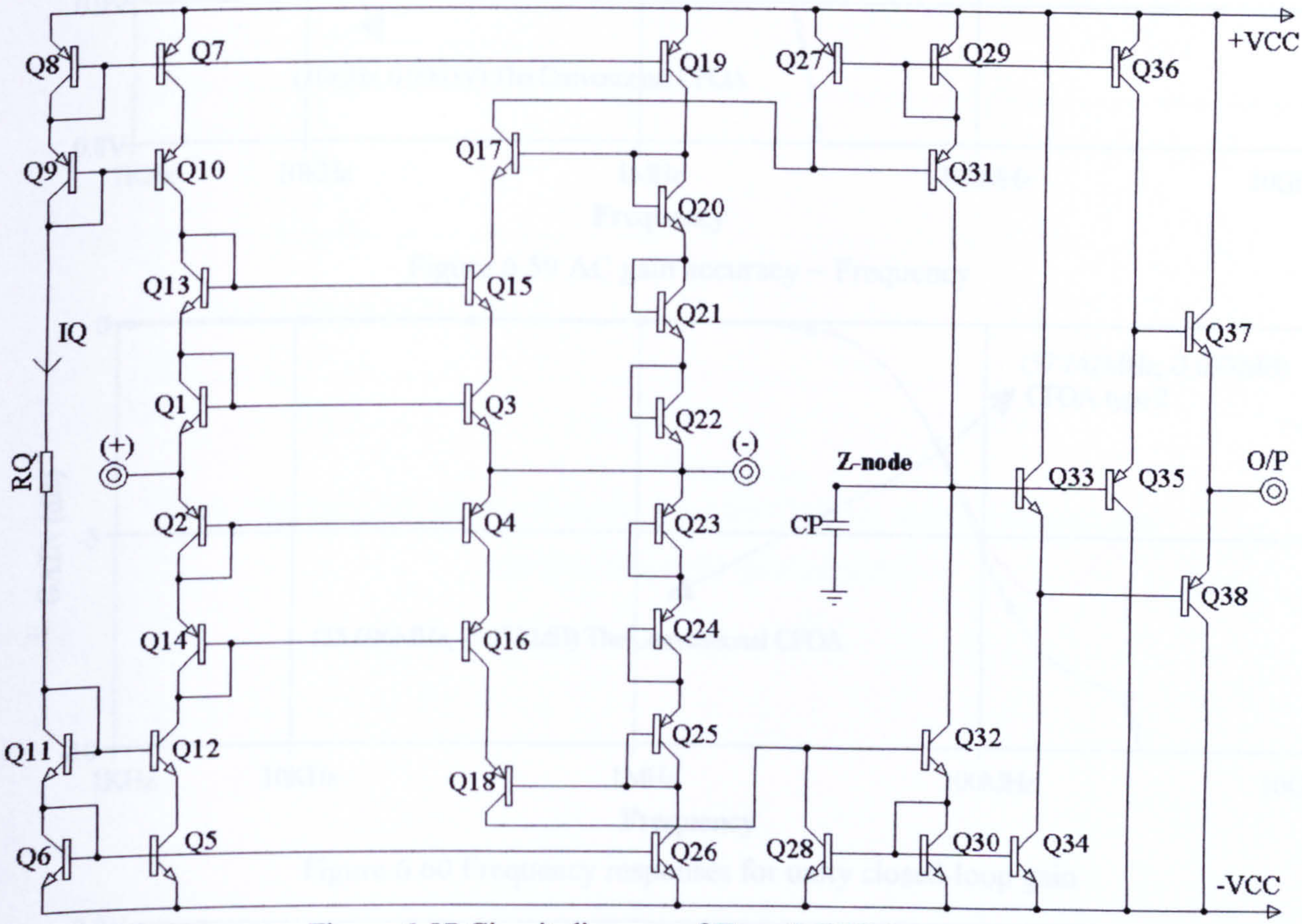


Figure 6.57 Circuit diagram of Type 2 CFOA

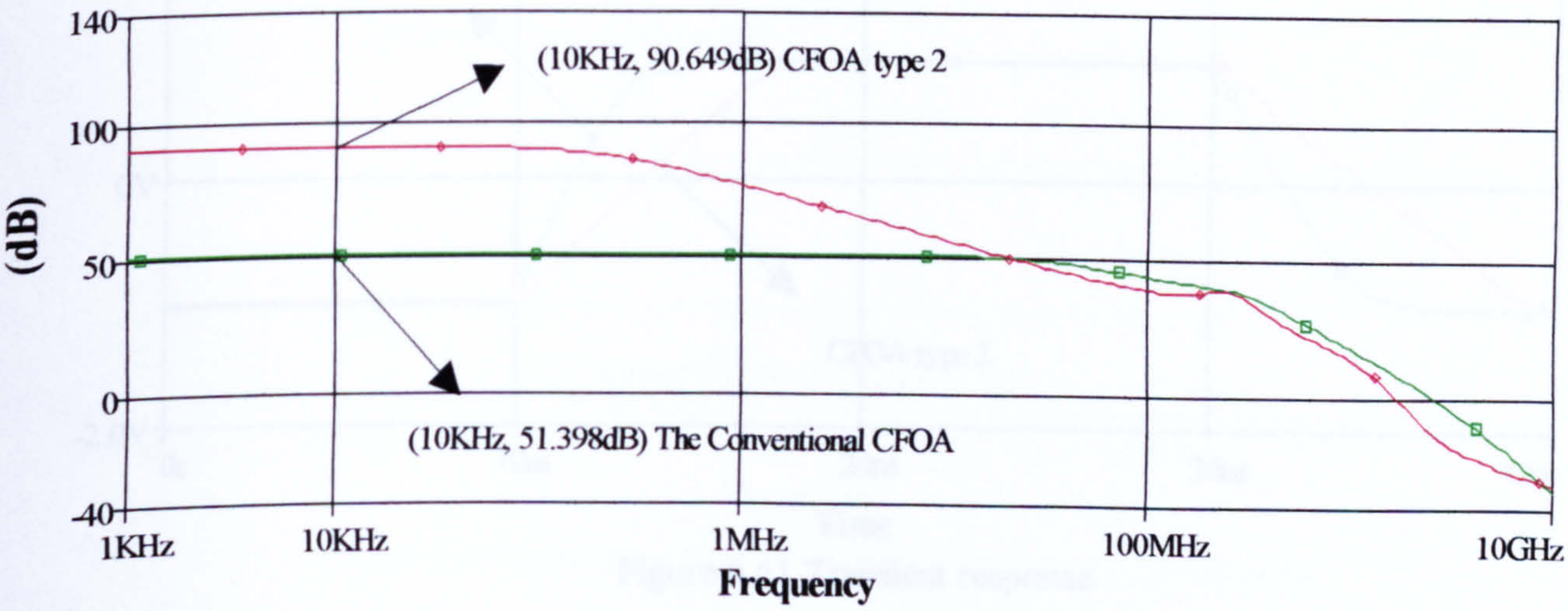


Figure 6.58 CMRR~Frequency

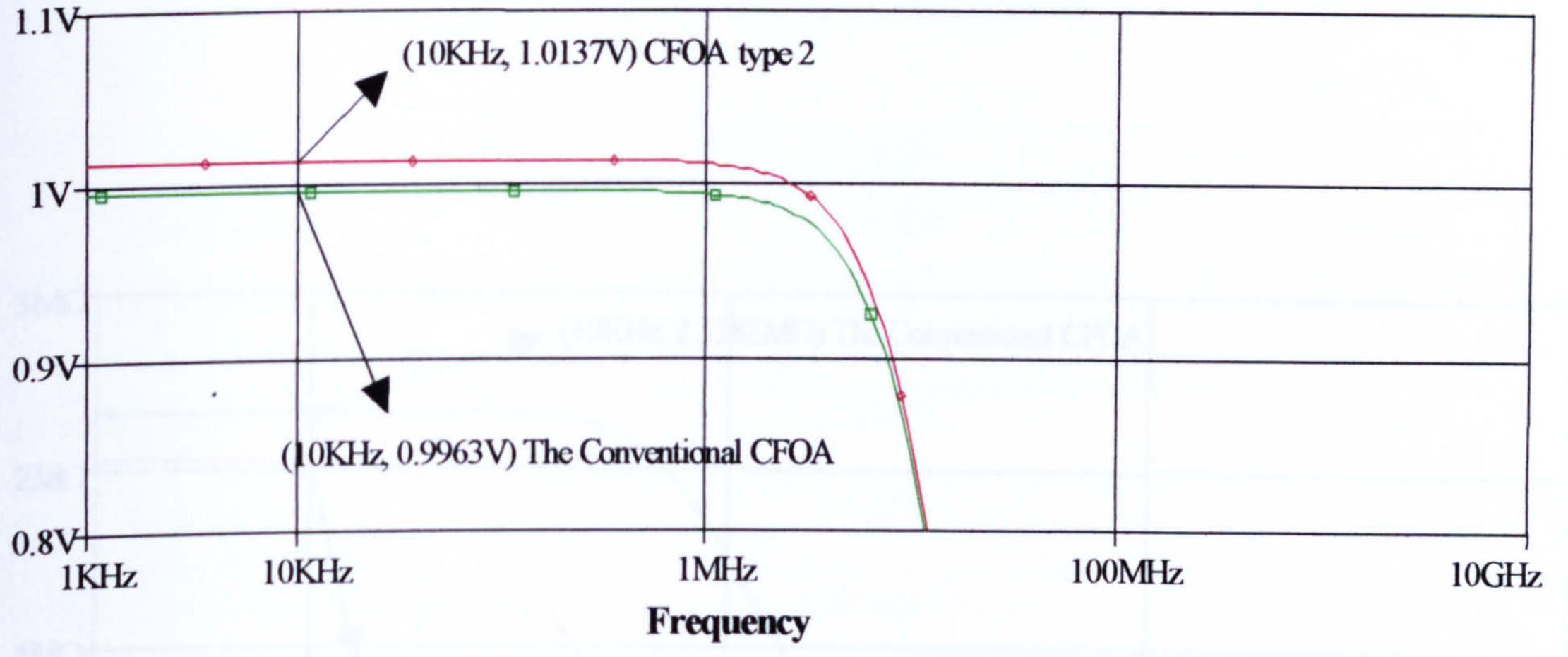


Figure 6.59 AC gain accuracy ~ Frequency

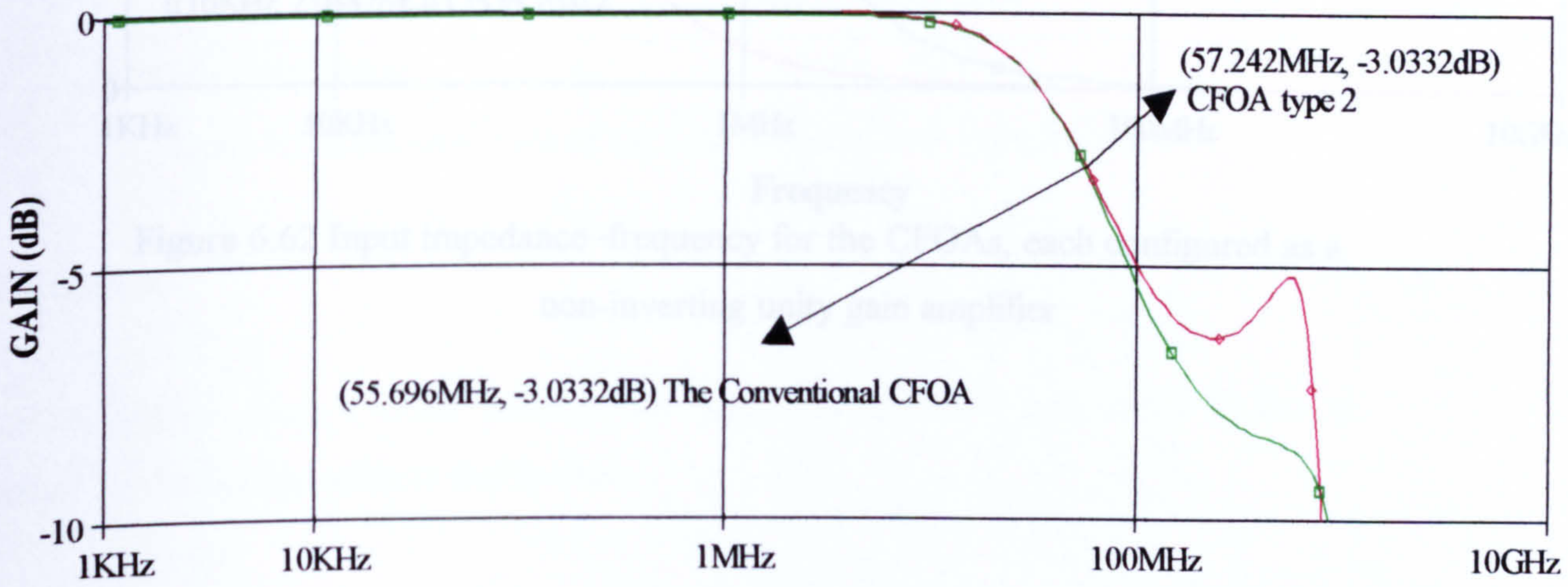


Figure 6.60 Frequency responses for unity closed-loop gain

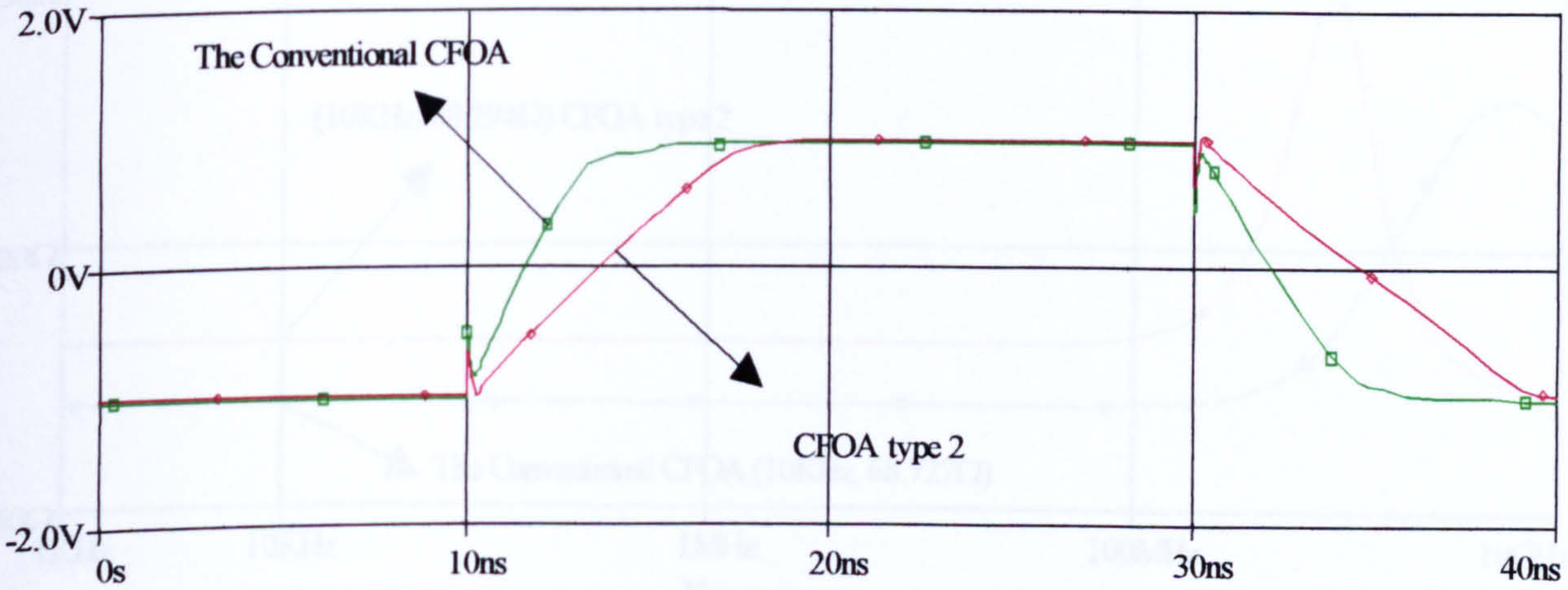


Figure 6.61 Transient response

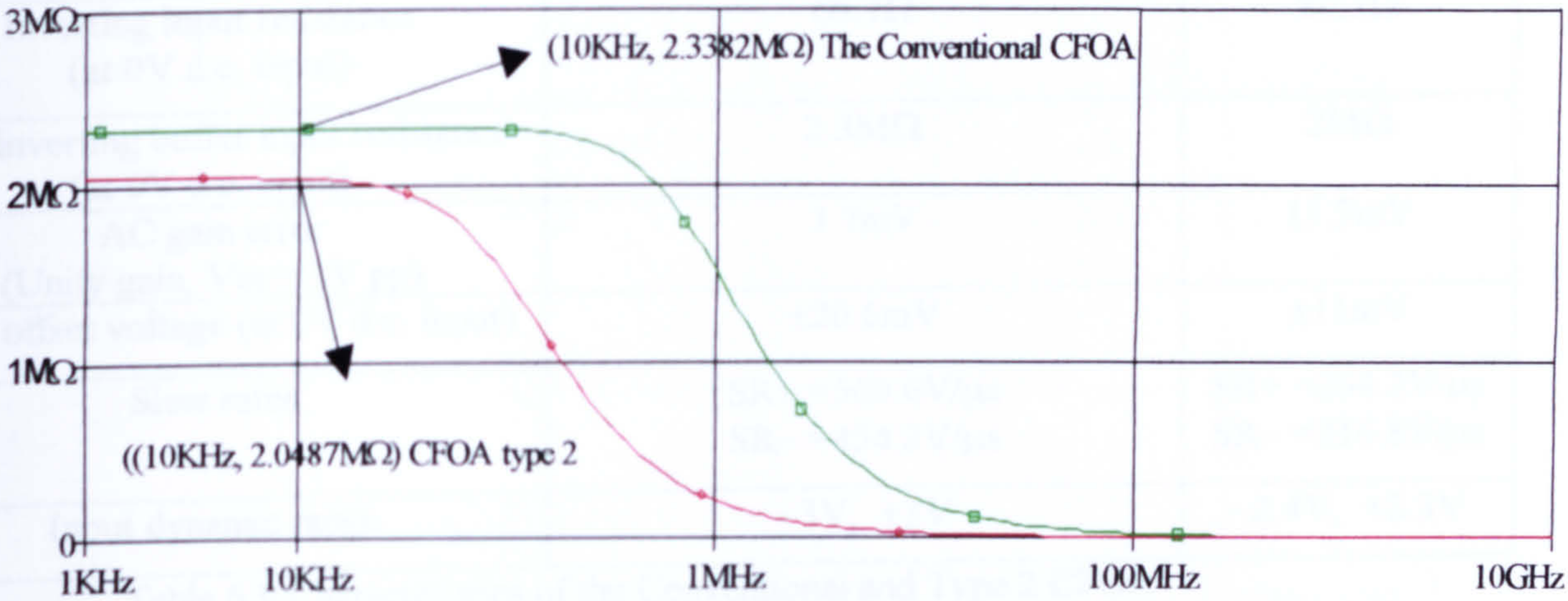


Figure 6.62 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

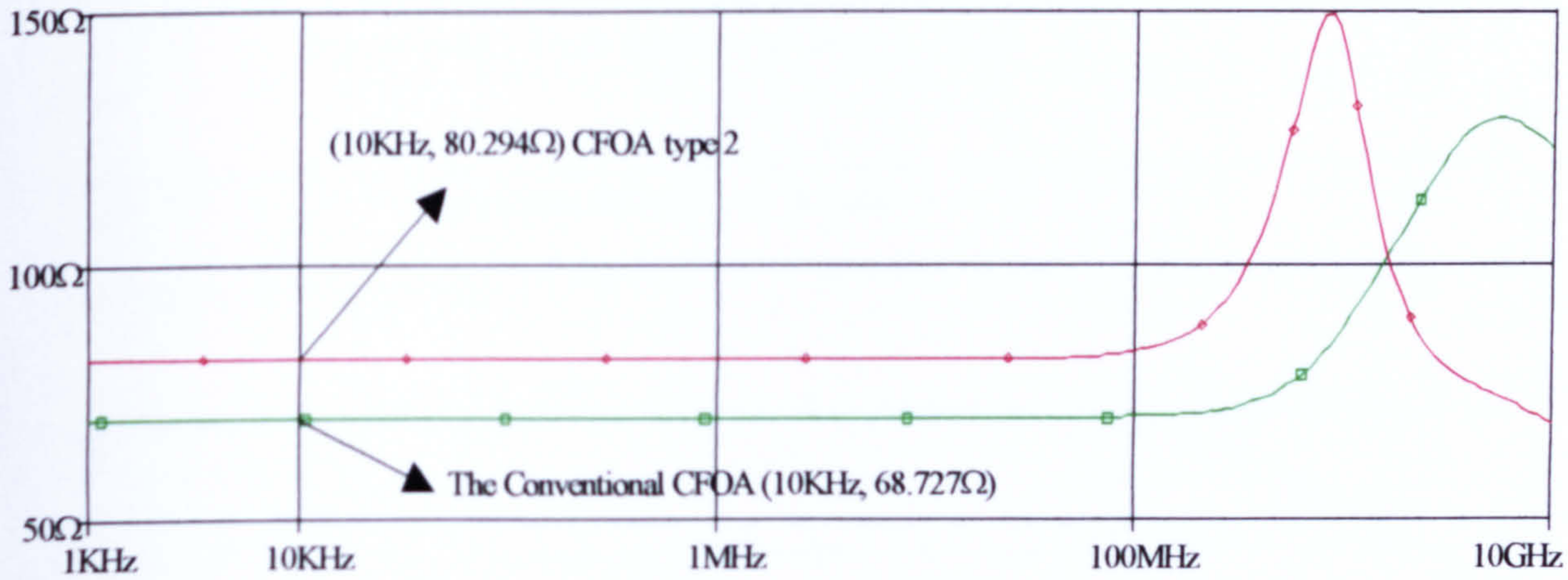


Figure 6.63 Input impedance (inverting)~Frequency comparisons

	CONVENTIONAL CFOA (5.1)	Type 2 CFOA (Fig 6.57)
CMRR	51.4dB	91dB
Bandwidth	55.7MHz	57.2MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	80.3Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	2MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	13.7mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±11mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =264.2V/μs SR– =216.8V/μs
Input dynamic range	–3V, +3V	–2.4V, +2.3V

Table 6.9 Characteristics of the Conventional and Type 2 CFOA

Discussion:

CFOA Type 2 show a better performance compared to CFOA half-circuit E: this is mainly to the biasing scheme that is used.

(6.4.3) Type 3 CFOA performance

This resembles Type 1, type 2 expect for current biasing scheme.

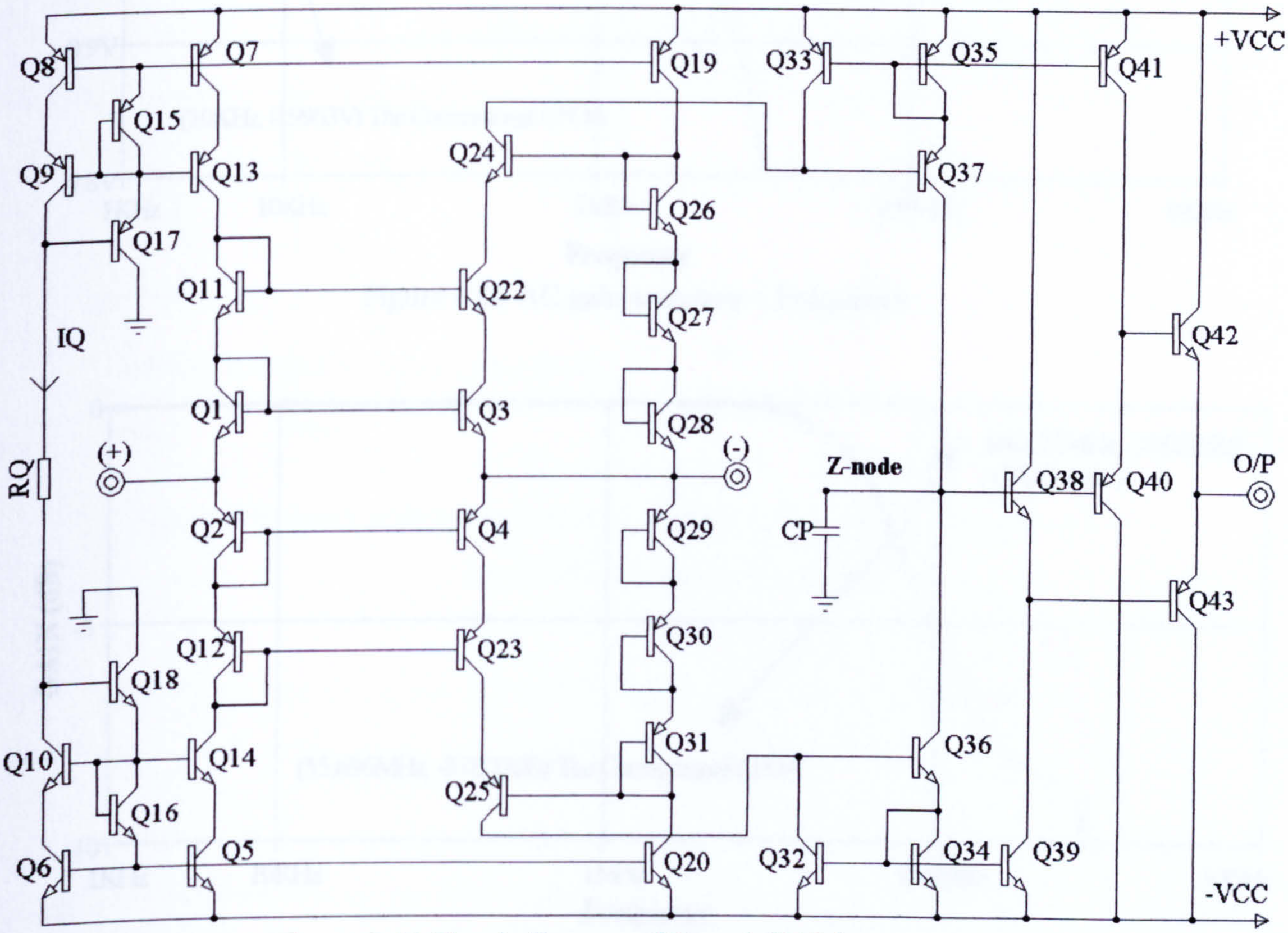


Figure 6.64 Circuit diagram of Type 3 CFOA

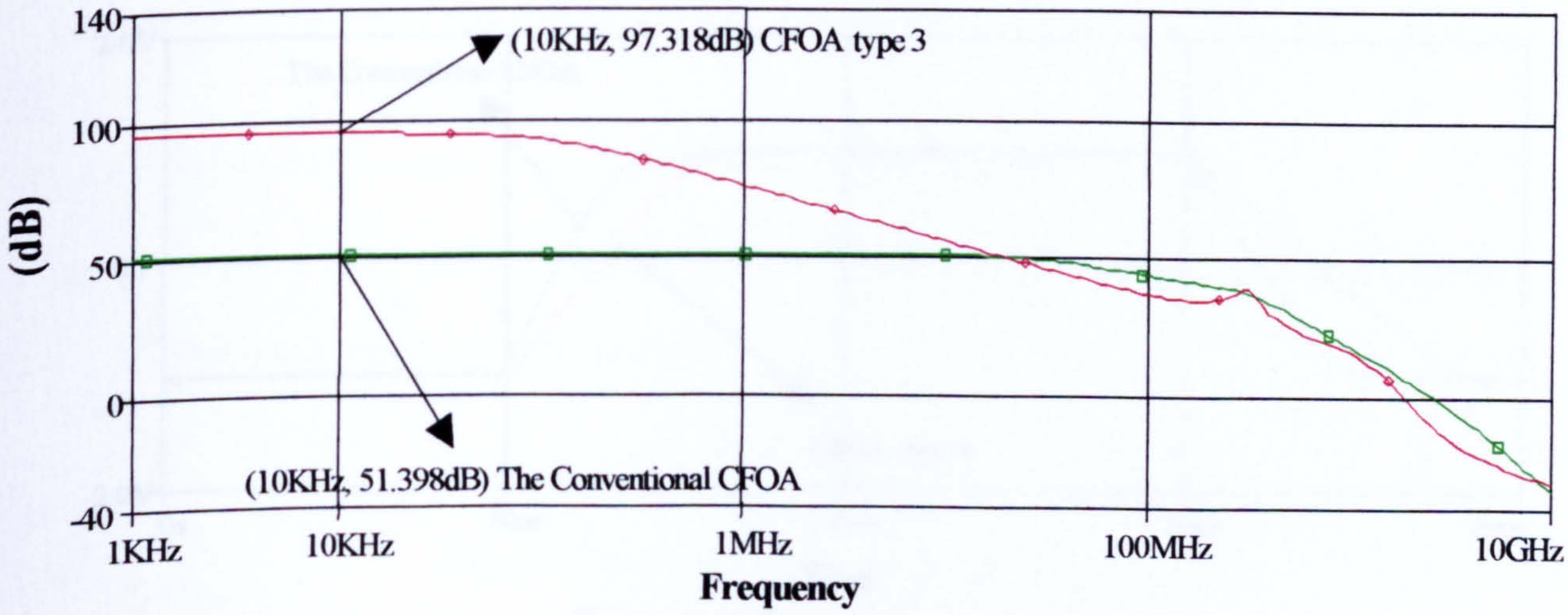


Figure 6.65 CMRR~Frequency

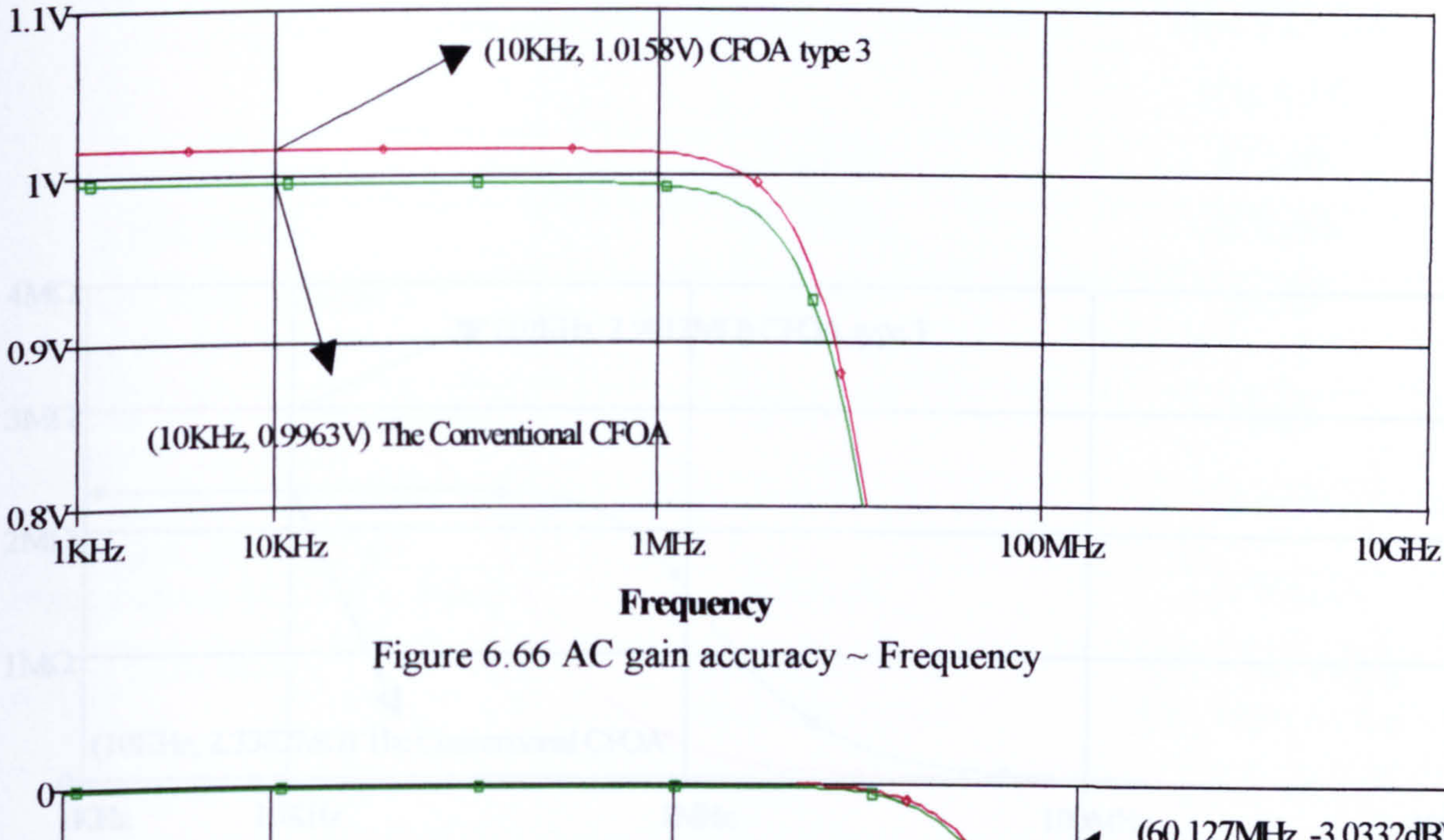


Figure 6.66 AC gain accuracy ~ Frequency

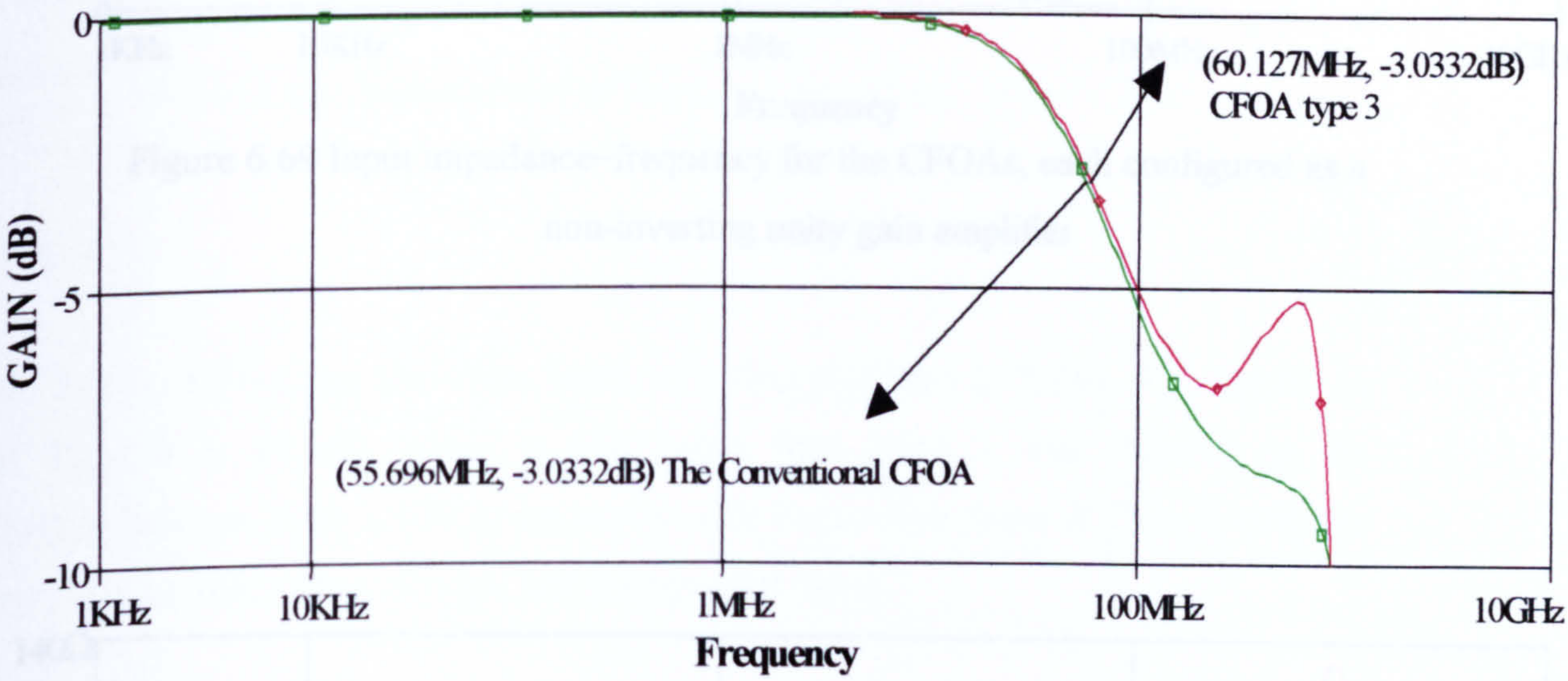


Figure 6.67 Frequency responses for unity closed-loop gain

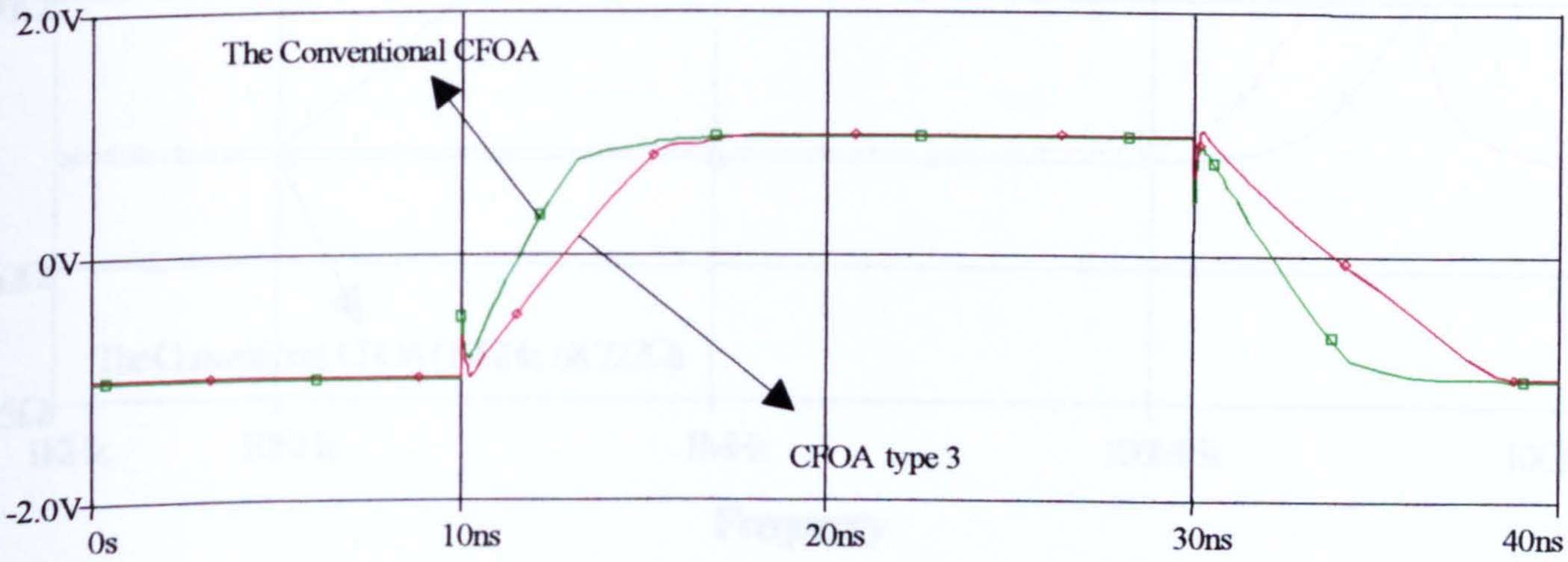


Figure 6.68 Transient response

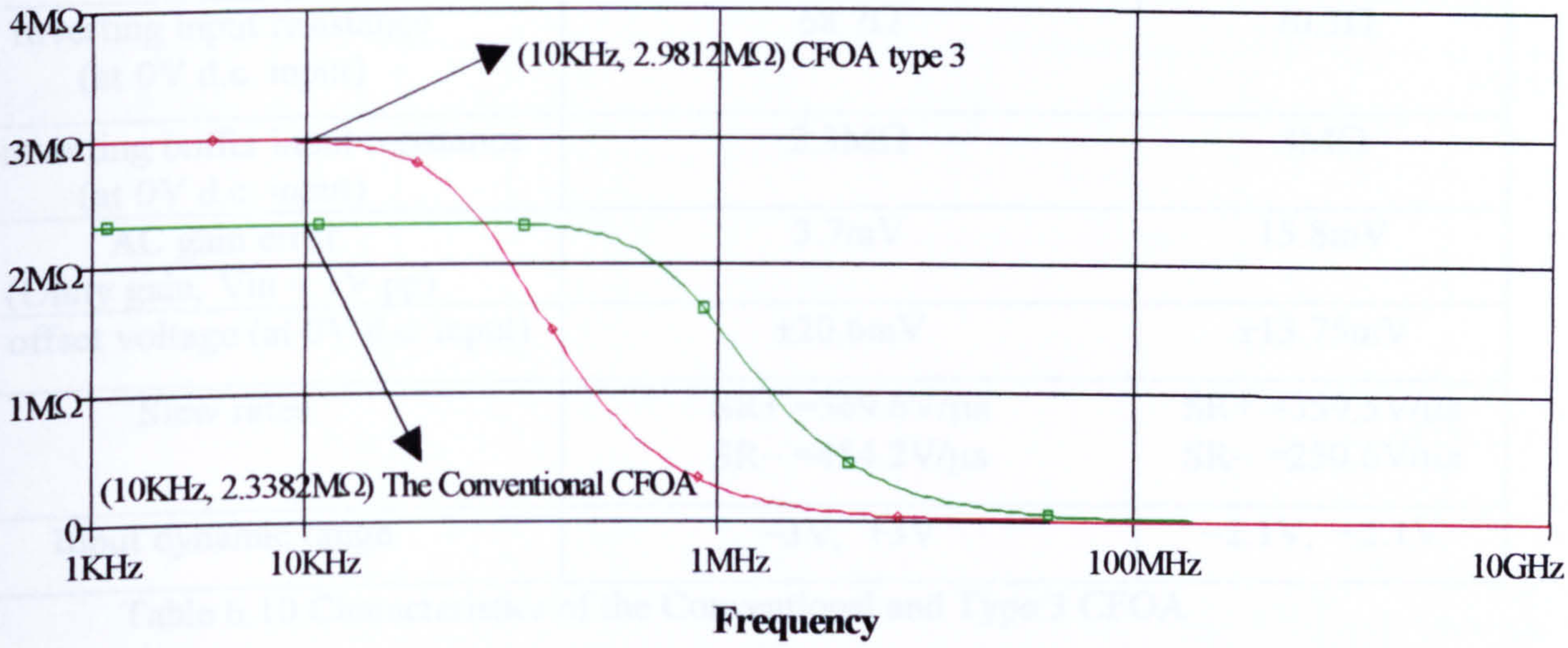


Figure 6.69 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

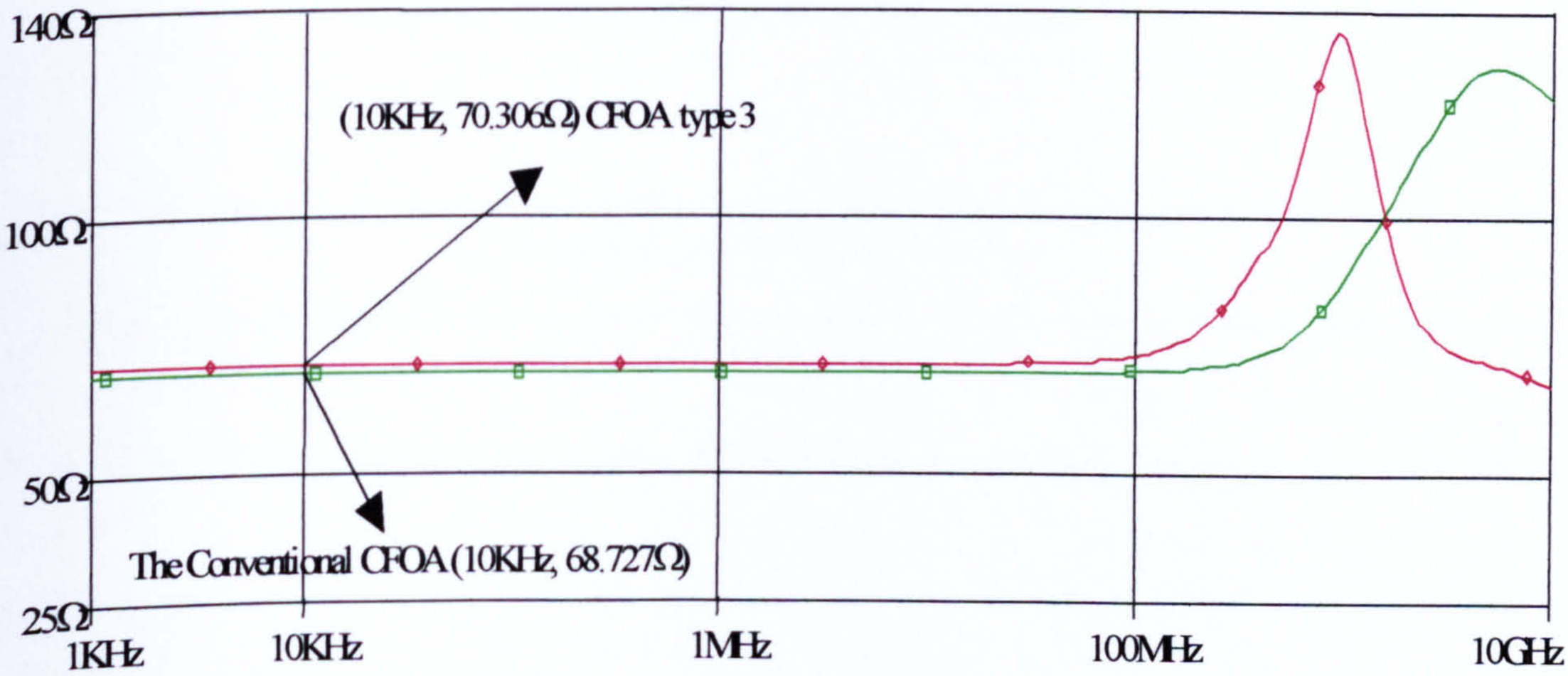


Figure 6.70 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	Type 3 CFOA (Fig 6.64)
CMRR	51.4dB	97.3dB
Bandwidth	55.7MHz	60.1MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	70.3Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	15.8mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±13.75mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =359.5V/μs SR– =250.6V/μs
Input dynamic range	–3V, +3V	–2.1V, +2.1V

Table 6.10 Characteristics of the Conventional and Type 3 CFOA

Discussion:

The Type 3 CFOA has the wider bandwidth than the Type 2 CFOA. The CMRR in the Type 3 is 97.3dB, which is 6dB better than Type 2. The majority of the characteristics of Type 3 CFOA are significantly better than those of Type 2, with the exception of input offset-voltage, and the dynamic range.

(6.4.4) Type 4 CFOA performance

Type 4 CFOA; shown in Fig.6.71 is a variation of G (I).

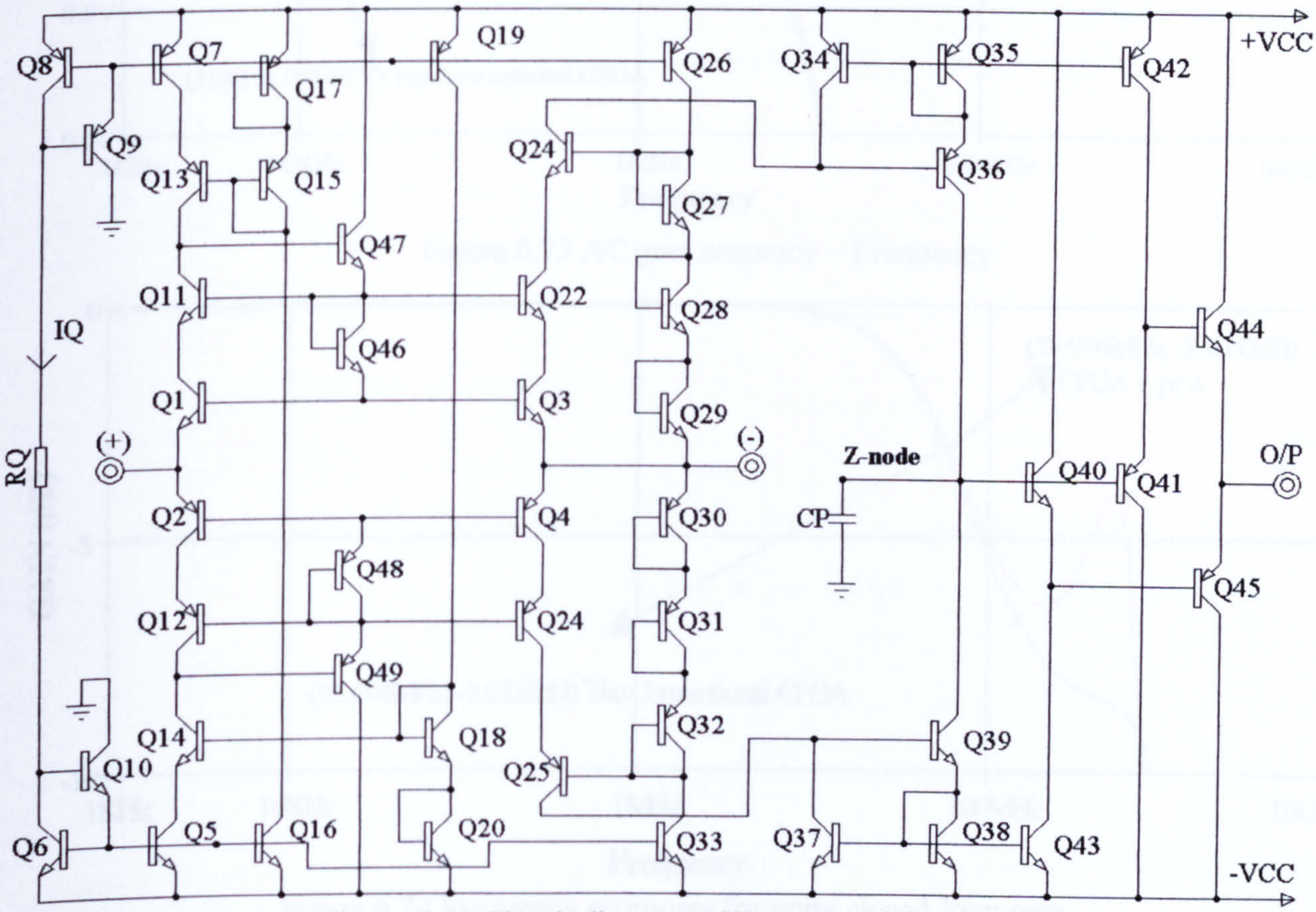


Figure 6.71 Circuit diagram of Type 4 CFOA

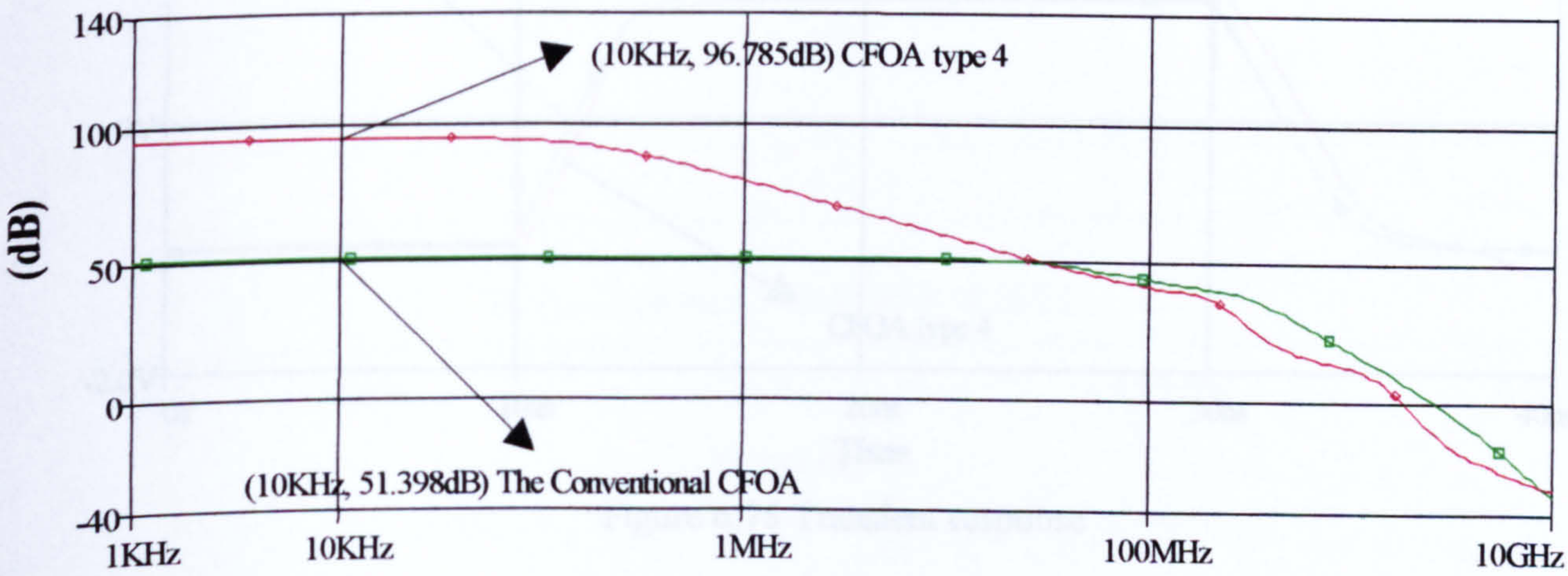


Figure 6.72 CMRR~Frequency

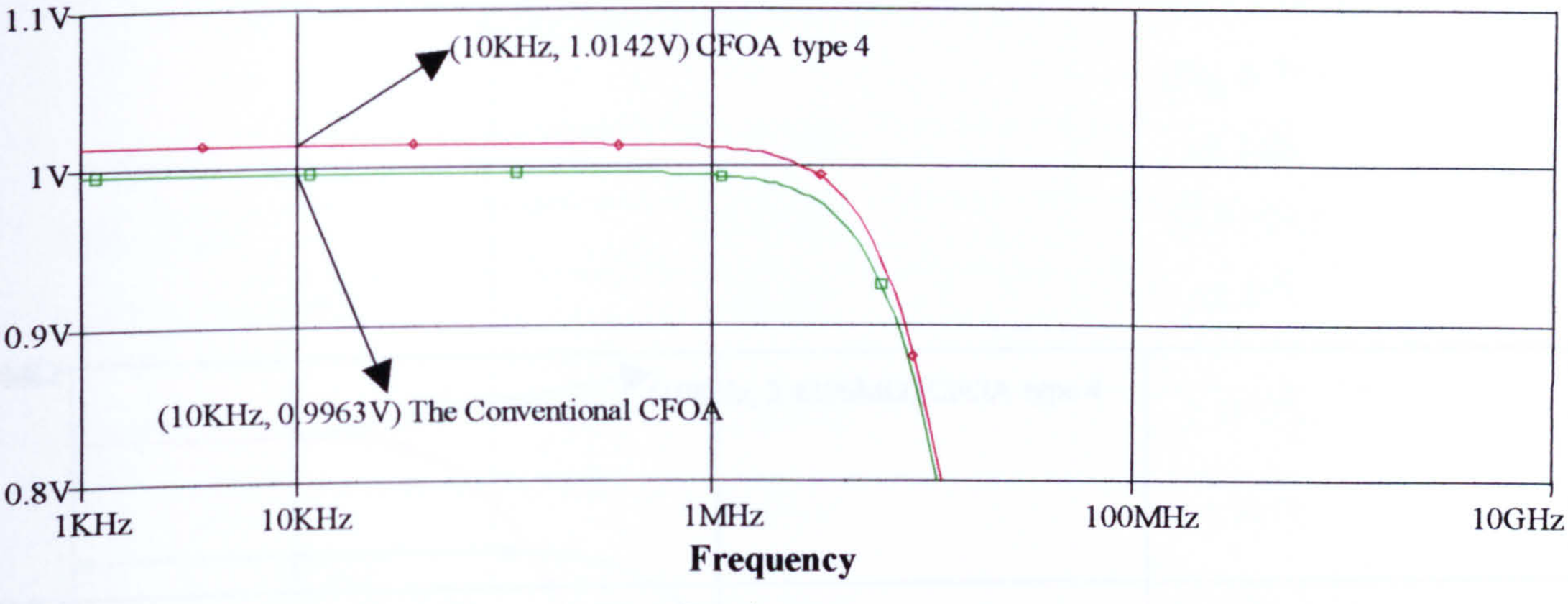


Figure 6.73 AC gain accuracy ~ Frequency

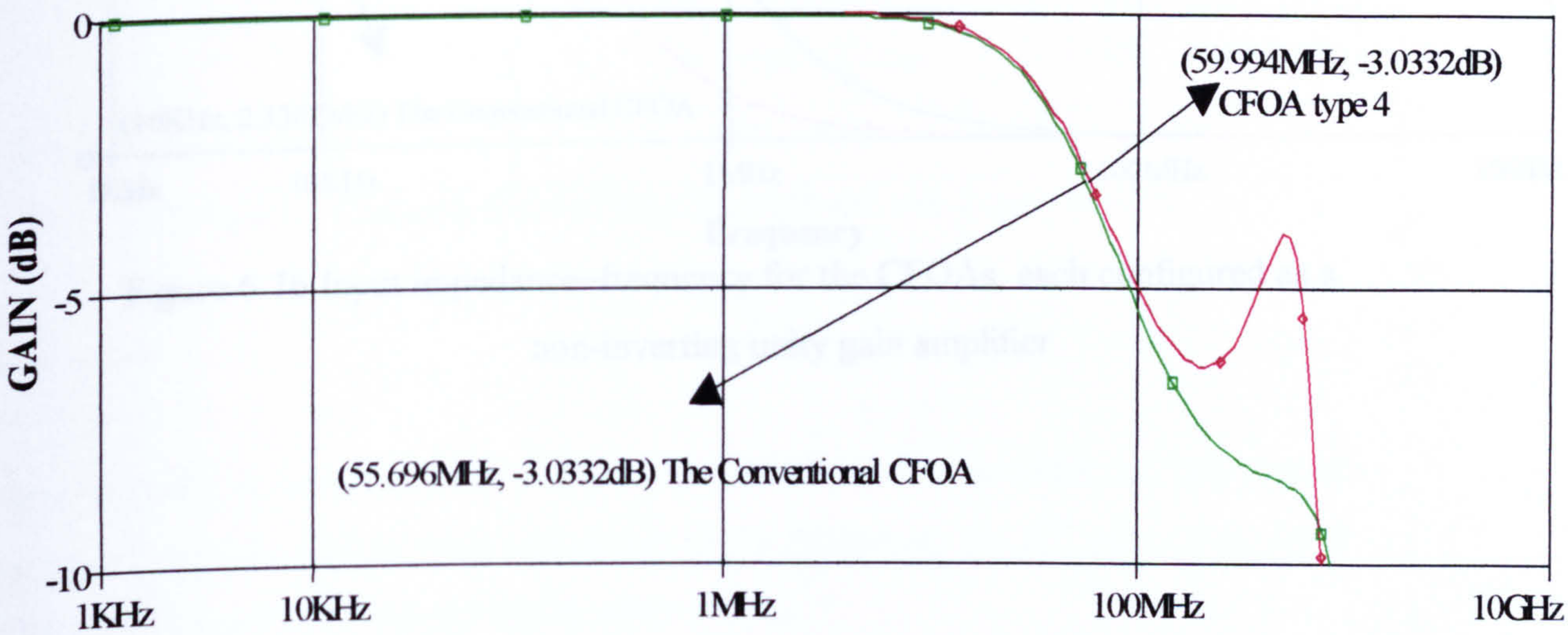


Figure 6.74 Frequency responses for unity closed-loop gain

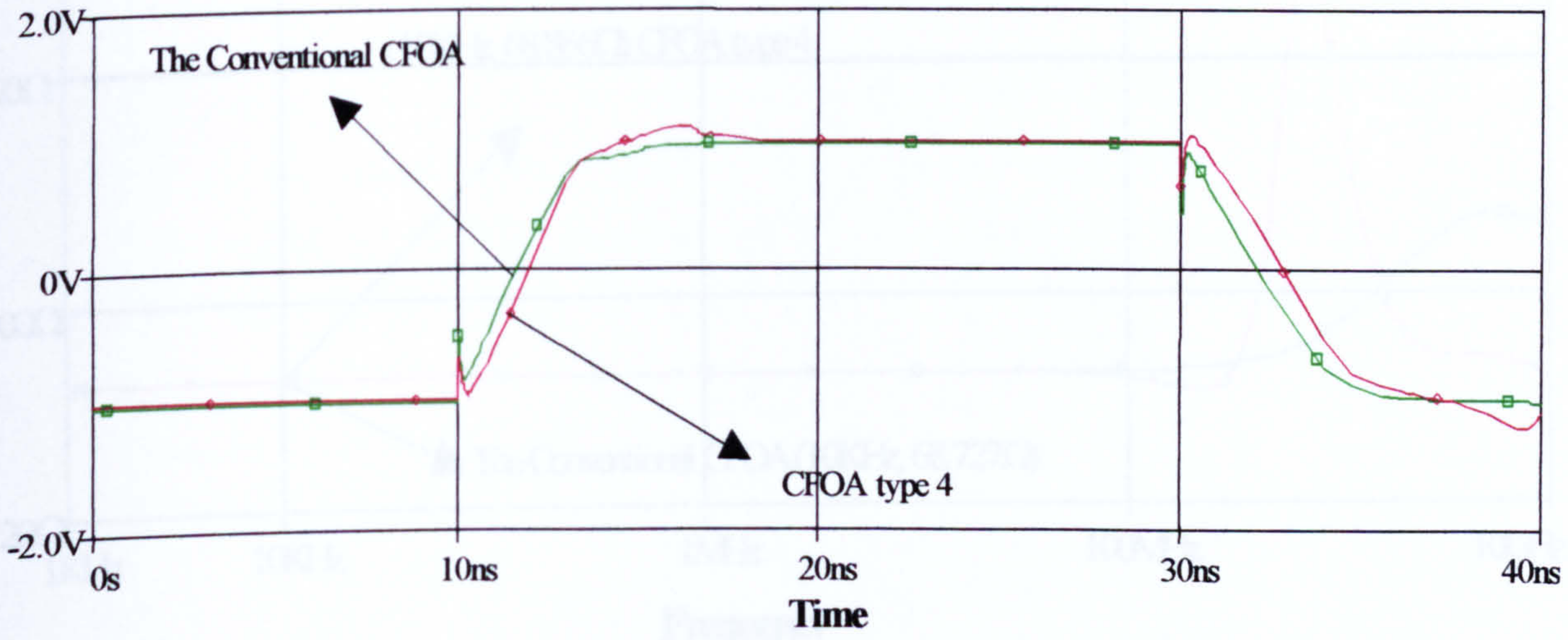


Figure 6.75 Transient response

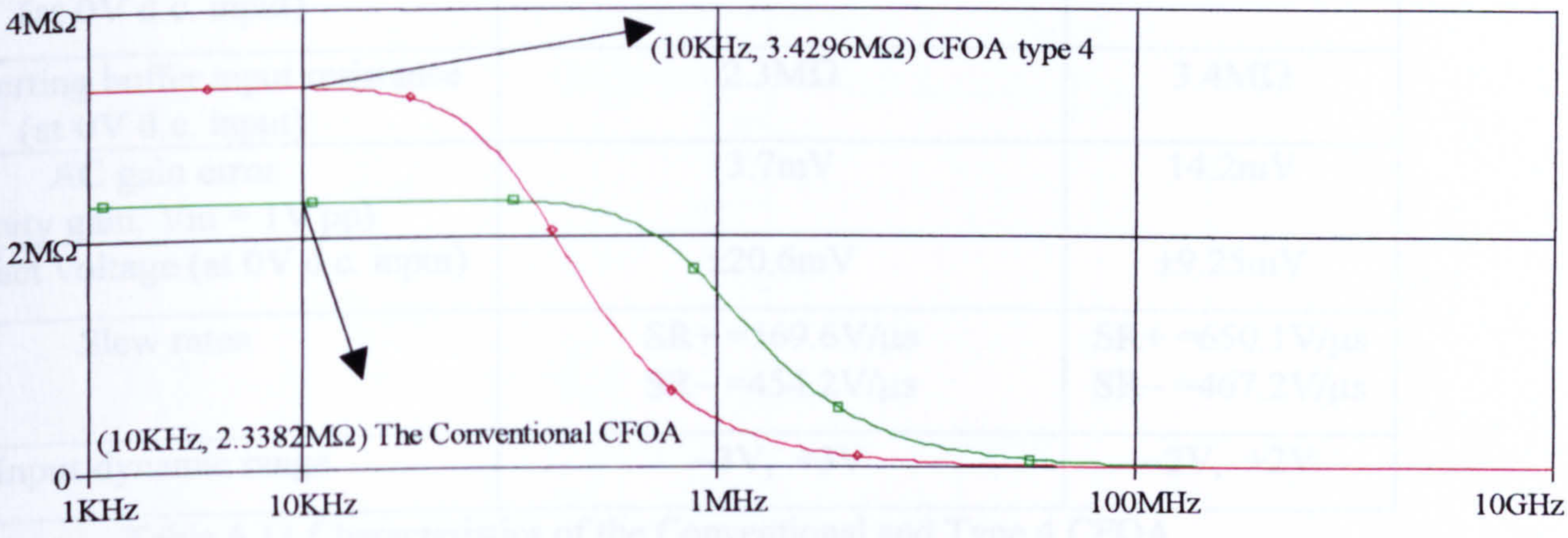


Figure 6.76 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

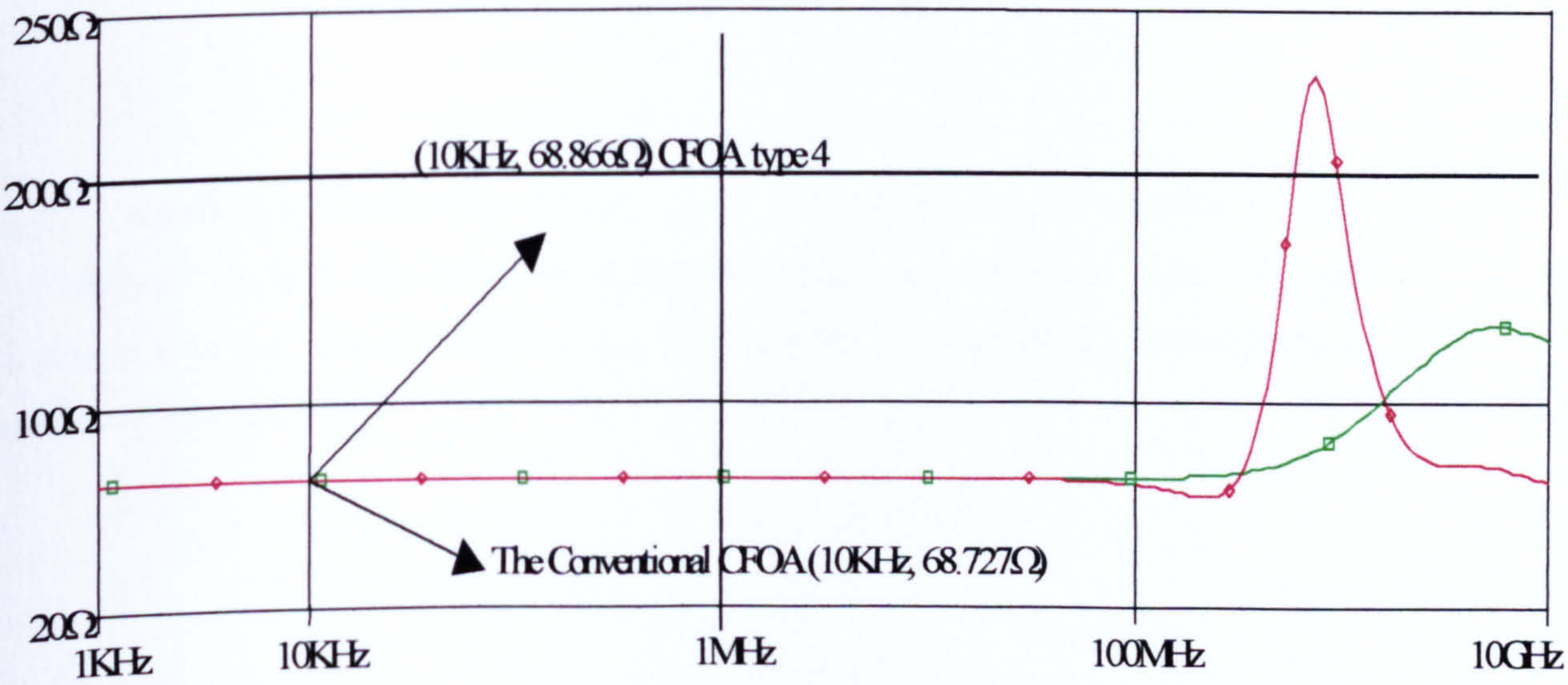


Figure 6.77 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	Type 4 CFOA (Fig 6.71)
CMRR	51.4dB	96.7dB
Bandwidth	55.7MHz	59.9MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	68.8Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3.4MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	14.2mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±9.25mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =650.1V/μs SR– =467.2V/μs
Input dynamic range	–3V, +3V	–2V, +2V

Table 6.11 Characteristics of the Conventional and Type 4 CFOA

Discussion:

There is only a marginal improvement in CMRR and bandwidth of this circuit compared with the CFOA with half-circuit G (I). However, the AC gain error, input offset-voltage and slew rate are significantly worse.

(6.4.5) Type 5 CFOA performance

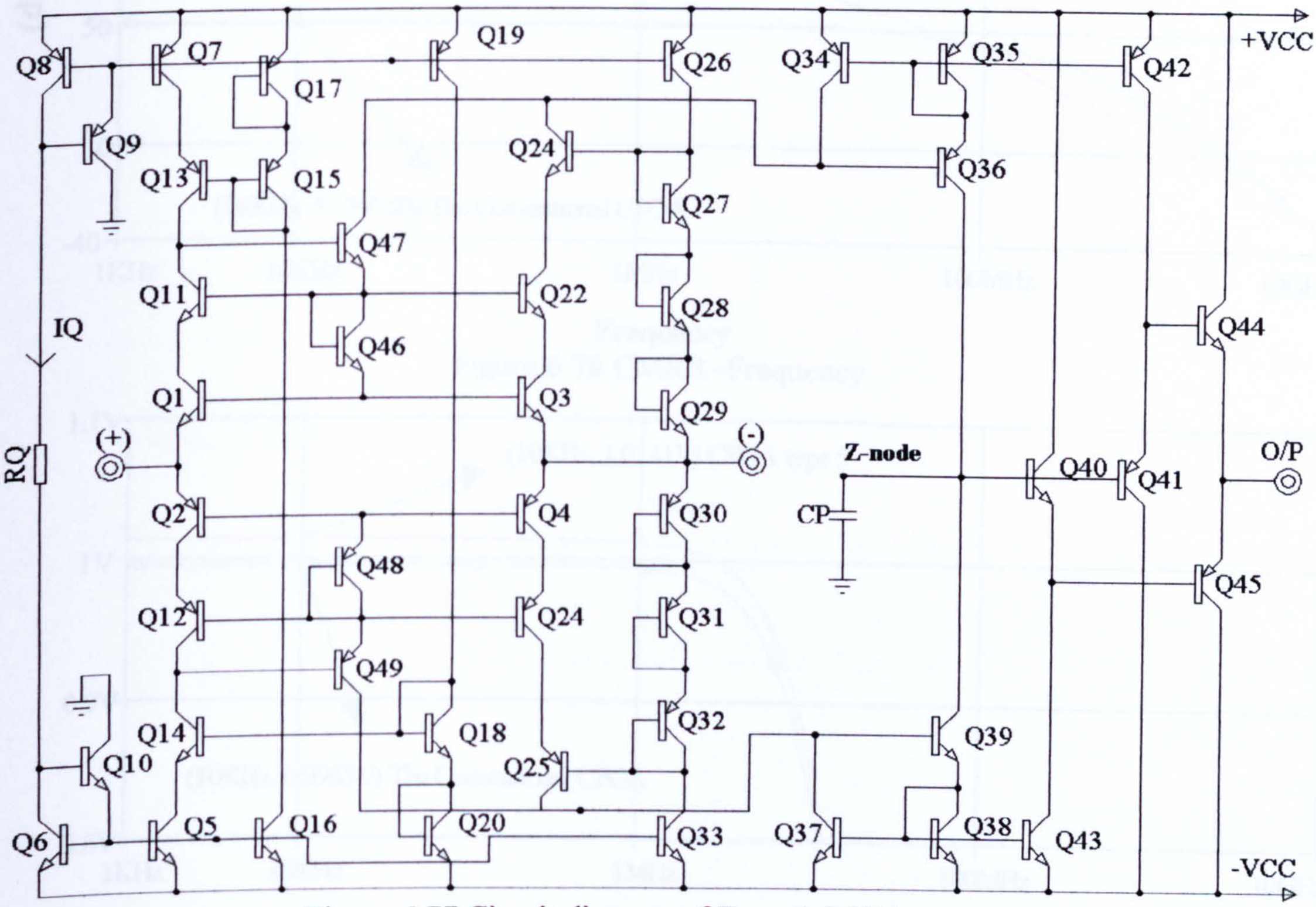


Figure 6.77 Circuit diagram of Type 5 CFOA

Fig.6.77 shows the circuit of the CFOA Type5. It is merely a small variation of Type 4. It differs from it in that collector of transistor Q_{47} is disconnected from $+V_{CC}$ and connected it to the base of transistor Q_{36}. Similarly the collector of Q_{49} is connected to the base of transistor Q_{39}.

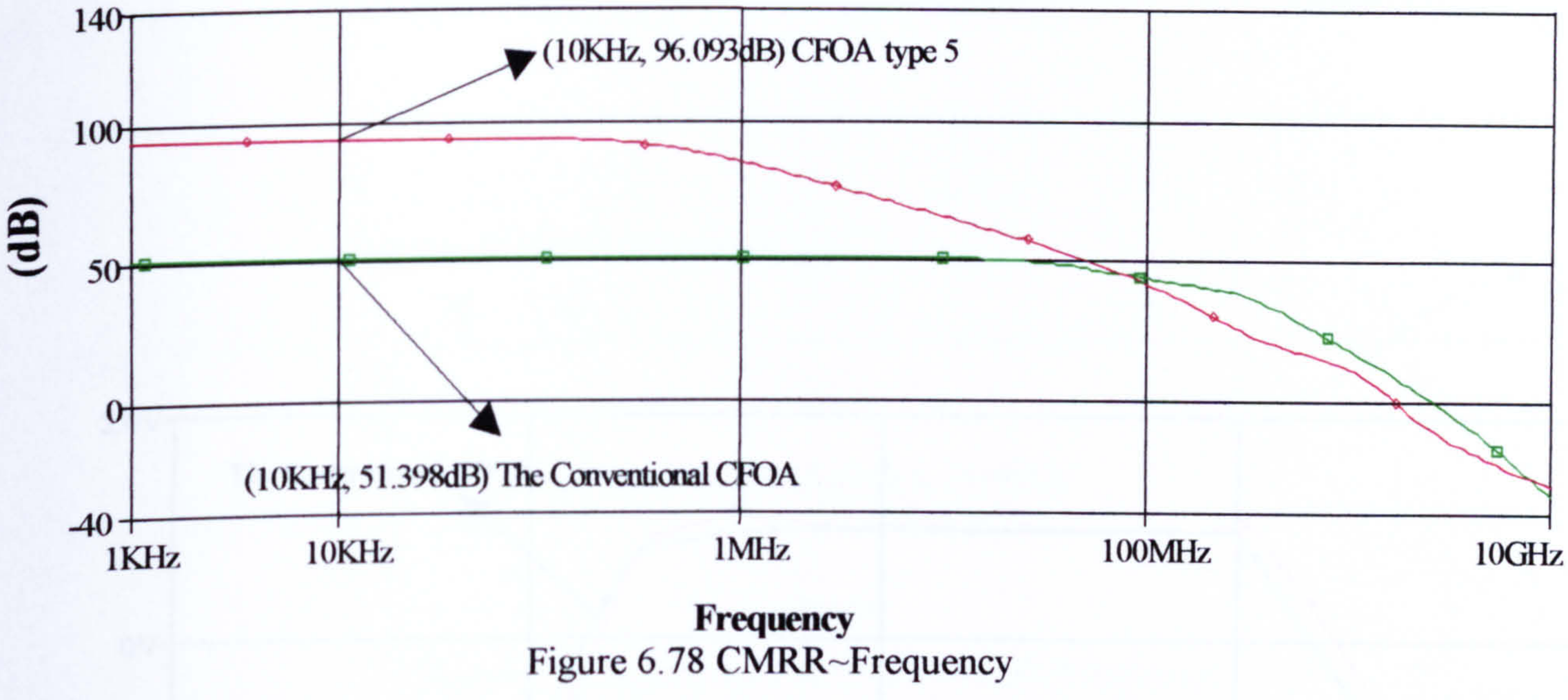


Figure 6.78 CMRR~Frequency

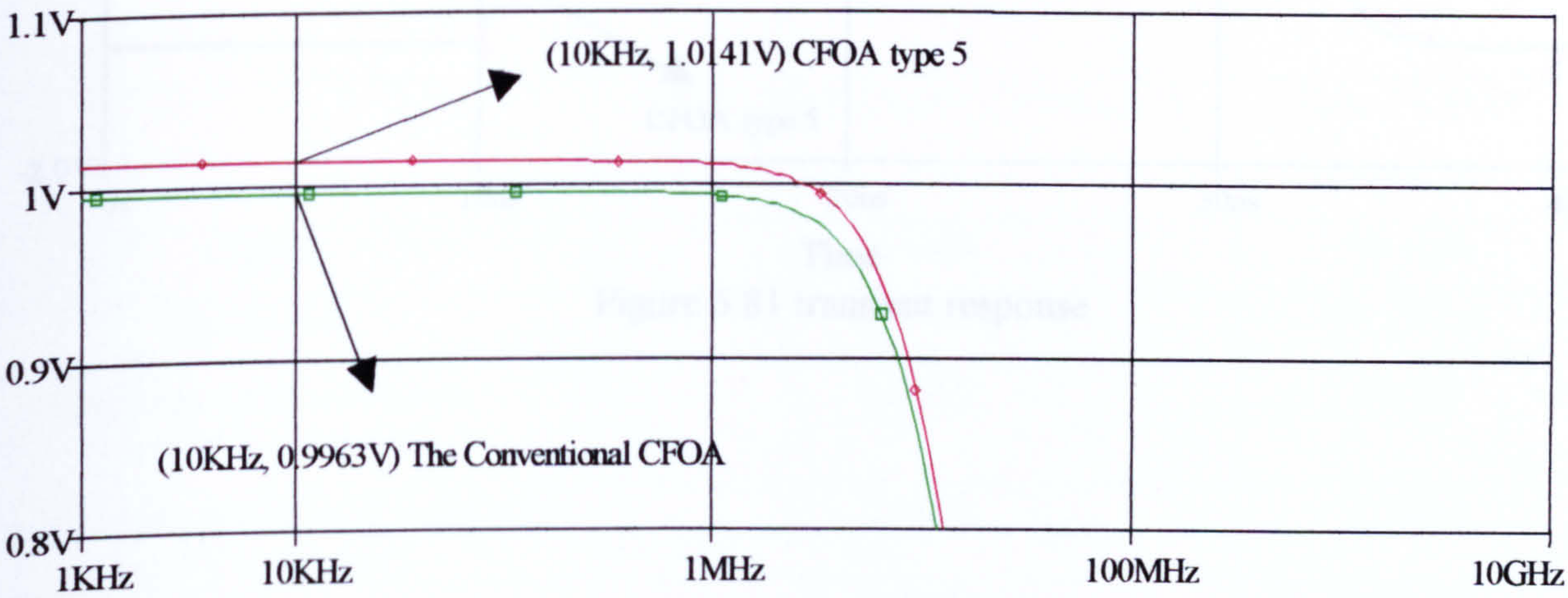


Figure 6.79 AC gain accuracy ~ Frequency

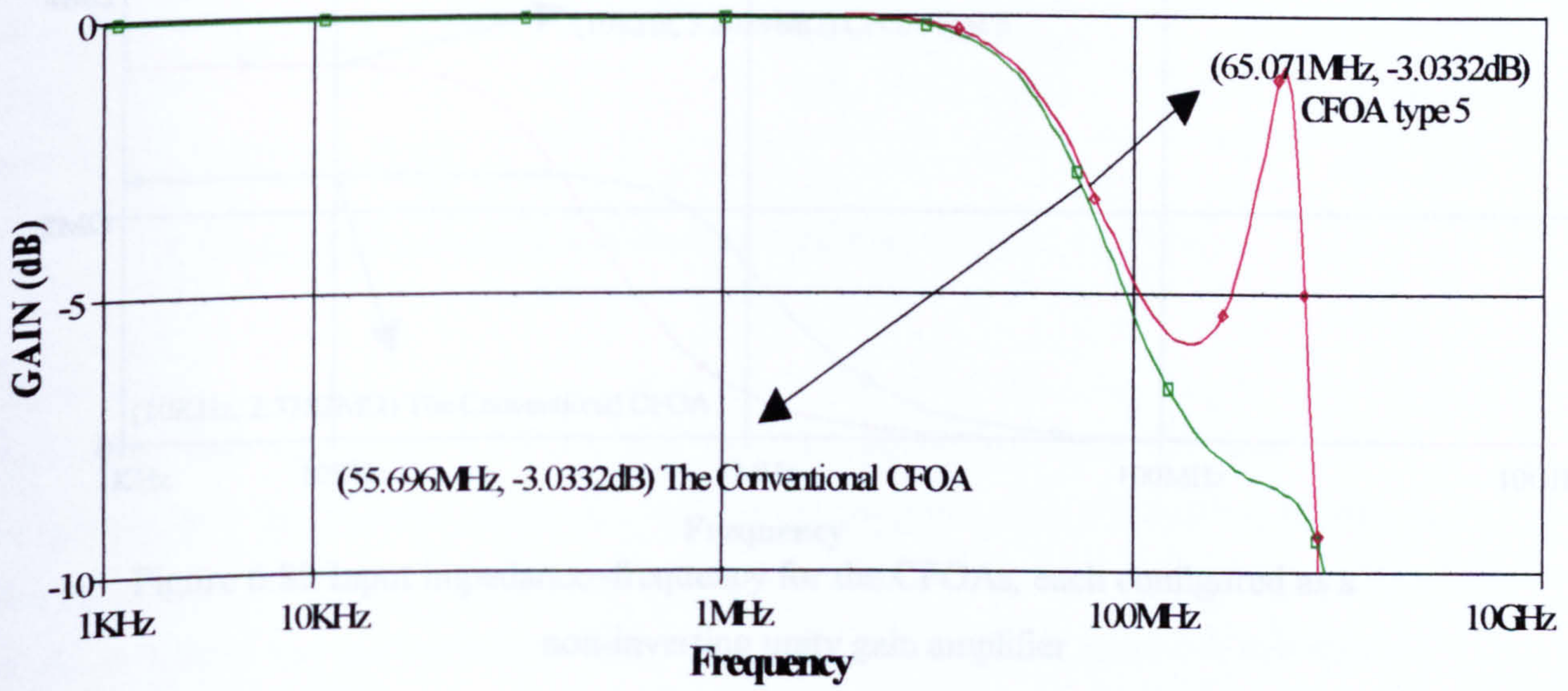


Figure 6.80 Frequency responses for unity closed-loop gain

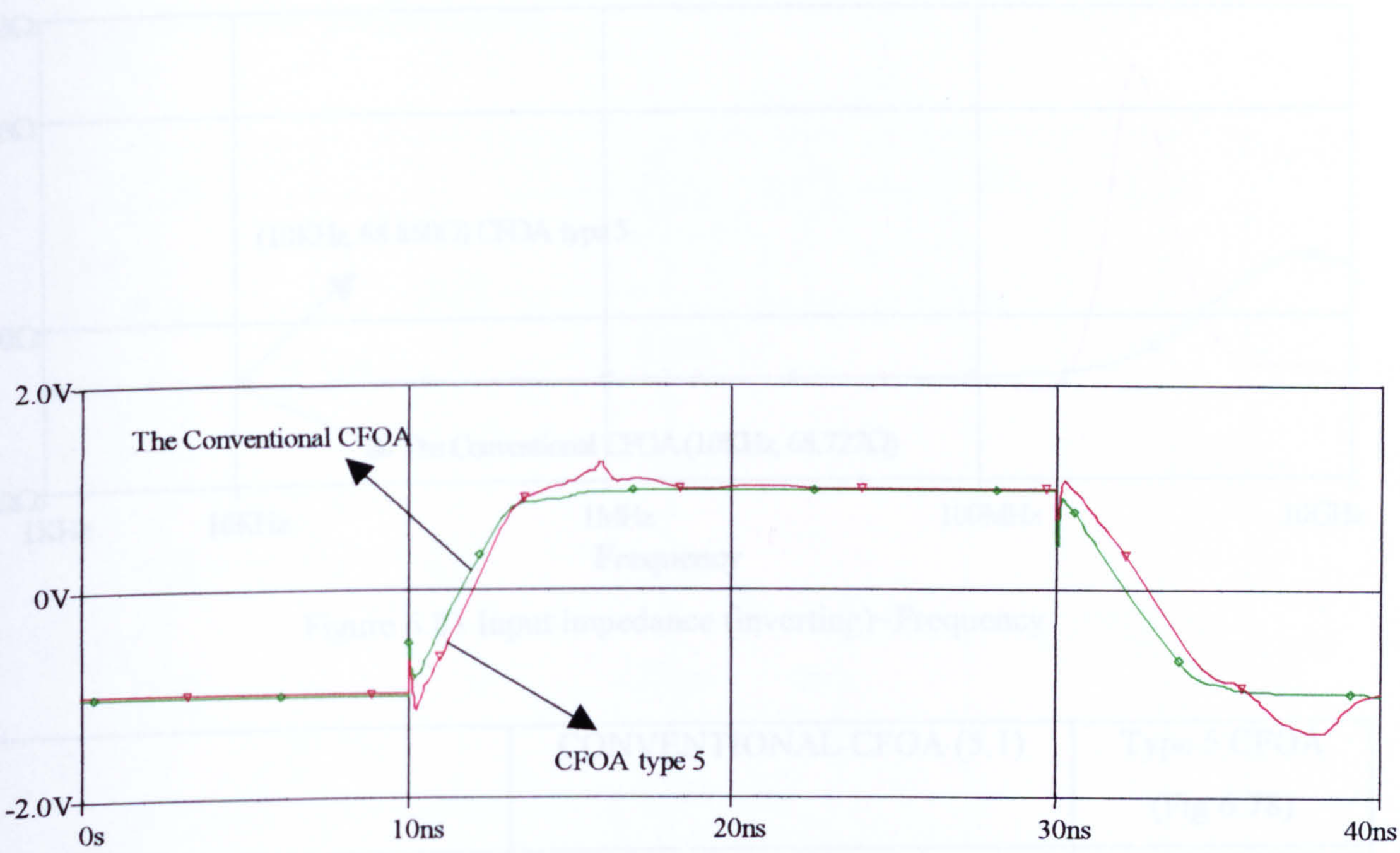


Figure 6.81 transient response

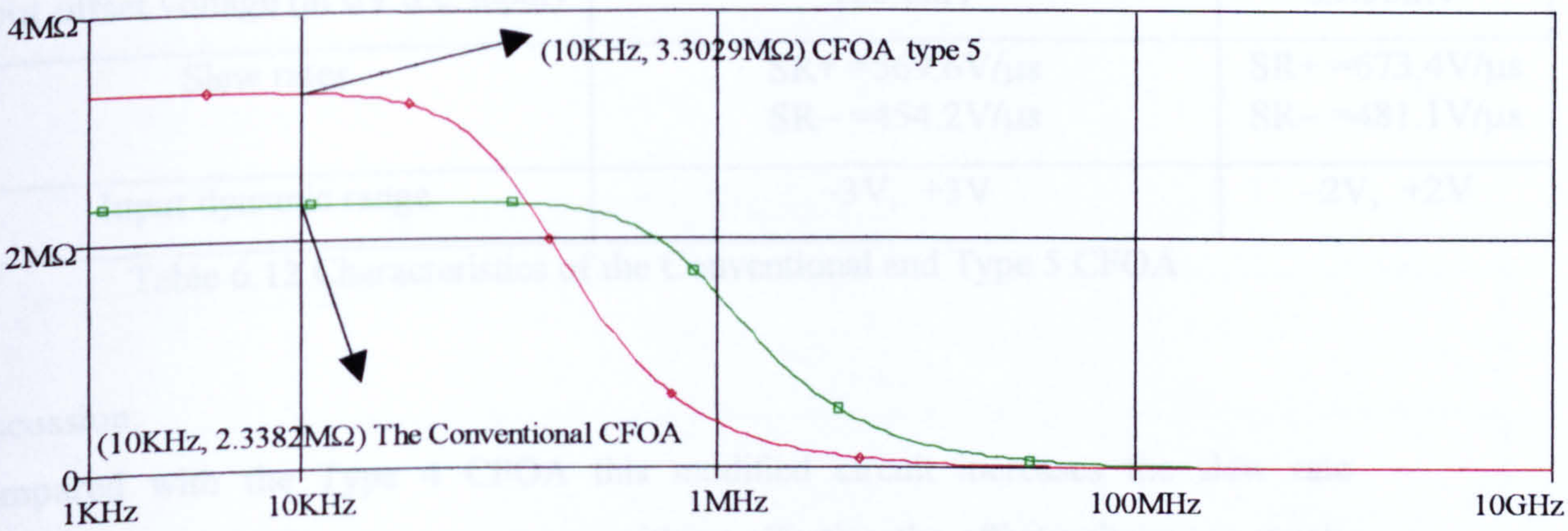


Figure 6.82 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

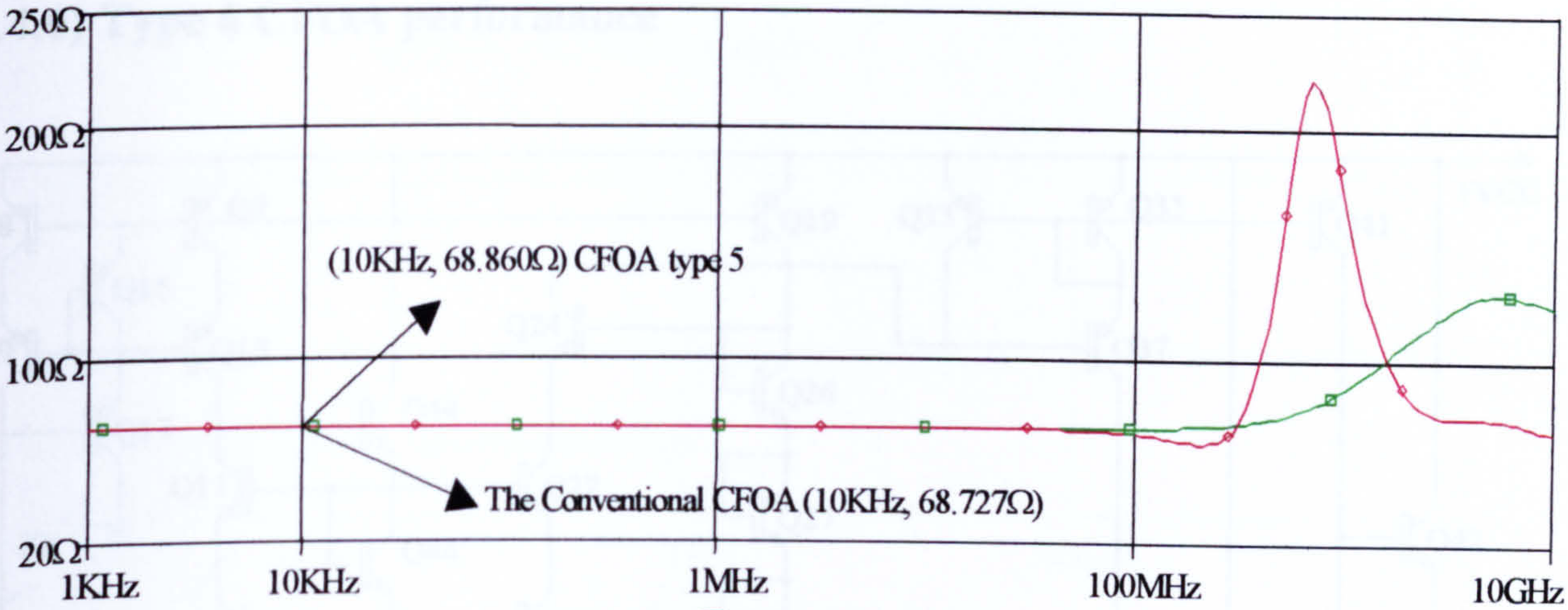


Figure 6.83 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	Type 5 CFOA (Fig 6.78)
CMRR	51.4dB	96.1dB
Bandwidth	55.7MHz	65.1MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	68.8Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3.3MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	14.1mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±9.35mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =673.4V/μs SR– =481.1V/μs
Input dynamic range	–3V, +3V	–2V, +2V

Table 6.12 Characteristics of the Conventional and Type 5 CFOA

Discussion:

Compared with the Type 4 CFOA this modified circuit increases the slew rate marginally, and the frequency response, without affecting the offset voltage too much. The reason for this is that the transient collector current of transistor Q_{47} is now used to drive harder the current-mirror Q_{34}, Q_{35}, Q_{36}. Similarly, the transient collector current of transistor Q_{49} is now used to drive harder the current-mirror Q_{37}, Q_{38}, Q_{39}.

(6.4.6) Type 6 CFOA performance

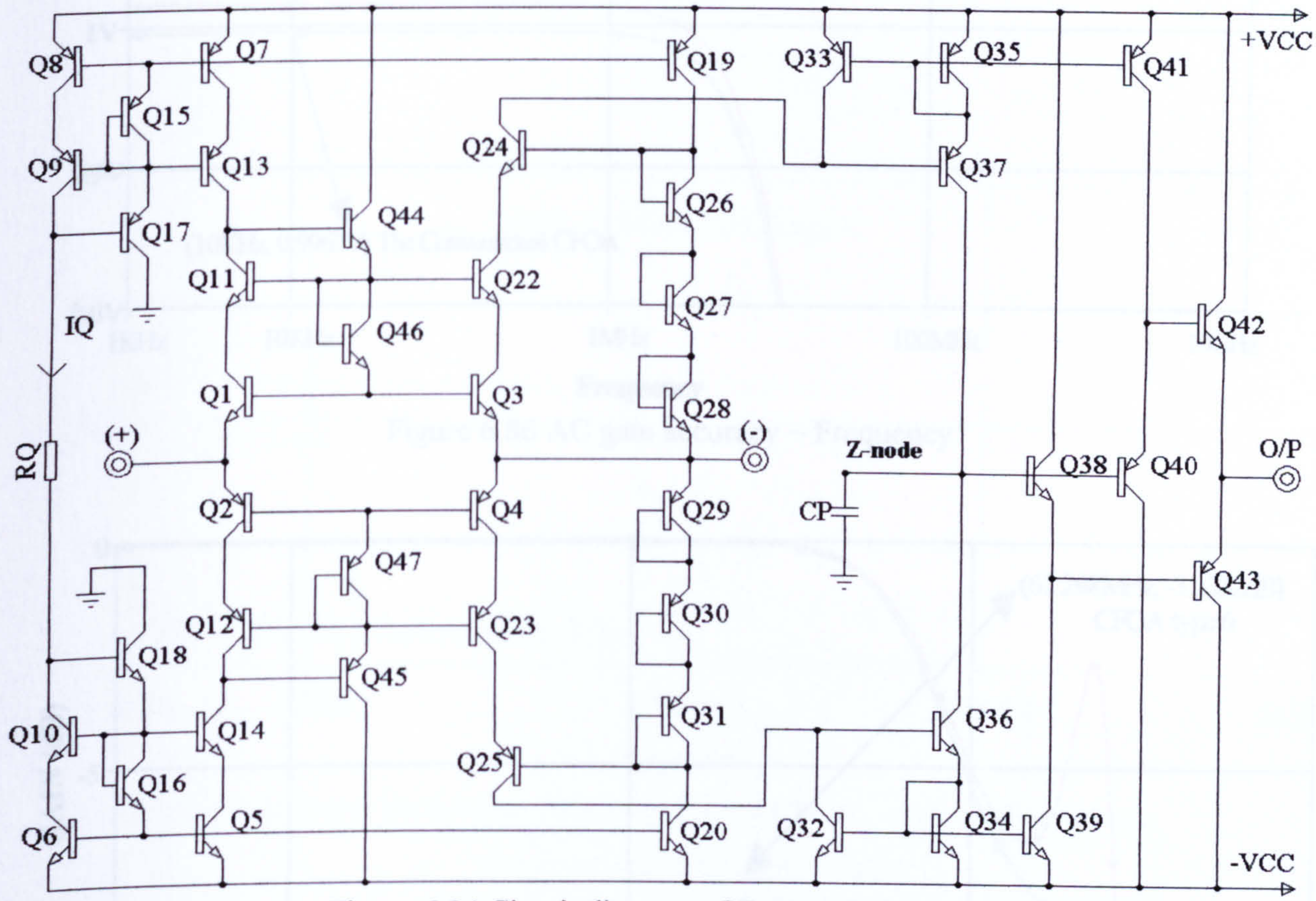


Figure 6.84 Circuit diagram of Type 6 CFOA

This scheme is a variation of a CFOA with G (II) input stage and biasing. The only difference in the provision of reverse as well as forward bootstrapping.

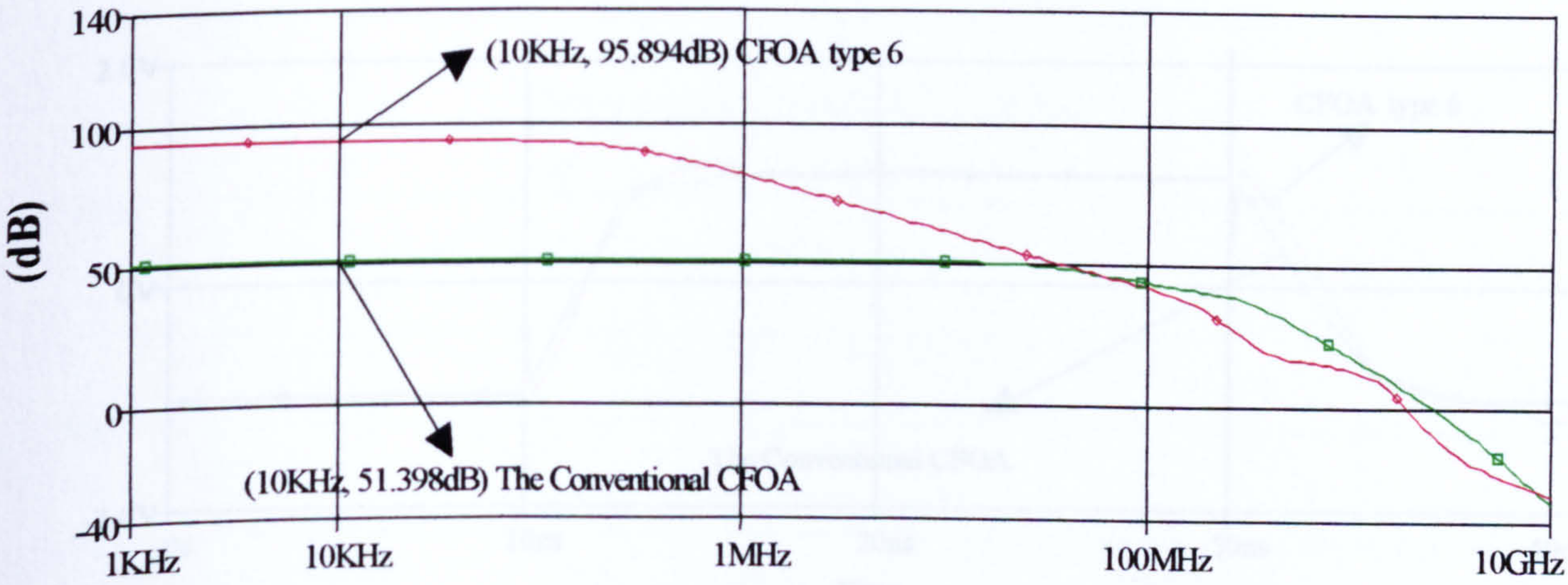


Figure 6.85 CMRR~Frequency

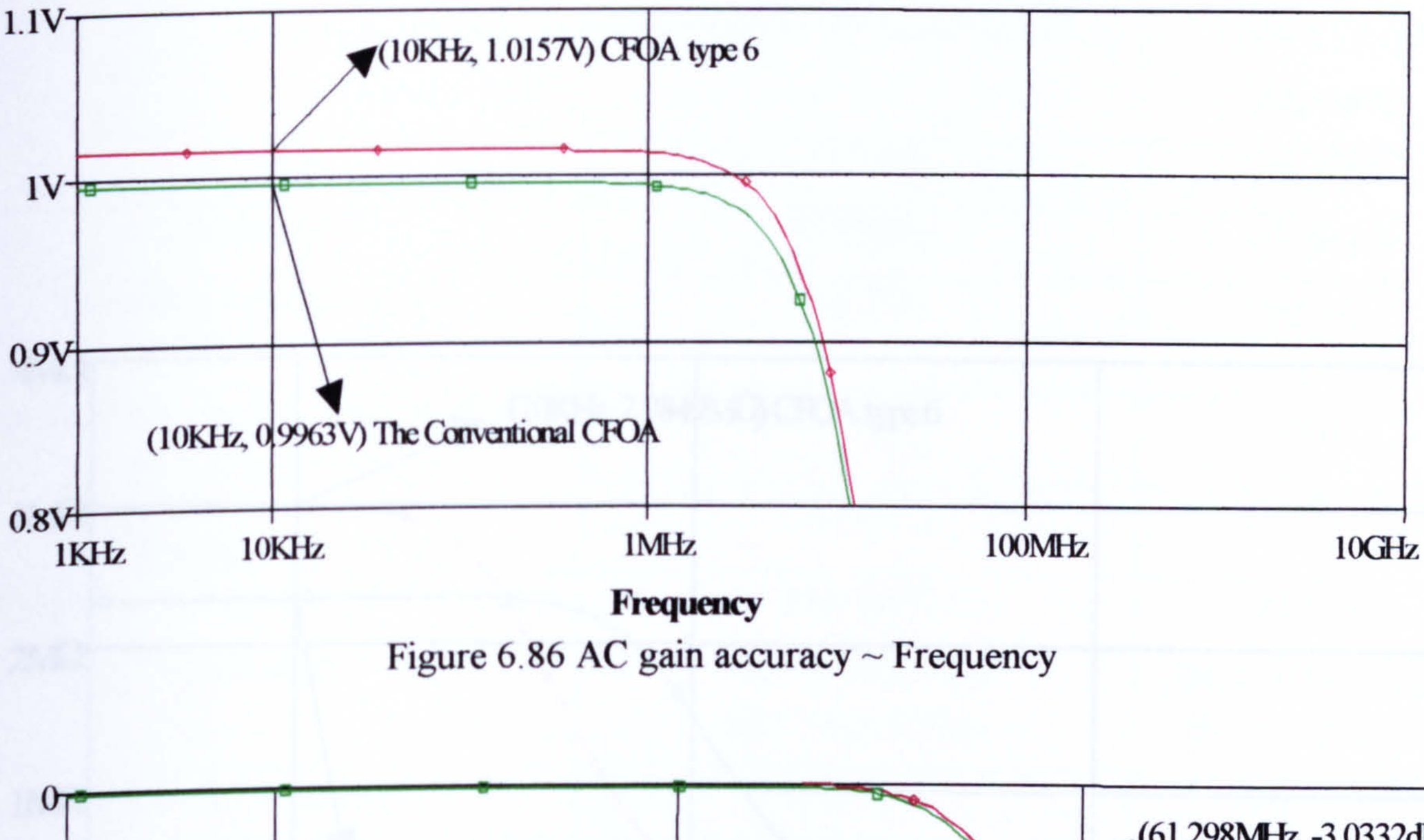


Figure 6.86 AC gain accuracy ~ Frequency

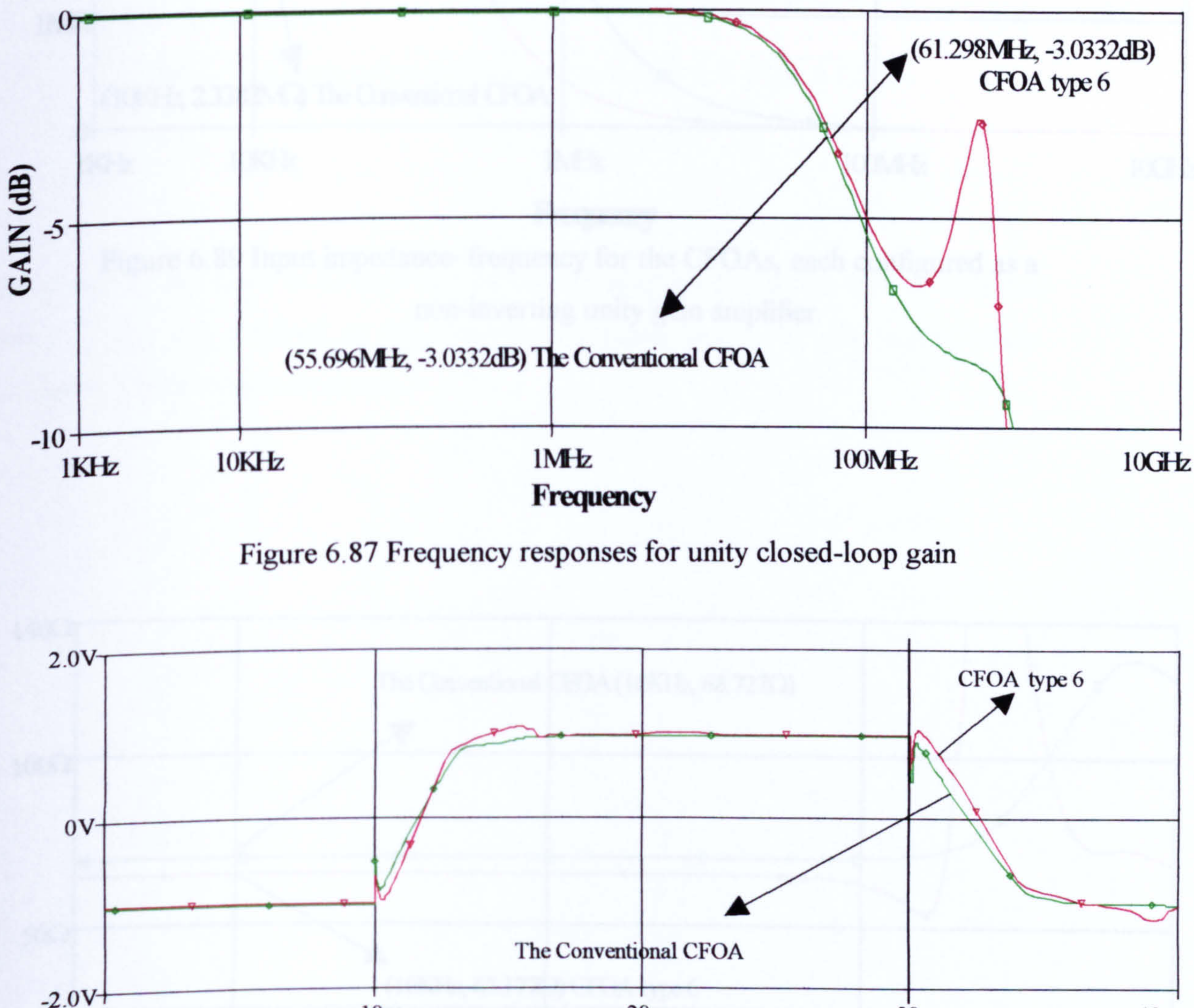


Figure 6.87 Frequency responses for unity closed-loop gain

Figure 6.88 Transient response

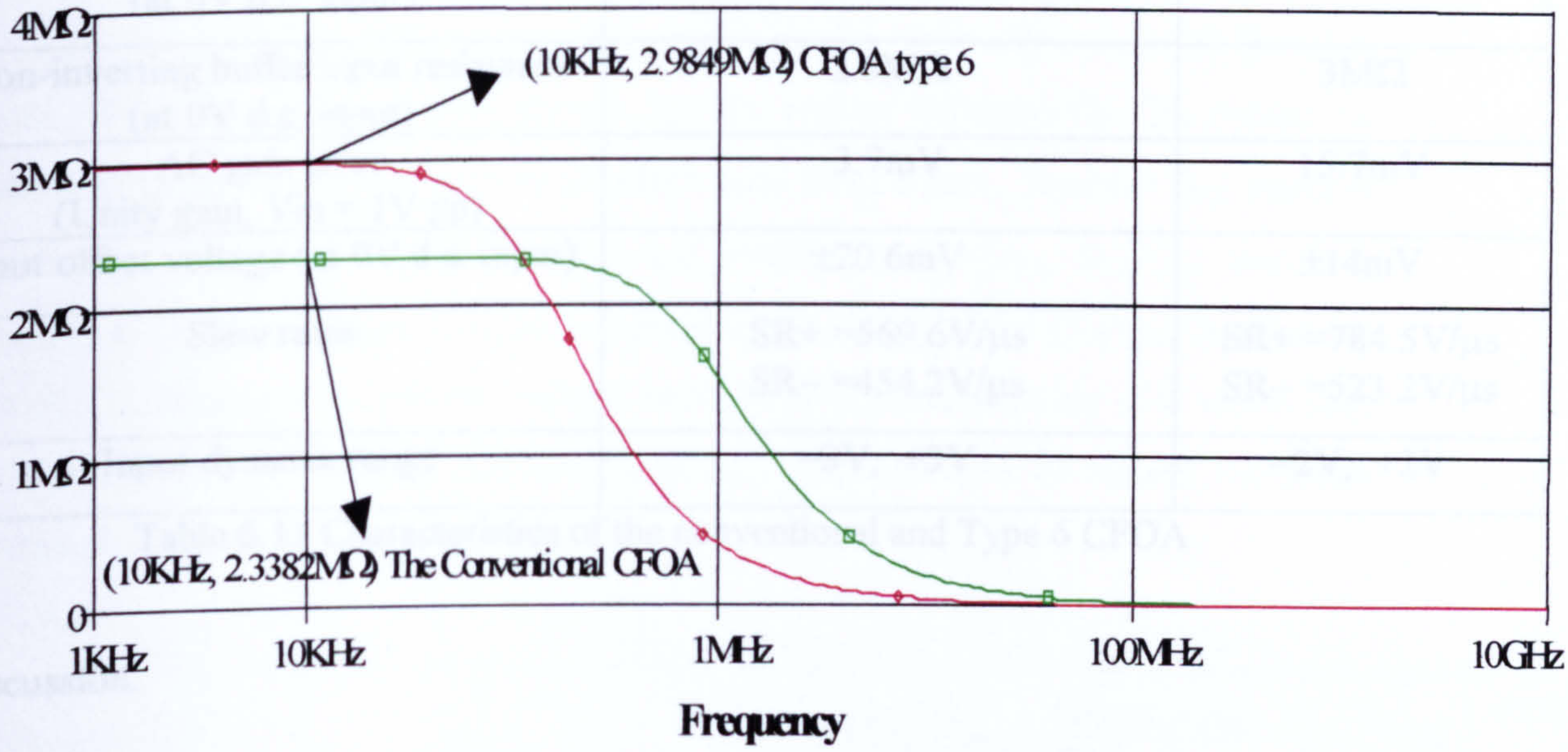


Figure 6.89 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

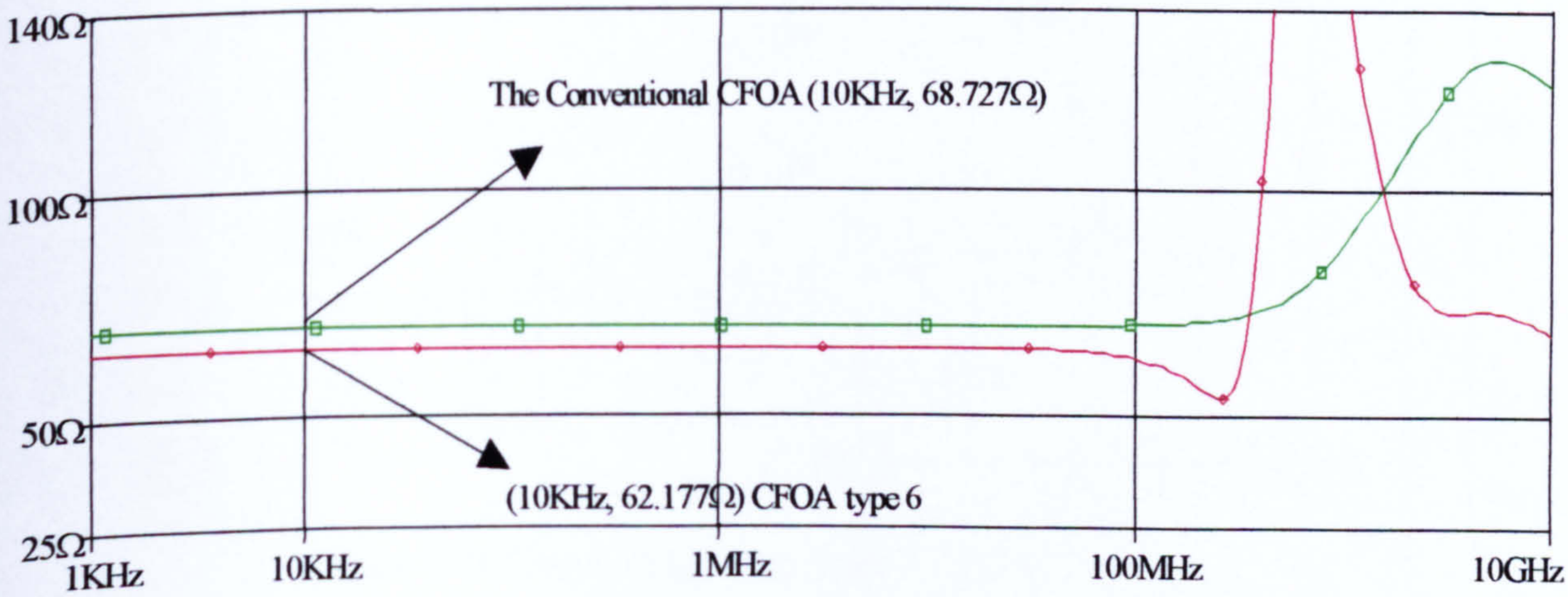


Figure 6.90 Input impedance (inverting)~Frequency

	CONVENTIONAL CFOA (5.1)	Type 6 CFOA (Fig.6.84)
CMRR	51.4dB	95.9dB
Bandwidth	55.7MHz	61.3MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	62.1Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	15.7mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±14mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =784.5V/μs SR– =523.2V/μs
Input dynamic range	–3V, +3V	–2V, +2V

Table 6.13 Characteristics of the conventional and Type 6 CFOA

Discussion:

The marginal increases in CMRR and bandwidth compared with the CFOA with half circuit G (II) are obtained at the expense of a much larger AC gain error, offset-voltage and reduction in slew rate.

(6.4.7) Type 7 CFOA performance

Type 7 CFOA (Fig. 6.91) shows a number of improvements on the circuit of Fig.5.1. These are included to reduce gain-error, reduce offset voltage and improve bandwidth. The circuit includes two biasing resistors R_{Q1}, R_{Q2}, instead of one: this is for flexibility in design. The resistor R_{Q1}, which can be externally connected for user-choice, determines the operating current, I_{Q1}: the emitter followers Q_9, Q_{10} reduce the finite-β error in the current mirrors of which they form a part. Resistor R_{Q2} supplies current I_{Q2} ($\neq I_{Q1}$) to the diode-connected transistors Q_{17}/Q_{19}, Q_{18}/Q_{20} and thus provides a d.c. bias voltage to cascode transistors $Q_{11}/Q_{39}/Q_{37}$ and $Q_{12}/Q_{40}/Q_{38}$ that are included to increase the collector output resistances of the transistors with which they are associated ($Q_{11}/Q_{33}/Q_{35}$ and $Q_{12}/Q_{34}/Q_{36}$). This increase in output resistance contributes to gain accuracy and linearity.

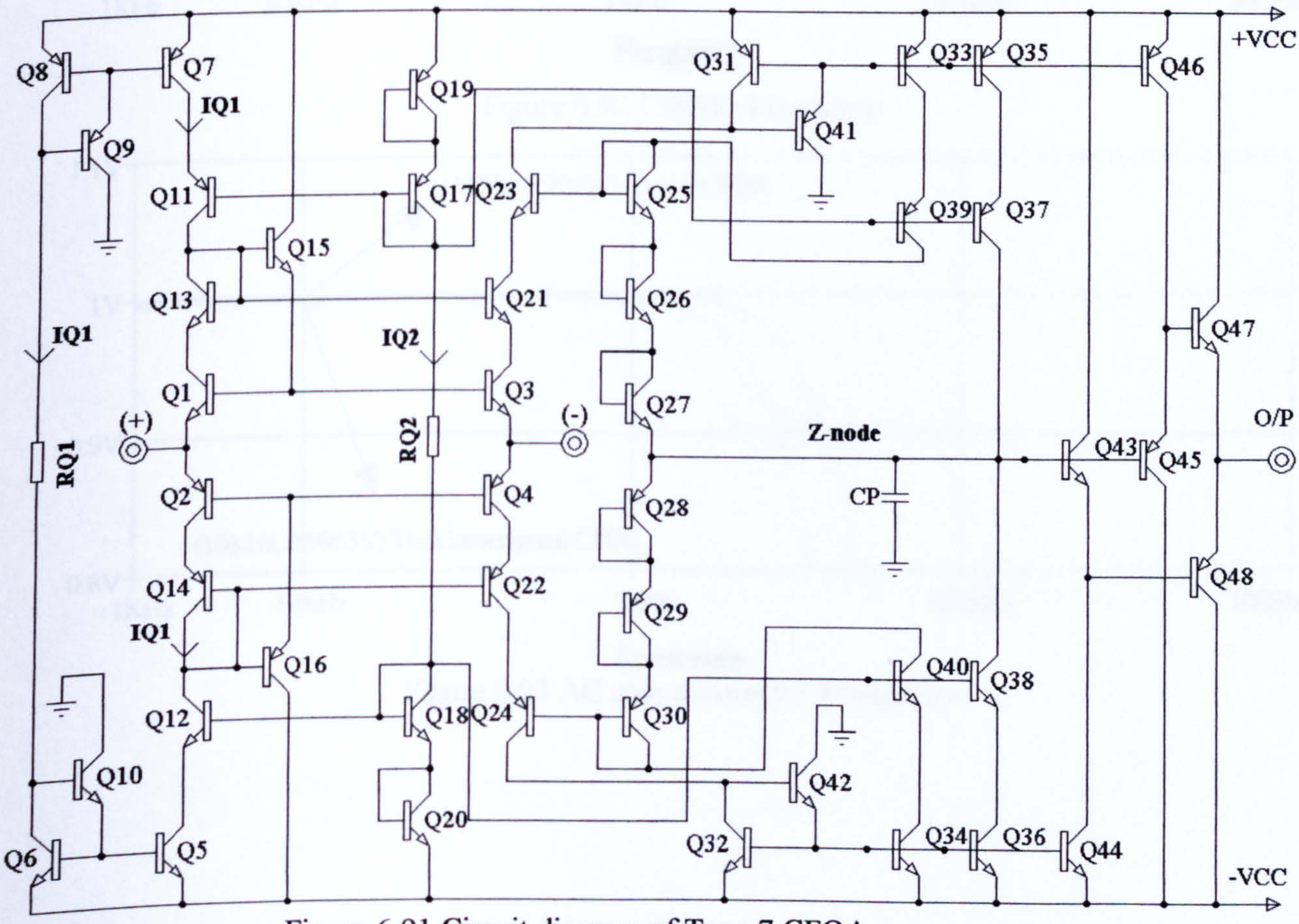


Figure 6.91 Circuit diagram of Type 7 CFOA

The choice of operating current for I_{Q2} (0.7mA) was, to some extent, arbitrary, being a compromise between a low value for reduced circuit dissipation **[6-3]**, and higher value for low impedance biasing at the collector of Q_{17}, Q_{18}.

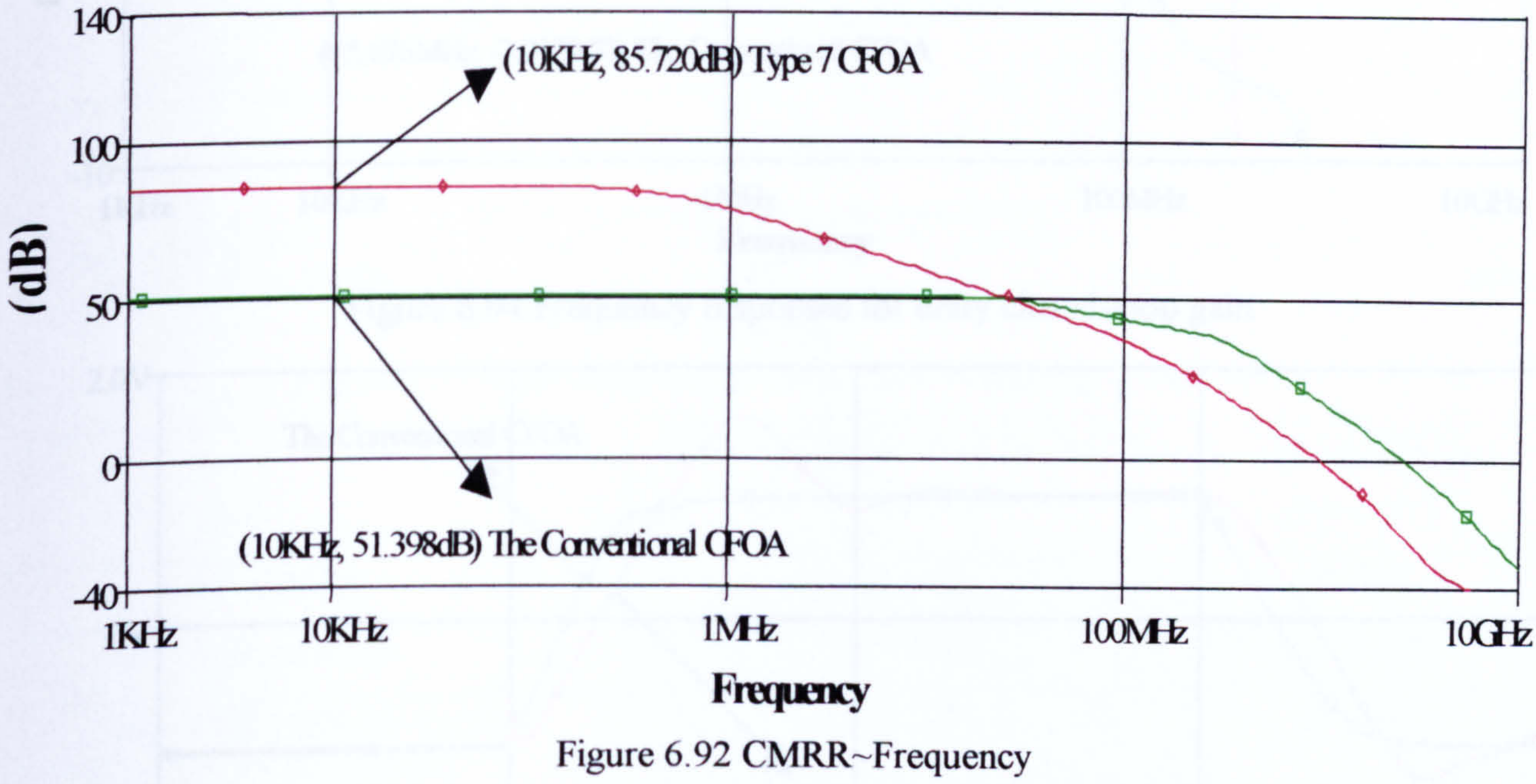


Figure 6.92 CMRR~Frequency

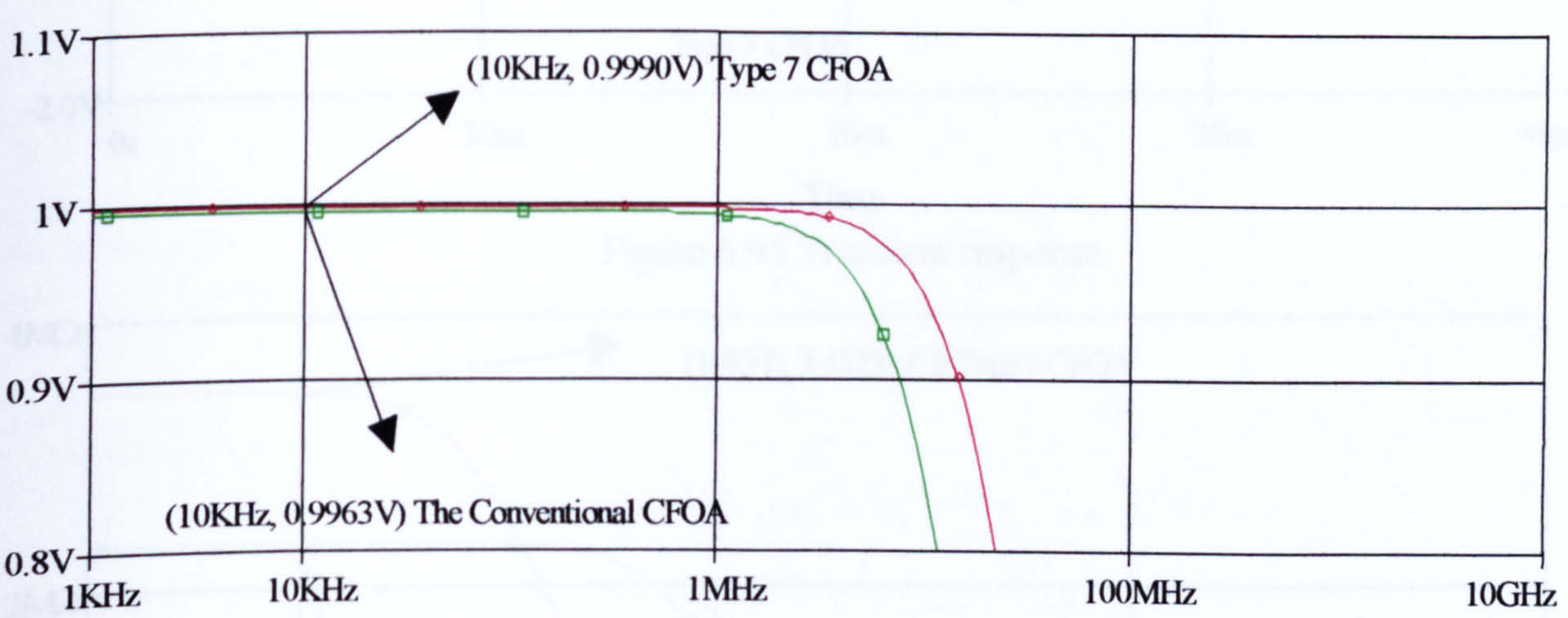


Figure 6.93 AC gain accuracy ~ Frequency

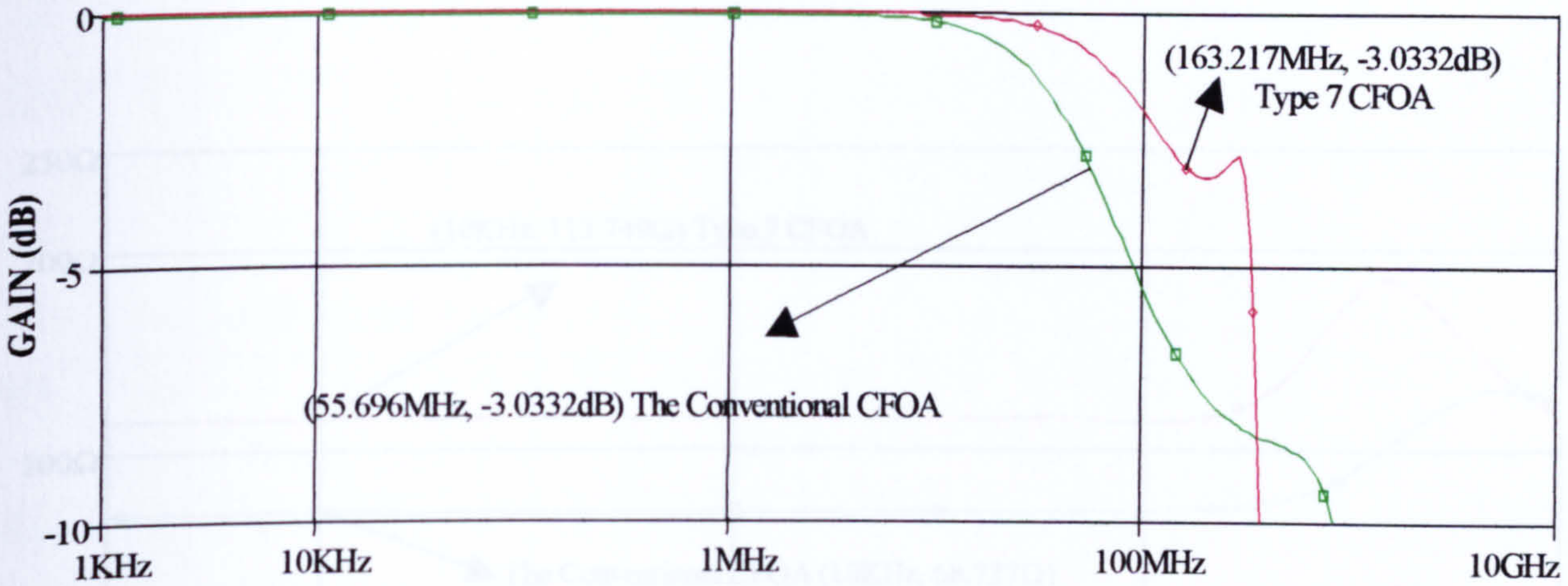


Figure 6.94 Frequency responses for unity closed-loop gain

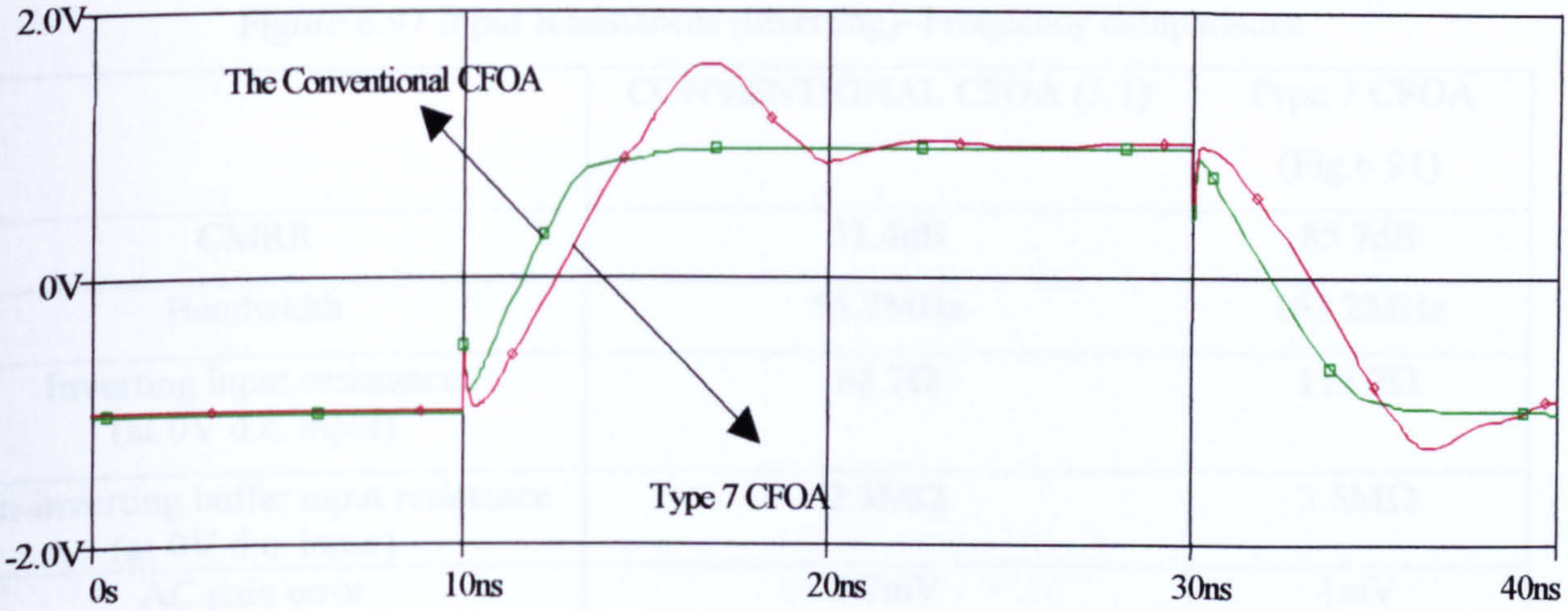


Figure 6.95 Transient response

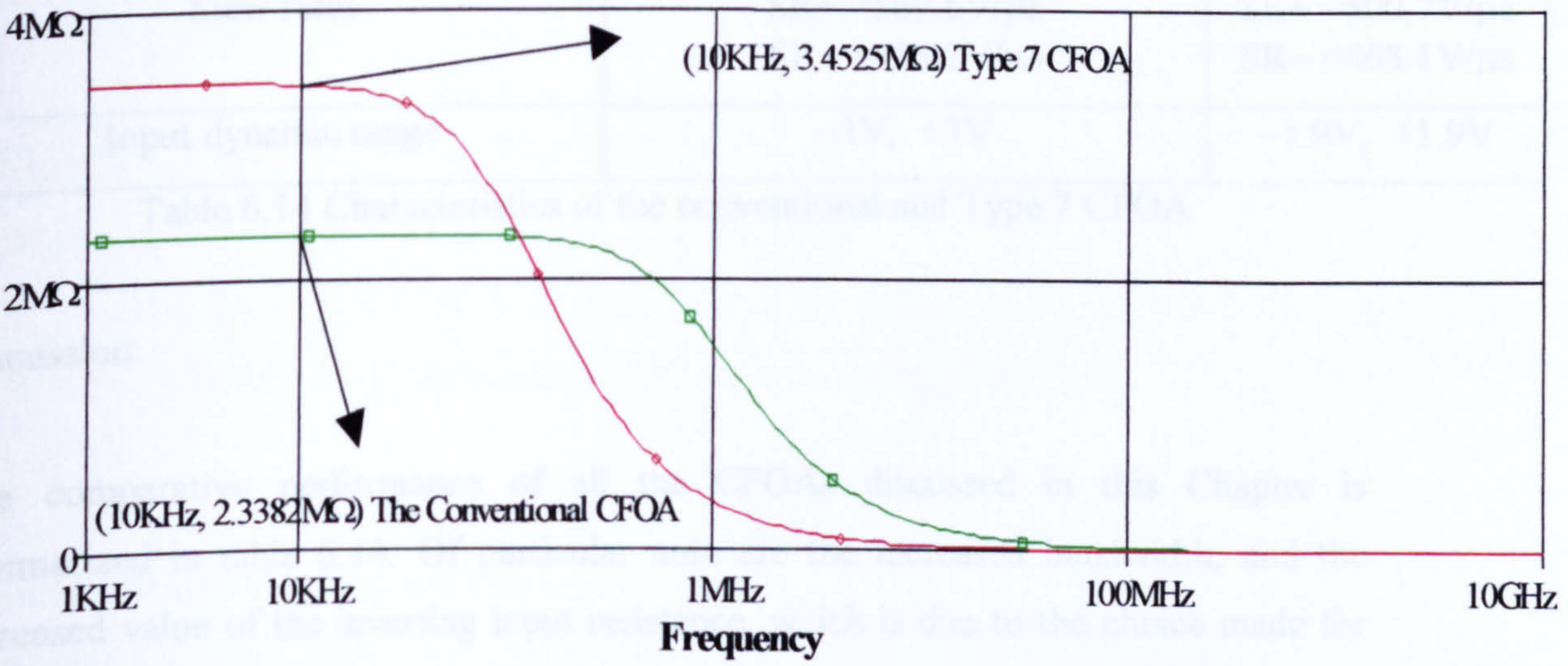


Figure 6.96 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

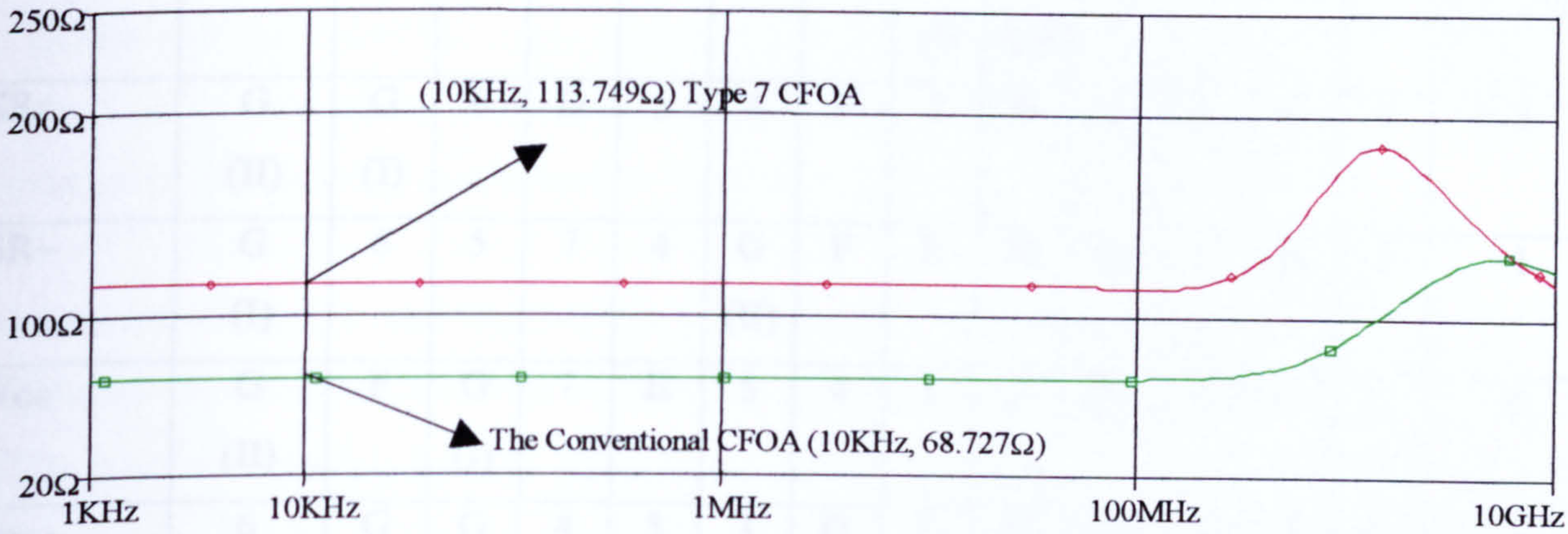


Figure 6.97 Input Resistances (inverting)~Frequency comparisons

	CONVENTIONAL CFOA (5.1)	Type 7 CFOA (Fig.6.91)
CMRR	51.4dB	85.7dB
Bandwidth	55.7MHz	163.2MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	113.7Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	3.5MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	1mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±3.25mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =500.7V/μs SR– =468.1V/μs
Input dynamic range	–3V, +3V	–1.9V, +1.9V

Table 6.14 Characteristics of the conventional and Type 7 CFOA

Discussion:

The comparative performance of all the CFOAs discussed in this Chapter is summarized in table 6.14. Of particular note are the increased bandwidth, and the increased value of the inverting input resistance, which is due to the choice made for this circuit biasing scheme and operation at two different biasing levels for the currents I_{Q1} (0.2mA) and I_{Q2} (0.7mA).

*	BEST	→	→	→	→	→	→	→	→	→	→	→	→	WORST
CMRR	1	3	4	C	5	6	D	G (I)	G (II)	2	F	E	7	B
SR+	G (II)	G (I)	6	D	5	4	F	7	B	C	3	E	1	2
SR–	G (I)	6	5	7	4	G (II)	F	E	D	C	3	B	2	1
V_{OS}	G (II)	F	G (I)	7	E	5	4	1	2	D	3	6	C	B
$R_{IN(-)}$	6	G (II)	G (I)	4	5	3	D	F	C	E	1	2	B	7
$R_{IN(+)}$	B	C	D	7	4	5	1	G (I)	6	3	G (II)	2	F	E
BW	7	5	G (II)	6	3	4	1	D	C	2	G (I)	F	E	B
A.C GAIN ERROR	7	G (II)	E	F	G (I)	B	2	5	4	1	D	C	6	3
DYNAMIC INPUT RANGE	B	C	E	F	2	1	3	D	G (I)	4	5	6	G (II)	7
DISSIPATION	E	F	G (I)	2	B	C	D	G (II)	3	1	6	4	5	7
TRANSISTOR COUNT	B 38	C 38	D 40	E 34	F 34	G (I) 38	G (II) 42	1 44	2 38	3 42	4 48	5 48	6 46	7 48

Table 6.14 Comparison of CFOA performance parameters

* A letter stands for half-circuit type

*A number denotes CFOA Type having both reverse and forward bootstrapping

Summary

A number of new CFOAs with performances much better than that of the conventional CFOA have been introduced in this chapter. A comparison of performance parameters is summarised in Table 6.14, on the previous page.

The circuits of Fig. 3.1, and Fig. 6.1, were subjected to SPICE simulation tests using BJT device models characteristic of an extra fast (f_T~4 GHz) complementary bipolar XFCB process of Analog Devices, Santa Clara, California. Comparative performance characteristics for the two types of CFOA are listed in Table 6.1, for $V_{CC} = \pm 5V$, $I_Q \approx 0.2mA$ - in both cases, the improvements in CMRR was apparent.

In this chapter, three new architectures of CFOAs are presented in Fig. 6.22, Fig. 6.29, and Fig. 6.36 in comparison to the conventional CFOA as shown in Fig.3.1. These amplifiers are being developed with the properties of having a high CMRR, low DC offset voltage, improved gain accuracy, and high slew-rate which can be used as a direct replacement part in all conventional CFOA application topologies. The slew rate performance of the CFOAs in Fig. 6.36 can be further improved by using the emitter-followers to drive Q_{25}, and Q_{26} as well as Q_3, Q_4.

This chapter presents the designs of two new CFOAs in Fig. 6.8 and Fig. 6.15 employing a reverse bootstrapping technique, that provide both high CMRR and slew-rate. Moreover, the new CFOA designs exhibit a low DC offset voltage, high bandwidth, and improved gain accuracy compared with the conventional CFOA as shown in Fig.3.1, enabling them to be used in applications requiring variable closed-loop gains with constant bandwidth, such as in automatic-gain-control, video, graphics and multimedia applications.

A new CFOA, based on the design and use in a repeated pattern of current transfer cell, has been presented and shown in Fig. 6.43. Compared with an existing configuration in Fig. 3.1, input referred offset voltage has been reduced significantly and the CMRR increased by approximately 41.4 dB. The figures for offset voltage are based on the assumption that the pairs Q_1, Q_3 and Q_2, Q_4 are perfectly matched. A

practical mismatched ΔA_E in nominal emitter area, A_E, produces an additional offset voltage equal to $V_T \cdot \log_e[1+(\Delta A_E / A_E)]$, V_T being the 'thermal' voltage ($\approx$ 25.8 mV, at room temperature): for a 2% mismatch this amounts to some 500 μV. Also, the A.C. gain accuracy has been improved, as have bandwidth and input resistances.

Also this chapter has considered the trade-offs involved in the design of six new CFOAs (type 1, type2, type 3, type 4, type 5, and type 6) to improve the performance of the CFOA, over that possible using the well-established CFOA configuration as shown Fig. 3.1, with respect to three major characteristics, *viz.*, CMRR, offset voltage and slew-rate. For the maximum output voltage swing, the well-established CFOA is the best option. For comparable slew-rate, but improved CMRR and reduced offset voltage, other choices are possible. The relative merits of these have been displayed in a comparison (Table 9, Table 10, Table 11, Table 12, and Table 13).

A new CFOA has been described, comparative performance figures for the two CFOAs, i.e. the conventional type as shown in Fig. 3.1 and the new type of Fig. 6.91, are shown in Table 6.14 of particular note are the increased bandwidth, and reduced gain error and the offset voltage. This design includes employing the optimum choice of operating current I_{Q1} and I_{Q2} to decrease the impedances biasing value at the collector of Q_{17}, Q_{18}.

The benefits of greater accuracy, reduced DC offset voltage, together with an architecture that provides a high CMRR and, in one case, an outstanding bandwidth (approximately 160 MHz) make the CFOAs a welcome and useful addition to the analogue designer's tool kit. However, the price paid for these improvements is a reduced output voltage swing, because of vertical transistor stacking, for given rail supply voltages.

(6.5) References for Chapter 6

[6-1] M. A. Vere Hunt, and F. J. Lidgey, "A high slew-rate voltage-mode op-amp," Proc. International Symposium on Circuits and Systems (ISCAS), San Diego, pp.2872-2875, 1992.

[6-2] Wenjun, Su, "Design and development of high CMRR wide bandwidth instrumentation Amplifiers", PhD thesis, Oxford Brookes University, 1997.

[6-3] D. Smith, *et al.*, "Evolution of high-speed op-amp architectures," IEEE J. Solid-State Circuits, Vol.29, No.10, pp. 1166-1179, October 1994.

CHAPTER 7

Current feedback operation amplifier designs using overall bootstrapping

(7.1) Introduction

In this chapter new CFOA architectures are introduced based on a combination of techniques. One of these technique is global bootstrapping (the floating technique) design previously reported [7-1].

In Section 7.3 the two designs described in [7-1], and [7-2] are combined to produce another new CFOA design which yields significant enhancement of both CMRR and input-referred offset. In Section 7.4 a new design is presented, modifying the CFOA input stage circuit by introducing a combination of a bootstrapping technique [7-1] and folded-cascode transistors [7-3]. Finally, in Section 7.5 a bootstrapping technique [7-1] is employed with Quasi-Darlingtons in the input stage. Simulation results show significant improvements in CMRR, PSRR, bandwidth and input-referred offset voltage, as well as a desirable reduction in inverting-input impedance.

(7.2) The Floating technique

The CMRR limitations of the conventional CFOA can be overcome by floating the entire input stage, as shown in Fig.7.1 **[7-4]**. The conventional CFOA can be described as a core current-conveyor, type CCII+, with the Z-node connected to an output voltage buffer **[7-5]**. The core CCII+ in this new design has a very simple topology, shown within the broken-line box in Fig.7.1.

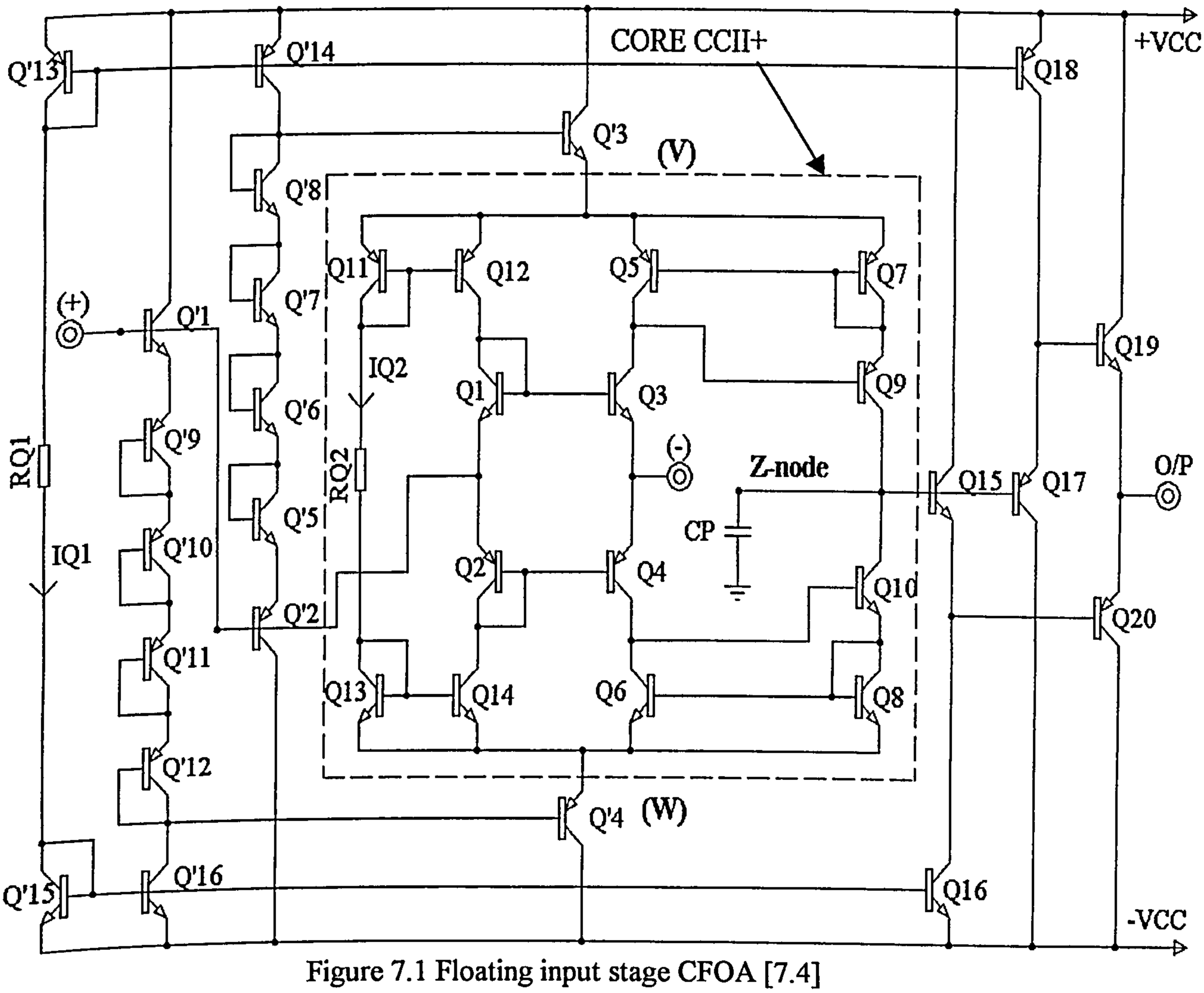


Figure 7.1 Floating input stage CFOA [7.4]

The transistor pairs Q_1/Q_3 and Q_2/Q_4 are both NPN and PNP, respectively, and so the matching between Q_1/Q_3 (and between Q_2/Q_4) is better than that of the conventional CFOA. Normally node-V and node-W would be connected to +Vcc and $-V_{CC}$ respectively. The composite voltage-followers Q'_1/Q'_4 and Q'_2/Q'_3 apply the

non-inverting input signal voltage to the emitters of Q_5 and Q_6, effectively floating the input stage. Diode-connected transistors Q'_5 to Q'_{12} provide appropriate DC biasing. With this arrangement, the signal voltage difference between the collector and base of both Q_3 and Q_4 is almost zero, so the influence of the Early-effect from Q_3 and Q_4 is greatly reduced, yielding a significant improvement in both CMRR and PSRR performance.

Another way of looking at the effect of floating the core amplifier is that the signal voltages appearing across the r_{ce} of the core amplifier are substantially reduced. Thus, the common–mode current flowing through the r_{ce} of the primary input transistors in the input stage is almost eliminated resulting in a high CMRR **[7-5]**.

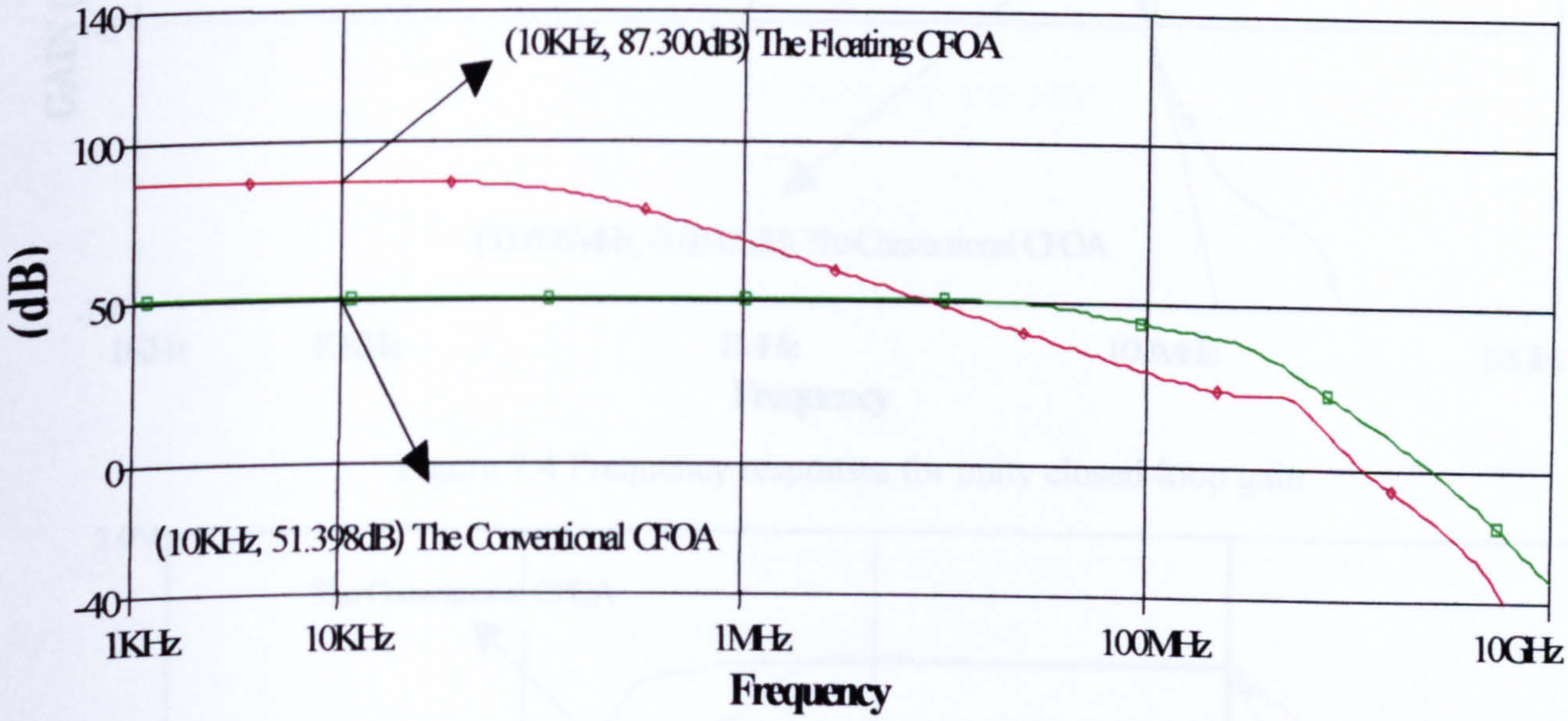


Figure 7.2 CMRR~Frequency

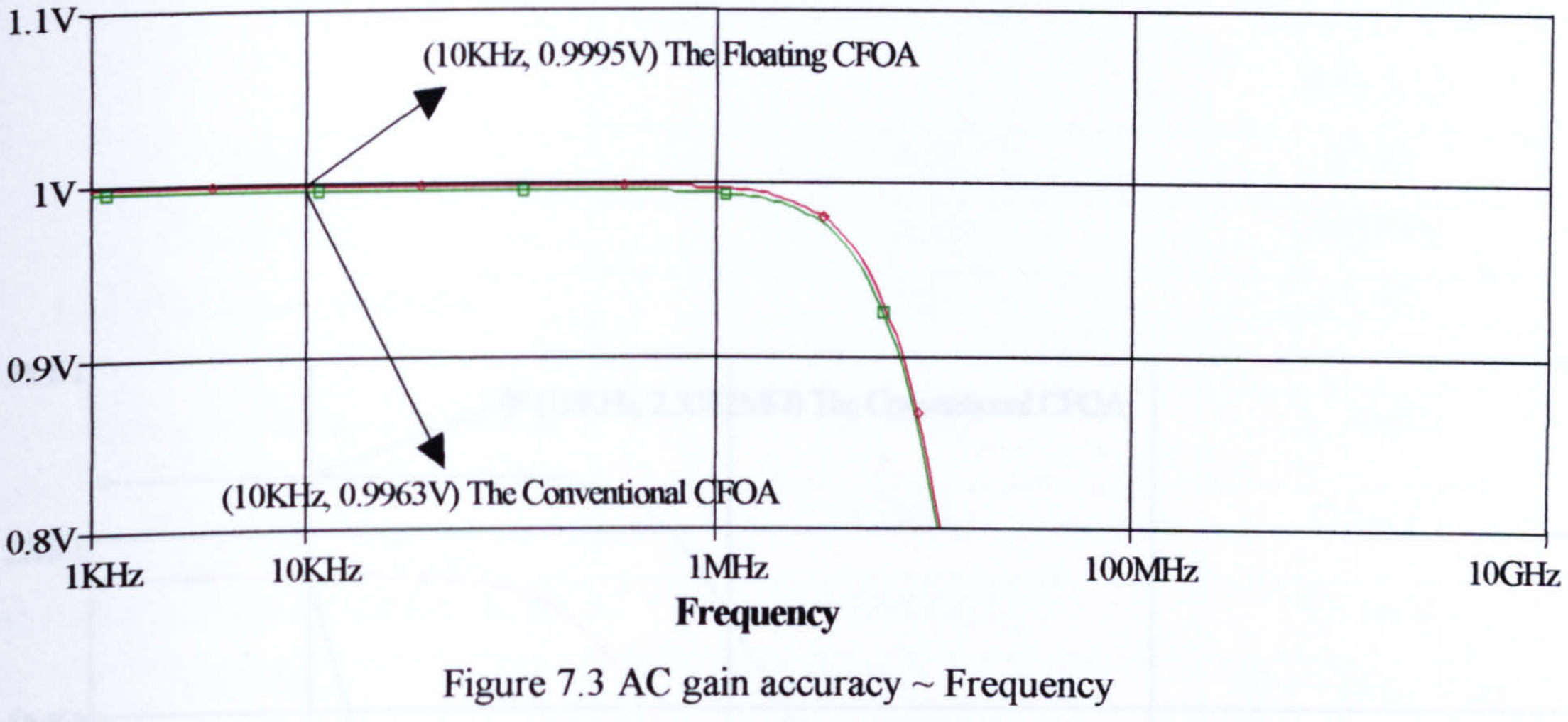


Figure 7.3 AC gain accuracy ~ Frequency

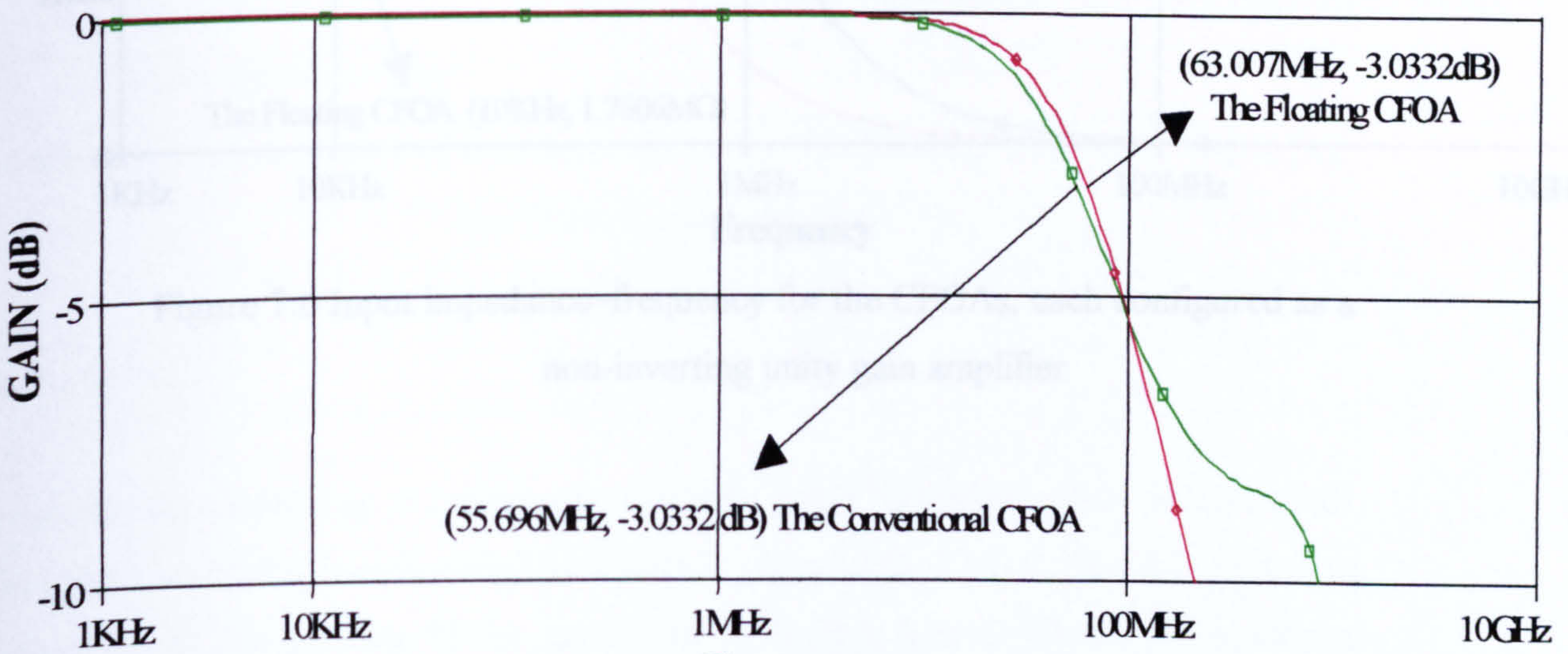


Figure 7.4 Frequency responses for unity closed-loop gain

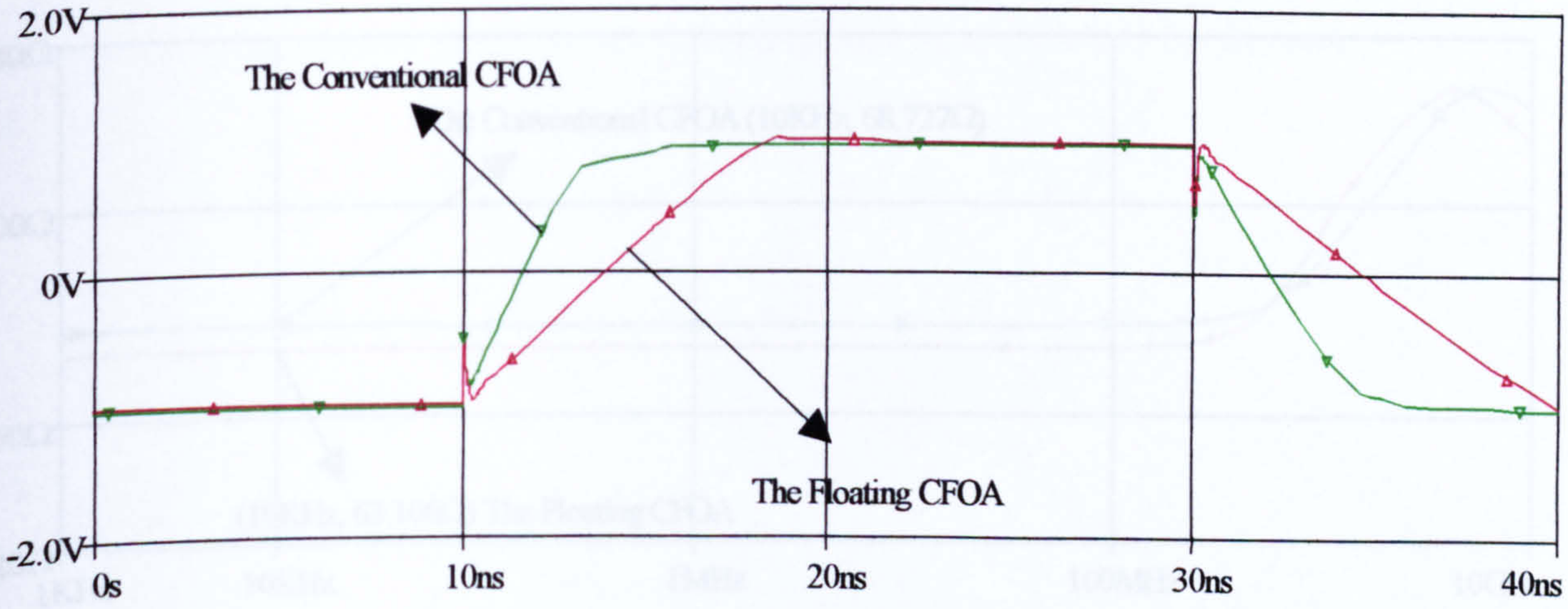


Figure 7.5 Transient response

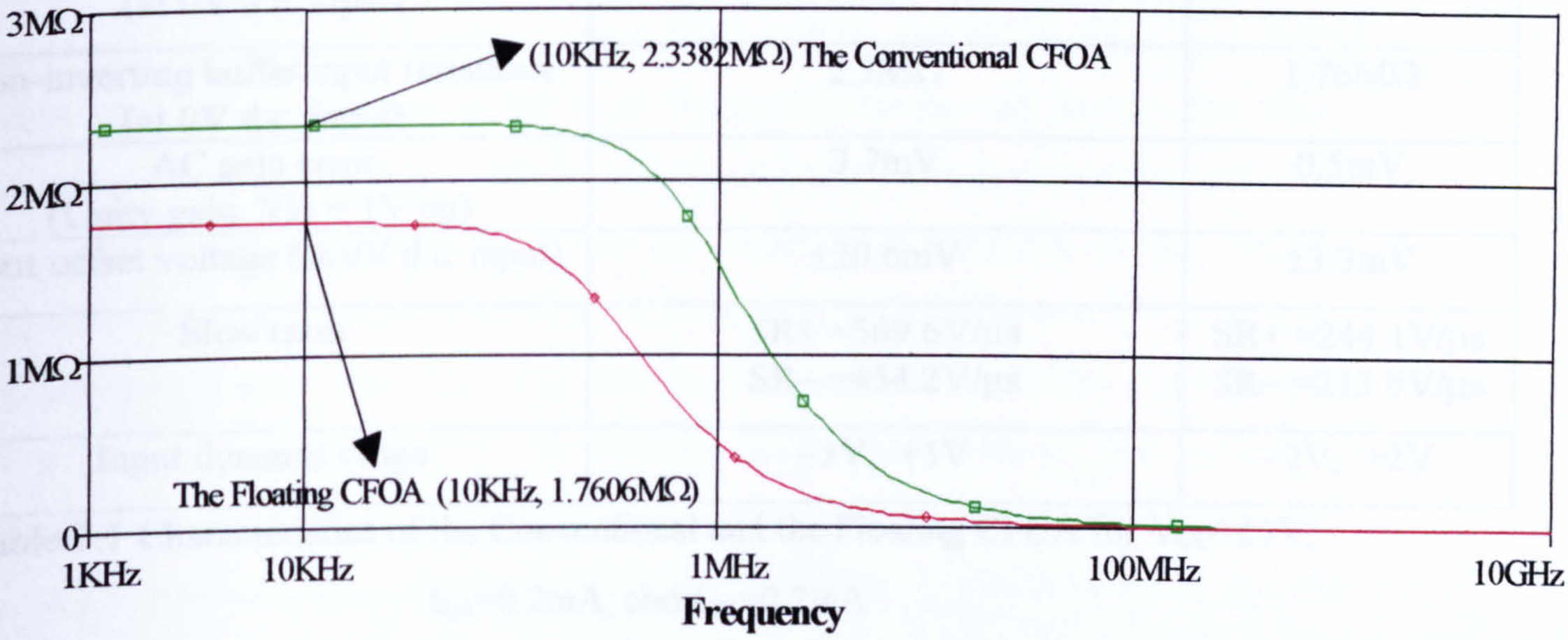


Figure 7.6 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

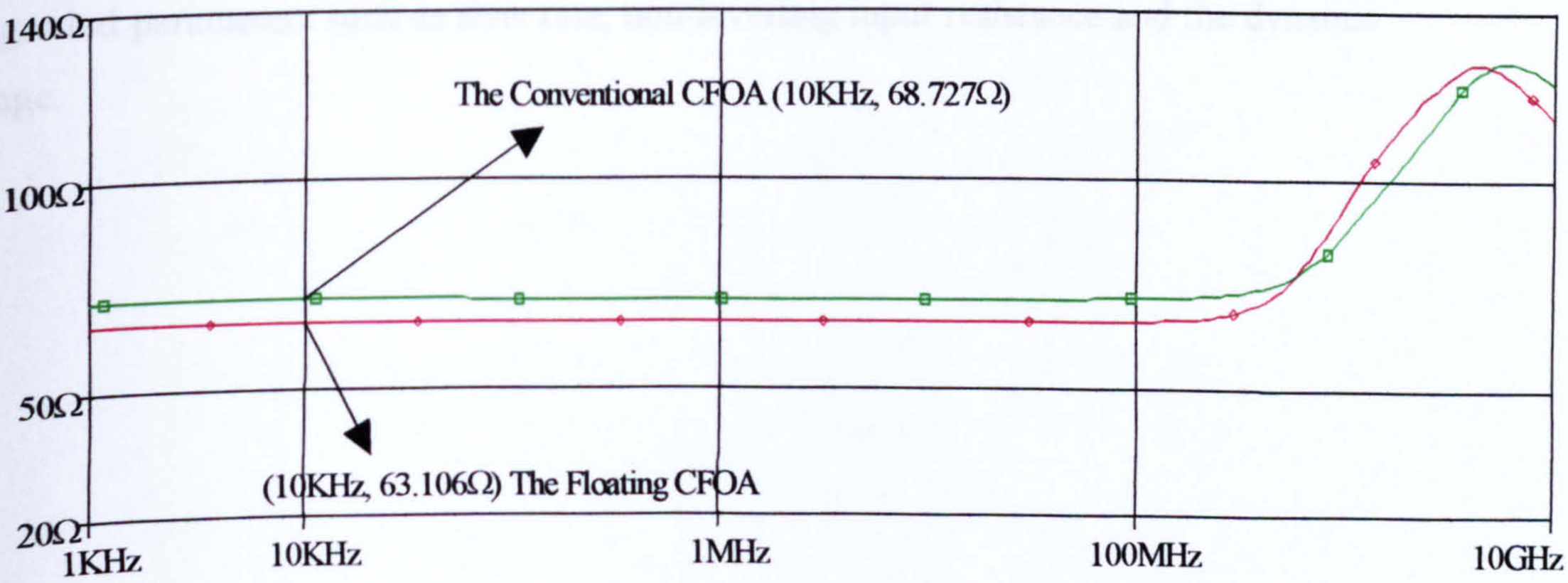


Figure 7.7 Input Resistances (inverting)~Frequency comparisons

	CONVENTIONAL CFOA (5.1)	Floating CFOA (Fig 7.1)
CMRR	51.4dB	87dB
Bandwidth	55.7MHz	63MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	63.1Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	1.76MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	0.5mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±3.3mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =244.1V/μs SR– =213.6V/μs
Input dynamic range	–3V, +3V	–2V, +2V

Table 7.1 Characteristics of the Conventional and the Floating CFOA for V_{CC}=±5V, I_{Q1}=0.2mA, and I_{Q2}=0.2mA

Discussion:

From the above reading, it can be seen that the CMRR has increased by at least 36dB. Also the bandwidth has increased by 7MHz in the floating CFOA. The AC gain-error is reduced in the floating CFOA, as shown in Fig.7.3. The simulated input-referred offset voltage of the floating CFOA (Table 7.1) is 3.3mV while in the conventional CFOA is 20.6mV. Most of the characteristics have been improved, but there are some degraded parameters such as slew rate, non-inverting input resistance and the dynamic range.

(7.3) A better CFOA

An alternative circuit-design approach which also yields improved CMRR was reported in **[7-2]** and is shown schematically in Fig.7.8. The input stage is shown in its simplest form with a conventional input complementary pair input buffer comprising D_1 / D_2 and Q_1 / Q_2 . The addition of Q_3 and Q_4 cascode Q_1 and Q_2 respectively and any common-mode input voltage is thereby fed via the bias chain comprising D_5 to D_{10} together with the associated DC current source/sink supplies of I_{BIAS} to the bases of Q_1 and Q_2. The net result of the addition of the cascode transistors Q_3, Q_4 are similar to that for the floating core CFOA shown in Fig.7.1, that the primary two input transistors, (Q_1 and Q_2 in the case of the CFOA Fig.7.8) have their collectors bootstrapped to the common-mode input voltage and hence the common-mode signal voltage appearing across the r_{ce} of these two devices approaches zero, again producing a significant improvement in CMRR. It should be noted that the output stage shown in Fig.7.8 uses a schematic macro-model representation of the current-mirror source and sink pair for simplicity and convenience. In practice these two current-mirrors are realised using the Wilson current-mirror design **[7-6]** shown in Fig.7.9.

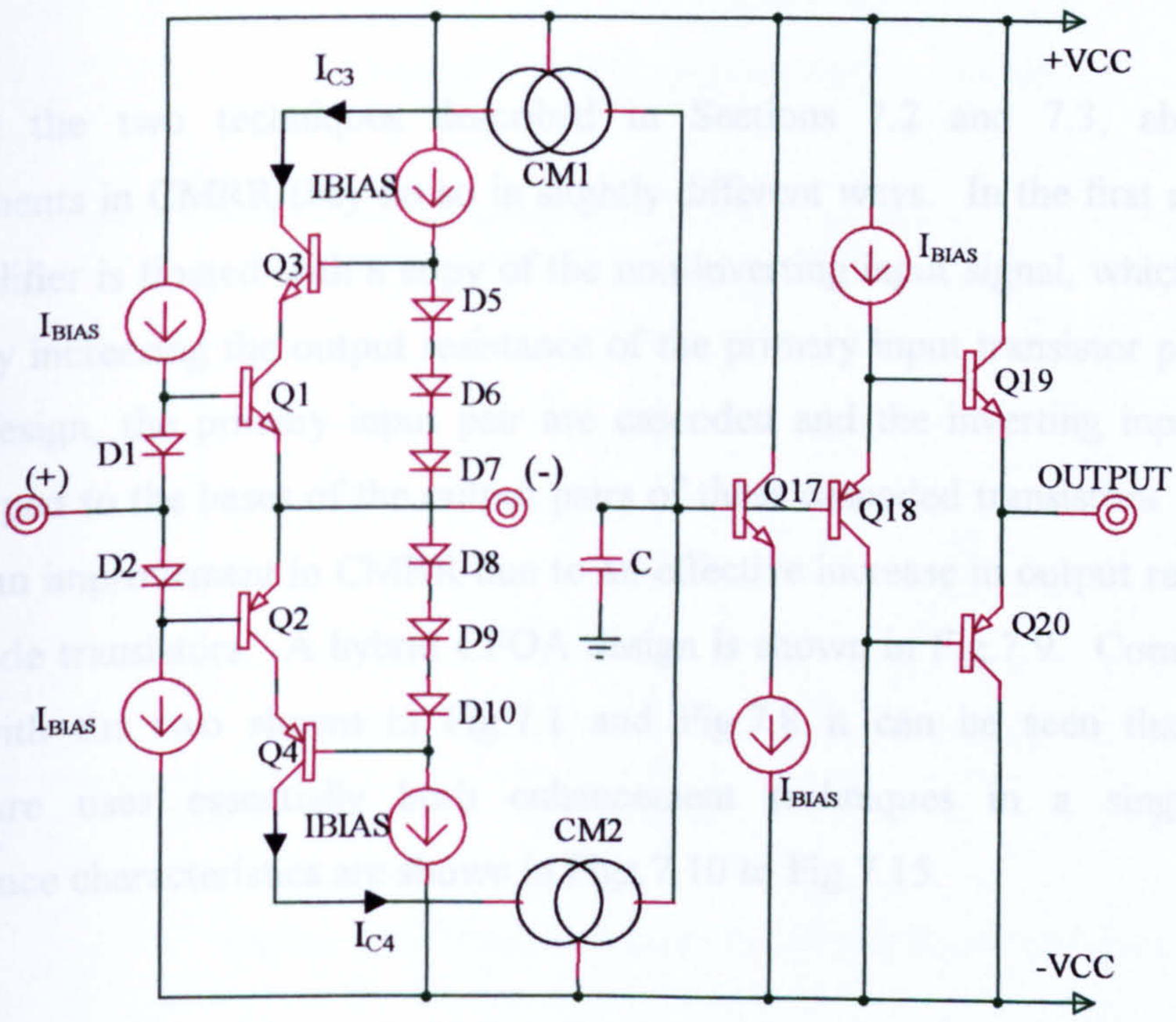


Figure 7.8 A Bootstrapped Single-Stage CFOA **[7-2]**

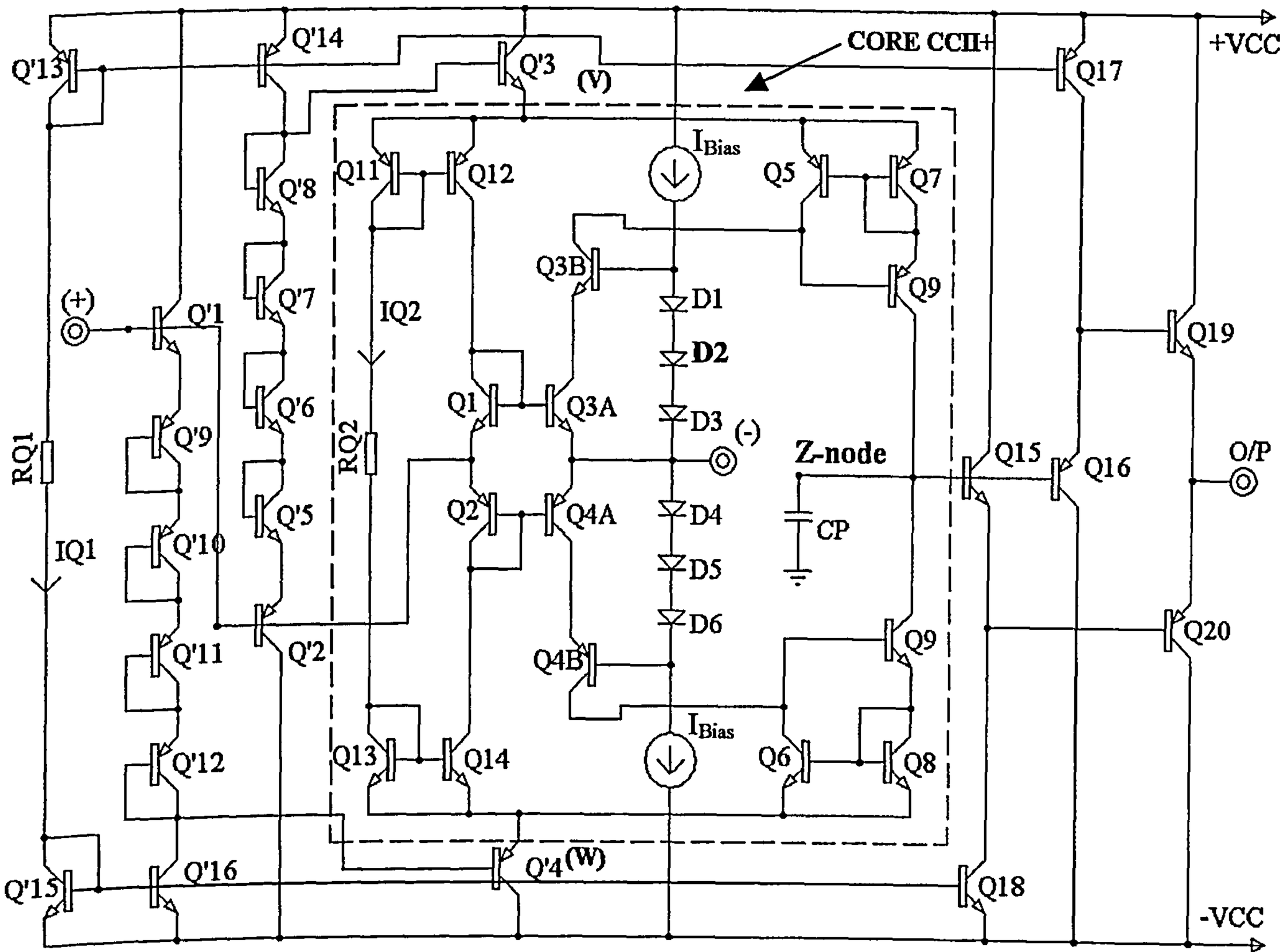


Figure 7.9 A better CFOA architecture

Although the two techniques described in Sections 7.2 and 7.3, above, yield improvements in CMRR they do so in slightly different ways. In the first method the core amplifier is floated with a copy of the non-inverting input signal, which results in effectively increasing the output resistance of the primary input transistor pair. In the second design, the primary input pair are cascoded and the inverting input stage is bootstrapped to the bases of the output pairs of these cascoded transistors. Again the result is an improvement in CMRR due to an effective increase in output resistance of the cascode transistors. A hybrid CFOA design is shown in Fig.7.9. Comparing this design with the two shown in Fig.7.1 and Fig.7.8 it can be seen that the new architecture uses essentially both enhancement techniques in a single CFOA. Performance characteristics are shown in Figs 7.10 to Fig 7.15.

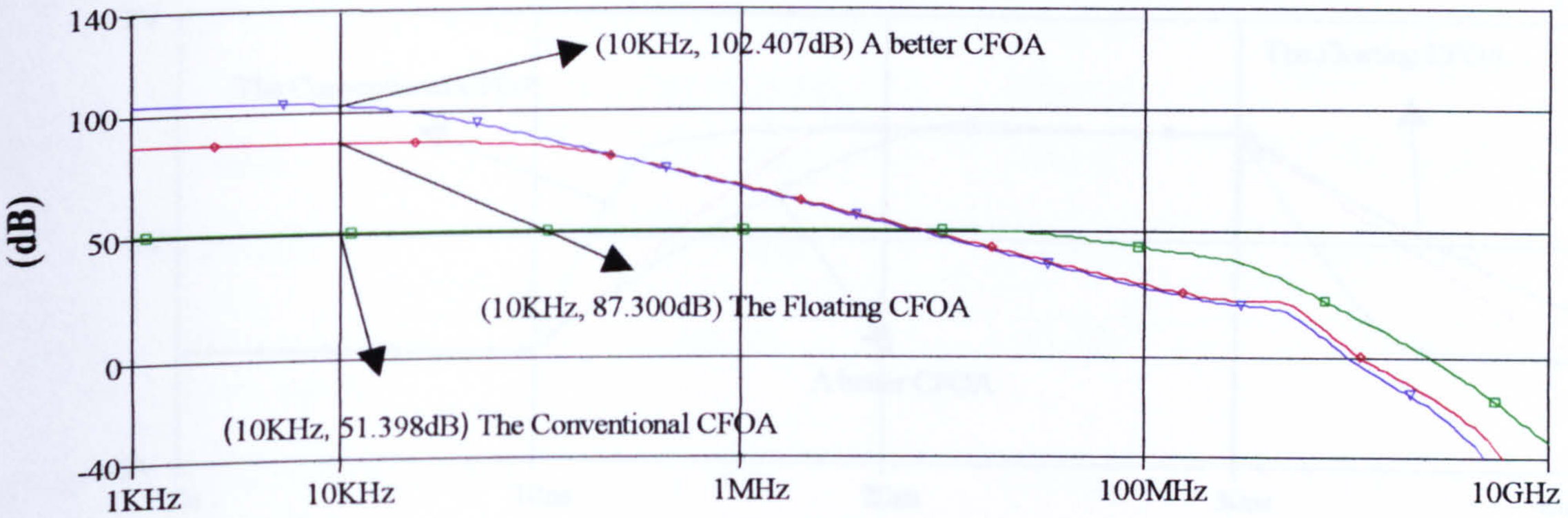


Figure 7.10 CMRR~Frequency

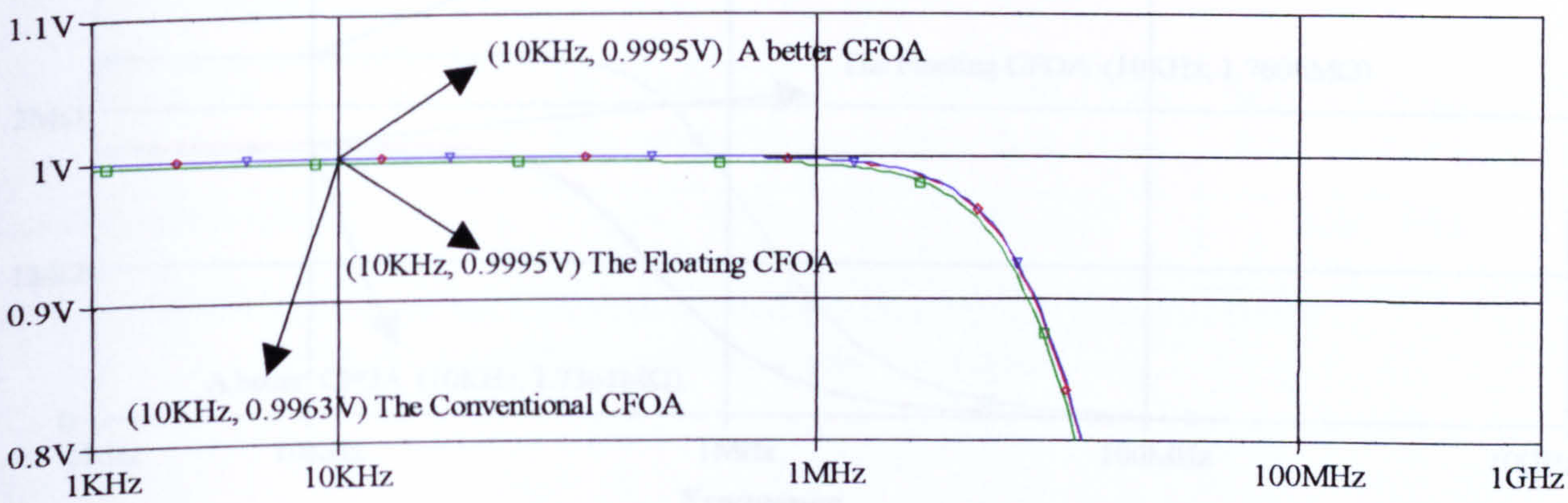


Figure 7.11 AC gain accuracy ~ Frequency

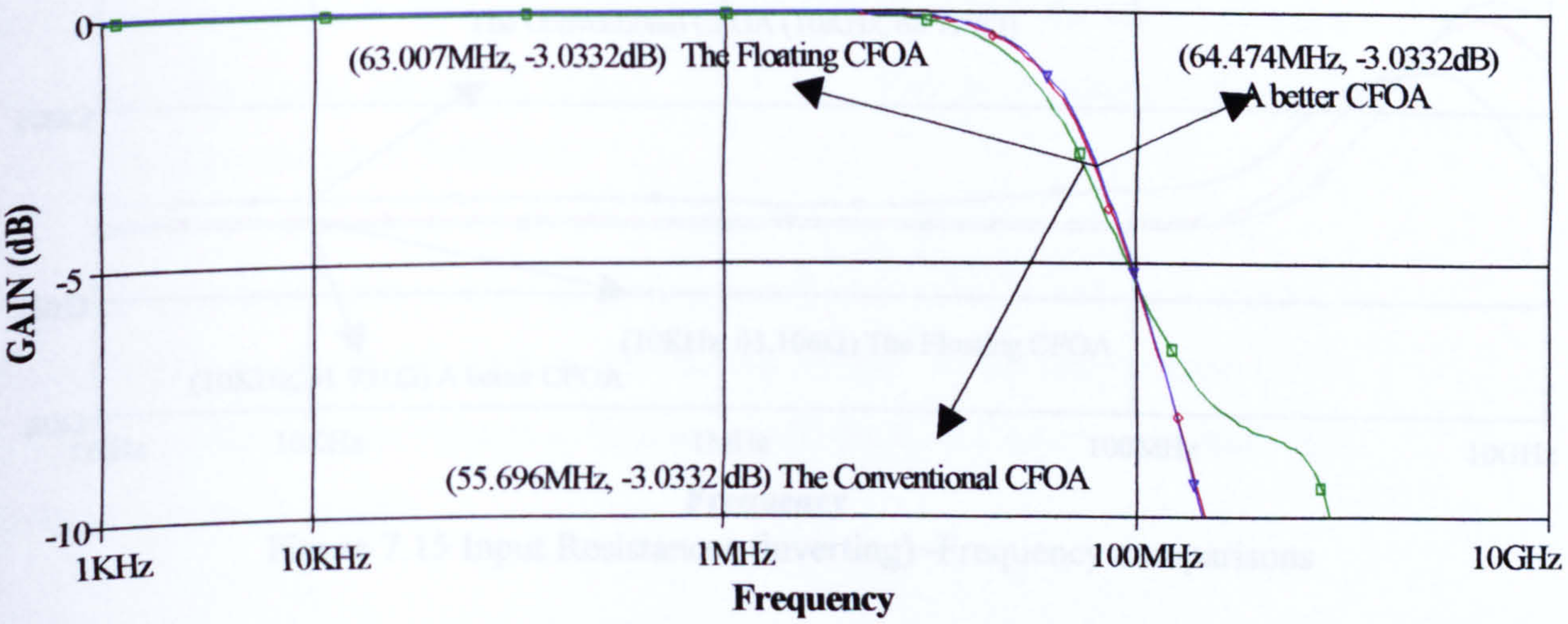


Figure 7.12 Frequency responses for unity closed-loop gain

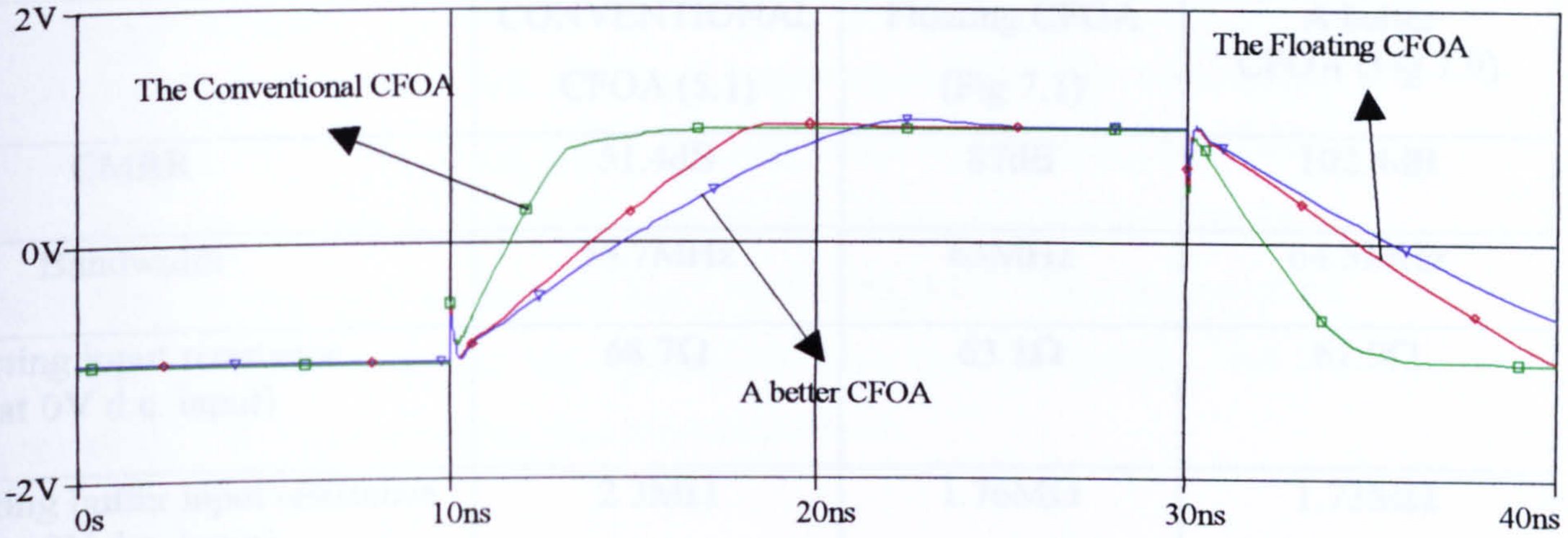


Figure 7.13 Transient response

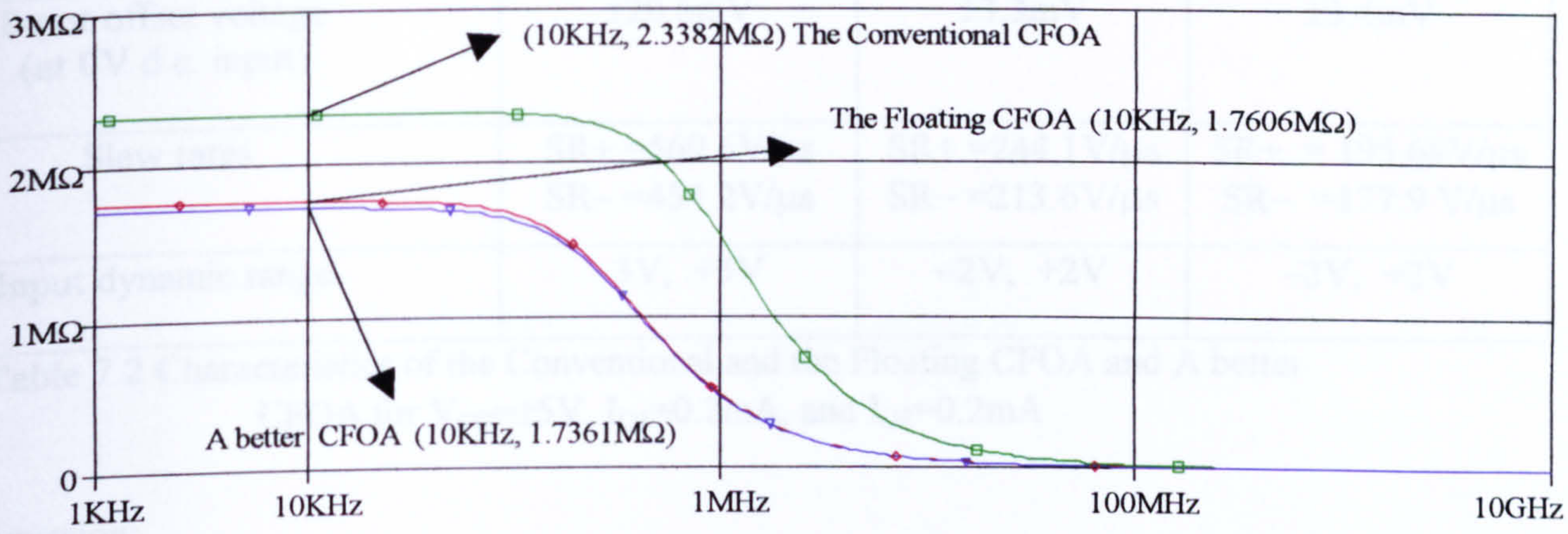


Figure 7.14 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

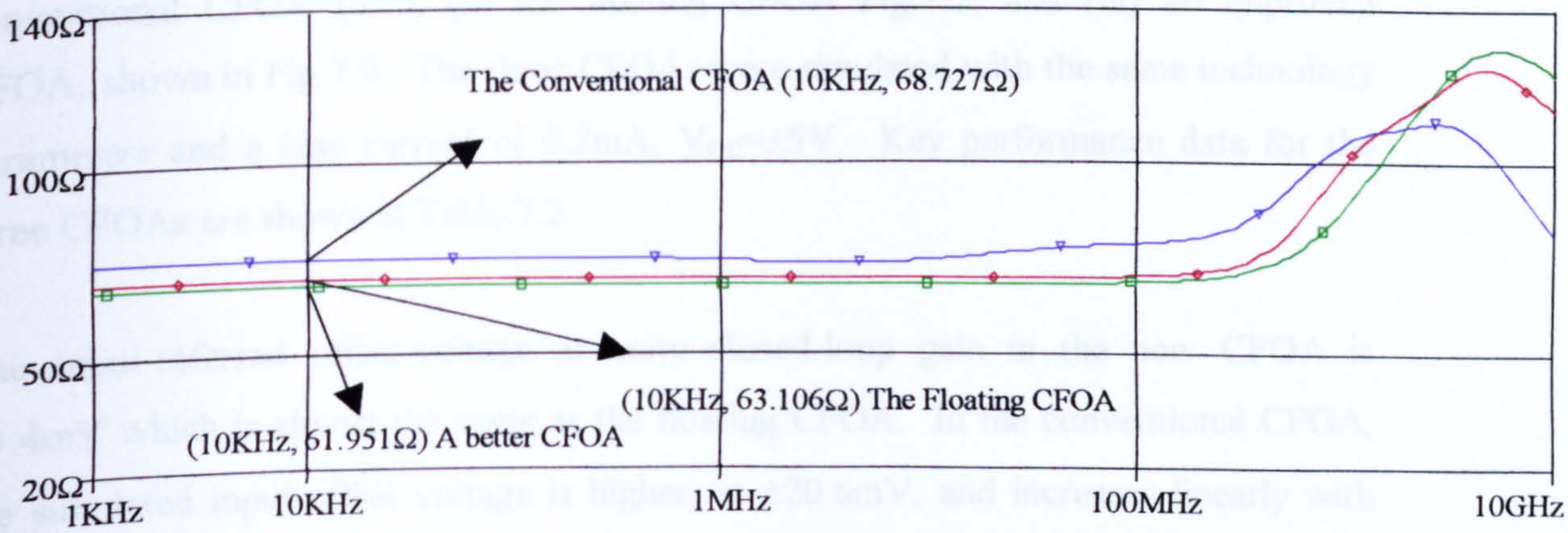


Figure 7.15 Input Resistances (inverting)~Frequency comparisons

	CONVENTIONAL CFOA (5.1)	Floating CFOA (Fig 7.1)	A better CFOA (Fig 7.9)
CMRR	51.4dB	87dB	102.4dB
Bandwidth	55.7MHz	63MHz	64.5MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	63.1Ω	61.9Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	1.76MΩ	1.73MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	0.5mV	0.5mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±3.3mV	±3.4mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =244.1V/μs SR– =213.6V/μs	SR+ = 195.68V/μs SR– =177.9 V/μs
Input dynamic range	–3V, +3V	–2V, +2V	–2V, +2V

Table 7.2 Characteristics of the Conventional and the Floating CFOA and A better CFOA for V_{CC}=±5V, I_{Q1}=0.2mA, and I_{Q2}=0.2mA

Discussion:

For comparative assessment, three CFOAs were simulated, namely (i) the conventional CFOA (5.1), (ii) the floating CFOA Fig.7.1, and (iii) an improved CFOA, shown in Fig.7.9. The three CFOAs were simulated with the same technology parameters and a bias current of 0.2mA, V_{CC}=±5V. Key performance data for the three CFOAs are shown in Table.7.2.

The input-referred offset-voltage at unity closed-loop gain in the new CFOA is ±3.4mV which is almost the same as the floating CFOA. In the conventional CFOA, the simulated input-offset voltage is higher, at ±20.6mV, and increases linearly with increasing closed-loop gain.

The simulated CMRR of the new CFOAs increase, dramatically, to 102dB, while in the floating CFOA, and the conventional CFOA it is 87dB, and 50dB, respectively, as shown in Fig.7.10. The frequency responses of all CFOAs, each configured for unity

closed-loop gain amplifier, the bandwidth of the new CFOA, and the floating CFOA are relatively close: however, they show an improvement over the conventional CFOA counterpart as shown in Fig.7.12. A consequence of improving the CMRR and the input-referred offset voltage is that the AC gain-error, and the inverting input impedance are also improved as shown in Fig.7.11, and Fig.7.15. The majority of the characteristics of the better CFOA are significantly better than the floating, and the conventional CFOA, with the notable exception of slew-rate.

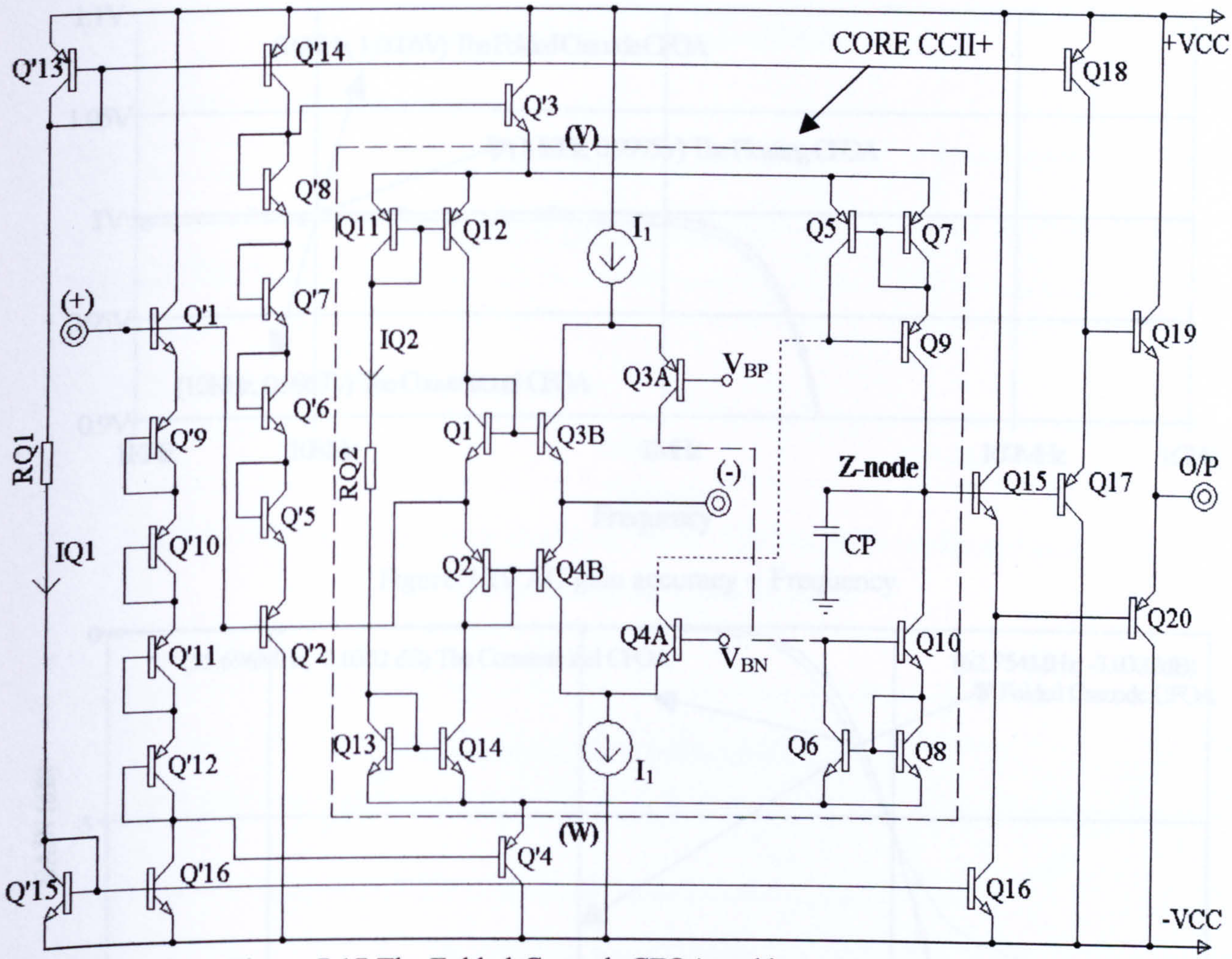


Figure 7.17 The Folded-Cascode CFOA architecture

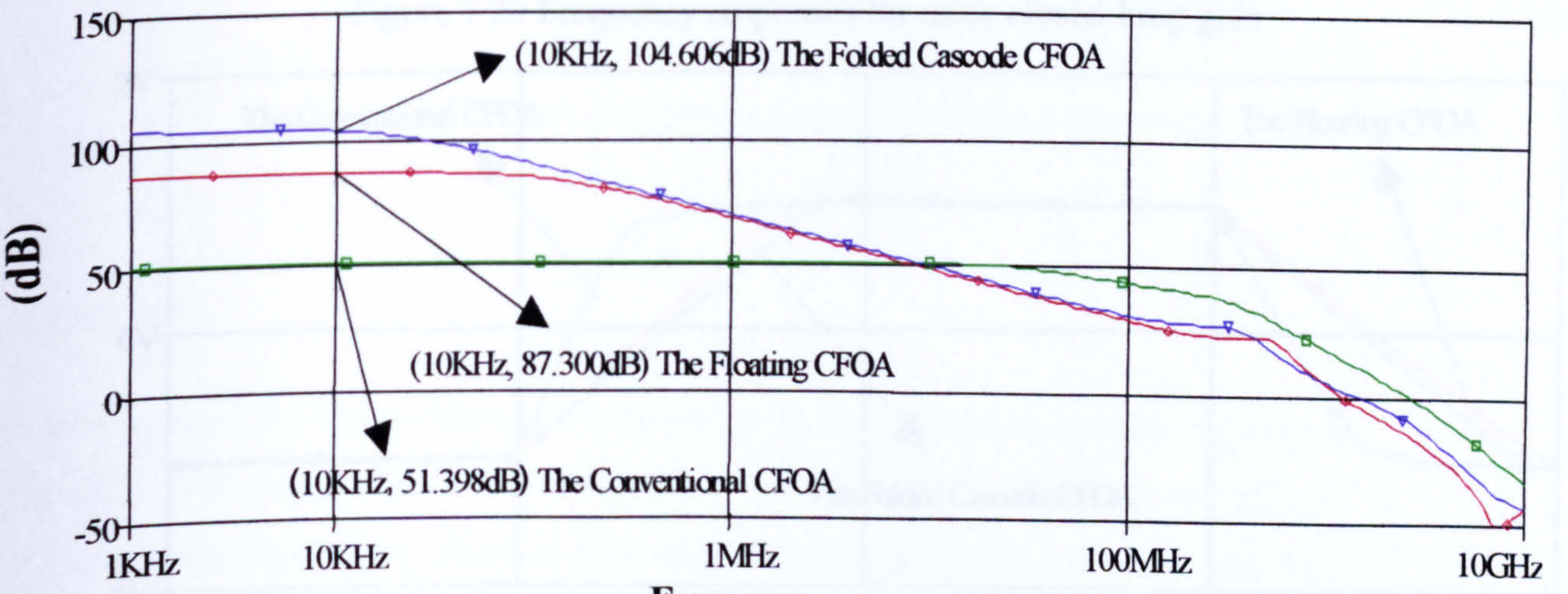


Figure 7.18 CMRR~Frequency

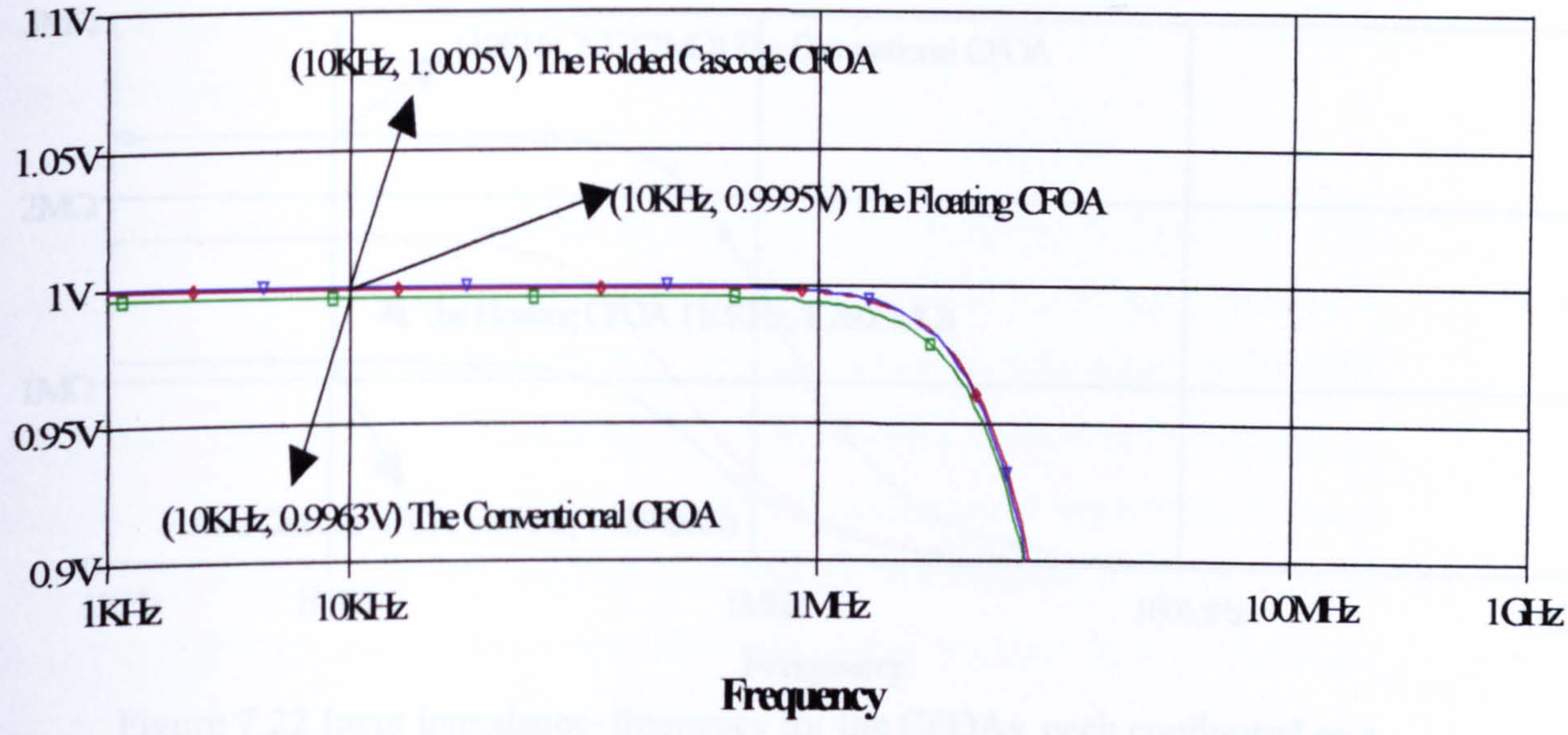


Figure 7.19 AC gain accuracy ~ Frequency

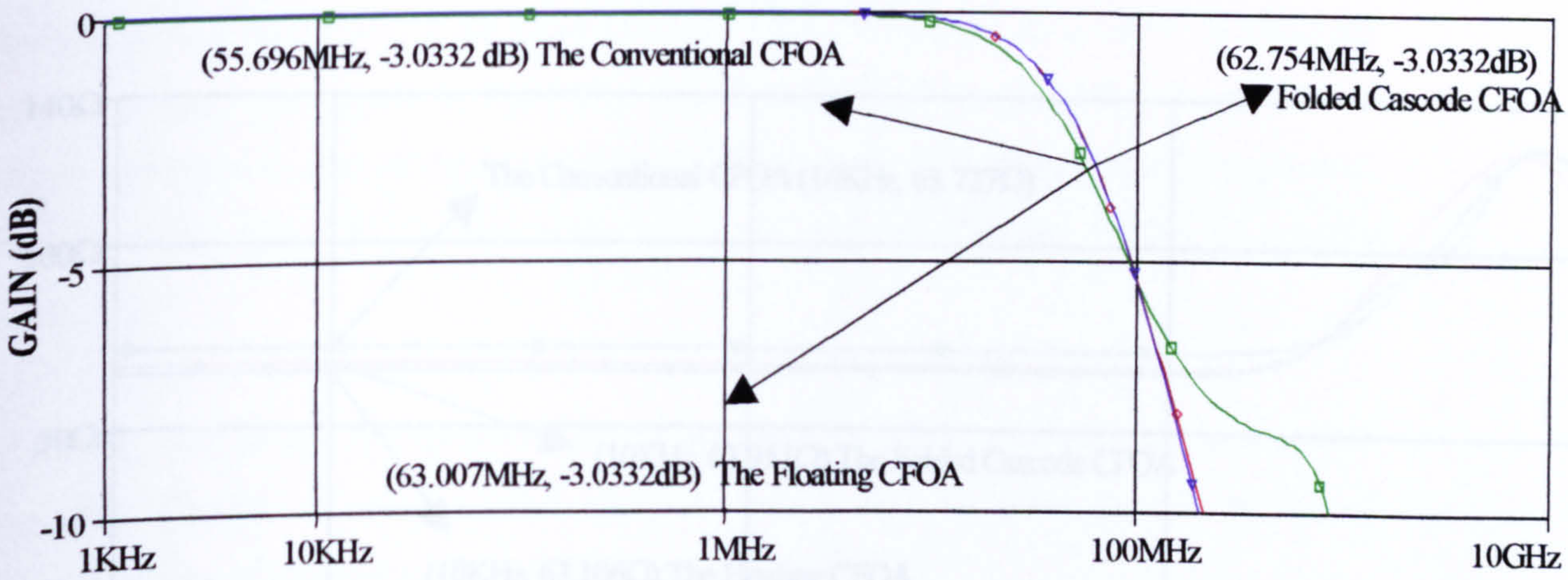


Figure 7.20 Frequency responses for unity closed-loop gain

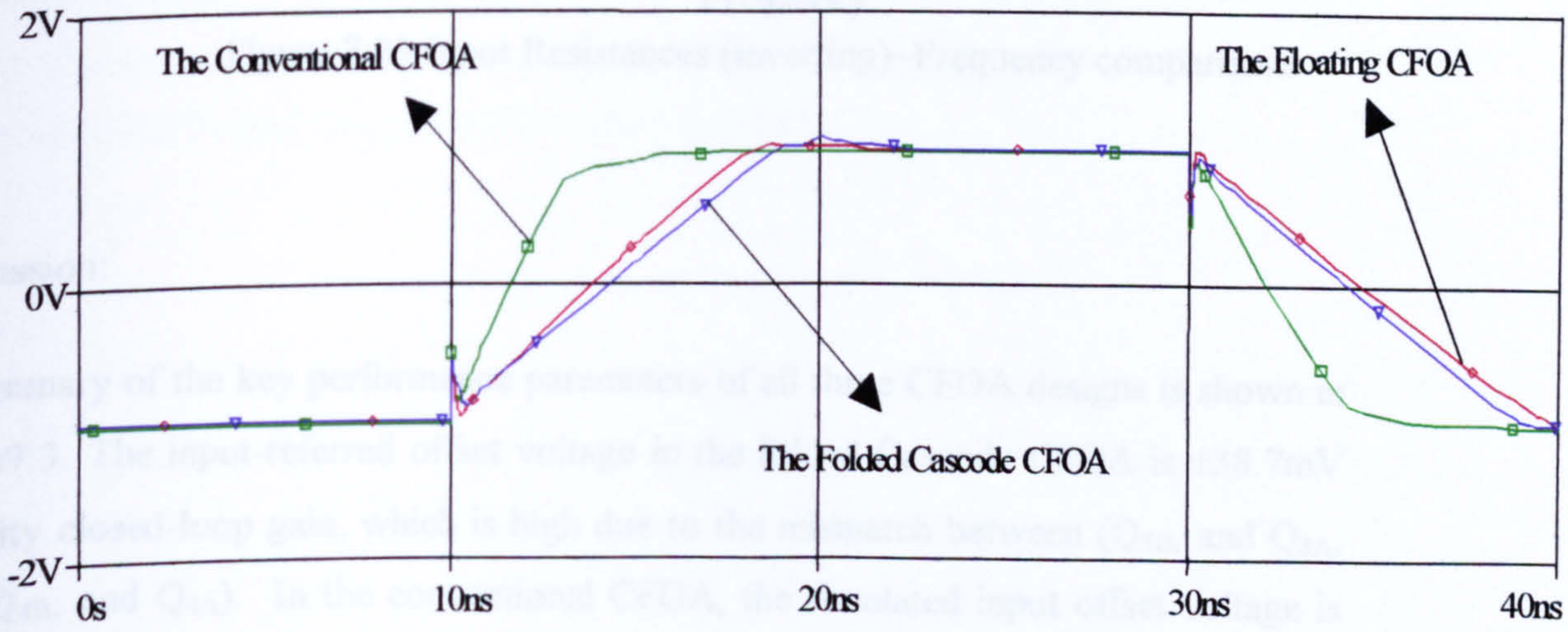


Figure 7.21 Transient response

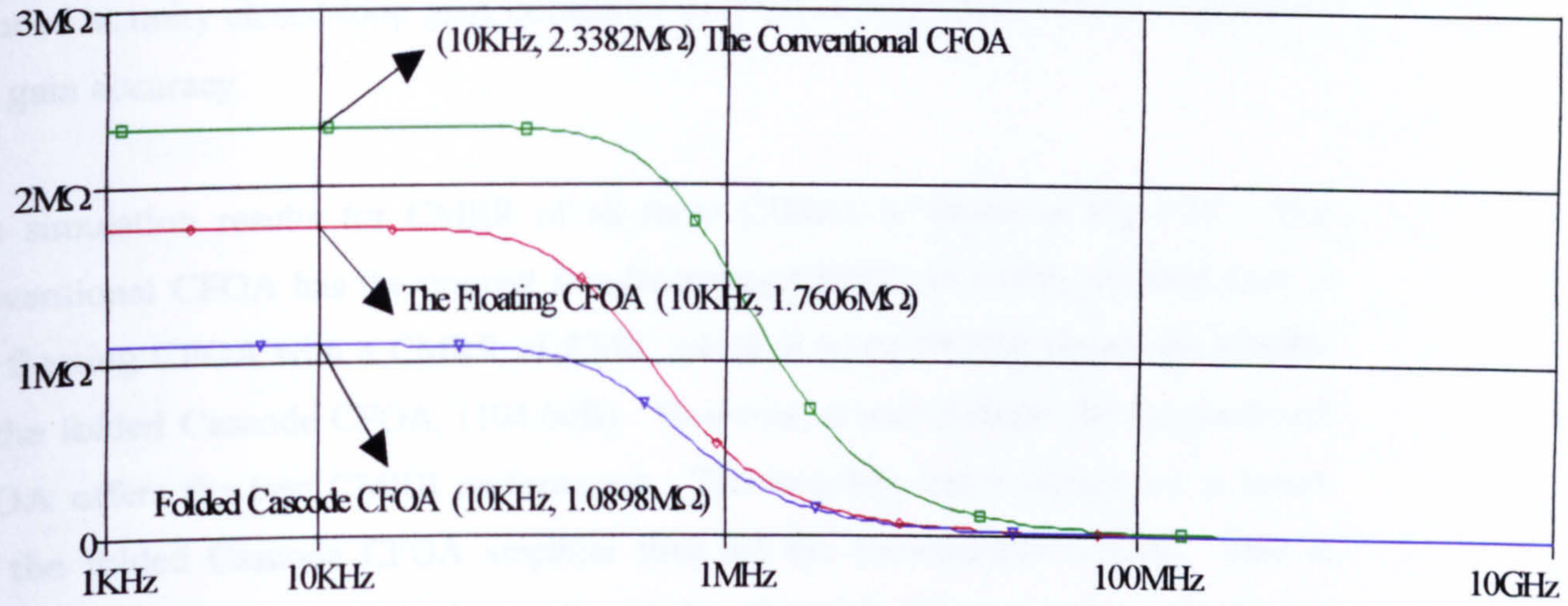


Figure 7.22 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

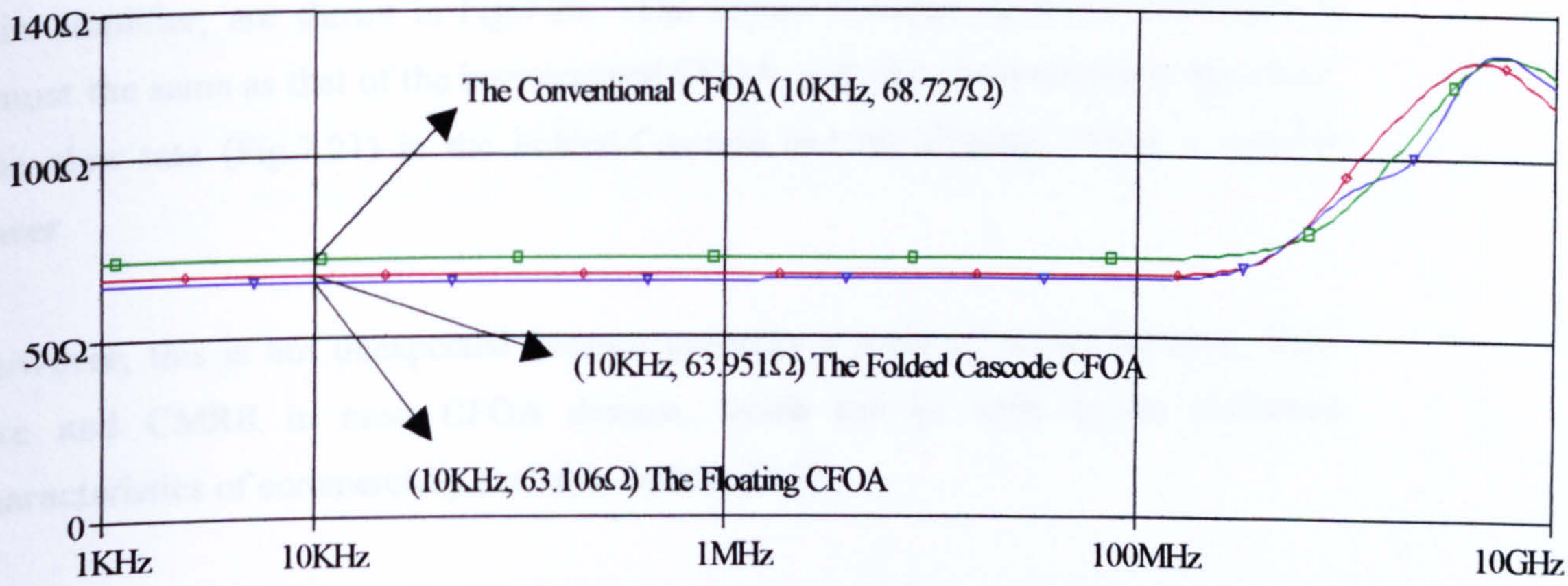


Figure 7.23 Input Resistances (inverting)~Frequency comparisons

Discussion:

A summary of the key performance parameters of all three CFOA designs is shown in Table7.3. The input-referred offset voltage in the folded Cascode CFOA is ±38.7mV at unity closed-loop gain, which is high due to the mismatch between (Q_{3B}, and Q_{3A}, and Q_{4B}, and Q_{4A}). In the conventional CFOA, the simulated input offset voltage is ±20.6mV, at unity closed-loop gain, and increases linearly with increasing closed-loop gain. A consequence of improving the CMRR is that the gain error has been

reduced at unity closed-loop gain, compared with the conventional CFOA counterpart AC gain accuracy.

The simulation results for CMRR of all three CFOAs is shown in Fig.7.18. The conventional CFOA has the poorest low-frequency CMRR, at 51dB; the next best is the floating CFOA with a CMRR of 87dB, which is some 18.5dB below the CMRR of the folded Cascode CFOA, (104.6dB). However, above 10MHz the conventional CFOA offers the best CMRR performance. The inverting input impedance is lower for the folded Cascode CFOA amplifier than for the conventional CFOA. This is indicated in Fig.7.23, which shows the relative inverting terminal input impedances for all three CFOAs.

The frequency responses of all three CFOAs, each configured as a unity closed-loop gain amplifier, are shown in Fig.7.20. The Folded-Cascode amplifier bandwidth is almost the same as that of the bootstrapped CFOA, with the conventional being lower. The slew-rate (Fig.7.21) in the Folded-Cascode and the floating CFOA is notably lower.

However, this is not unexpected because generally a trade-off exists between slew-rate and CMRR in most CFOA designs, which can be seen in the published characteristics of commercially available devices [7-7].

The non–inverting input stage of the conventional CFOA, and the bootstrapped CFOA designs is found to have a significantly better performance than the new CFOA with the Folded Cascode CFOA, (See Fig.7.22).

	CONVENTIONAL CFOA (5.1)	Floating CFOA (Fig 7.1)	Folded Cascode CFOA (Fig 7.17)
CMRR	51.4dB	87dB	104.6dB
Bandwidth	55.7MHz	63MHz	62.7MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	63.1Ω	63.9Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	1.76MΩ	1.1MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	0.5mV	0.5mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±3.3mV	±38.7mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =244.1V/μs SR– =213.6V/μs	SR+ = 232.9V/μs SR– = 223.2V/μs
Input dynamic range	–3V, +3V	–2V, +2V	–2V, +2V

Table 7.3 Characteristics of the Conventional and the Floating CFOA and the Folded Cascode CFOA for V_{CC}=±5V, I_{Q1}=0.2mA, and I_{Q2}=0.2mA

(7.5) The 'Quasi-Darlington' CFOA

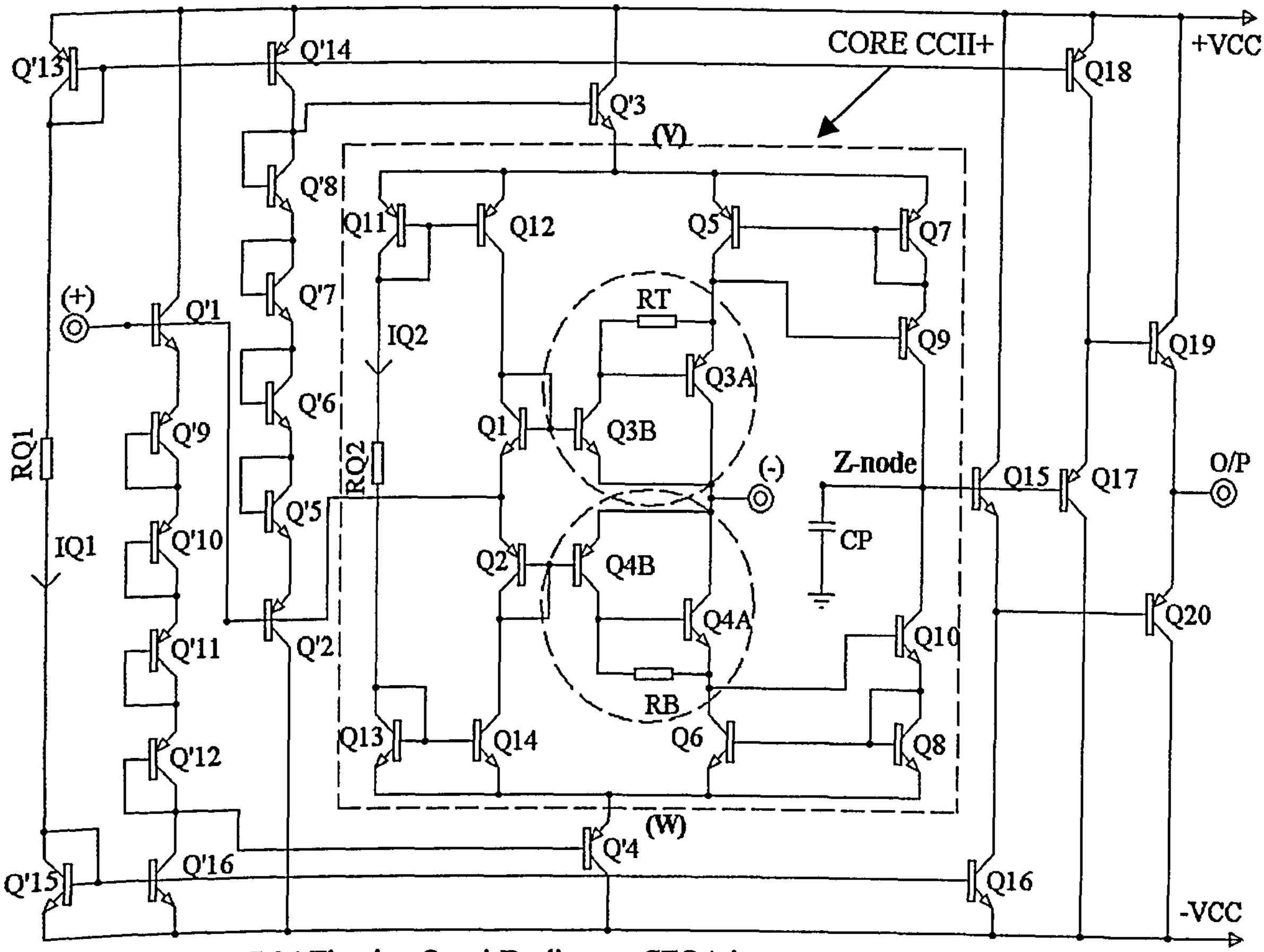


Figure 7.24 Floating Quasi-Darlington CFOA input stage CFOA

The CFOA is in reality a hybrid amplifier based on a combination of a voltage-follower and current-follower. In the CFOA design above (Fig.7.24), the conventional CFOA voltage-follower has been replaced by a floating buffer design together with a so-called 'Quasi–Darlington' stage to reduce the inverting input resistance, Rin(-), an analysis of which is presented in Appendix 7.1.

The core CCII+ in this new design has a simple topology, shown within the broken-line box. 'Quasi–Darlingtons' $Q_{3A/3B}$ and $Q_{4A/4B}$ are employed, instead of single transistors, to provide higher current gain and reduced inverting-input terminal impedance. The two resistors R_T and R_B bleed additional collector bias current from

the collector circuits of Q_5, Q_6 respectively, to optimize the high frequency performance of the quasi-Darlingtons.

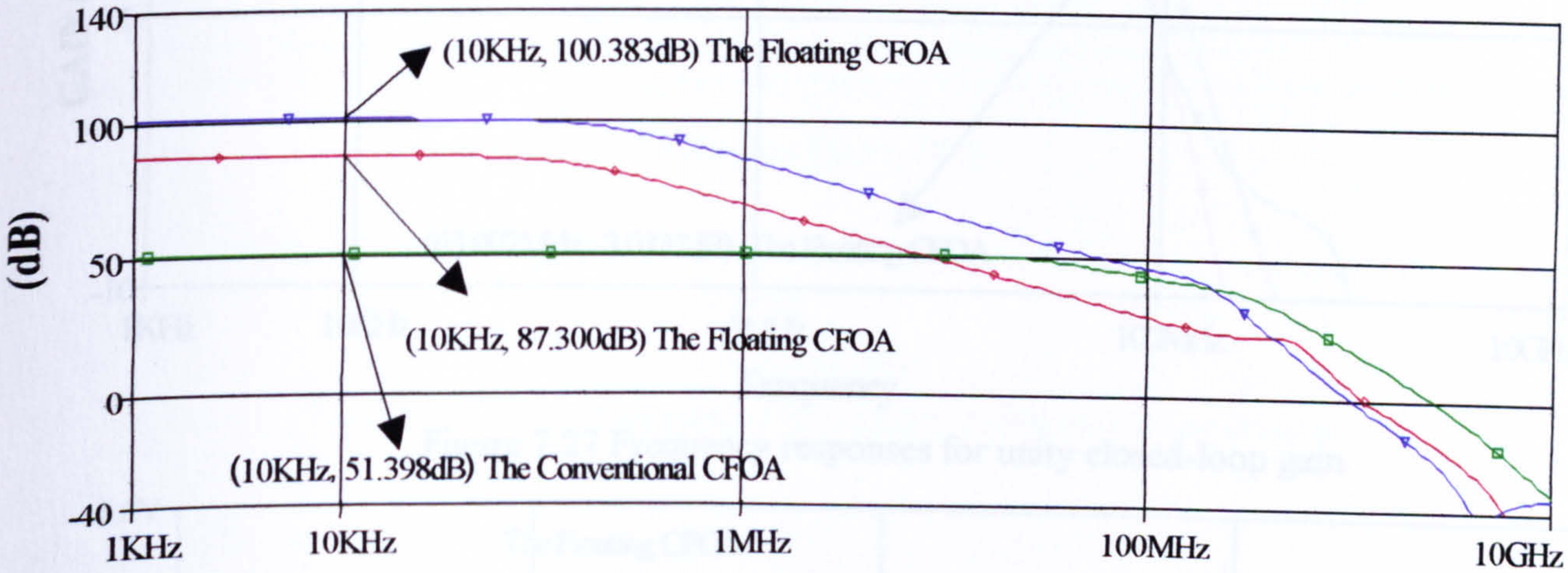


Figure 7.25 CMRR~Frequency

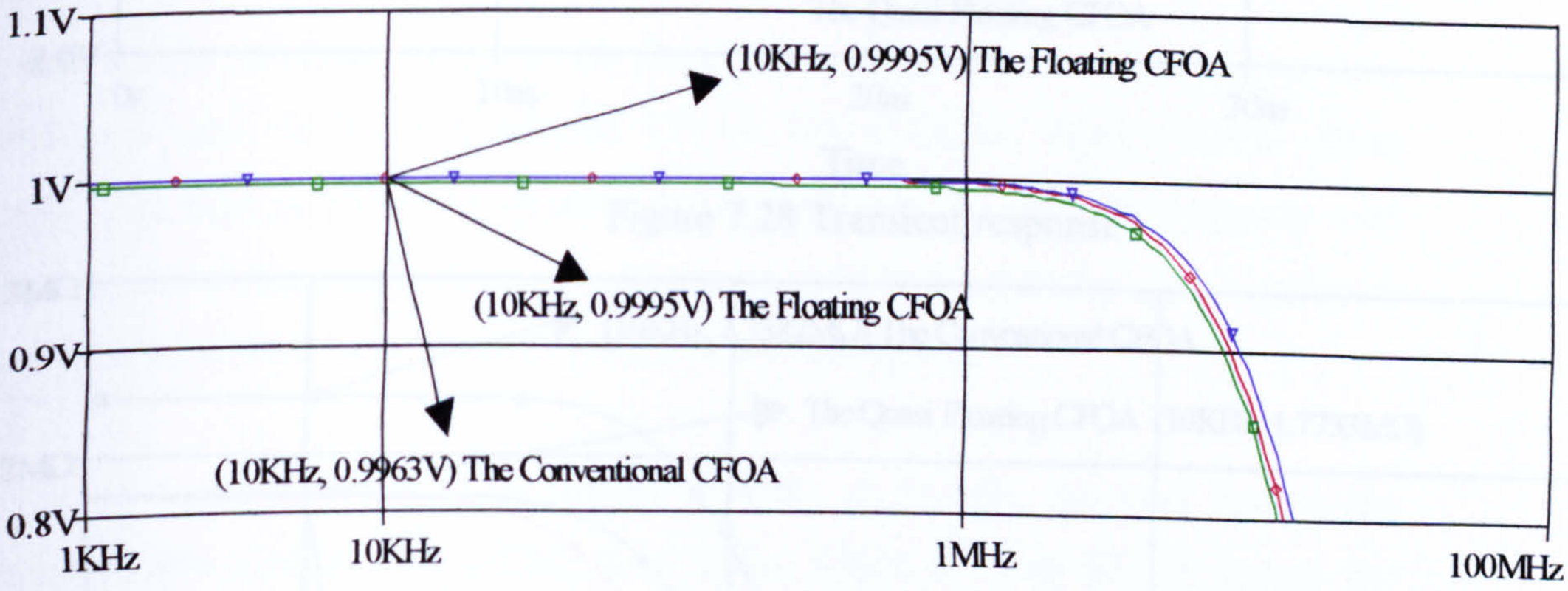


Figure 7.26 AC gain accuracy ~ Frequency

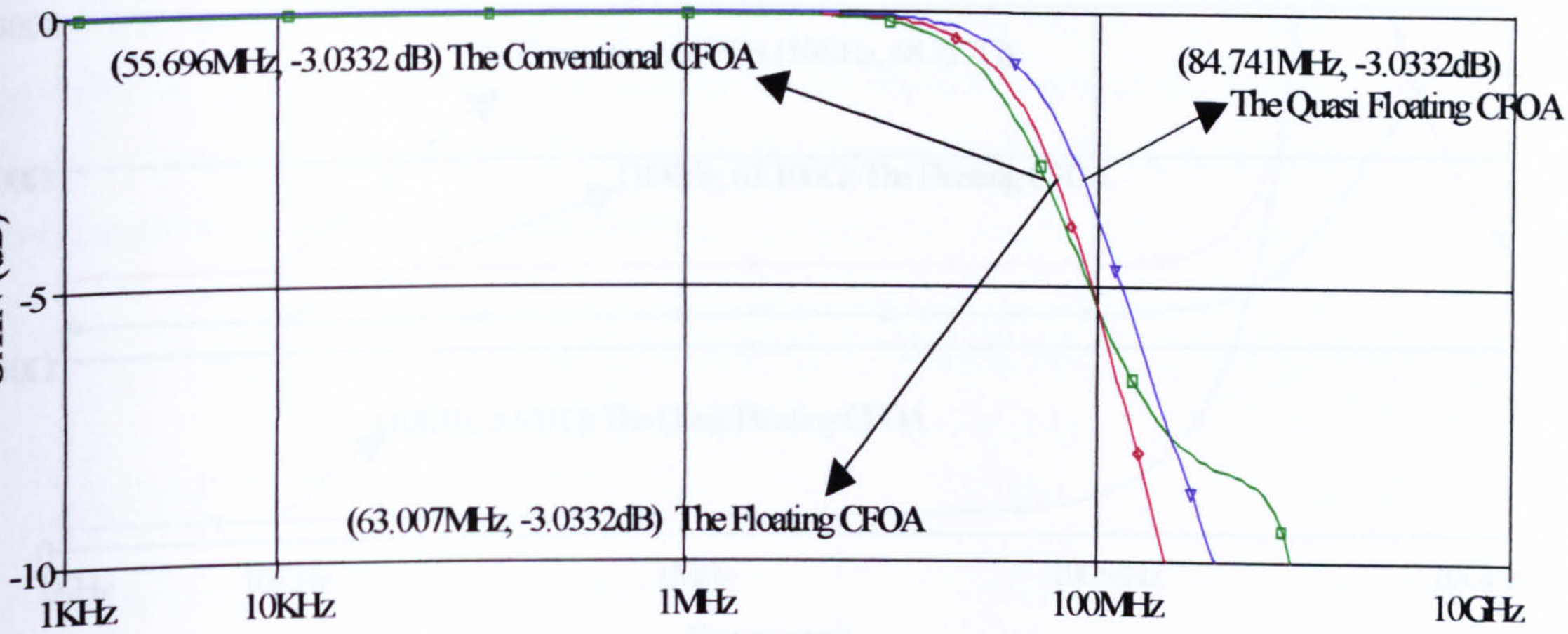


Figure 7.27 Frequency responses for unity closed-loop gain

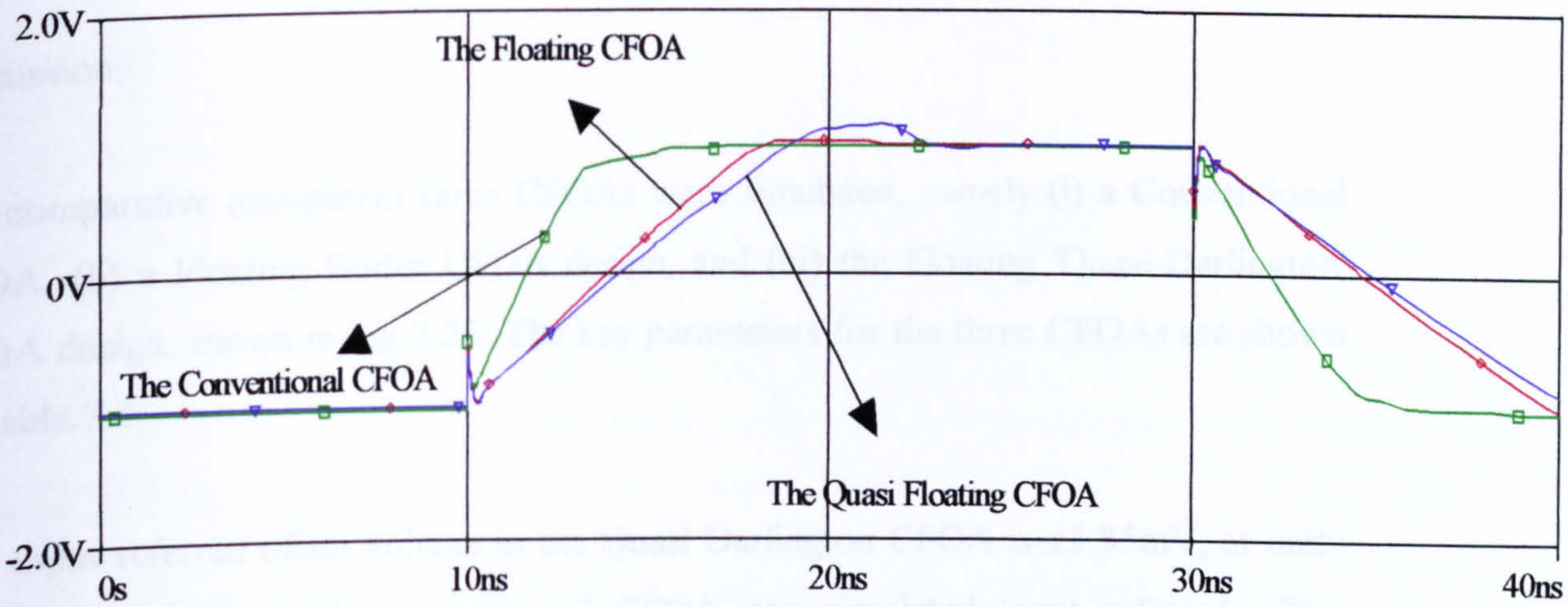


Figure 7.28 Transient response

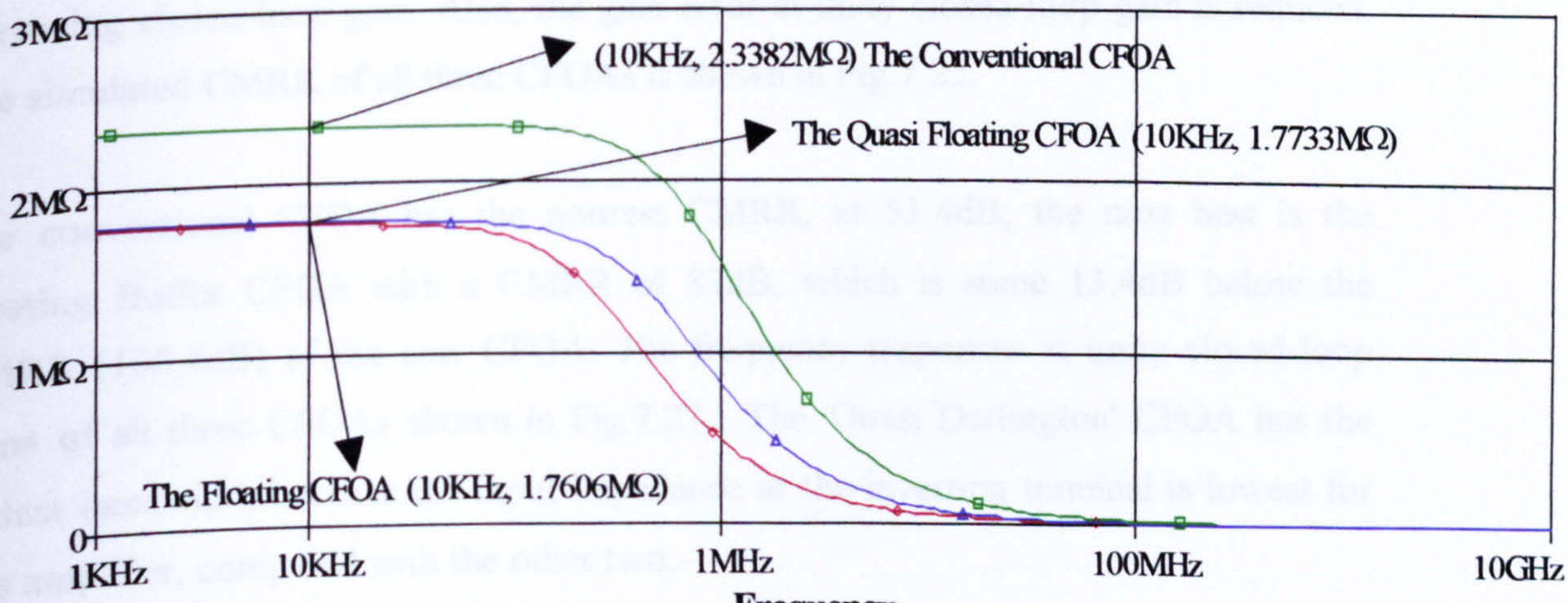


Figure 7.29 Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier

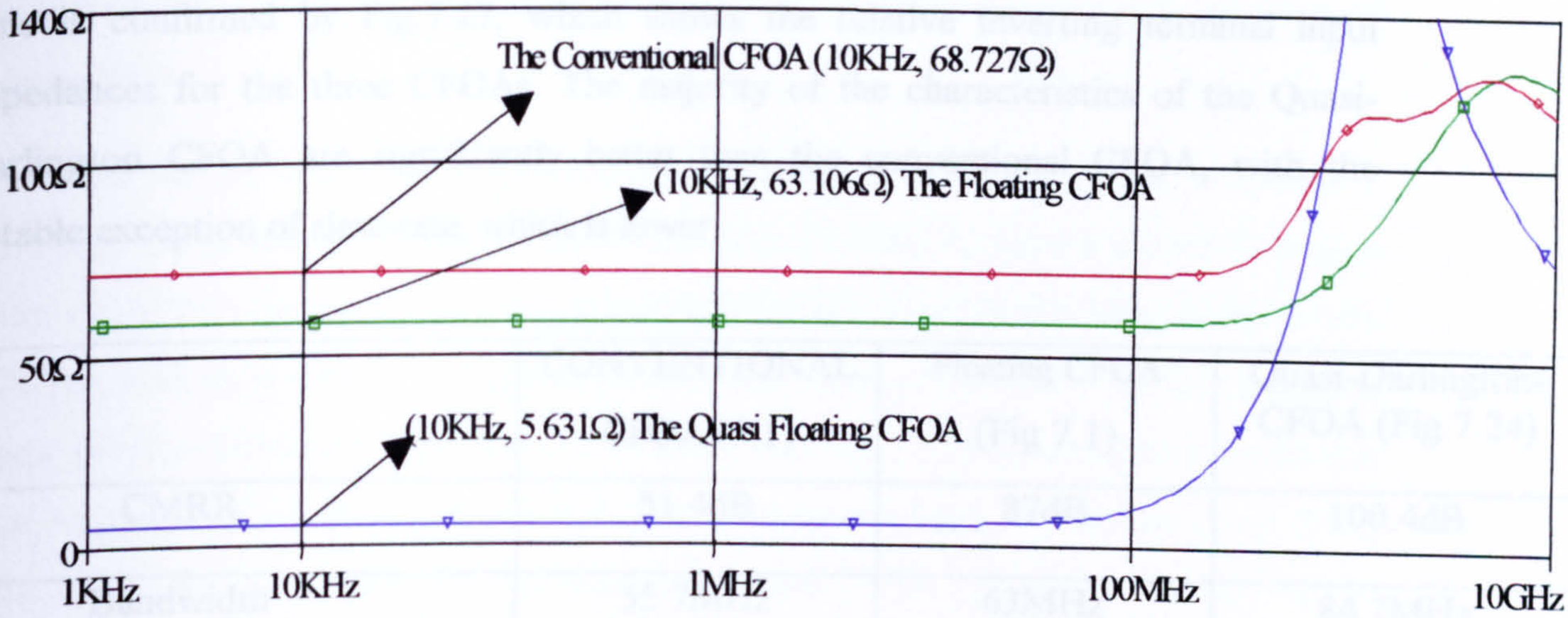


Figure 7.30 Input Resistances (inverting)~Frequency comparisons

Discussion:

For comparative assessment three CFOAs were simulated, namely (i) a Conventional CFOA, (ii) a Floating Buffer CFOA design, and (iii) the Floating 'Quasi-Darlington' CFOA design, shown in Fig.7.25. The key parameters for the three CFOAs are shown in Table.7.4.

The input referred offset voltage in the Quasi Darlington CFOA is ±3.85mV, at unity closed-loop gain. In the conventional CFOA, the simulated input referred offset voltage is as high as ±20.6mV, at unity closed-loop gain, and increased linearly with increasing closed-loop gain. Also, the gain-error at unity closed-loop gain is reduced. The simulated CMRR of all three CFOAs is shown in Fig.7.25.

The conventional CFOA has the poorest CMRR, at 51.4dB; the next best is the Floating Buffer CFOA with a CMRR of 87dB, which is some 13.4dB below the CMRR (100.4dB) of the new CFOA. The frequency responses at unity closed-loop gains of all three CFOAs shown in Fig.7.27. The 'Quasi Darlington' CFOA has the widest bandwidth because the input impedance at the inverting terminal is lowest for this amplifier, compared with the other two.

This is confirmed by Fig.7.27, which shows the relative inverting terminal input impedances for the three CFOAs. The majority of the characteristics of the Quasi-Darlington CFOA are significantly better than the conventional CFOA, with the notable exception of slew-rate, which is lower.

	CONVENTIONAL CFOA (5.1)	Floating CFOA (Fig 7.1)	Quasi-Darlingtons CFOA (Fig 7.24)
CMRR	51.4dB	87dB	100.4dB
Bandwidth	55.7MHz	63MHz	84.7MHz
Inverting input resistance (at 0V d.c. input)	68.7Ω	63.1Ω	5.6Ω
Non-inverting buffer input resistance (at 0V d.c. input)	2.3MΩ	1.76MΩ	1.77MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.7mV	0.5mV	0.5mV
Input offset voltage (at 0V d.c. input)	±20.6mV	±3.3mV	±3.85mV
Slew rates	SR+ =569.6V/μs SR– =454.2V/μs	SR+ =244.1V/μs SR– =213.6V/μs	SR+ = 215.6V/μs SR– = 200.6V/μs
Input dynamic range	–3V, +3V	–2V, +2V	–2V, +2V

Table 7.4 Characteristics of the Conventional and the Floating CFOA and the Quasi-Darlington CFOA for V_{CC}=±5V, I_{Q1}=0.2mA, and I_{Q2}=0.2mA

Summary

Since the CFOA has one single gain stage compared with the VOA, therefore it exhibits a much lower equivalent open-loop gain. In order to have a closed-loop gain accuracy, a high open-loop gain or transimpedance is a must. In this chapter three new CFOAs, with improved CMRR performances have been presented. The first design is based on two previously reported CFOA designs **[7-1], [7-2]**. In comparison with the conventional CFOA, the input referred offset voltage has been reduced by about 85%, the CMRR has been increased significantly by some 51dB. Also, the majority of the other characteristics have been improved, with the notable exception of the slew-rate, which has been reduced to about 60% of the conventional CFOA design.

The second design is based on floating input stage and uses a Folded Cascode architecture. The folded cascode was used rather than a simple cascode to ensure that headroom is not lost. In comparison with the conventional CFOA, the CMRR increased significantly by some 53dB. Also, A.C. gain error has been improved at a unity gain, as has the input dynamic range. However, these improvements have been at the expense of a reduction in some parameters, most notably the slew-rate performance.

Finally, a third design based on Floating input stage architecture with 'Quasi-Darlington' transistors with good D.C. and CMRR performance is presented. Early-effects in the input stage of the conventional CFOA limit CMRR, PSRR and D.C. performance, in the input stage to reduce the influence of the Early-effect resulting in improved performance.

Another advantage of this design is that the inverting input impedance is reduced significantly which results in further improvements in the CMRR, the bandwidth and the input referred offset. In comparison with the conventional CFOA, the input bandwidth has been increased to about 35%, the CMRR increased significantly by some 50dB.

Also, the closed-loop unity gain accuracy has been improved, and most of the other characteristics such as input offset voltage and inverting input terminal input impedance has been reduced to 5.6Ω. However, these improvements have again been at the expense of a reduction in slew-rate performance though the slew-rate in the new CFOA is still more than adequate for many CFOA application requirements. However, the trade-off between the slew-rate and the CMRR has been overcome in the designs presented in Chapters Five, and Six.

The primary disadvantage of the new CFOA designs is that moderately high power-supply voltages are required, because of vertical transistor-stacking. We cannot achieve a high voltage gain in the floating circuit since all nodes have the same voltage, but we can obtain a current gain from the floating circuit.

(7.6) References

[7-1] F J Lidgey, W J Su and K Hayatleh. 'Novel current-feedback operational amplifier design based on a floating circuit technique', IEE Colloquium on Analogue Signal Processing', Oct1998, Oxford, pp. 9/1–94

[7-2] Vere Hunt M.A, 'Design and development of a high slew-rate operational amplifier', PhD thesis, Oxford Brookes University, 1992, pp. 76–92.

[7-3] P R Gray and R G Meyer, 'Analysis and Design of Analog Integrated Circuits', Wiley, 3rd Edition, 1993, pp. 465-478-623.

[7-4] Wenjun, Su, 'Design and development of high CMRR wide bandwidth instrumentation Amplifiers', PhD thesis, Oxford Brookes University, 1997, pp. 93–118.

[7.5] F J Lidgey and W J Su, 'High accuracy, high speed voltage–follower', IEEE Proceedings of ISCAS' 1998, ref 0-7803-4455-3/98

[7-6] G R Wilson, 'A monolithic junction FET-NPN operational amplifier', IEEE JSCC, December 1968, Vol SC-3, pp.341-348.

[7-7] Elantec Inc., 'EL2020C 50MHz current feedback amplifier, ' Datasheet,1996 Tarob Court, Milpitas, CA 95035, USA.

APPENDIX 7

APP 7.1 Calculation the output impedance of the Quasi-Darlington

APP 7.1 Calculation the output impedance for the Quasi-Darlington

Fig A 7.1 shows the equivalent circuit for calculation of the output resistance of the equivalent 'Quasi Darlingtion', including the resistor R_T.

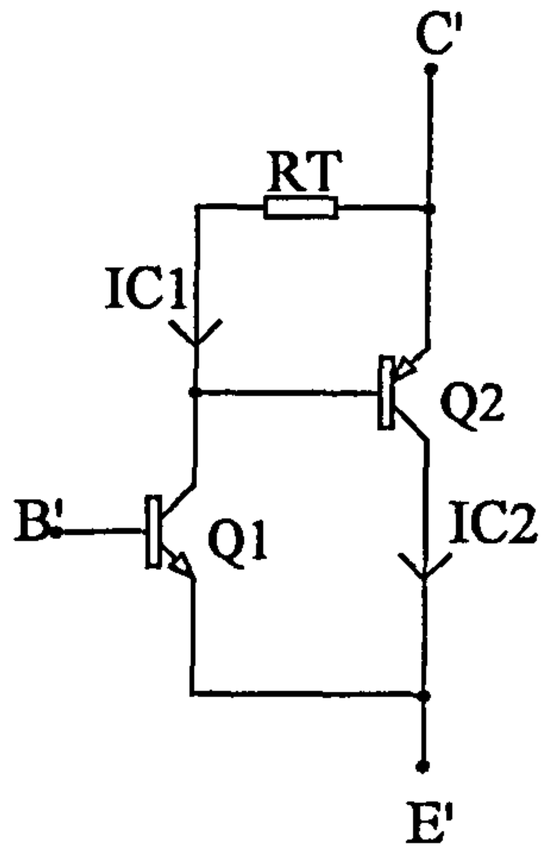


Figure A 7.1

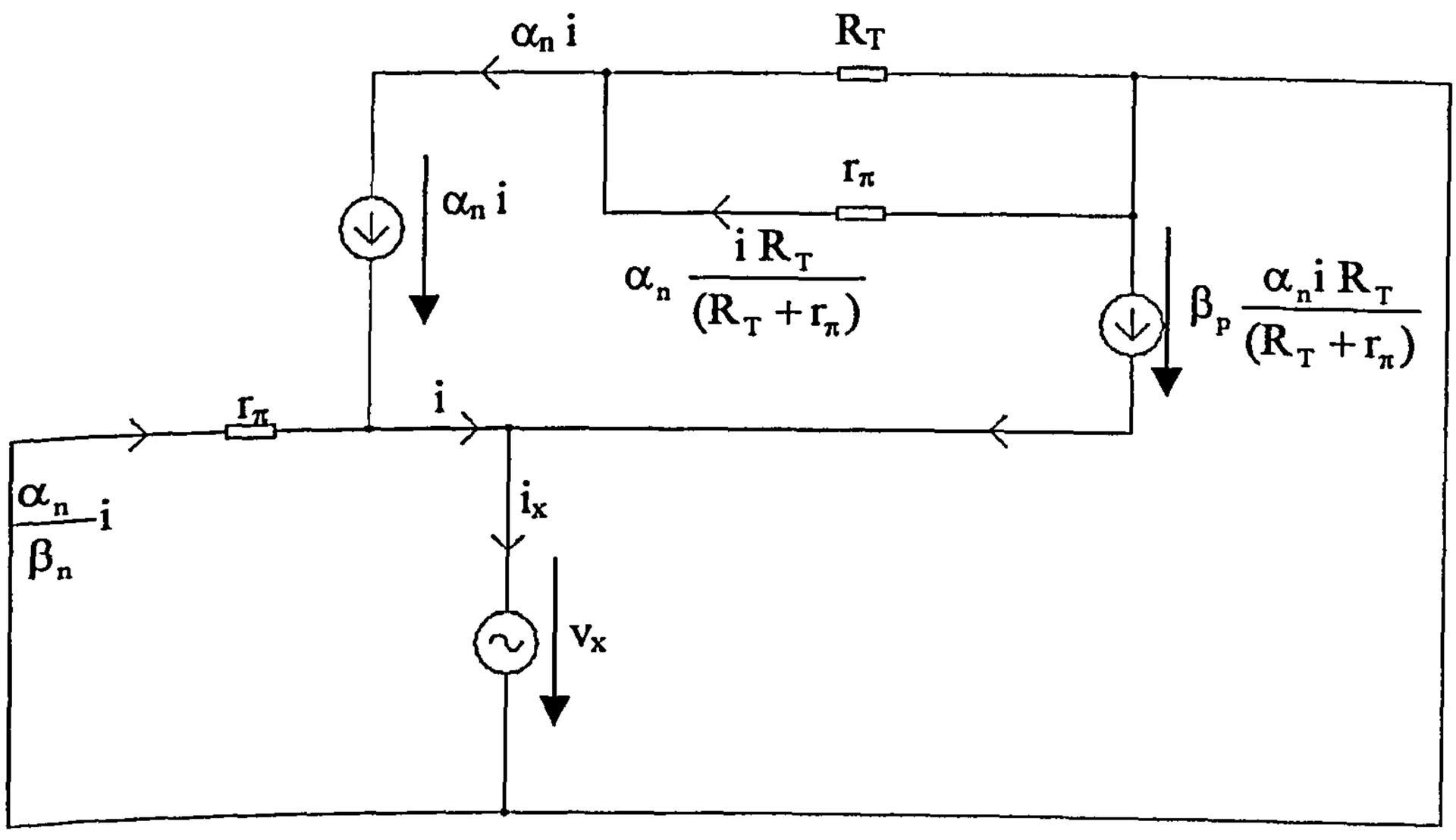


Figure A 7.2

$$i_x = i\left[1+\beta_p \frac{\alpha_n R_T}{(R_T + r_\pi)}\right]$$

But $r_\pi \frac{\alpha_n}{\beta_n} i = v_x$

Or, $i = \frac{v_x}{r_\pi} \frac{\beta_n}{\alpha_n}$

$$\therefore\ i = \frac{v_x}{r_\pi} \frac{\beta_n}{\alpha_n}[1+\frac{\beta_p \alpha_n R_T}{(R_T + r_\pi)}]$$

$$\therefore\ i = \frac{v_x}{\beta_n} \frac{g_m \beta_n}{\alpha_n}[1+\frac{\alpha_n \beta_p R_T}{(R_T + r_\pi)}]$$

because $\frac{1}{r_\pi} = \frac{g_m}{\beta}$

$$\therefore\ (\frac{v_x}{i_x}) = r_o\ (\text{with F.B}) = [\frac{\frac{\alpha_n}{g_m}}{1+\frac{\alpha_n \beta_p R_T}{(R_T + r_\pi)}}]$$

This is of the form,

$$r_o\ (\text{with F.B}) = \frac{r_o\ (\text{without F.B})}{[1+|L.G|]}$$

where, $|L.G|$=Magnitude of loop gain $=\dfrac{\alpha_n \beta_p R_T}{(R_T + r_\pi)}$.

Substituting V_T=25.8mV, I_{CQ3A}=0.1mA, β_p=53.52, R_T=3.9KΩ, assuming α_n=0.9816, gives $r_o \approx$11.571Ω.

CHAPTER 8

Thesis Conclusions

For many years the VFOA featured prominently in the design of analogue signal processing systems but, in the 1980s, the requirements of certain sections of the telecommunications industry saw the emergence of the CFOA having a high slew-rate and a wide bandwidth that was almost independent of closed-loop voltage gain. However, currently established CFOA designs exhibit a CMRR that are only modest compared with that possible with VFOAs. That shortcoming is overcome in several new and novel CFOA designs presented in this thesis.

Although all of the CFOA parameters the design electronic engineer may wish to measure can be quantified by direct measurement, this is not always convenient, and straightforward. Chapter Two illustrates a simple computer simulation test/measurement that can be used as an approximation to, or indirect measure of, the desired parameter of CFOA. In all of the following tests, and testing in general, the test conditions were specified, and defined so that repeatable results could be obtained in later Chapters (Six and Seven), and meaningful comparisons made. This includes factors such as resistive and capacitive loading.

In Chapter Three the author follows an investigation and evaluation of the conventional CFOA archecitecture and identifies the main reasons for the internal limitation of several parameters that includes the following study: of the D.C. input current and linear voltage range; input offset-voltage, quiescent power dissipation; the input and output small-signal impedances; analysis of differential-mode operation, and finally the analysis of common-mode operation. These results were used to

inform the development of several new architecture CFOA designs which addresses the short-comings speciffically in terms of the CMRR. The new CFOA provide significant improvements to this paramter.

Chapter Four presents further reviews, and studies on the basic theory of the conventional CFOA in terms of the closed-loop output impedance, the closed-loop low-frequency and DC behaviour, the closed-loop frequency response and the slew-rate. This data is used later in the thesis as a bench-mark for performance comparisons.

Chapter Five considers the trade-offs involved in the design of the new input stages intended to improve the performance of a CFOA, over that possible using an established input circuit configuration, with respect to three major characteristics, *viz.*, CMRR, offset-voltage and slew-rate. Also included in this Chapter is a detailed review of several current-sources/mirrors, because of their importance as building-blocks within the field of CFOA design.

Chapter 6 presents several new designs and performances of the new CFOAs, which are based on employing the 'reverse' bootstrapping technique, 'forward' bootstrapping technique, and a combination of the both previous techniques using bipolar junction transistors, for use in applications such as video line driving. In comparison with the conventional CFOA, the CMRR increased significantly, by almost +47dB in some designs. The frequency response of the new CFOA circuits demonstrates that for a unity closed-loop gain the available bandwidth is at least 108MHz greater than that of the conventional CFOA constructed with the same semiconductor technology. Moreover compared with the established CFOA, the input referred offset voltage has been reduced by ±19.85mV, and the slew-rate increased by approximately (SR = +381V/μs and -116.2V/μs). Also, AC gain-error has been improved at a unity gain, by 2.7mV.

However, these improvements have been at the expense of a moderately higher power supply voltage requirement, although the input dynamic range is still more than adequate for typical CFOA application requirements.

Finally, Chapter 7 presents a family of designs all of which use an overall bootstrapping technique with folded cascode, and quasi-Darlingtons in the input stage to reduce the influence of the Early-effect. This resulted in an improved performance, in particular CMRR which increased significantly by almost +54dB in the case of bootstrapping technique with folded cascode. Another advantage of using the overall bootstrapping technique with quasi-Darlingtons is that the inverting input impedance is reduced significantly which results in further improvements in the CMRR, the closed-loop bandwidth and the input-referred offset.

(8.1) Future work

Slew-rate limiting is a major cause of distortion in high-frequency amplifiers that are handling large amplitude output signal levels, such as in video signal processing applications. But, comparing the CFOA to the VOA, which inevitably uses higher collector-current bias values with emitter degeneration there is less the relative input-referred noise **[8-1]**.

The author did not tackle the input-referred noise performance of the CFOAs for two reasons. Firstly, the conventional CFOA has a lower figure of input-referred noise due it is topology, as direct result of the use of current as the feedback error signal. Secondly, the author uses a very small biasing current throughout the analysis and the designs in this thesis, which is in the range I_Q = 0.1mA to 0.7mA. Thus the input-referred noise will typically be in the region of (2 to 3 $nV/\sqrt{Hz}$) **[8-2]**, and is therefore not likely to be significant in most CFOA applications. Nevertheless, a detailed study of noise performance was beyond the scope of this research project although it would be of interest to explore the relative noise performance of the new designs presented.

Finally, several of the new designs presented in this thesis have been fully verified by analysis and simulation, and in most aspects the performances are significantly better than the conventional CFOA. The designs techniques are fully articulated and the next step for future work is to realise these designs in silicon.

(8.2) References

[8-1] F J Lidgey, and K Hayatleh. 'Current-feedback operational amplifier and applications', IEE, Electronics & Communication Engineering Journal, Aug1997, pp. 176–182.

[8-2] Analog Devices, Inc., 'AD8072/AD8073: Current feedback amplifiers', Data sheet, USA, 2002, pp. 1-12.

REFERENCES IN ALPHABETICAL ORDER

Reference list

[1-2] Analog Devices, Inc., 'Linear Design Seminar', USA, October, 1987, pp.II-1-II-16.

[8.2] Analog Devices, Inc., 'AD8072/AD8073: Current feedback amplifiers', Data sheet, USA, 2002, pp.1-12.

[2-7] Boylestad R.L, Nashelsky L, 'Electronic Devices and Circuit Theory', Prentice Hall International, Inc., USA, 7th Edition, 1999, pp.630-633.

[1-14] 'CCII01 Current Conveyor Amplifier', Data sheet. LTP Electronics Ltd., Oxford, UK, 1993.

[6.3] D. Smith, *et. al.*,: "Evolution of high-speed op-amp architectures," IEEE J. Solid-State Circuits, Vol.29, No.10, pp. 1166-1179, October 1994.

[7.7] Elantec Inc., 'EL2020C 50MHz current feedback amplifier,' Datasheet,1996 Tarob Court, Milpitas, CA 95035, USA.

[1.12] Elantec Inc., 'EL2020C 50MHz current feedback amplifier, ' datasheet,1996 Tarob Court, Milpitas, CA 95035, USA.

[1-11] F J Lidgey, and K Hayatleh. 'Current-feedback operational amplifier and applications', IEE, Electronics & Communication Engineering Journal, Aug1997, pp.176–182.

[7.1] F J Lidgey, W J Su and K Hayatleh. 'Novel current-feedback operational amplifier design based on a floating circuit technique', IEE Colloquium on Analogue Signal Processing', Oct., 1998, Oxford, pp. 9/1–94

[7.5] F J Lidgey and W J Su, 'High accuracy, high speed voltage–follower', IEEE Proceedings of ISCAS 1998, ref 0-7803-4455-3/98

[8.1] F J Lidgey, and K Hayatleh. 'Current-feedback operational amplifier and applications', IEE, Electronics & Communication Engineering Journal, Aug., 1997, pp. 176–182.

[1-7] Franco S, 'Current-feedback amplifiers benefit high-speed designs', EDN, January 5, 1989, pp.161-172.

[2-2] Franco S, 'Design with operational amplifiers and analog integrated circuits', McGraw-Hill Companies, Inc, 3rd Edition, 2002, pp.71-79.

[1-5] Graeme J.G, Tobey G.E, Huelsman L.P, 'Operational amplifiers design and applications', Burr-Brown Research Corporation, USA, 1971, p.xvii.

[2-4] Gray P.R, Meyer R.G, 'Analysis and Design of Analog Integrated Circuits', John Wiley & Sons, Inc., Canada, 1984, pp.208-362.

[3.3] Gray, P. R., and Meyer R. G., 1993, Analysis and Design of Analog Integrated Circuits, 3rd Edition (New York: Wiley).

[5.4] Gray, P. R., and Meyer R. G., 1993, 'Analysis and Design of Analog Integrated Circuits', (Wiley, 3rd Edition), pp. 269–353.

[7.6] G R Wilson, 'A monolithic junction FET-NPN operational amplifier', IEEE JSCC, December 1968, Vol SC-3, pp.341-348.

[1-10] Harold P, 'Current-feedback op amps ease high-speed circuit design', EDN, July 7, 1988.

[2-3] Hart B.L, 'Common-mode rejection explained', Wireless World, September 1983, pp.36-38.

[1-4] Hart B.L, 'Current feedback operational amplifiers: A tutorial', International Journal of Electrical Engineering Education. Vol. 32, no. 2, April 1995, pp. 108-23.

[1-1] IEEE Annals of History of Computing, July-September 1985 (Vol.7, No. 3)

[4.2] Introduction to Electronics; Gray. P. E., John Wiley, New York 1967, Chapter 5, pp. 183-195.

[1-13] Krabbe H, 'A high performance monolithic instrumentation amplifier', ISSCC Dig. Tech. Tech. Papers, Feb.1971.

[3.2] Lidgey, F. J., Su, W. J., and Hayatleh, K., Oct1998, 'Novel current-feedback operational amplifier design based on a floating circuit technique'. IEE Colloquium on Analogue Signal Processing', Oxford, 9/1-94.

[2-1] Lunn C, 'The Essence of Analog Electronics', Prentice Hall Europe, 1997, pp 60-62.

[6.1] M. A. Vere Hunt, and F. J. Lidgey, "A high slew-rate voltage-mode op-amp," Proc. International Symposium on Circuits and Systems (ISCAS), San Diego, pp.2872-2875, 1992.

[2-5] Maddock R.J, Calcutt D.M, 'Electronics for Engineers', Longman Scientific & Technical, UK, 2nd Edition, 1994, pp.514-590.

[7.3] P R Gray and R G Meyer, 'Analysis and Design of Analog Integrated Circuits', Wiley, 3rd Edition, 1993, pp. 465-478-623.

[1-3] Roon T.V, Operational Amplifier http://www.uoguelph.ca/~antoon/gadgets/741/741.html

[2-6] Sedra A.S, Smith K.C, 'Microelectronic Circuits', Oxford University Press, UK, 4th Edition, 1998, pp.28-47.

[5.3] Sedra, A. S., and Smith K. C., 1998, 'Microelectronic Circuits', (Oxford University Press, 4th Edition), pp. 485–631.

[4.1] Seevinck, E, Wassenaar, R.F, Leeuwen, M.G.van, Boom, G, Holle, E and Wal, R.Vande, 'Wide band voltage to current converter circuit', Dig. Tech. Papers European Solid State Conference. (ESSCIRC, Toulouse, France), Sept. 1985, pp. 108-112.

[5.1] S. Franco, 'Design with Operational Amplifiers and Analog ICs,' Mc Graw Hill, 3rd Edition, Chapter 6, p. 294, 2002.

[1-15] Smither M.A, Pugh D.R, and Woolard L.M, 'CMRR analysis of the 3 op-amp instrumentation amplifier', IEE Electronics Letters, Vol.13, August 1977.

[1-9] Soliman A.M, 'Design of high-frequency amplifiers', IEEE Circuits and Systems, June 1983.

[1] Tammam A.A, Hayatleh K, and Lidgey F.J, 'Novel high performance Current-Feedback op-amp', IEEE Proceedings of International Symposium on Circuits and Systems, Arizona, USA, May 2002, pp.705-708.

[2] Tammam A.A, Hayatleh K, and Lidgey F.J, 'High performance Current Feedback operational amplifier design', IEEE Proceedings of IEE ASP2002, Oxford, UK, 2002, pp.12-1-12-6.

[3] Tammam A.A, Hayatleh K, and Lidgey F.J, 'High CMRR Current-Feedback operational amplifier', International Journal of Electronics, 2003, Vol.90, No. 2, pp. 87-97.

[4] Tammam A.A, Hayatleh K, Hart B, and Lidgey F.J, 'A new Current-Feedback operational amplifier with a high CMRR', IEE Electronics Letters, 2003, Vol.39, No.21, p.1483.

[5] Tammam A.A, Hayatleh K, Hart B, and Lidgey F.J, 'High performance Current Feedback op-amps', IEEE Proceedings of International Symposium on Circuits and Systems, Vancouver, Canada, May 2004, pp.825-828.

[6] Tammam A.A, Hayatleh K, Hart B, and Lidgey F.J, 'A hierarchy of input stages for Current Feedback operational amplifiers', IEEE Proceedings of International Symposium on Circuits and Systems, Vancouver, Canada, May 2004, pp.821-824.

[1-6] Truitt. T.D, and Rogers,A.E , 'Basics of Analog Computers', International John F. Rider Publisher Inc. 1960.

[3.1] Vere-Hunt, M. A., and Lidgey, F. J., 1991, 'A novel transconductance cell. Proceedings of the European Conference on Circuit Therory and Design' (ECCTD), pp. 1341–1348.

[5.2] Vere Hunt, M. A., Charles K. 'Design and development of a high slew-rate operational amplifier.' Ph.D Thesis. Oxford Brookes University, 1992. pp 33–55.

[5.5] Vere Hunt M.A, 'Design and development of high slew-rate operational amplifier', PhD thesis, Oxford Brookes University, 1992, pp 45–46.

[7.2] Vere Hunt M.A, 'Design and development of high slew-rate operational amplifier', PhD thesis, Oxford Brookes University, 1992, pp76–92.

[6.2] Wenjun, Su. 1997, "Design and development of high CMRR wide bandwidth instrumentation Amplifiers", PhD thesis, Oxford Brookes University.

[7.4] Wenjun, Su, 'Design and development of high CMRR wide bandwidth instrumentation Amplifiers', PhD thesis, Oxford Brookes University, 1997, pp. 93–118.

[1-8] Wong J, 'Current-feedback op-amps extend high-frequency performance', EDN, October 26, 1989, pp.211-216.

PUBLICATIONS BY THE AUTHOR

PAGE/PAGES
EXCLUDED
UNDER
INSTRUCTION
FROM
UNIVERSITY