CMOS/Bipolar Current Conveyor Design and Development

by

Anthony John Robinson

School of Technology
Oxford Brookes University

A thesis submitted in partial fulfilment of the requirements of Oxford Brookes University for the degree of

Doctor of Philosophy

September 2007

Abstract

The aim of this research programme was to design and develop a novel CMOS current conveyor, to improve areas such as bandwidth, slew rate, gain, and Power Supply Reject Ratio (PSRR). The current conveyor can be used in low frequency applications such as LED drivers for mobile phones and televisions, and high frequency applications such as mixers for up/down converters used in anything from radios to mobile phones.

The initial part of the research looked into improving the Power Supply Rejection Ration (PSRR) of the current follower (mirror) by increasing its output impedance. Several types of current mirror were compared using analytical and simulation methods, using a new generic low frequency transistor model which was used to highlight the differences in impedance between BJT and CMOS current mirrors. It was found that the best type of mirror was the regulated cascode current mirror which offered the largest value of output impedance when built from CMOS transistors.

Work then moved onto the voltage follower. By initially using a typical CMOS source follower, it was found that the voltage gain suffered from low values transconductance, drain/source resistance, and a larger than expected value of source resistance, which was extracted from simulation and was found to be around 300-350Ω. The best design was a two stage un-buffered amplifier which offered the best Power Supply Rejection (PSRR) voltage gain and bandwidth.

Several different types of current conveyor (CCII+) were simulated and the results were compared. It was found that the best types of current conveyor were the cascode type conveyors which offered a voltage gain error of less than 1%. The regulated cascode type current conveyor offered the highest figure of PSRR that of around 60dB.

Finally the new cascode type current conveyors were used to build examples of current feedback operational amplifiers (CFOAs), and the cascode type CCII+ offered a voltage gain error of less than 1%, largest bandwidth and best PSRR.

Acknowledgements

I would like to thank my supervisor Prof. John Lidgey and Dr. Khaled Hayatleh for their guidance and support, and Maxim Integrated Products (UK) Ltd for sponsoring me to finish this thesis. Finally special thanks are due to my wife and my friends for their long lasting support throughout this research project.

Original work

There have been several areas of original work in this thesis, a summary is shown below:

i) Chapter Two analyses the difference in using a CMOS device and BJT devices for several examples of current mirror. Showing weaknesses in some popular current mirror architectures such as the Wilson current mirror.

ii) Chapter Two includes the development and generation of a new generic small signal model that can be used for both CMOS and BJT devices, this was used in the analysis of the current mirrors.

iii) Chapter Three highlights the affects of the source resistance on the overall gain of the source follower, and shows the increased affects of source resistance on shrinking process technology. It also shows how the source resistance can be extracted from simulation, and highlights problems with current process design kits that do not include this in their current simulation models. A paper has been submitted for technical publication through Maxim in Chip Design (www.chipdesignmag.com).

iv) Chapter Four presents the new current conveyor using an un-buffered voltage follower with several types of current mirrors (followers), which offers the Power Supply Rejection Ratio (PSRR) of an Operational Transconductance Amplifier (OTA) type current conveyor, without the limitations of the bandwidth. A second paper has been submitted for technical publication again through Maxim.

v) Chapter Five gives examples of how the new current conveyor can be used to build a new type of current feedback operational amplifier.

List of principal symbols and achronyms

β	Bipolar transistor DC current gain.
CCI	Current conveyor (type I).
CCII	Current conveyor (type II).
CFOA	Current feedback op-amp.
g_m	Transconductance.
g	Conductance.
I_S	Forward saturation current.
λ	CMOS transistor channel modulation effect.
PSRR	Power-supply rejection ratio.
r_{ce}	Bipolar transistor collector emitter resistance.
r_{be}	Bipolar transistor base emitter resistance.
VT	Thermal voltage (KT/q).
Ea	Early Voltage.
V_{be}	Transistor base-emitter voltage.
Uo	Surface Mobility of the CMOS channel.
Cox	Gate oxide capacitance for a CMOS device.
Vgs	Gate Source Volatge of a CMOS device.
VTH	Threshold Volatge of a CMOS device.
r_{ds}	CMOS transistor drain source resistance resistance.
r_{gs}	CMOS transistor gate source resistance resistance.
TSMC	Tiawainese Semiconductor Manufacturing Corporation.
f_T	Frequency transition – the frequency where where gain falls to unity.
BJT	Bipolar Junction Transistor.
CMOS	Complementary Metal Oxide Silicon.
OTA	Operational Transconductance Amplifier.

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CHAPTER 1

Thesis Introduction

1.1 The current conveyor concept explained

The first current conveyors were proposed by Smith and Sedra in 1968 **[1-1],** they have a distinct advantage over the commonly used operational amplifier which uses voltage feedback, as they are not bandwidth limited in the same way as its voltage feedback counterpart i.e. by the necessity of a compensation capacitor which is needed for closed loop stability.

Actually a current conveyor is potentially limited only by the bandwidth of the transistors used in the design, and by the architecture of the current conveyor, these limitations will be discussed with examples later on in the thesis.

There are several types of current conveyor the CCI, CCII, CCII+, and CCII-. The subtle differences are explained in this section.

Figure 1-1 below shows a black box of a CCII:

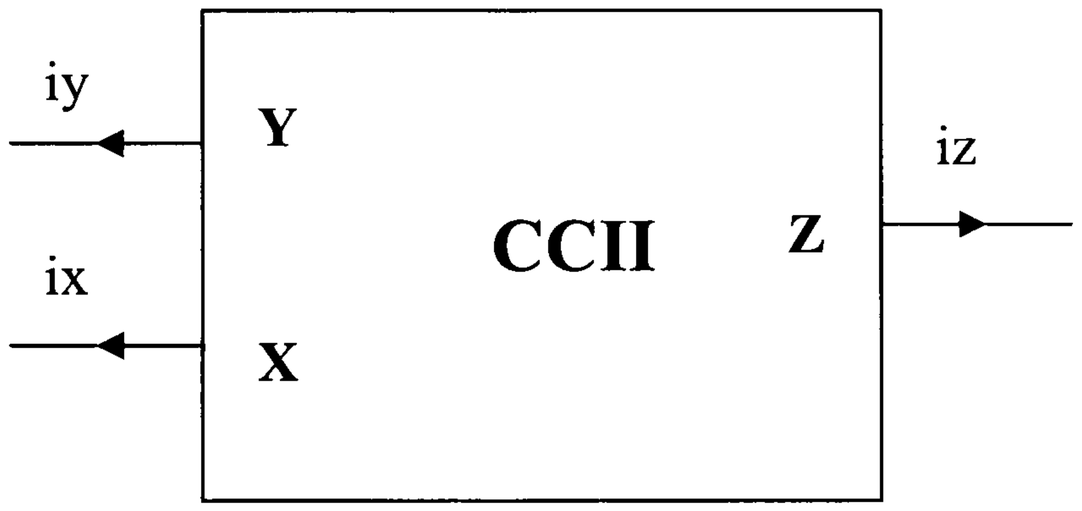

Figure 1-1 : The Black Box version of the CCII

Using Figure 1-1 the CCI/CCII matrix is shown below:

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix}$$

i*, v* refer to the currents and voltages respectively at the appropriate named nodes.

From the matrix above:

'a' is the current gain from node Y to node X (iy/ix).

'b' is the current gain from node X to node Z (iz/ix).

The gain of the voltage follower part of the current conveyor is set to unity in this matrix.

The characteristics of the different current conveyors are as follows:

1) If b>0 the current conveyor is a CC+ (for a typical current conveyor this is set to unity).

2) If b<0 the current conveyor is a CC- (for a typical current conveyor this is set to unity).

3) If a=1 the circuit is a CCI.

4) If a=0 the circuit is a CCII.

So for example a CCI+ current conveyor must have the following attributes:

'b' > 0 (most commonly close to unity), and 'a' is also unity.

And another example would be the CCII+ current conveyor must have the following attributes:

'b' > 0 (again most commonly close to unity) and 'a' approximately zero (signifying a high input impedance into Node Y of the current conveyor).

As the current conveyor is also known as the ideal transistor **[1-11],** it is a good idea to show the relationship between the current conveyor and the 2 types of transistor used in this thesis the BJT and the CMOS transistor.

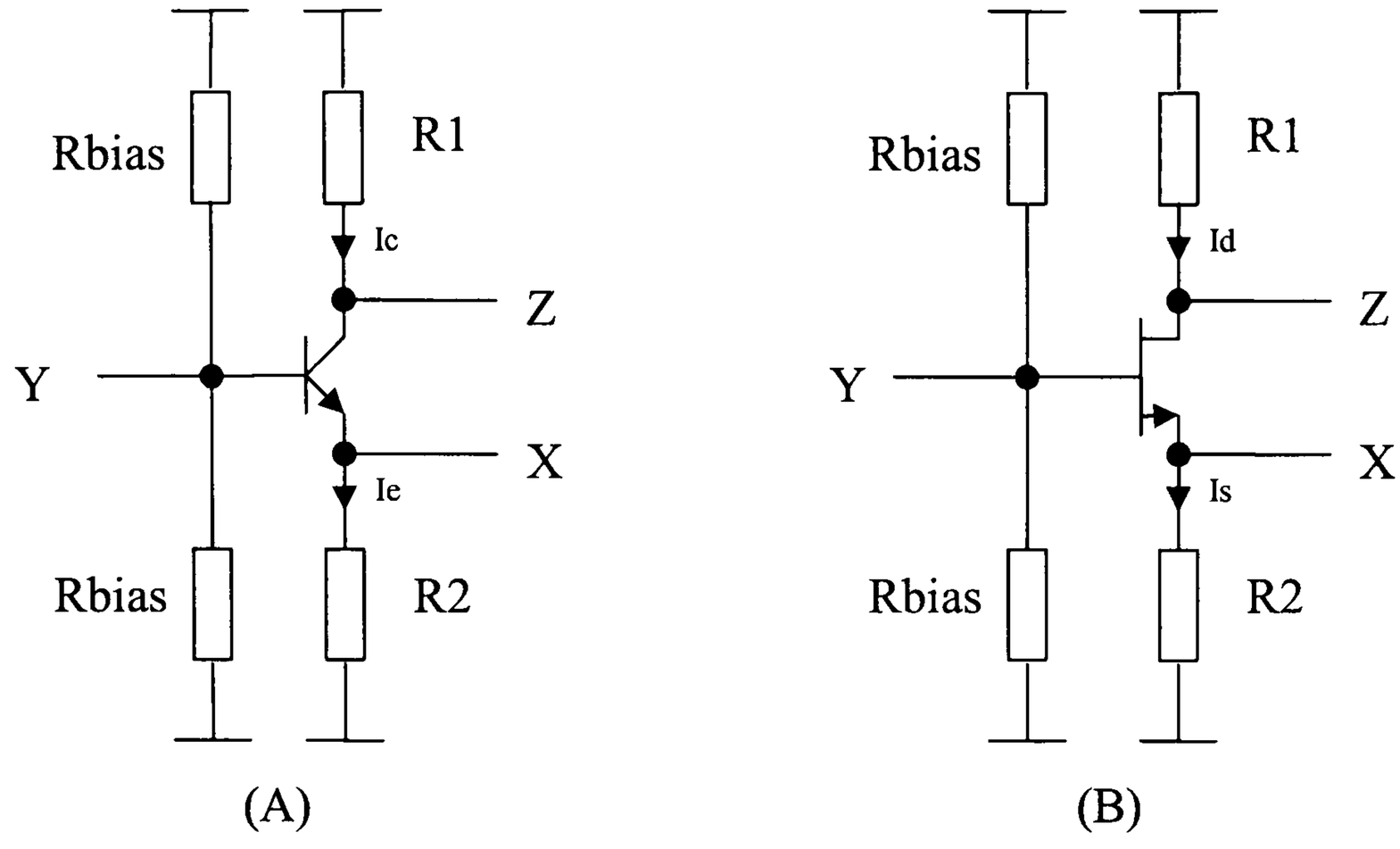

Figure 1-2 : (A) A simple BJT Amplifier; (B) A simple CMOS Amplifier.

Figure 1-2 shows two types of amplifier a BJT and a CMOS, the nodes are labelled as a CCII would be. A CCI is similar except the input impedance of node Y is much lower (equivalent to impedance of the emitter in a BJT or the impedance of the source in a CMOS transistor). The '-' and '+' after CCII refers to the direction of the Collector current (Ic) in a BJT or the Drain current (Id) in a CMOS transistor; a true BJT/CMOS transistor would have the current going into the Collector/Drain respectively, the current conveyor equivalent is known as a CCII- where the current goes into node Z **[1-11]**, the more common CCII+ **[1-8],** has the current coming out of node Z, this is because they are easier to implement and is much more useful in applications.

1.2 History of the current conveyor

The original current conveyor, or CCI, (which can be regarded as an ideal transistor) was initially proposed by Smith and Sedra in 1968 **[1-1],[1-2],[1-9],** Figure 1-3 below shows the initial CCI realisation proposed by Smith and Sedra, using BJTs.

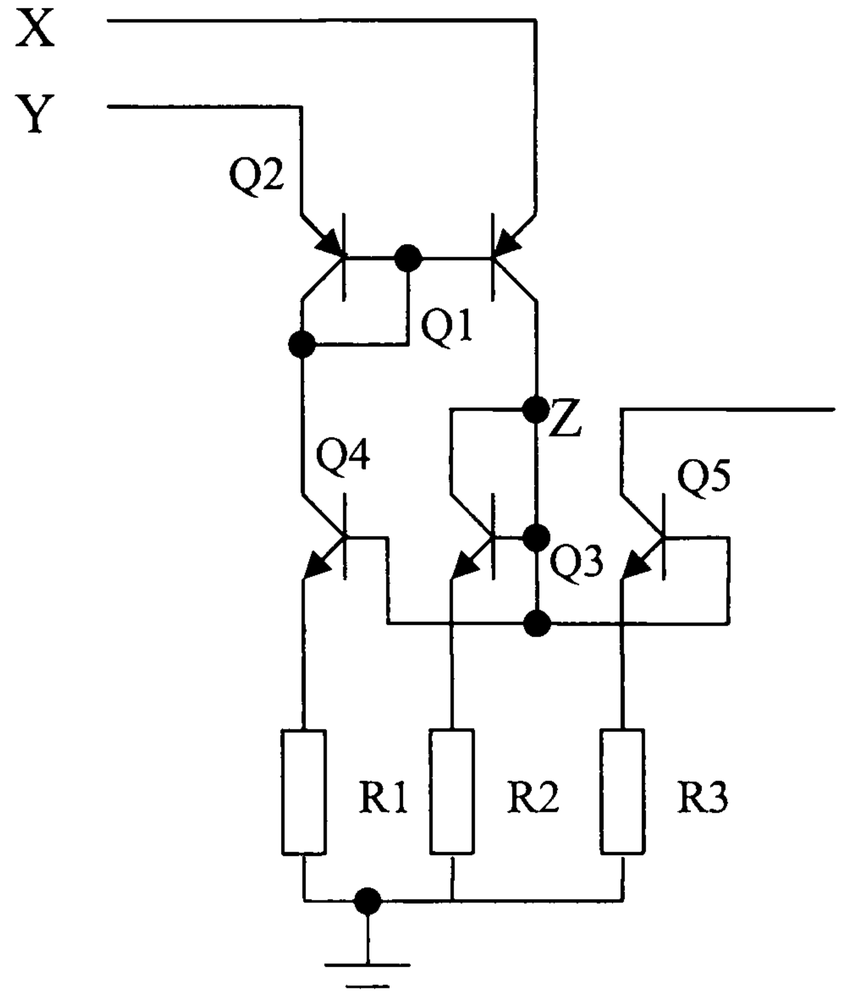

Figure 1-3: The CCI+ using BJTs

Looking at Figure 1-3, the current conveyor has 3 nodes (X,Y,Z), these mimic the nodes of the base (Y), emitter (X), and the collector (Z) of a BJT; Or in the case of the CMOS transistor the gate (Y), source (X), and the drain (Z). Simply transistors Q1 and Q2 and Q3 and Q4 form current mirror pairs and assuming the correct biasing (i.e. R1,R2,R3 are matched), and nodes X has the appropriate load then the Voltage on X will match Y (An emitter/source follower), Q5 is used to mirror the current from Q3 and Q4 to nodes Z (collector/drain). The CCI current conveyor has a voltage gain of unity between Y and X and –A between Y and Z where 'A' is the ratio of load on Z to that on X.

The problem with the CCI was even though it approaches an ideal transistor from a voltage point of view, it does not to have the high input impedance expected on the Y node which mimicked the base of a BJT or the gate of the CMOS transistor.

So it was then replaced by a more versatile second generation device in 1970 the CCII **[1-1],[1-4],[1-5],[1-6]**. The CCII can be described as a combination of a voltage follower and a current follower within the same integrated circuit. Figure 1-4 shows a basic block diagram of what the CCII was aiming for.

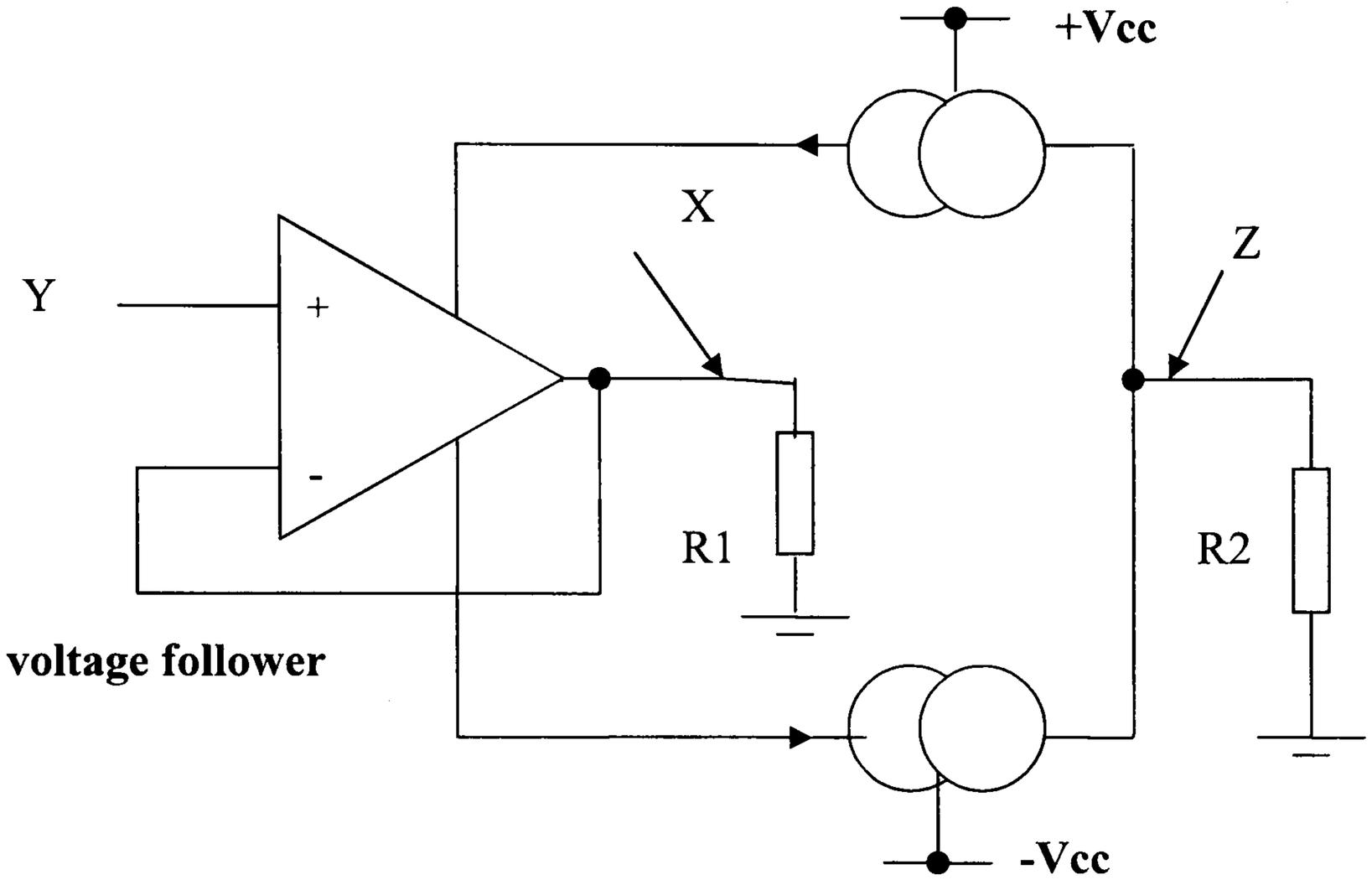

Figure 1-4 : Block Diagram of the CCII

Figure 1-4 has an ideal voltage follower (with a unity voltage gain) between Y and X and a current follower (with a unity current gain) between X and Z **[1-3]**. Y has an infinite impedance and the voltage gain between X and Z is the ratio of their load impedances.

In reality it is impossible to achieve the desired impedance levels, but if the design of a current conveyor can get as close as possible to the ideal attributes of the current conveyor as described in the previous paragraph the better it will work.

Figure 1-5 below shows a relatively simple BJT CCII+ current conveyor configured as an amplifier.

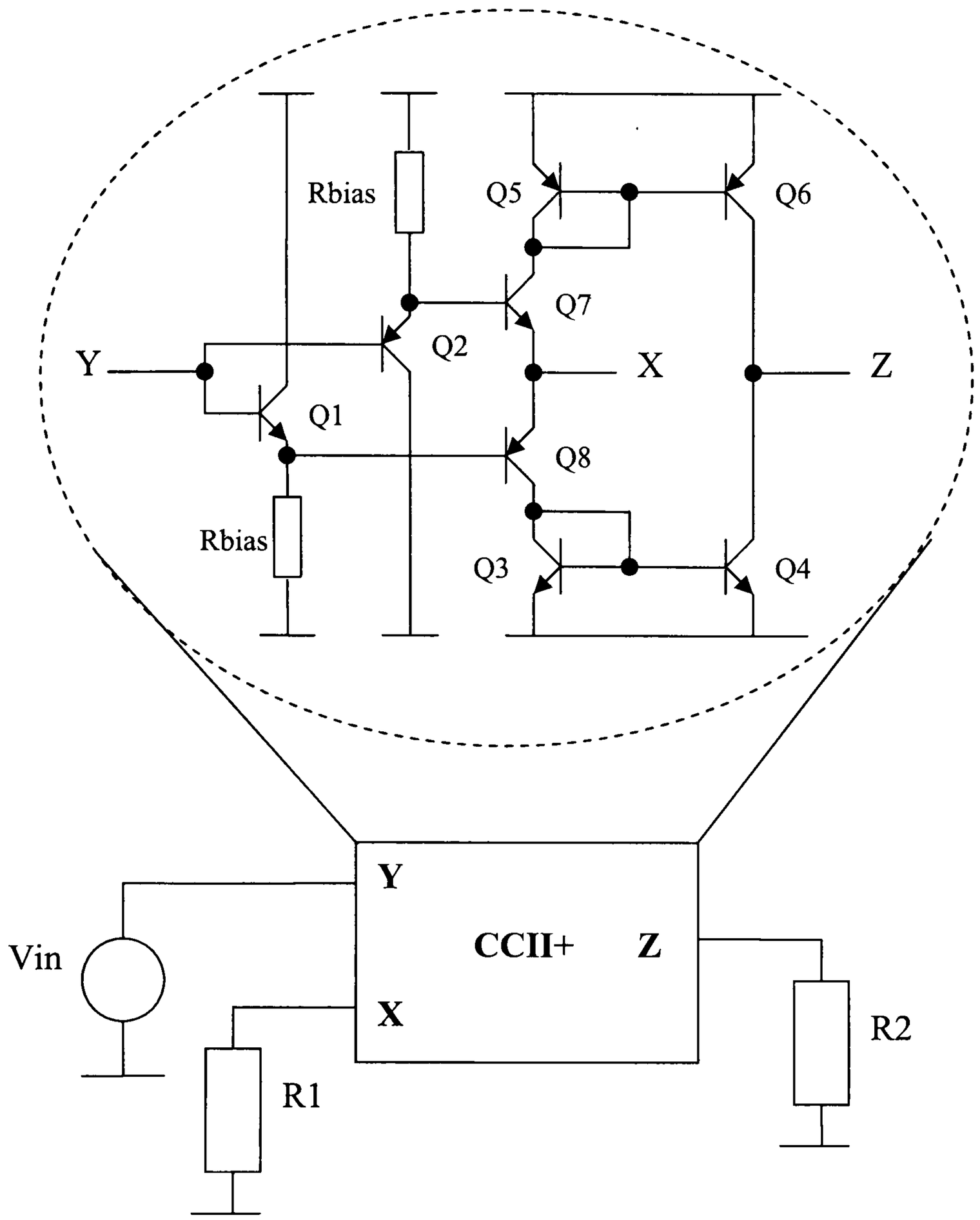

Figure 1-5 : A BJT CCII+ current conveyor configured as an amplifier.

Figure 1-5 shows a class A-B BJT current conveyor configured as an amplifier with loads R1 and R2 and this will be used to explain the operation of the current conveyor, and illustrates how it can be used to provide amplification.

The BJT current conveyor operates in the following way, node X tracks Y as a voltage follower (Q1,Q2 and Q7, Q8), the current through R1 is mirrored to R2 through the current mirror pairs Q3, Q4 and Q5, Q6; Q1 and Q2 are used to bias Q7 and Q8 in the active region when $V_y = 0$.

This type of current conveyor shown in Figure 1-5 does not perform well when implemented in CMOS technology due the inherent low trans-conductance (g_m) values, and lower equivalent Early voltages (V_A) compared with that of a BJT device, which in turn gives rise to a lower gain on the voltage follower stage of the current conveyor. The values of g_m and V_A are getting even worse with shrinking geometries, but as most processes these days prefer to use CMOS primarily for cost reasons, other methods have to be looked into to, to improve the output impedance of Z, and the voltage follower gain between nodes Y and X.

There are at present current conveyors available that use an operational trans-conductance amplifier (OTA) as the building blocks **[1-8].** The main problem with these devices is they are bandwidth limited to the gain-bandwidth of the OTA being used and hence the full bandwidth potential of the transistors making up the OTA is not realised. Other CMOS current conveyors rely on accurate transistor matching to work correctly **[1-10].**

The applications for the CCII are considerable **[1-3], [1-4],** especially with present day requirements in mobile communications and high speed networking, which rely on high gain-bandwidth devices, basically anything that needs an amplifier could utilize a current conveyor. The CCII is very versatile and can be used to create a wide range of analogue functions from a simple amplifier stage to filters, including the much researched Current Feedback Operational Amplifier CFOA **[1-7]** which uses the current conveyor within a closed loop as the main building block. Therefore improving the design to give today's designers a better CMOS alternative to conventional OTA based CCII which are bandwidth restricted while offering the usual features of amplifiers such as good Power Supply Rejection Ratio (PSRR).

1.3 Research Aims

The aim of the research programme was to design a CCII+ current conveyor in CMOS with an appropriate gain between the voltage follower nodes Y and X (as close as possible to unity), and a high as possible output impedance on node Z, other factors such as improving the Power Supply Reject Ratio (PSRR) were also looked at. The research program was aimed at an existing foundry process (TSMC 0.18μm), and all simulation data including the CMOS transistor models were produced from this design kit.

The thesis is divided into six chapters, the thesis has been structured in a way to describe all the building blocks of the CMOS current conveyor, before putting them together to form the full device. Applications of current conveyor are briefly described focusing on the Current Feedback Operational Amplifier (CFOA) which uses the current conveyor as its major build block.

Chapter Two deals with the current follower (bi-directional current mirror); analysis and comparisons in current gain and output impedance was undertaken for several different types of current mirror. The results also compared the effects of output impedance of the current mirrors using BJT and CMOS devices. Each design has been investigated using Matlab, and the output impedances are plotted for all current mirrors analysed. Examples of all the current mirrors were simulated using CMOS devices taken from the TSMC 0.18μm process, and the results were evaluated, giving pros and cons for each current mirror.

Chapter Three deals with the voltage follower part of the current conveyor, again using the TSMC 0.18μm process CMOS transistors. The chapter begins with the source follower which is analysed, simulated and discussed. Improvements to the basic source follower are presented and simulated, and then compared with the original source follower.

Chapter Four combines the results in Chapters Two and Three to deliver several examples of the new proposed current conveyor, comparing areas such as voltage gain between all the nodes in the CCII, Power Supply Rejection Ratio (PSRR), and overhead (power supply) issues. The first circuit compared is the CMOS equivalent of

the CCII+ shown in Figure 1-5, as this is the easiest circuit to implement and is more beneficial to compare with existing BJT design. This chapter also deals with the conversion of CCII+ to the CCII-. Although the CCII+ is a more useful device there are applications for the CCII-, really anything that needs a common (source/emitter) amplifier can use a CCII-, as they tend to have a much higher value of output impedance than just the single transistor approach, while offering a better bandwidth solution than the basic OTA.

Chapter Five will briefly go through the some of the applications that the proposed CMOS current conveyor can be used for, and will focus on the Current Feedback Operational Amplifier (CFOA), concentrating on two specific examples of how Current Feedback Operational Amplifier can be implemented, these designs are based on the Cascode and Regulated Cascode current conveyors described in Chapter Four. Each of the two implementations of the Current Feedback Operational Amplifier were simulated and the simulation results were recorded and compared.

Chapter Six briefly summarises the previous chapters and future work is discussed.

1.4 References

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CHAPTER 2

The Current Follower

2.1 Introduction

This chapter will deal with analysis of the 'Current Follower' which makes up part of the Current Conveyor, as explained in Chapter One, section 1.1, 'The Current Conveyor Explained'.

The chapter starts with a brief history of the transistor, to show how the BJT and the CMOS transistors have a common background, and will highlight some of their similarities and differences.

In Section 2.3, 'The proposed Generic Transistor Model', will deal with the theory and analysis behind the generic transistor model to be used in the analysis of the current followers in this chapter. The similarities and differences of the BJT and the CMOS transistor are highlighted from a mathematical point of view.

Section 2.4 deals with several types of current mirrors, with the aim of looking at the specific attributes such as output impedance and current gain which are major factors in governing the accuracy of the current mirror **[2-1].** The analysis was undertaken using Matlab.

The results were recorded for both the BJT model and the CMOS model and then compared to highlight and identify their significant differences.

2.2 A brief history of the transistor

To explain the reasoning behind the comparison between the BJT and the CMOS transistor, it will be useful to explain the history surrounding the transistor.

The first patent for the transistor were registered in Germany in 1928 by Julius Edgar Lilienfeld. In 1934 German physicist Dr. Oskar Heil patented the field-effect transistor. It is not clear whether either design was ever built, and this is generally considered unlikely **[2-2],[2-3]**.

On 22 December 1947 William Shockley, John Bardeen and Walter Brattain succeeded in building the first practical point-contact transistor at Bell Labs **[2-4]** shown below in Figure 2-1, The First Point Contact Transistor. This work followed from their war-time efforts to produce extremely pure germanium "crystal" mixer diodes, used as a frequency mixer element in microwave radar receivers.

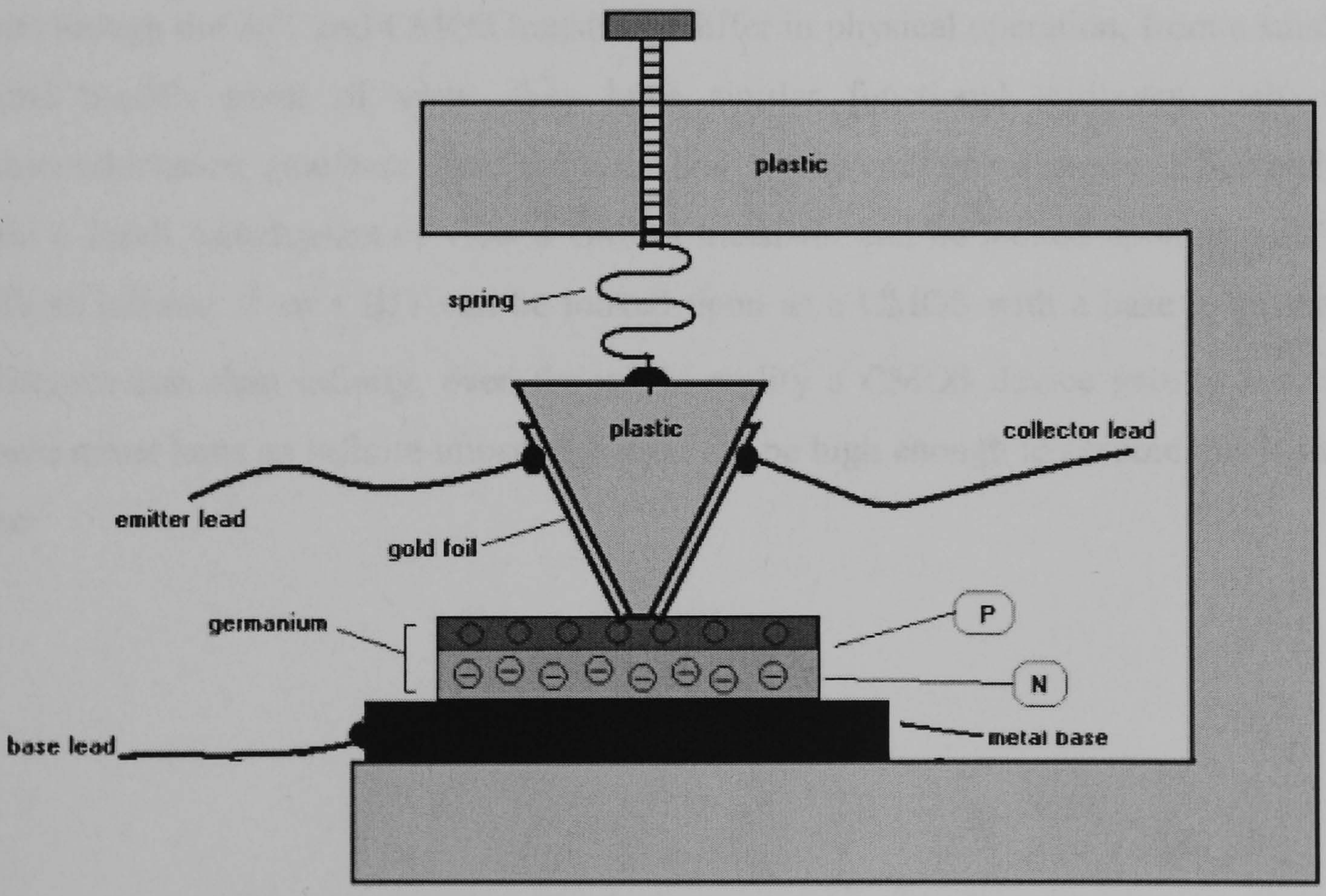

Figure 2-1: The First Point Contact transistor ([2-5]).

The point-contact transistor was commercialized and sold by Western Electric and others but was rather quickly superseded by the junction transistor more commonly known as the BJT because it was easier to manufacture and more rugged. The original designs used germanium **[2-5]** but have now been superseded by silicon which is much easier to manufacturer, has lower temperature dependence and the raw material has a virtual unlimited supply.

The concept of the Field Effect Transistor (FET), of which the CMOS device is part of this family, date back before the Point Contact Transistor. Indeed, the aim of the original research at Bell Labs was to replace the fragile glass vacuum tube amplifier, which could be described as the fore runner to the CMOS transistor. However, due to manufacturing processes at the time the BJTs were easier to produce. Only recently with the dramatic cost reductions in producing CMOS on silicon and improvements in parameters such as transconductance **[2-6]** has the FET become the replacement to the BJT device.

Even though the BJT and CMOS transistors differ in physical operation, from a small signal models point of view, they have similar functional attributes such as transconductance, gate/base drain/collector and source/emitter resistance. Effectively from a small signal point of view a CMOS transistor can be looked upon as a BJT with an infinite β or a BJT can be looked upon as a CMOS with a base to emitter resistance less than infinity, even though in reality a CMOS device gate to source would never have an infinite impedance it would be high enough to assume this is the case.

2.3 The Generic Transistor Model

As previously mentioned from a small signal point of view the CMOS device can be looked upon as a BJT with infinite β. This concept will be used later in this chapter when comparing the current mirrors attributes. As the CMOS and the BJT share similar attributes a model was devised which could be used for both BJT and CMOS transistor types. The model is shown below.

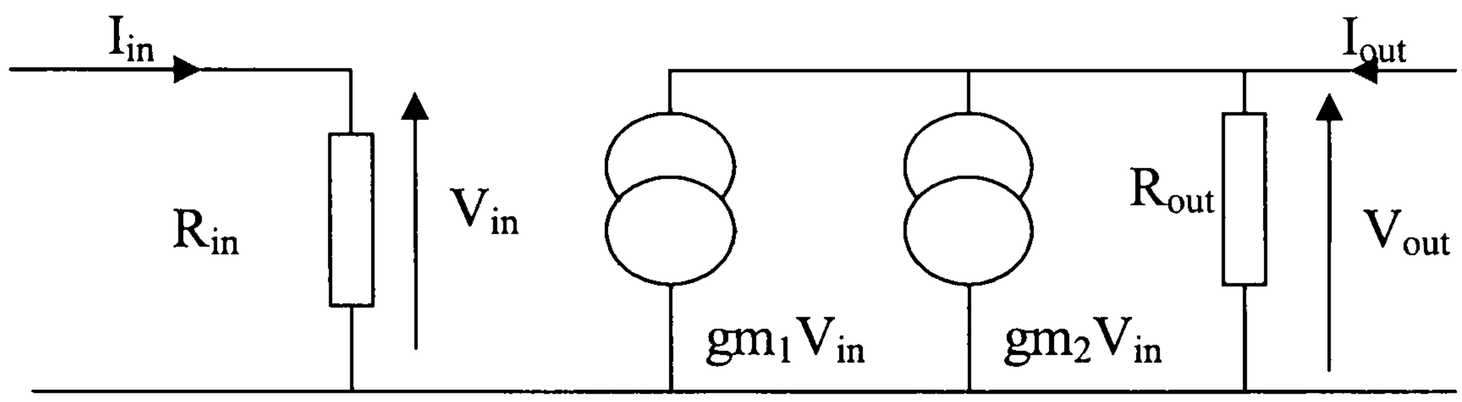

Figure 2-2: New Generic Small Signal Model for both BJT and CMOS FETs.

From Figure 2-2 the Generic Transistor has an input impedance, two small signal current generators, and an output impedance, it is noted that this model does not contain the obvious capacitances which would be associated with the BJT and CMOS devices as the model is a low frequency model **[2-7].** These attributes are not needed in this analysis for the current mirror as this chapter only deals with the DC and low frequency behaviour of the current mirrors being considered.

To help with the understanding of the model shown in Figure 2-2, a general graph of the current voltage (IV) characteristics of the Generic Transistor model is shown below:

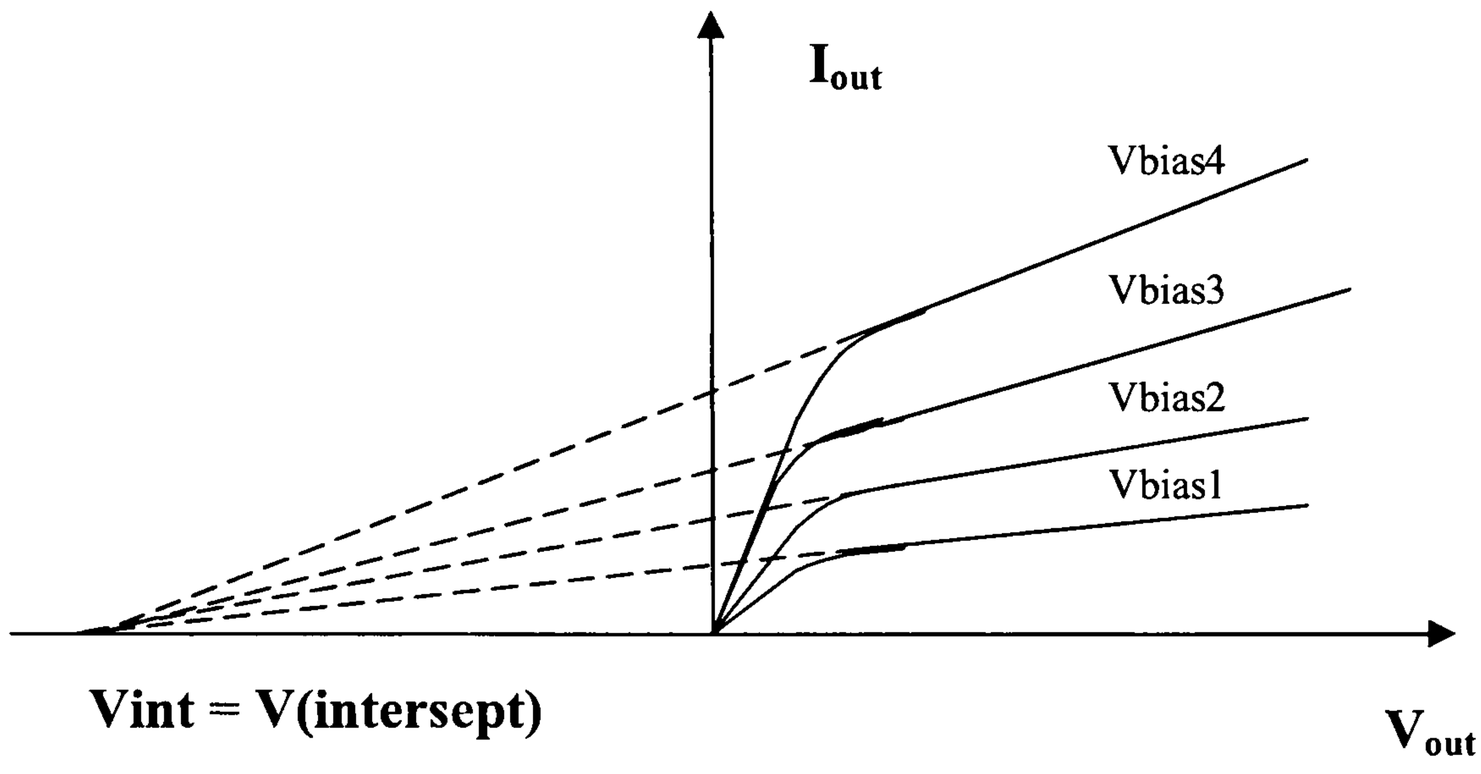

Figure 2-3: Generic Transistor IV Characteristics

Figure 2-3 shows the IV (Collector/Emitter(BJT)); Drain/Source(CMOS)) transfer characteristics of the Generic Model shown in Figure 2-2, Vbias(x) refers to the DC bias of the device (V_{be} for the BJT and V_{gs} for the CMOS transistor).

From Figures 2-2, 2-3 the following generic equations can be derived:

$$R_{in} = \frac{\beta}{gm_1} \qquad (2.1)$$

$$R_{out} = \frac{V\,\mathrm{int}}{I_{out0}} \qquad (2.2)$$

(where I_{out0} is the current at V_{out} = 0V; This is the inverse of the gradient of the slope Shown in Figure 2-3 for the appropriate Vbias).

From Figure 2-2, taking the two current generators, and the output resistance from

equation (2).

$$I_{out} = gm_1 V_{in} + gm_2 V_{in} + \frac{V_{out}}{R_{out}} \quad (2.3)$$

I_{in} is simply the input voltage (V_{in}) over the measured small signal resistance (R_{in})

$$I_{in} = \frac{V_{in}}{R_{in}} \quad (2.4)$$

Using these above equations and model in Figure 2-2, the small signal models for the BJT and CMOS transistors are derived using the model parameter equations shown both in Table 2-1 **[2-15],[2-16]**.

Table 2-1: The Generic Model Equation translation table

Model Parameter	**CMOS Equation**	**BJT Equation**
V_{int}	$\frac{1}{\lambda}$	Ev
β	∞	50 to 100
R_{in}	R_{gs}	R_{be}
I_{out} (Large Signal)	$\frac{W\mu_o C_{ox}}{2L}(V_{gs} - V_{th})^2(1 + \lambda V_{ds})$	$Is.e^{\frac{Vbe}{Vt}}(1 + \frac{V_{ce}}{Ev})$
I_{out0} (Large Signal)	$\frac{W\mu_o C_{ox}}{2L}(V_{gs} - V_{th})^2$	$Is.e^{\frac{Vbe}{Vt}}$
gm_1	$\frac{I_{D0} W.e^{\frac{Vgs}{Vt}}}{L.V_t}$	$\frac{Is.e^{\frac{Vbe}{Vt}}}{V_t}(1 + \frac{Vce}{V_A})$
gm_2	$\frac{W\mu oC_{ox}}{L}(V_{gs} - V_{th})(1 + \lambda V_{ds})$	N/A

Note:

1) **For device equations V_t refers to the thermal voltage, around 26mV at 300K.**
2) **For the CMOS device 'g' refers to the gate; 's' refers to the source; 'd' refers to the drain. V_{th} refers to the threshold voltage for the device.**
3) **For the BJT device 'b' refers to the base; 'e' refers to the emitter; 'c'**

refers to the collector.

4) **For the CMOS device λ refers to the channel modulation parameter.**
5) **For the BJT device E_v refers to the Early Voltage.**
6) **For the CMOS device I_{D0} refers to a process dependant parameter based on the source/bulk voltage and the threshold voltage (V_{th}).**

From Table 2-1 it can be seen that from a small signal point of view the CMOS and BJTs are similar. They both have exponential generators, the BJT does lack the square law generator though. They both have an input resistance even though CMOS devices has an extremely high value, this value is actually falling as processes are shrinking, and in the lower geometries the CMOS device is beginning to behave more like a BJT device. The devices also have a similar output resistance independent of their current generators, and the method of calculating this resistance from V_{int} shown in Figure 2-3 can be used for both the CMOS and the BJT devices.

2.4 Current Mirror Analysis

As explained in the introduction to this chapter, for the current follower (generally built with two current mirrors) to work successfully it must have the ability to copy current accurately, and its output impedance must be as high as possible so that the output current is equal to the input current irrespective of the value of the load. Ideally the output impedance of the current mirror should be infinite meaning that any change in voltage on the output would not affect the output current, in reality this is not possible, but certain current mirror architectures can be used to increase output impedance and hence improve performance.

This section will look at the architectures of several different current mirrors, particularly their relative output impedances, and how changing transistor types from BJT to CMOS affects their output impedances. Advantages and disadvantage will be discussed and their ability to be used with the new conveyor will be reviewed briefly, as this will be discussed in more detail in Chapter Four.

The following current mirror architectures were compared against the benchmark of the simple two transistor current mirror circuits namely the:

1) Cascode Current Mirror;
2) Wilson Current Mirror;
3) Improved Wilson Current Mirror and the
4) Regulated Cascode Current Mirror.

The analysis undertaken for each of the current mirrors will be based on the BJT and from Table 2-1 it will be assumed that for the CMOS analysis that the β of the transistor will be infinite.

2.4.1 The Simple Current Mirror

Figures 2-5a and b below show two implementations of a simple current mirror **[2-9]** which will be used for the analysis:

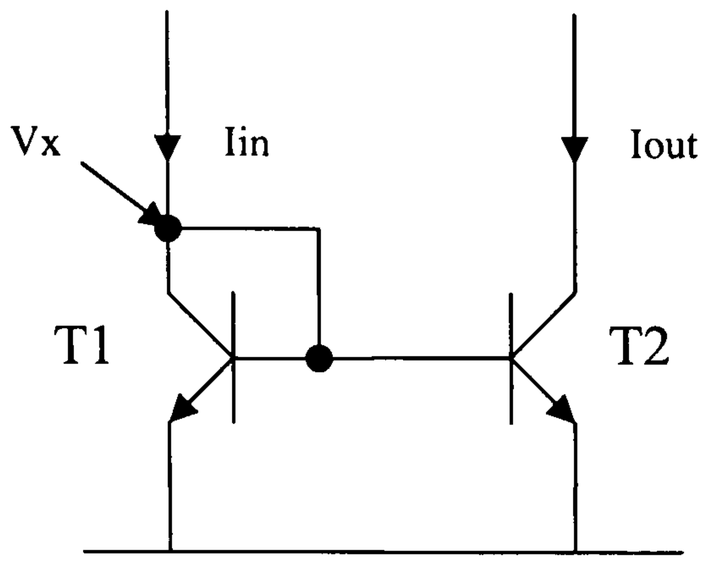

Figure 2-5a: A BJT simple current mirror.

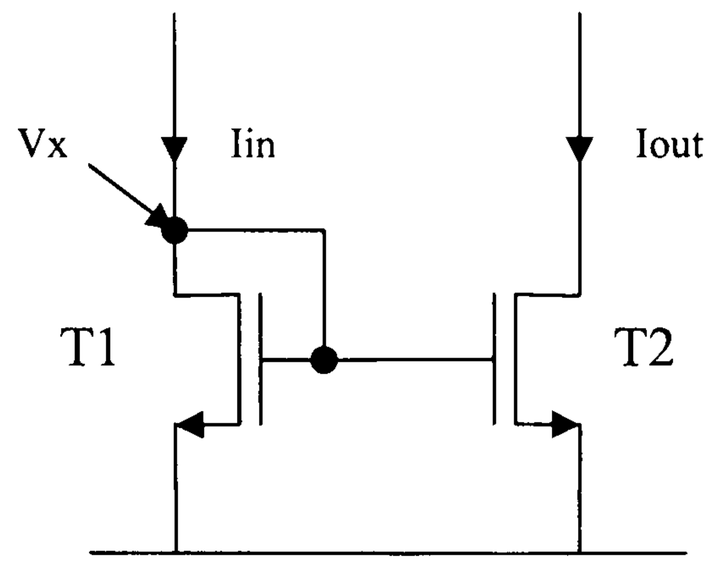

Figure 2-5b: A CMOS simple current mirror.

From Figures 2-5a and b transistor T1 is the input diode connected transistor and the current is mirrored to the output via T2, as both transistors share the same base voltage (Vx), then if both transistors are identical then the current mirrored at the output Iout is to a first approximation the same as Iin.

2.4.1.1 Analysis of Output Impedance

From Figures 2-5a and b the following equivalent small signal model of the current mirror can be drawn, shown in Figure 2-6 below:

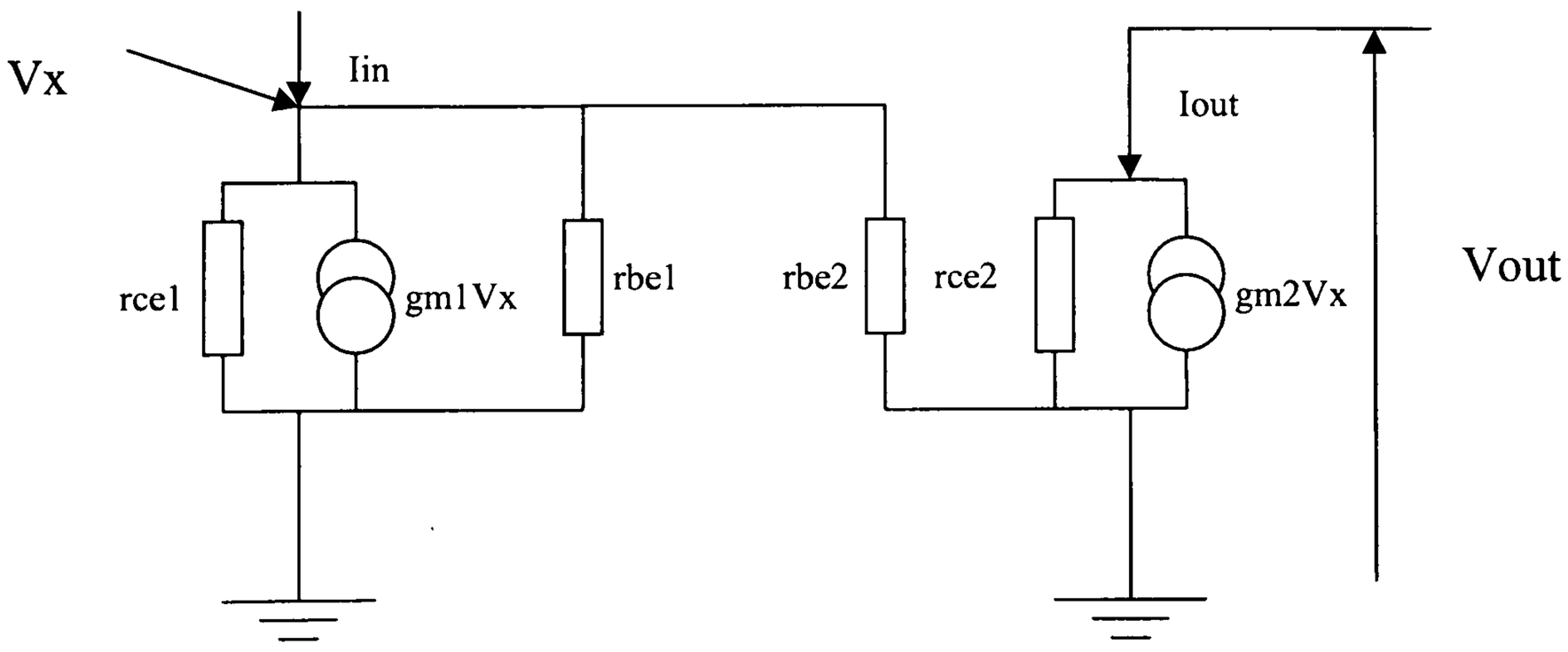

Figure 2-6: Small Signal Equivalent Model of the Simple Current Mirror.

From Figure 2-6 assuming Iin is an ideal current source:

$Iin = 0;$ $Vx = 0;$ (AC Small Signal)

and:

$$Iout = \frac{Vout}{r_{ce2}} + gm2.Vx \qquad (2.5)$$

then From (2.5):

$$Iout = \frac{Vout}{r_{ce2}} \qquad (2.6)$$

as $Vx = 0;$

so from (2.6):

$$Rout = \frac{Vout}{Iout} = r_{ce2} \qquad (2.7)$$

Equation (2.7) shows the BJT equivalent output impedance which is simply the collector to emitter or drain to source impedance of the output transistor and is not affected by the β of the transistors.

Therefore taking equation (2.7) and translating to the CMOS transistor:

$$Rout = \frac{Vout}{Iout} = r_{ds2} \qquad (2.8)$$

It can be seen that the impedances for both the BJT and CMOS mirrors have similar attributes. As the β of the transistor has no effect on the output impedance of the devices, it was not necessary to use Matlab in this case.

2.4.2 The Cascode Current Mirror

This circuit technique increases the output impedance of the simple current mirror using an extra transistor on the output **[2-10]**. Considering it is very popular in common source amplifier design, as it reduces the Miller effect capacitance on the input of the amplifier **[2-8],** this has the effect of increasing the effective bandwidth. This is done by clamping the collector of the input transistor (T2 Figure 2-7a) as close as possible to its base voltage, this has the effect of reducing the signal voltage across the collector base capacitor, thus increasing bandwidth. Figure 2-7b works in the same way.

Figures 2-7a and b below show two implementations of the cascode current mirror which will now be analysed using the generic transistor model described in Section 2.3:

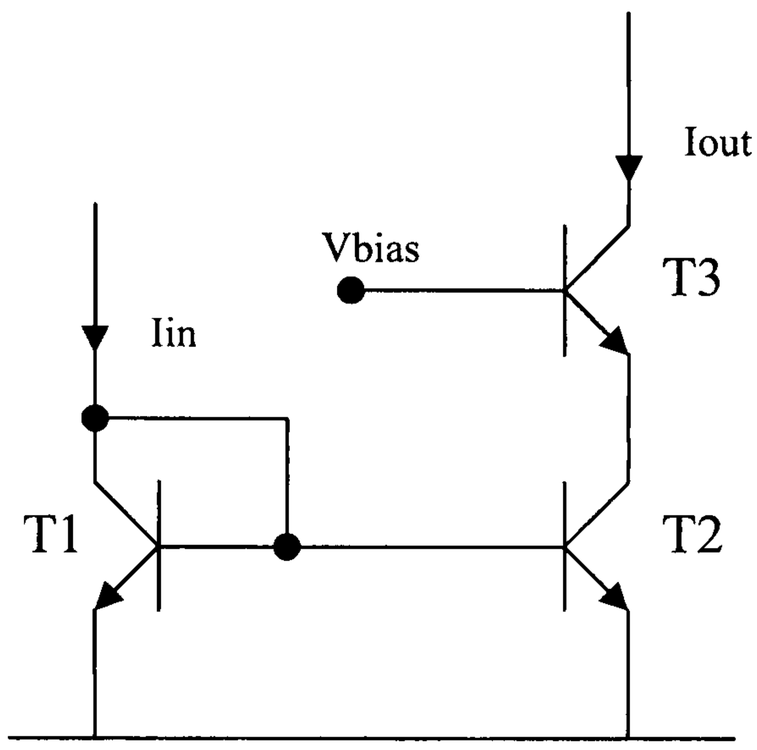

Figure 2-7a: BJT Cascode Current Mirror.

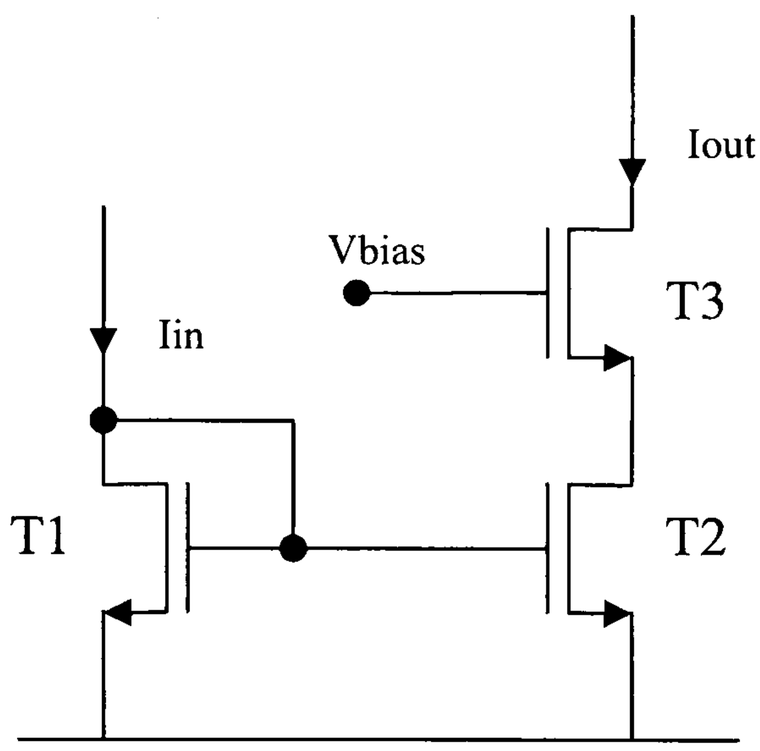

Figure 2-7b: CMOS Cascode Current Mirror.

The cascode current mirrors shown in Figures 2-7a and b, have the same structures as the current mirrors in section 2.4.1 'The Simple Current Mirror', except transistor T3 is added. This is the cascode transistor and is tied to a fixed DC voltage (Vbias), the current is mirrored from Iin through the diode connected transistor T1 to Iout through transistor T2, and again if both T1 and T2 are identical then Iin and Iout will closely match.

Note that the dimensions of transistor T3 does not affect the output current translation of T1 and T2. This transistor is deliberately added to increase the output impedance of the current mirror, as the analysis in the next section will show.

2.4.2.1 Analysis of Output Impedance

From Figures 2-7a and b the following equivalent small signal model of the mirror can be drawn, shown in Figure 2-8 below:

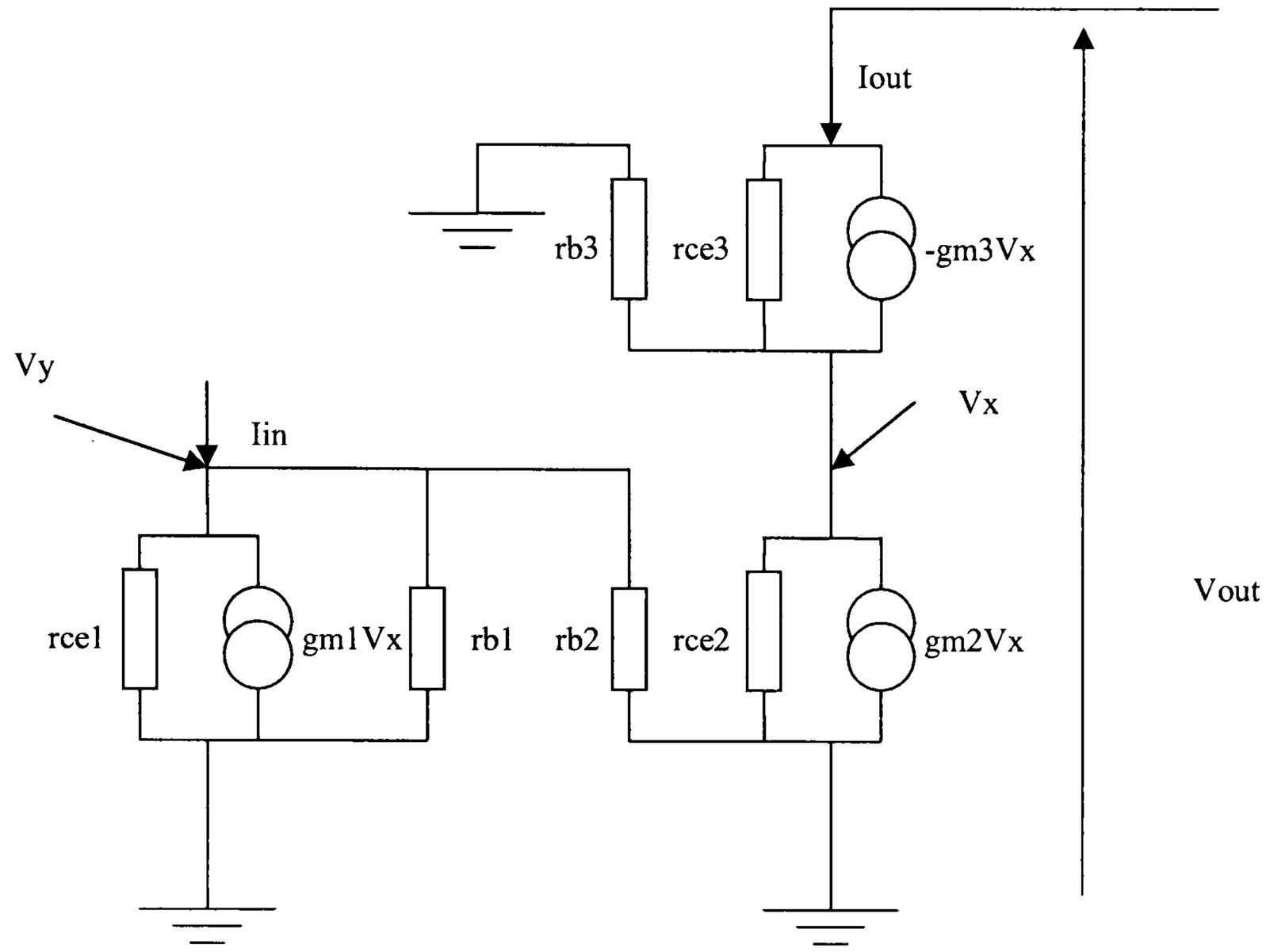

Figure 2-8: Small Signal Equivalent model of the Cascode Current Mirror.

From Figure 2-8, assuming Iin is an ideal current source:

$Iin = 0$; $Vy = 0$; (AC small Signal)

and:

$$Vout = Iout(r_{ce3} + \frac{\beta_3 . r_{ce2}(1 + gm_3 . r_{ce3})}{(gm_3 . r_{ce2} + \beta_3)}) \qquad (2.9)$$

so:

$$\frac{Vout}{Iout} = r_{out} = (r_{ce3} + \frac{\beta_3 . r_{ce2}(1 + gm_3 . r_{ce3})}{(gm_3 . r_{ce2} + \beta_3)}) \qquad (2.10)$$

Equation 2.10 represents the exact value of the output impedance of the cascode current mirror using BJT devices. So from equation (2.10) assuming that $\beta_3.r_{ce2} >> r_{ce3}$, $gm_3.r_{ce3} >> 1$ and $gm_3.r_{ce2} >> \beta_3$, the approximate output impedance of the mirror using BJTs is:

$$r_{out} \approx \frac{\beta_3.r_{ce2}.gm_3.r_{ce3}}{gm_3.r_{ce2}} \qquad (2.11)$$

which simplifies to:

$$r_{out} \approx \beta_3.r_{ce2} \qquad (2.12)$$

Referring to Figure 2-7b:

$\beta_3 \longrightarrow \infty$ (for a CMOS device)

so:

$$r_{out} \approx r_{ds2}(1 + gm_3.r_{ds3}) \qquad (2.13)$$

which simplifies to:

$$r_{out} \approx r_{ds2}.gm_3.r_{ds3} \qquad (2.14)$$

From Equation (2.12) that for the BJT equivalent, the impedance has increased by a factor of β_3 compared to that of the simple current mirror, and for the CMOS equivalent the impedance has been increased by a factor of $gm_3.r_{ds3}$ (Equation (2.14)). This factor can be made high so r_{out} is much higher than rds2.

2.4.2.2 Matlab Results

To give a better idea of how the BJT and CMOS transistor affects the output impedance of the cascode current mirrors, a Matlab model was generated using Equation (2.10) shown in Section 2.4.2.1. The Matlab scripts for this are shown in the Appendices at the end of this chapter.

Two different Matlab scripts were written with the following objectives:

1) To show the differences in impedance with BJTs set to a β of 50, and CMOS transistors where the value of β was set to 10,000. The transconductance and their output impedances were set to the same values for both types of mirrors, these values are arbitrary and are shown in the Appendix at the end of this chapter.
2) To show the effects on the output impedance of the current mirror by increasing β from 1 to 10,000 i.e. moving from a BJT mirror to a CMOS mirror.

The results from Script1 are as follows:

i) BJT cascode current mirror's output impedance (from Equation 2.10):

$r_{out} = 347K\Omega$

ii) CMOS cascode current mirror's output impedance (from Equation 2.10):

$r_{out} = 1.01M\Omega$

Now using Script1 the approximate values of the cascode current mirror are as follows:

iii) BJT cascode current mirror's output impedance (from Equation 2.12):

$r_{out} = 500K\Omega$

iv) CMOS cascode current mirror's output impedance (from Equation 2.14):

$r_{out} = 1M\Omega$

Now using Script2 as explained previously the β of the cascode current mirror was increased from 1 to 10,000 the graph (Figure 2-9) below shows changes in the output impedance as the value of β is increased:

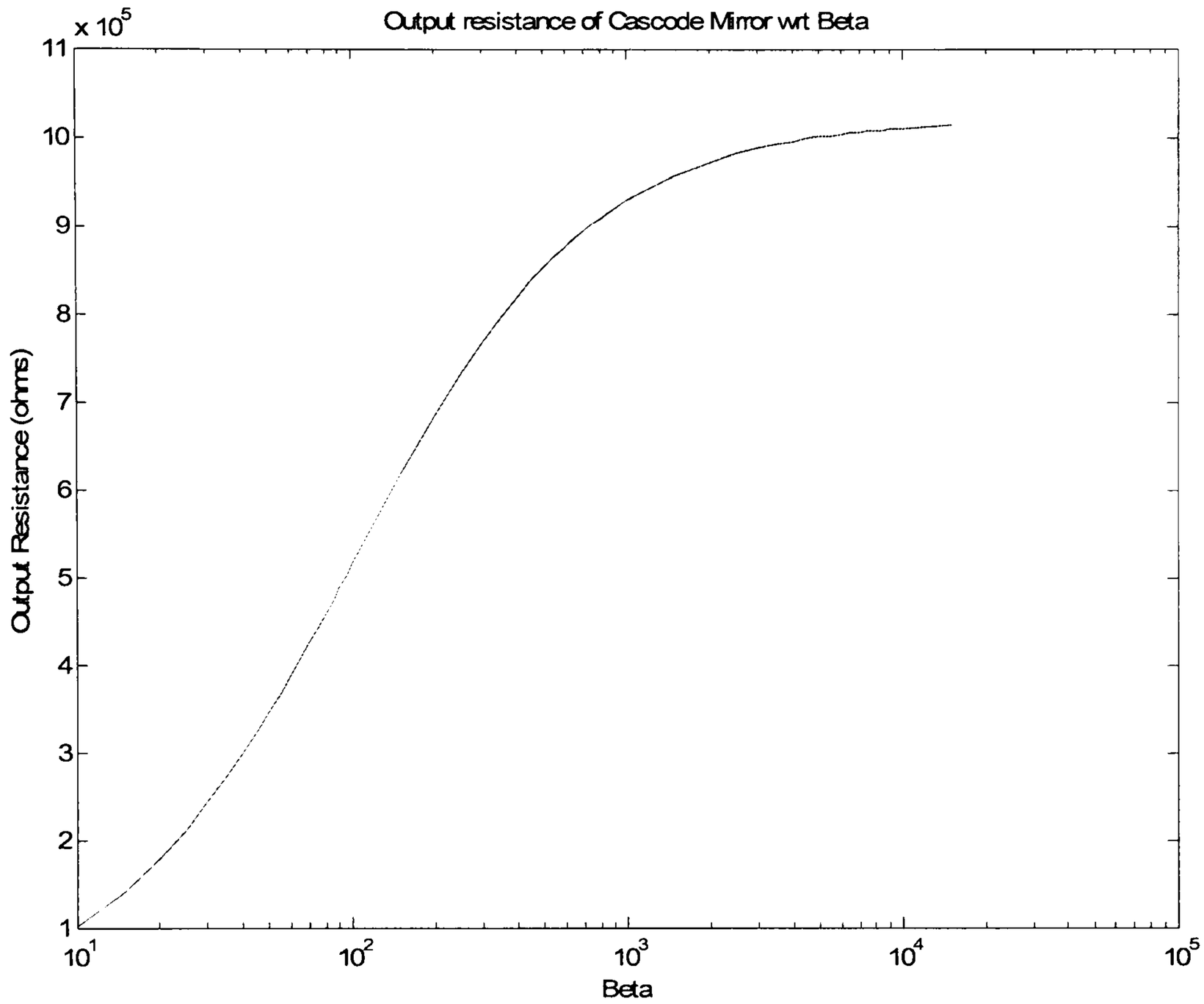

Figure 2-9: The effects of a transistors β on the output impedance of a Cascode Current Mirror.

Figure 2-9 shows that as β increases the output impedance of the current mirror increases and limits at about $1\text{M}\Omega$ as β approaches 10,000, taking into account that the transconductance and output impedance of the transistors match. This impedance is equivalent to the Cascode type current mirror, but the base/gate of transistor T3 does not need extra circuitry to bias it as it is biased by the collector/drain of T1.

2.4.3 The Wilson Current Mirror

This circuit technique is another used to improve the output impedance of the simple current mirror using an extra transistor on the output **[2-11]**. This time unlike the cascode current mirror, T3 base is connected to the input of the mirror, and as the output current increases, it increases the collector/emitter voltage (Figure 2-10a) of T2. This reduces the base/emitter voltage of T3, as the base of T3 is fixed, reducing the flow of current through T3 and T2 until it reaches approximately Iin. Figure 2-10b works in the same way.

Figures 2-10a and b below show two implementations of the Wilson current mirror which will be analysed using the generic transistor model described in Section 2.3:

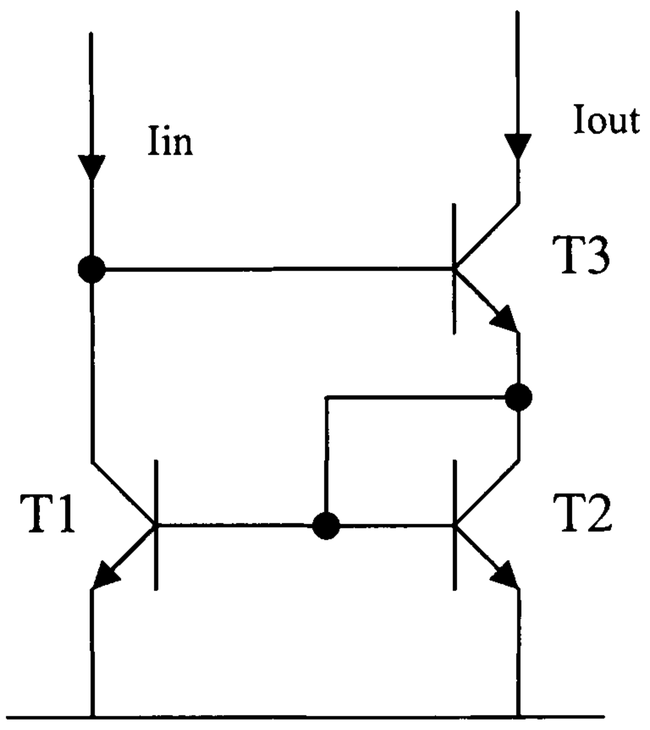

Figure 2-10a: A BJT Wilson Current Mirror.

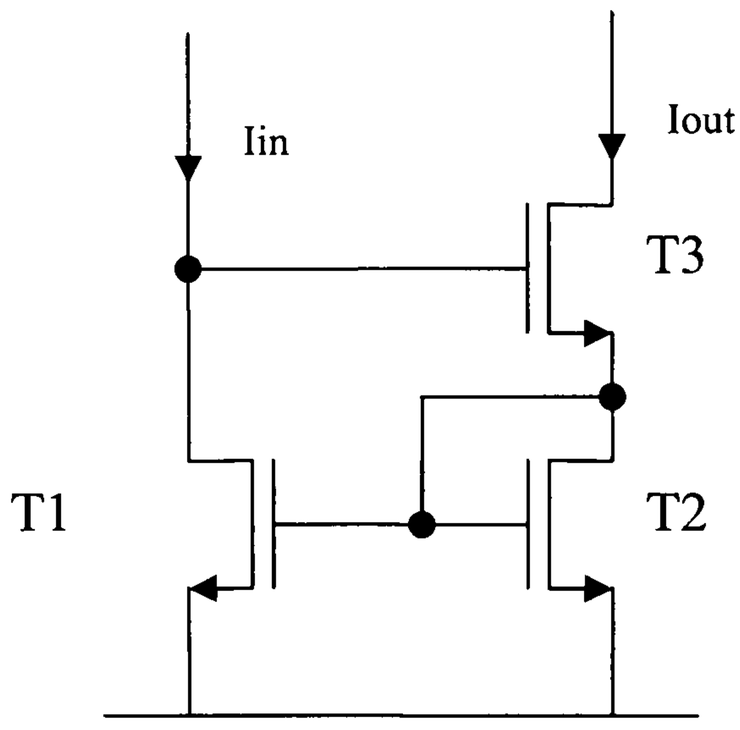

Figure 2-10b: A CMOS Wilson Current Mirror.

2.4.3.1 Analysis of Output Impedance

From Figures 2-10a and b the following small signal equivalent circuit of the Wilson current mirror can be drawn, shown in Figure 2-11 below:

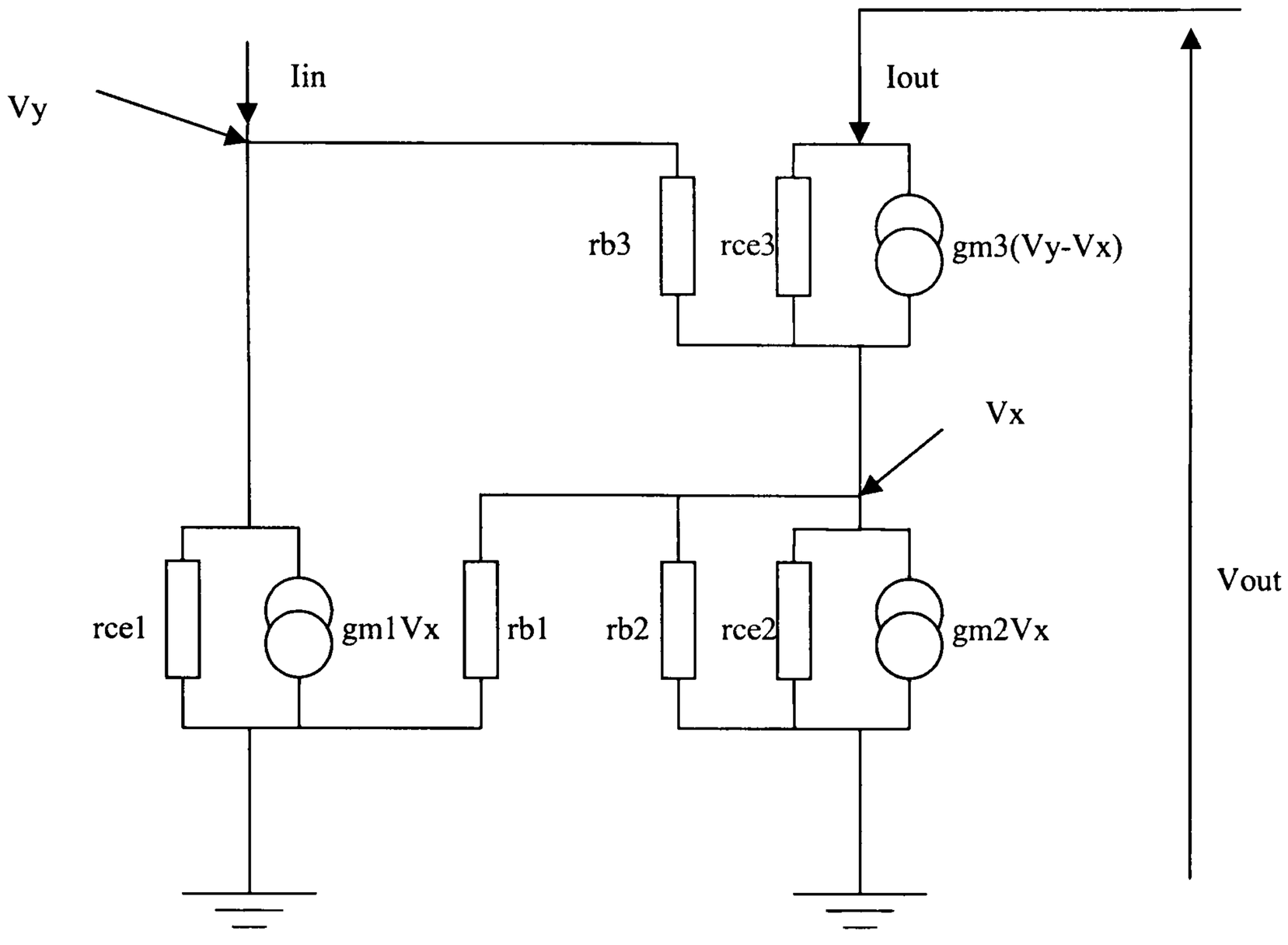

Figure 2-11: Small Signal Equivalent Model of the Wilson Current Mirror.

From Figure 2-11 assuming Iin is an ideal current source:

$Iin = 0$; (AC small Signal)

so:

$$\frac{Vout}{Iout} = r_{out} = (r_{ce3} - gm_3.Bgy.Bgx.r_{ce3} + Bgx.gm_3.r_{ce3} + Bgx) \quad (2.15)$$

where

$$Bgx = \frac{\beta_3.\beta_2.\beta_1}{(gm_1.\beta_2.\beta_3.r_{ce2} + gm_2.\beta_1.\beta_3.r_{ce2} + gm_2.\beta_1.\beta_2.\beta_3.r_{ce2} + \beta_1.\beta_2.\beta_3 - gm_3.\beta_1.\beta_2.r_{ce2}(Bgy - 1))} \qquad (2.16)$$

and:

$$Bgy = \frac{gm_3.r_{ce1} - gm_1.\beta_3.r_{ce1}}{\beta_3 + gm_3.r_{ce1}} \qquad (2.17)$$

Equation 2.15 represents the exact value of the output impedance of the Wilson current mirror using BJT devices. So From (2.15) simplifying the equation the approximate output impedance of the mirror using BJTs is:

$$r_{out} \approx \frac{\beta_3.r_{ce3}}{2} \qquad (2.18)$$

Referring to Figure 2-10b:

$\beta_1, \beta_2, \beta_3 \longrightarrow \infty$ (For a CMOS device)

so:

$$rout \approx rds3 + rds2\frac{(gm3.gm1.rds1.rds3 + gm3.rds3 + 1)}{(gm2.rds2 + 1)} \qquad (2.19)$$

which simplifies to:

$$r_{out} \approx \frac{gm_3.gm_1.r_{ds1}.r_{ds3}}{gm_2} \qquad (2.20)$$

From Equation (2.18) that for the BJT equivalent, the impedance has increased by a factor of $\frac{\beta_3}{2}$ compared to that of the simple current mirror, and for the CMOS equivalent the impedance has been increased by a factor of 'gm3.gm1.rds3/gm2'. If all the transistors for a CMOS equivalent Wilson current mirror match then the output impedance would match that of the Cascode current mirror.

2.4.3.2 Matlab Results

To give a better idea of how the BJT and CMOS transistor affects the Wilson current mirrors' output impedance, a Matlab model was generated using equations (2.15,2.16,2.17) shown in section 2.4.3.1. The Matlab scripts for this are shown in the Appendices at the end of this chapter.

Two different Matlab scripts were written with the following objectives:

1) To show the differences in impedance with BJTs set to a β of 50, and CMOS transistors where the value of β was set to a very 10,000. The transconductance and their output impedances were set to the same values for both types of mirrors, these values are arbitrary and are shown in the Appendix at the end of this chapter.
2) To show the effects on the output impedance of the current mirror by increasing β from 1 to 10,000 i.e. moving from a BJT mirror to a CMOS mirror.

The results from Script1 are as follows:

i) BJT Wilson current mirror's output impedance (from Equation 2.15):

$$r_{out} = 205K\Omega$$

ii) CMOS Wilson current mirror's output impedance (from Equation 2.15):

$$r_{out} = 990K\Omega$$

Now using Script1 the approximate values of the Wilson current mirror are as follows:

iii) BJT Wilson current mirror's output impedance (from Equation 2.18):

$$r_{out} = 250K\Omega$$

iv) CMOS Wilson current mirror's output impedance (from Equation 2.20):

$$r_{out} = 1.01M\Omega$$

Now using Script2 as explained previously the β of the Wilson current mirror was increased from 1 to 10,000, the graph (Figure 2-12) below shows changes in the

output impedance as the value of β is increased:

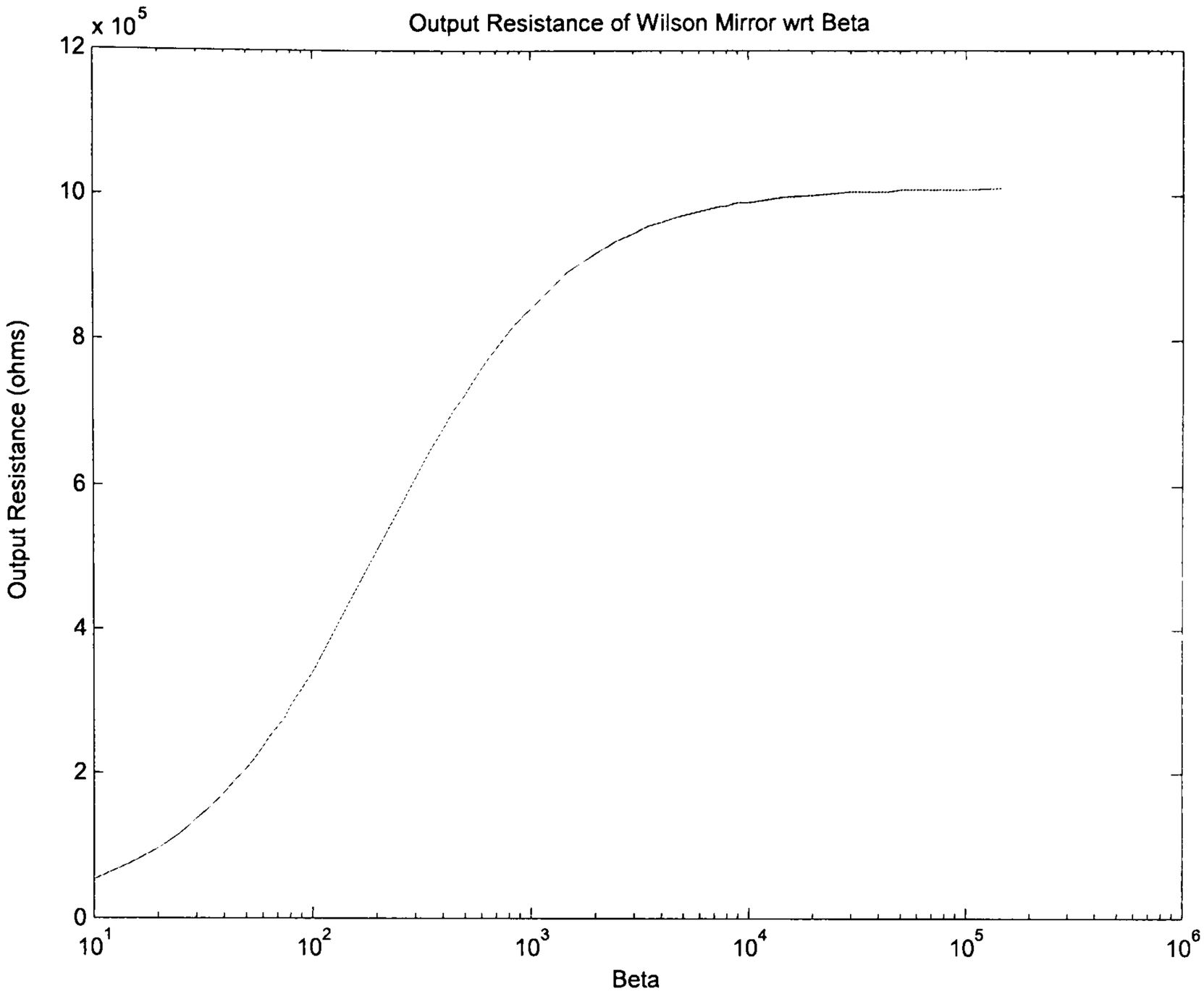

Figure 2-12: The effects of a transistors β on the output impedance of a Wilson Current Mirror.

Figure 2-12 shows that as β increases the output impedance of the current mirror increases and reaches $1\text{M}\Omega$ as β approaches infinity, taking into account that the transconductance and output impedance of the transistors match. This is the same as the Cascode current mirror.

2.4.4 The Improved Wilson Current Mirror

This current mirror is an improved version of the Wilson current mirror **[2-12]**, but with the addition of transistor T4 which is diode connected, the current through T4 will match that of T3, and because of the symmetry of the circuit current through T1, will match that at the output of the mirror T2 meaning that Iin is more precisely matched to Iout.

Figures 2-13a and b below show two implementations of the Improved Wilson current mirror which will be used for the analysis:

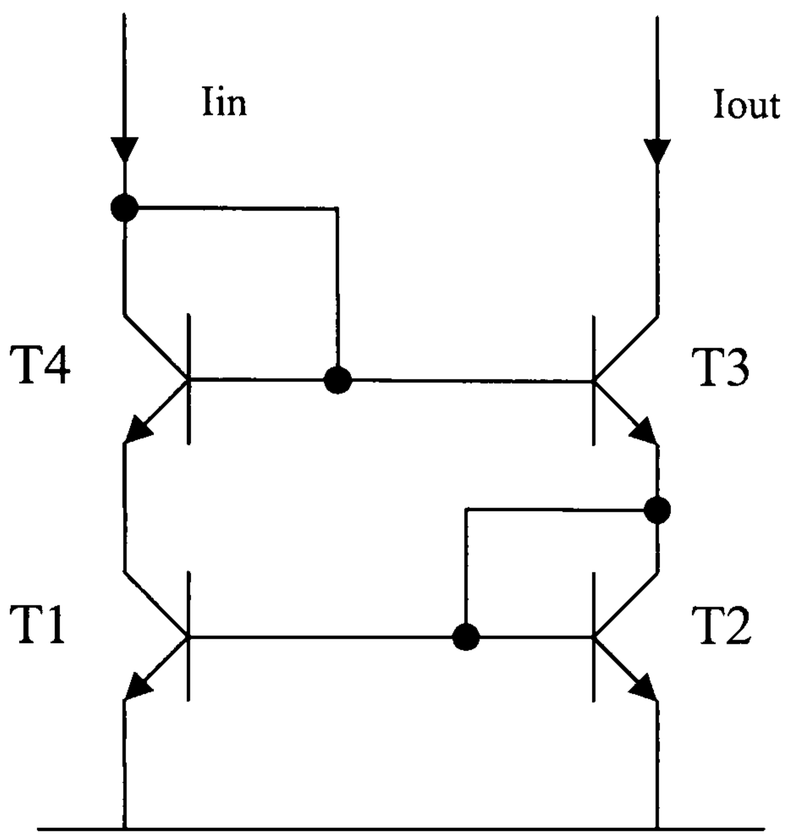

Figure 2-13a: A BJT Improved Wilson Current Mirror.

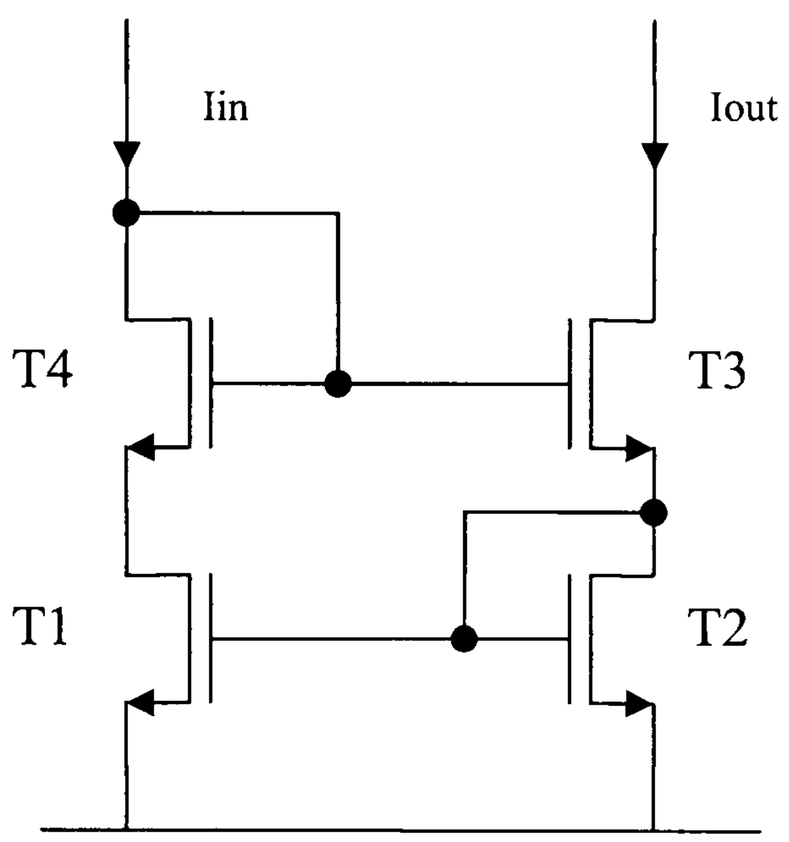

Figure 2-13a: A CMOS Improved Wilson Current Mirror.

2.4.4.1 Analysis of Output Impedance

From Figures 2-13a and b the following equivalent small signal model of the current mirror can be drawn, as shown in Figure 2-14 below:

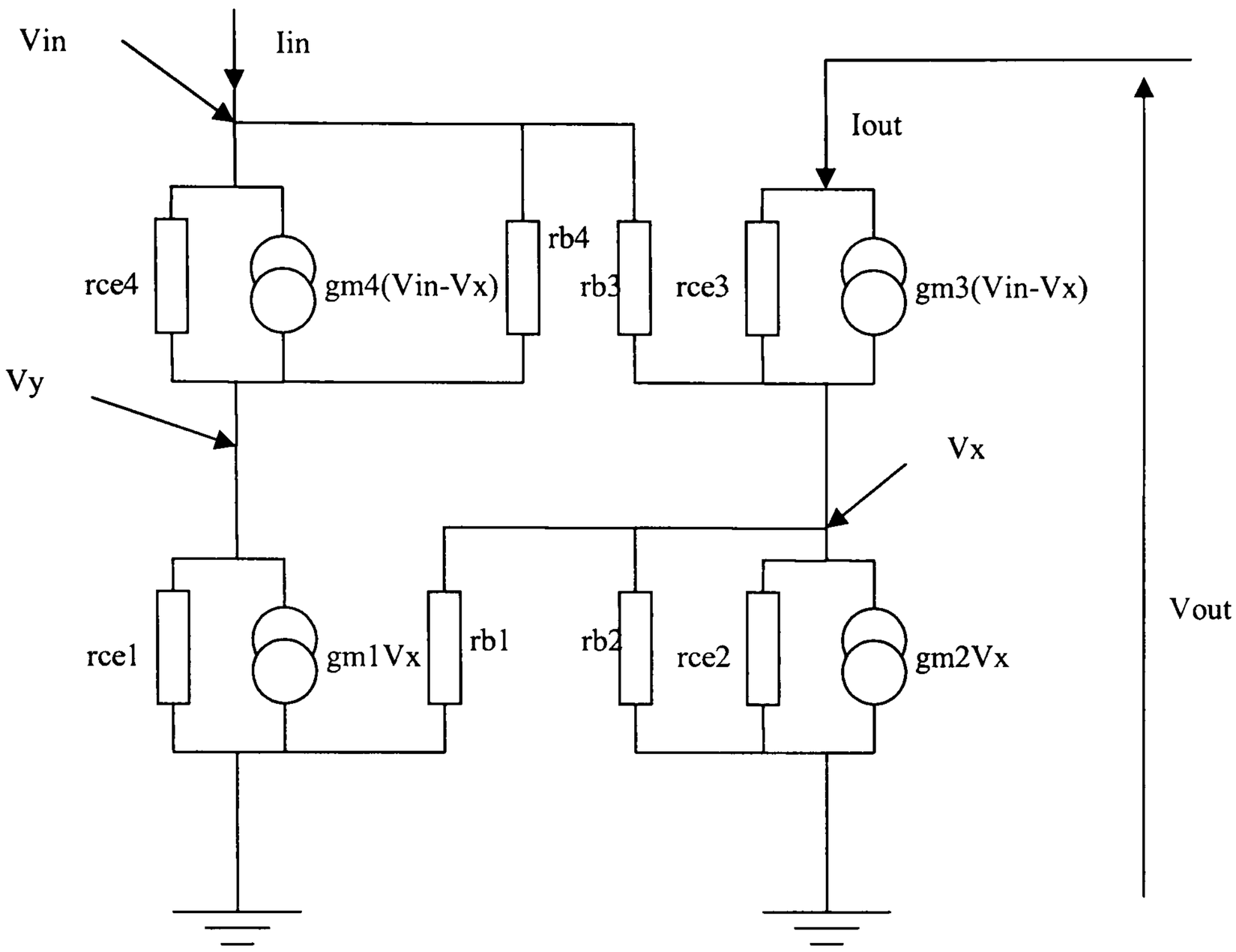

Figure 2-14: Small Signal Equivalent model of the Improved Wilson Current Mirror.

From Figure 2-14 assuming Iin is an ideal current source:

$Iin = 0$; Vin = 0; (AC small Signal)

so:

$$\frac{Vout}{Iout} = r_{out} = r_{ce3} + Bx + gm_3.r_{ce3}.Bx(1 - Bin.By.\beta_3 - Bin.gm_3.Rd1) \qquad (2.21)$$

where:

$$Rd1 = \frac{r_{ce1}.\beta_1}{(\beta_1 + gm_1.r_{ce1}.\beta_1 + gm_1.r_{ce1})} \qquad (2.22)$$

$$Rd4 = \frac{r_{ce4}.\beta_4}{(\beta_4 + gm_4.r_{ce4}.\beta_4 + gm_4.r_{ce4})} \tag{2.23}$$

and:

$$Bin = \frac{1}{(\beta_3 + gm_3.Rd1)} \tag{2.24}$$

$$By = \frac{gm_2.Rd1.r_{ce2} - Bin.gm_3.Rd1.r_{ce2}}{(Bin.\beta_3.r_{ce2} - r_{ce2} - Rd1)} \tag{2.25}$$

$$Bx = \frac{Rd1.Rd4}{(Rd1 + By.Rd4 + gm_1.Rd1Rd4 - Bin.By.\beta_3.Rd4 - Bin.gm_3.Rd1.Rd4)} \tag{2.26}$$

Equation 2.21 represents the exact value of the output impedance of the improved Wilson current mirror using BJT devices. So from (2.21) simplifying the equation, the approximate output impedance of the mirror using BJTs is:

$$r_{out} \approx \frac{\beta_3.r_{ce3}}{2} \tag{2.27}$$

Referring to Figure 2-13b:

$\beta_1, \beta_2, \beta_3, \beta_4 \longrightarrow \infty$ (for a CMOS device)

so:

$$r_{out} \approx r_{ds3} + \frac{\beta_3.r_{ds1}(1 + gm_3.r_{ds3})}{(gm_3.r_{ds1} + \beta_3)} \tag{2.28}$$

From Equation (2.27), that for the BJT equivalent, the impedance has increased by a factor of β_3 compared to that of the simple current mirror, and for the CMOS equivalent the impedance has been increased by a factor of ' $\frac{\beta_3(1 + gm_3.r_{ds3})}{(gm_3.r_{ds1} + \beta_3)}$, as shown in Equation (2.28). For the BJT equivalent, the output impedance matches that of the cascode current mirror.

2.4.4.2 Matlab Results

To give a better idea of how the BJT and CMOS transistor affects the improved Wilson current mirrors' output impedance, a Matlab model was generated using Equations (2.21 to 2.26) as shown in Section 2.4.4.1. The Matlab scripts for this are shown in the Appendices at the end of this chapter.

Two different Matlab scripts were written with the following objectives:

1) To show the differences in impedance with BJTs set to a β of 50, and CMOS transistors where the value of β was set to 10,000. The transconductance and their output impedances were set to the same values for both types of current mirrors, these values are arbitrary and are shown in the appendix at the end of this chapter.
2) To show the effects on the output impedance of the current mirror by increasing β from 1 to 10,000 i.e. moving from a BJT current mirror to a CMOS current mirror.

The results from Script1 are as follows:

i) BJT improved Wilson current mirror's output impedance (from Equation 2.21):

$r_{out} = 255K\Omega$;

ii) CMOS improved Wilson current mirror's output impedance (from Equation 2.21):

$r_{out} = 509K\Omega$.

Now using Script1 the approximate values of the Improved Wilson current mirror are as follows:

iii) BJT improved Wilson current mirror's output impedance (from Equation 2.27):

$r_{out} = 250K\Omega$;

iv) CMOS improved Wilson current mirror's output impedance (from Equation 2.28):

$r_{out} = 494K\Omega$.

Now using Script2, as explained previously the β of the improved Wilson current mirror was increased from 1 to 10,000 the graph (Figure 2-15) below shows changes in the output impedance as the value of β is increased:

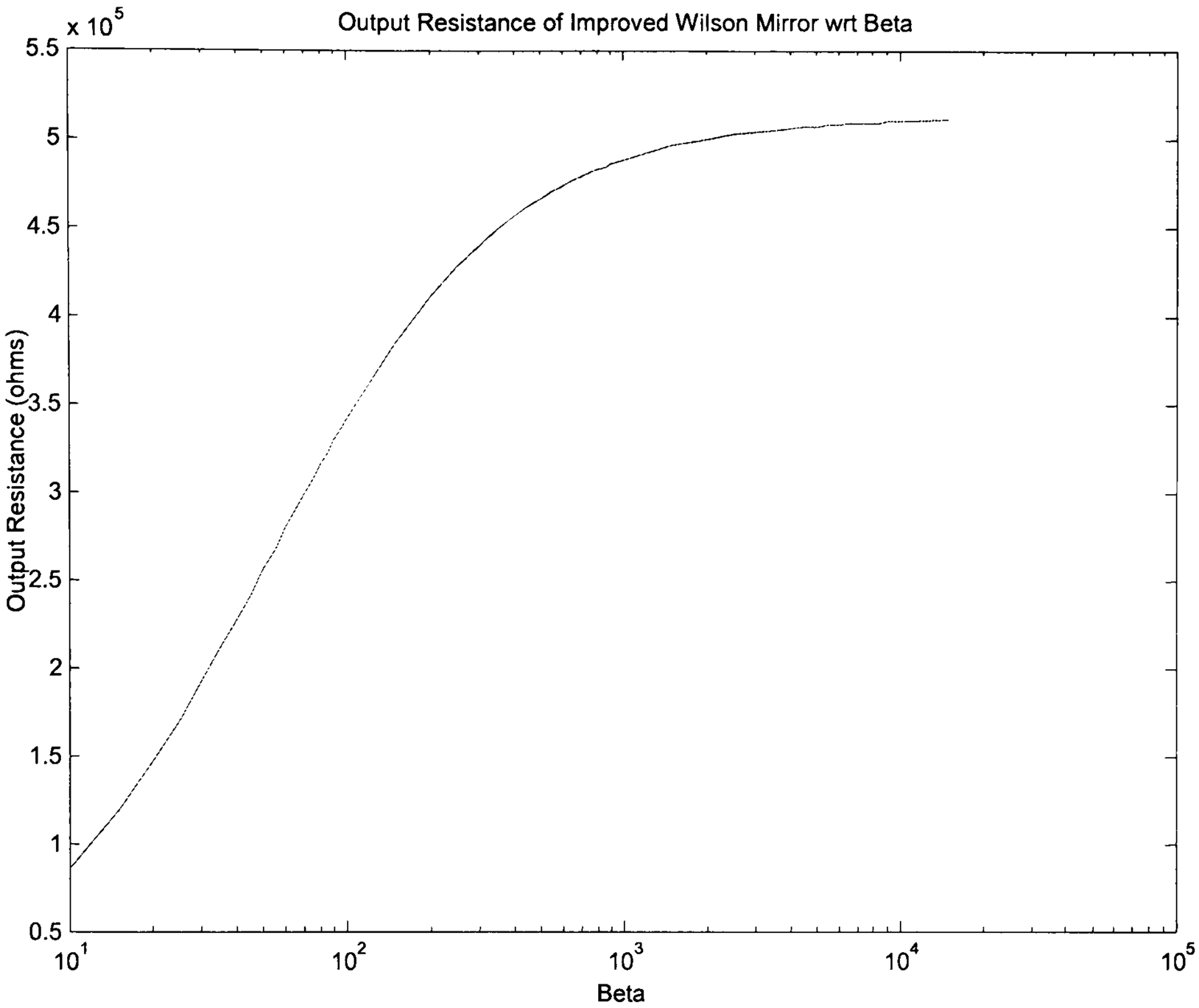

Figure 2-15: The effects of a transistors β on the output impedance of an Improved Wilson Current Mirror.

Figure 2-15 shows that as β increases the output impedance of the current mirror increases and reaches 494KΩ as β approaches infinity, taking into account that the transconductance and output impedance of the transistors match. This impedance has dropped by half compared to that of a cascode or Wilson current mirror. However, this type of circuit has the advantage of being more symmetrical than the previous current mirrors so current is more precisely copied from input to output.

2.4.5 The Regulated Cascode Current Mirror

The regulated cascode current mirror **[2-13]**, uses the same building blocks as the cascode current mirror shown in Figure 2-7a, except another transistor (T4) is added, and is connected to the emitter and base of T3, unlike the cascode current mirror which is biased by a fixed voltage, transistor T4 regulates the bias voltage on the base of T3 using a fixed bias current through T4's collector/emitter.

As current Iout increases it forces transistor T2 collector/emitter voltage to rise this has the effect of increasing the base/emitter of T4, as T4 has a fixed current this forces the base of T3 to drop, this has the overall effect of reducing the base/emitter voltage of T3, shutting down the current flow through to T2 and constrains Iout which effectively increases the output impedance.

For the regulated cascode current mirror to work another fixed current supply above that of the input current Iin is needed. This Ibias current does not have to match the input current Iin but must be high enough to bias transistors T3 and T4.

Note: Unlike the Wilson and Improved Wilson current mirrors the input current is not part of the feedback path.

Figures 2-16a and b below show two implementations of the regulated cascode current mirror which will be analysed to obtain its main characteristics:

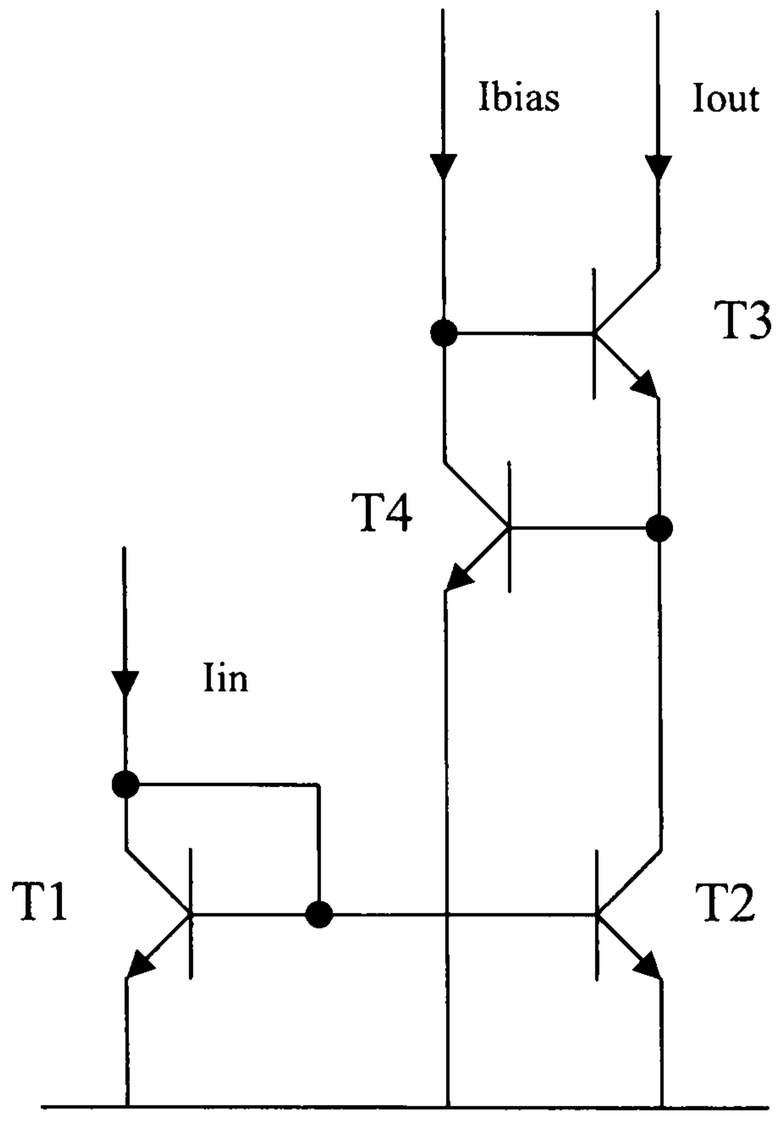

Figure 2-16a: A BJT Regulated Cascode Current Mirror.

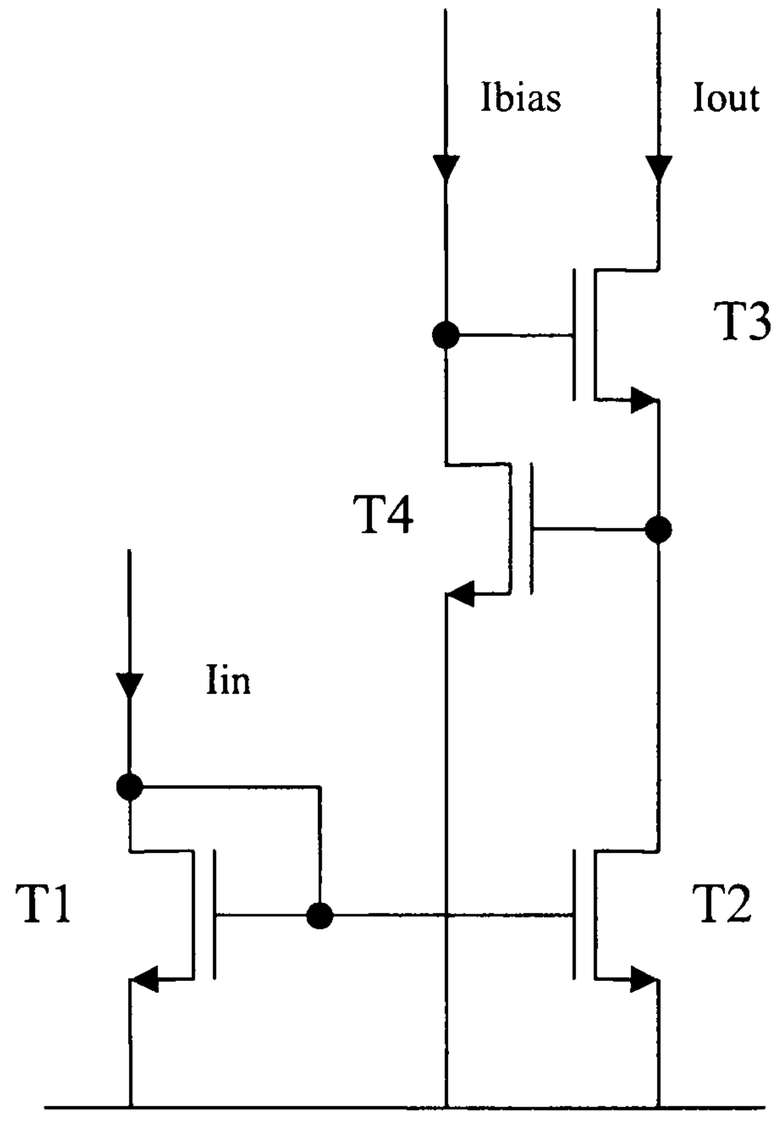

Figure 2-16b: A CMOS Regulated Cascode Current Mirror.

2.4.5.1 Analysis of Output Impedance

From Figures 2-16a and b the following equivalent small signal model of the current mirror can be drawn, shown in Figure 2-17 below:

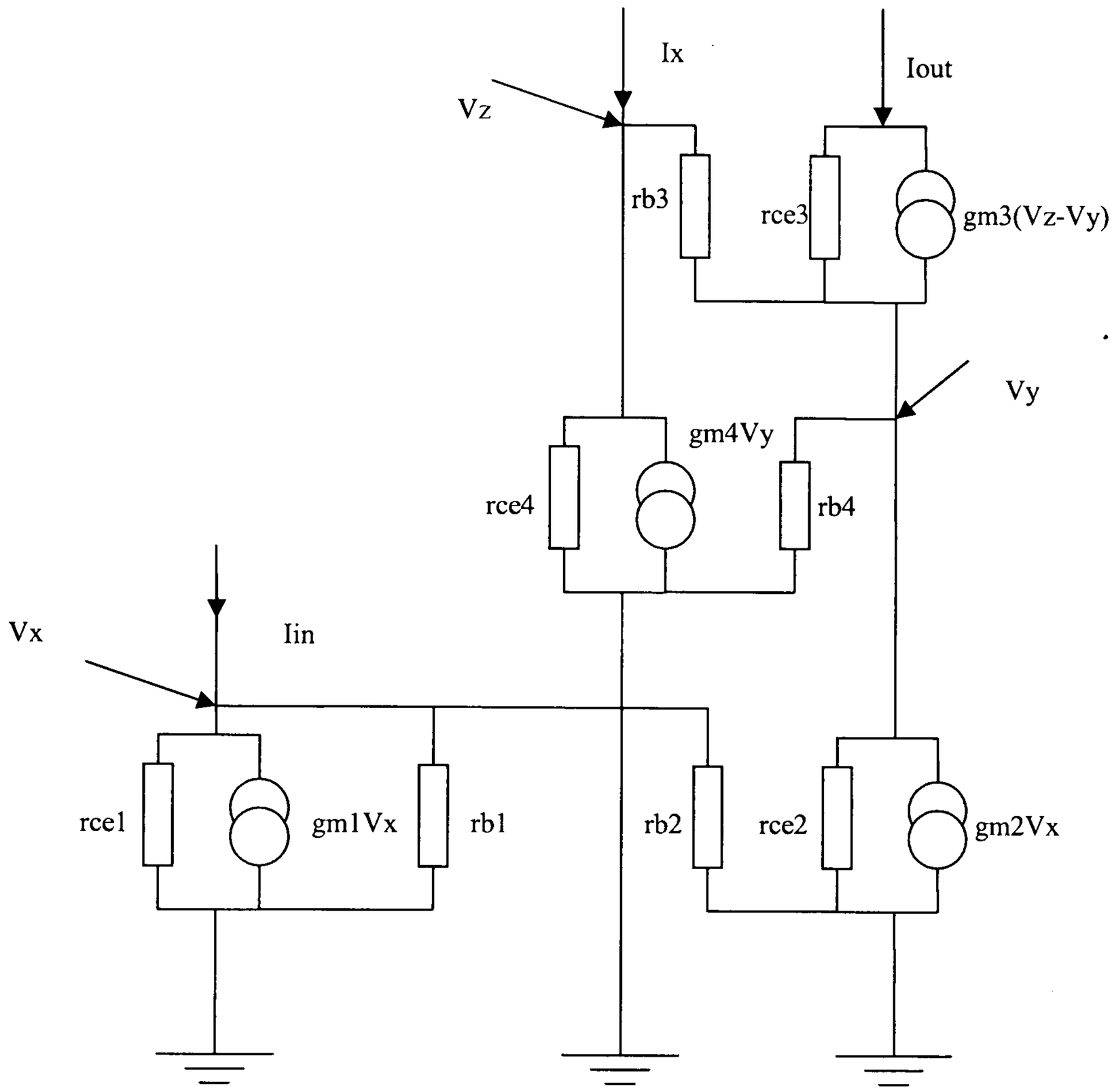

Figure 2-17: Small Signal Equivalent Model of the Regulated Cascode Current Mirror.

From Figure 2-17 assuming Iin is an ideal current source:

Iin = 0 ; Vx = 0; (AC small Signal)

Then:

$$\frac{Vout}{Iout} = r_{out} = r_{ce3} + Bgy - gm_3.Bgz.Bgy.r_{ce3} + gm_3.Bgy.r_{ce3} \qquad (2.29)$$

where:

$$Bgy = \frac{r_{ce2}.\beta_4.\beta_3}{(\beta_4.\beta_3 - gm_3.Bgz.\beta_4.r_{ce2} + gm_3.\beta_4.r_{ce2} + \beta_3.gm_4.r_{ce2})} \qquad (2.30)$$

$$Bgz = \frac{gm_3.r_{ce4} - gm_4.\beta_3.r_{ce4}}{gm_3.r_{ce4} + \beta_3} \qquad (2.31)$$

Equation 2.29 represents the exact value of the output impedance of the regulated cascode current mirror using BJT devices. So From (2.29) simplifying the equation the approximate output impedance of the current mirror using BJTs is:

$$r_{out} \approx \beta_3.r_{ce3} \qquad (2.32)$$

Referring to Figure 2-16b:

$\beta_1, \beta_2, \beta_3, \beta_4 \longrightarrow \infty$ (For a CMOS device)

So:

$$r_{out} \approx gm_3.gm_4.r_{ce4}.r_{ce2}.r_{ce3} \qquad (2.33)$$

From equation (2.32) that for the BJT equivalent the impedance has increased by a factor of β_3. The CMOS equivalent impedance has been increased by a factor of 'gm3.gm4.rce4.rce3' shown in equation (2.33).

2.4.5.2 Matlab Results

To give a better idea of how the BJT and CMOS transistor affects the regulated cascode current mirrors' output impedance, a Matlab model was designed using equations (2.29 to 2.31) shown in Section 2.4.5.1. The scripts for this are shown in the Appendices at the end of this chapter.

But two scripts were written:

1) To Show the differences in impedance with BJTs set to a β of 50, and CMOS transistors where the value of β was set to 10,000. The transconductance and their output impedances were set to the same values for both types of current mirrors, these values are arbitrary and are shown in the Appendix at the end of this chapter.
2) To show the effects on the output impedance of the current mirror, by increasing β from 1 to 1,000,000 ie. moving from a BJT current mirror to a CMOS current mirror. This is higher than the other versions of the current mirror analysis, this is because the output impedance of the regulated cascode current mirror is more sensitive to the smaller values of β.

The results from Script1 are as follows:

i) BJT regulated cascode current mirror's output impedance (from Equation 2.29):

$$r_{out} = 488K\Omega$$

ii) CMOS regulated cascode current mirror's output impedance (from Equation 2.32):

$$r_{out} = 99.8M\Omega$$

Now using Script1 the approximate values of the regulated cascode current mirror are as follows:

iii) BJT regulated cascode current mirror's output impedance (from Equation 2.29):

$$r_{out} = 500K\Omega$$

iv) CMOS regulated cascode current mirror's output impedance (from Equation 2.33):

$$r_{out} = 100M\Omega$$

Clearly the regulated cascode current mirror does not offer any improvement in output for the BJT circuit . However, the CMOS realization is significantly better.

Now using Script2 as explained previously the β of the regulated cascode current mirror was increased from 1 to 1,000,000 the graph (Figure 2-18) below shows changes in the output impedance as the value of β is increased:

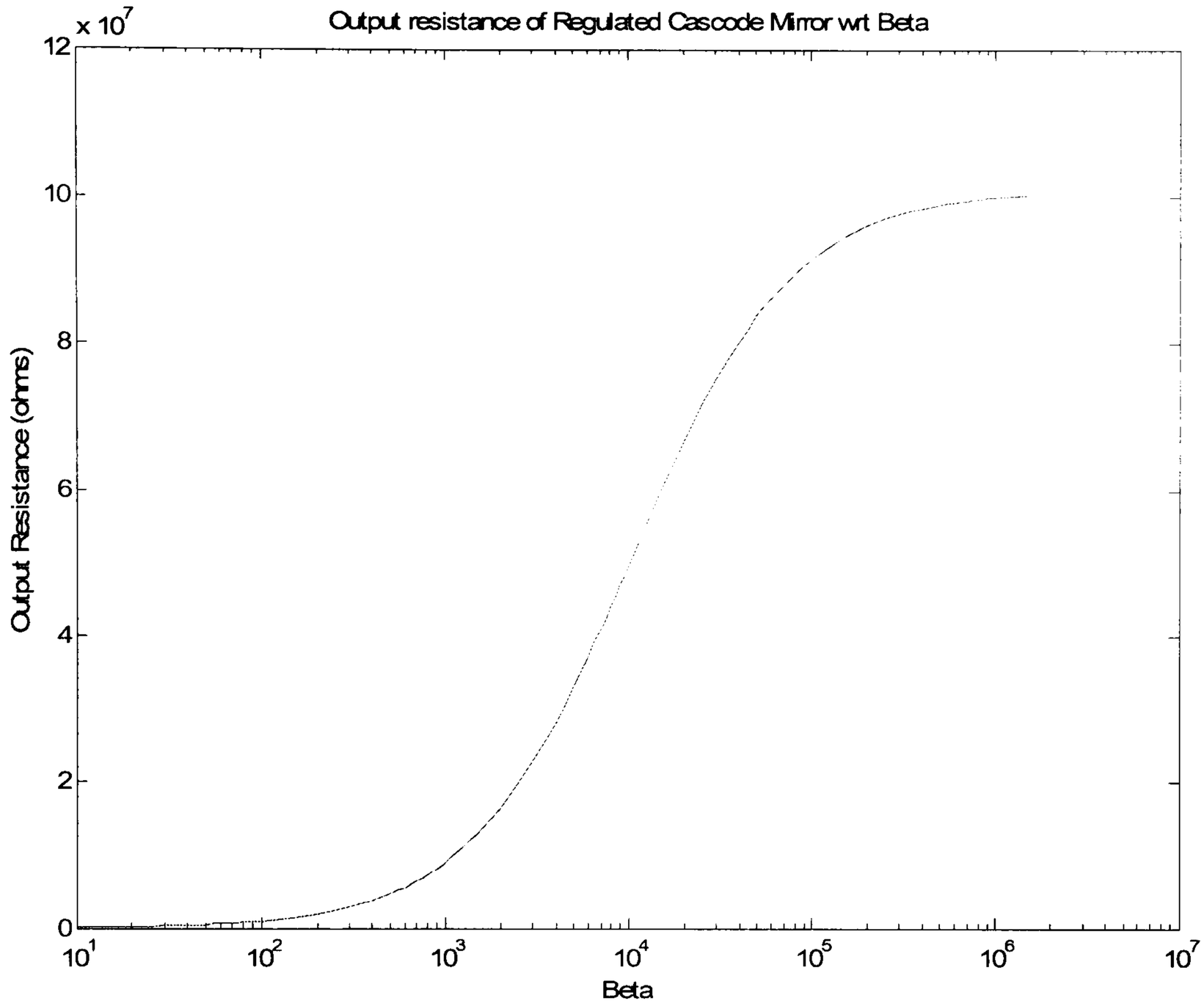

Figure 2-18: The effects of a transistors β on the output impedance of a Regulated Cascode Current Mirror.

Figure 2-18 shows that as β is increased the output impedance of the current mirror increases, reaching $100\text{M}\Omega$ as β approaches infinity, taking into account that the transconductance and output impedance of the transistors match. This is a 100 times increase in impedance on the Cascode and Wilson mirror if implemented in CMOS.

2.5 Simulation of Current Mirrors using CMOS devices

As the aim of this research is to design a current conveyor using CMOS transistors. Many of the simulations were undertaken on all the current mirrors analysed in Section 2.4. These simulations used the models from the TSMC 0.18μm process **[2-14]**. To give a fair comparison of all the current mirror architectures, all transistors in the design were identical in their dimensions were that of:

Width = 20μm

Length = 0.18μm

All test circuits used an input current of 1mA and an output voltage of 1.8V, these figures were taken from a high frequency transceiver 1mA being the source reference current.

2.5.1 A Simple Current Mirror

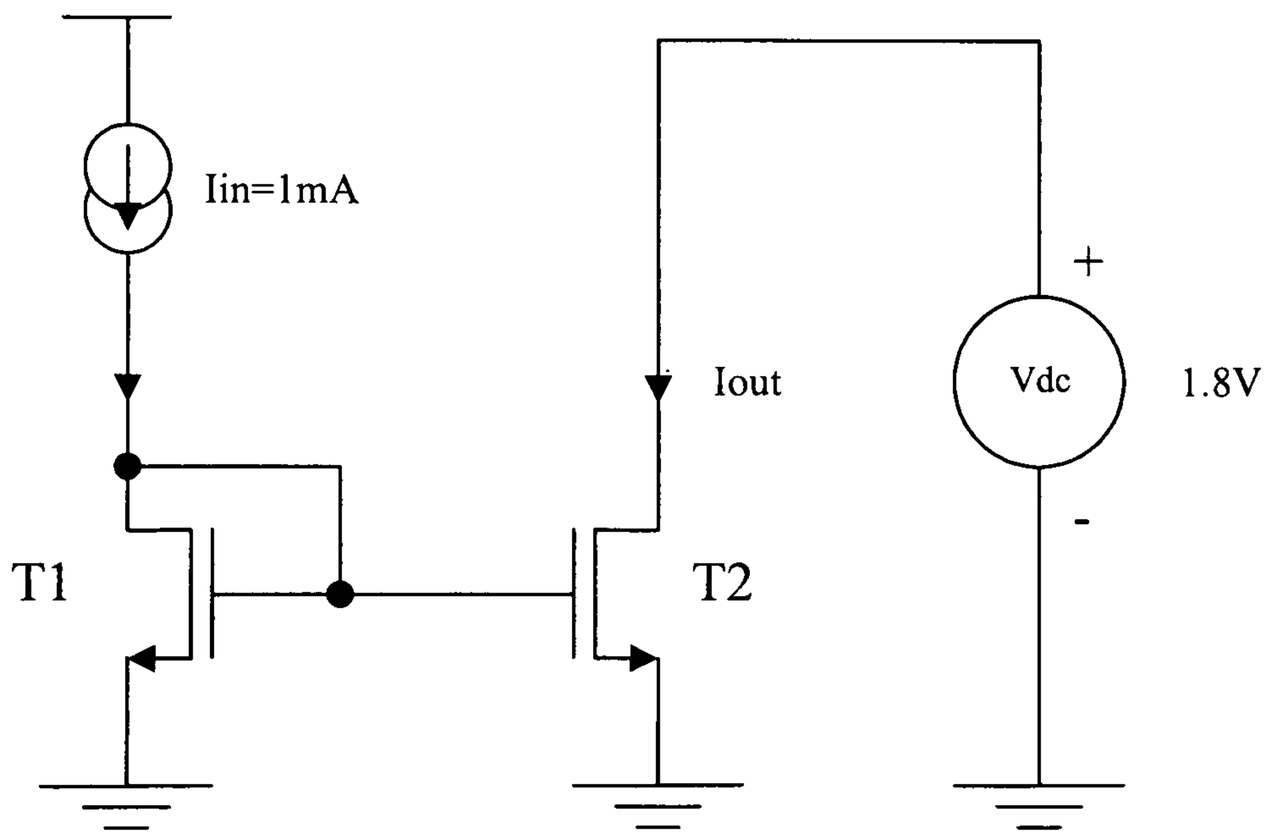

Figure 2-19: The test circuit for the simple current mirror.

Figure 2-19 shows the test circuit used to measure the current mirror accuracy and the output impedance of the current mirror. From this the following results were obtained:

1) Input current (DC) = 1mA (from ideal source)
2) Output current (DC) = 1.6mA.
3) Output impedance = 2.07KΩ (dropping to 1.42KΩ @ 316MHz)

Note: This was used to bench mark the rest of the current mirrors that were tested.

2.5.2 The Cascode Current Mirror

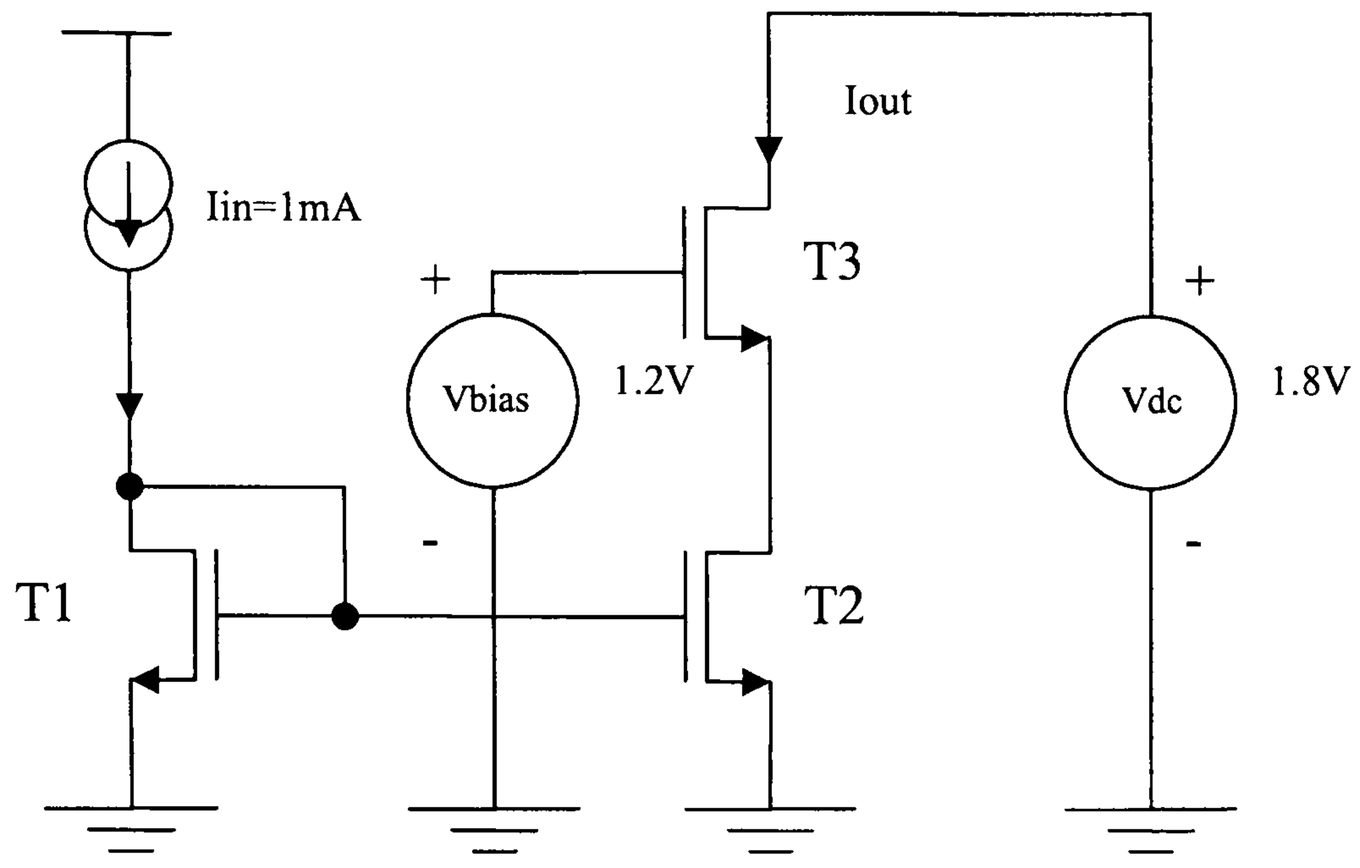

Figure 2-20: The test circuit for the cascode current mirror.

Figure 2-20 shows the test circuit used to measure the current mirror accuracy and the output impedance of the cascode current mirror.

From this the following results were obtained:

1) Input current (DC) = 1mA (from ideal source)
2) Output current (DC) = 1.05mA.
3) Output impedance = 129KΩ (dropping to 100KΩ @ 4.5MHz)

2.5.3 The Wilson Current Mirror

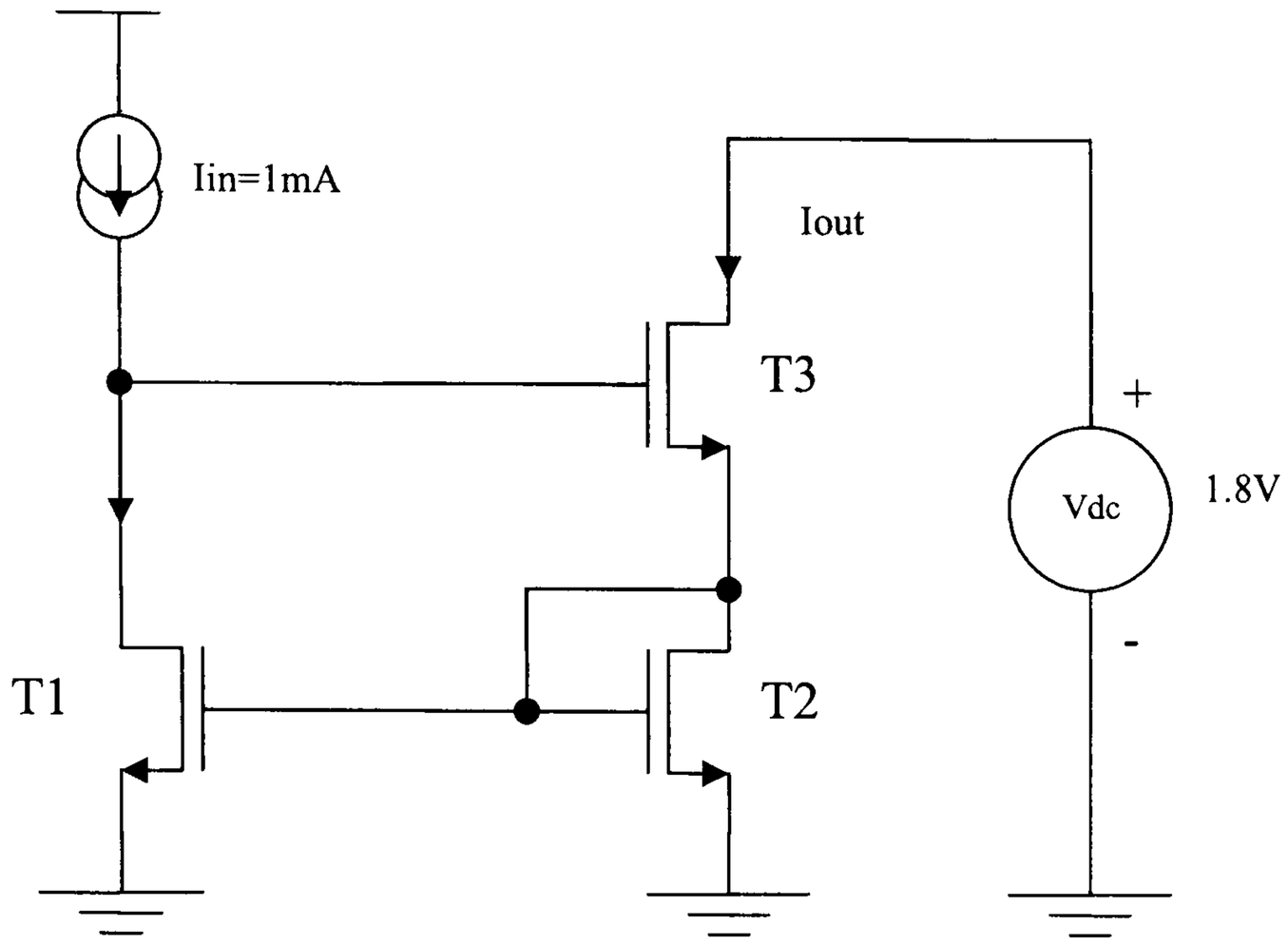

Figure 2-21: The test circuit for the Wilson current mirror.

Figure 2-21 shows the test circuit used to measure the current mirror accuracy and the output impedance of the Wilson current mirror.

From this the following results were obtained:

1) Input current (DC) = 1mA (from ideal source)
2) Output current (DC) = 0.775mA.
3) Output impedance = 130KΩ (dropping to 100KΩ @ 4.45MHz)

2.5.4 The Improved Wilson Current Mirror

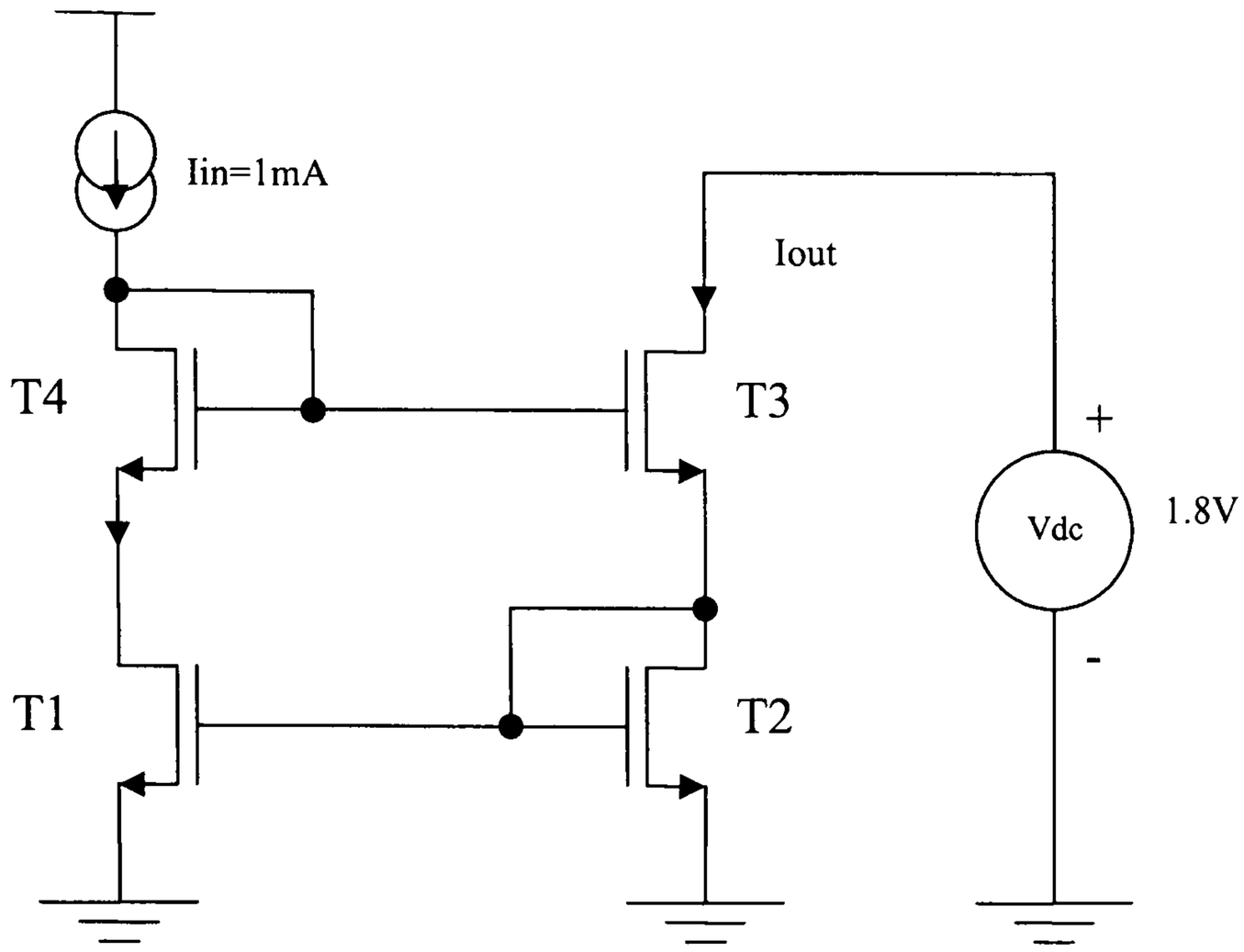

Figure 2-22: The test circuit for the improved Wilson current mirror.

Figure 2-22 shows the test circuit used to measure the current mirror accuracy and the output impedance of the improved Wilson current mirror.

From this the following results were obtained:

1) Input current (DC) = 1mA (from ideal source)
2) Output current (DC) = 1mA.
3) Output impedance = 93.8KΩ dropping to 50KΩ @ 10.9MHz)

2.5.5 The Regulated Cascode Current Mirror

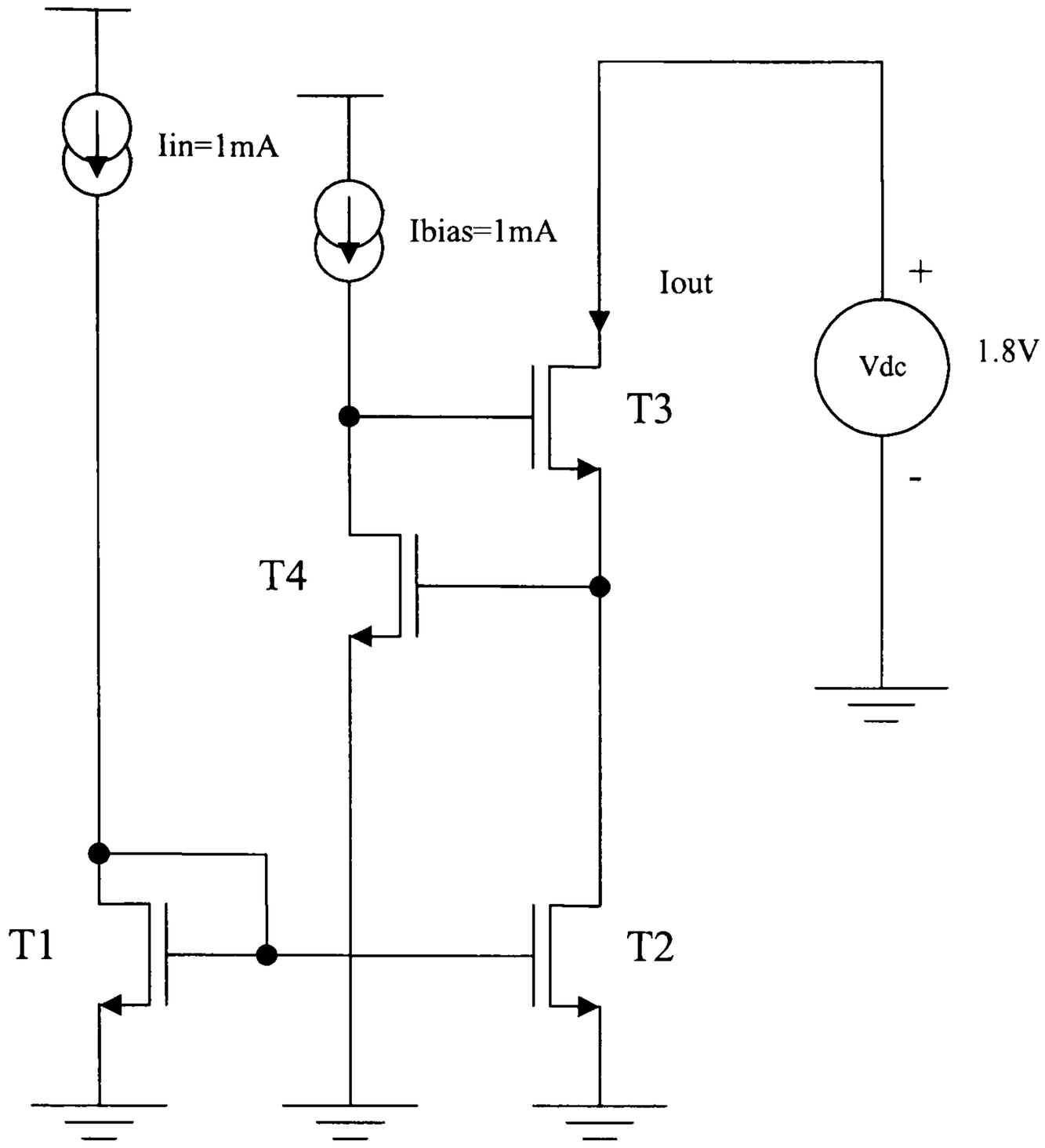

Figure 2-22: The test circuit for the regulated cascode current mirror.

Figure 2-22 shows the test circuit used to measure the current mirror accuracy and the output impedance of the regulated cascode current mirror.

From this the following results were obtained:

1) Input current (DC) = 1mA (from ideal source)
2) Output current (DC) = 0.993mA.
3) Output impedance = 1.49MΩ (dropping to 1MΩ@ 758KHz)

2.6 Review of Results

To help summarise the results the following table below was drawn up based on all the transistors having the same gm, and r_{ds}/r_{ce} parameters.

Table 2-2: Summary of the characteristics of the current mirror (part1)

	Simple Mirror	Cascode Mirror	Wilson Mirror
BJT Equation	**rce**	**β .rce**	**β .rce/2**
CMOS Equation	**rds**	**gm.rds^2**	**gm.rds^2**
Matlab: BJT results	**N/A**	**500KΩ**	**250KΩ**
Matlab: CMOS results	**N/A**	**1MΩ**	**1MΩ**
Spice: CMOS results	**1.42kΩ**	**129KΩ**	**130KΩ**
Spice: The current seen at the output as a % of the input.	**160**	**105**	**77.5**

Table 2-3: Summary of the characteristics of the current mirror (part2)

	Improved Wilson Mirror	Regulated Cascode Mirror	
BJT Equation	**β .rce/2**	**β .rce**	
CMOS Equation	**gm.rds^2**	**gm^2.rds^3**	
Matlab: BJT results	**250KΩ**	**500KΩ**	
Matlab: CMOS results	**494KΩ**	**100MΩ**	
Spice: CMOS results	**93.8KΩ**	**1.49MΩ**	
Spice: The current seen at the output as a % of the input.	**100**	**99.3**	

Tables 2-2 and 2-3 shows the relative characteristics of the five current mirrors studied simplifying comparisons made in this chapter.

Firstly it can be noted that using CMOS devices can improve the output impedance dramatically by using these architectures, where BJT devices can only improve their output impedance by a factor of β.

As can be seen from Table 2-2 and Table 2-3 the regulated cascode current mirror exhibits the highest value of output impedance by a factor of over 100 times the closest rival.

Also to note is the DC copying capability of the current mirrors, and this shows up the need to improve the output impedance of the current mirror, as the simple current mirror had copied 160% of the original input current due to the extra current through the Drain/Source resistance of the output transistor of the current mirror. The cascode current mirror had improved this figure to only 105% of the input current, and the Improved Wilson and regulated cascode current mirror had got this figure close to the desired 100% of the input current. Only the Wilson current mirror suffered with only copying 77.5% of the input current, this was due to the fact that the input transistor to the current mirror was not diode connected and the input current was then split between the Drain/Source resistance and its DC current generator, as only the DC current generator is copied, 22.5% of the current (in this example) was lost through its Drain/Source resistance and was not copied to the output of the current mirror. This high percentage loss in the accuracy of the Wilson current mirror was due to the channel modulation effect of the CMOS transistors used in the simulation.

Another factor to take into account is the bandwidth of each of the current mirrors, this will be explained in more detail in Chapter Four, but because each transistor is limited (due to process) by its Gate/Source, Gate/Drain capacitance its inherent bandwidth is limited by its output impedance (equivalent to a RC low pass network), in simple terms as the output impedance of the current mirror increases its bandwidth drops, so for a high bandwidth current mirror then the best type would be a simple current mirror and for a low bandwidth high accurate current mirror a regulated cascode current mirror would be best. In reality a compromise would have to be made.

To summarize when choosing a current mirror for a current conveyor it is important to take into account its application. For example a high bandwidth conveyor may use a simple current mirror as its follower, but an audio application would use a regulated cascode current follower which is less susceptible to noise on the power supply, but does not have a high bandwidth requirement.

2.7 References

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APPENDIX 2

(APP 2.1) Detail Analysis of Current Mirrors.

(APP 2.1.1) The Cascode Current Mirror.

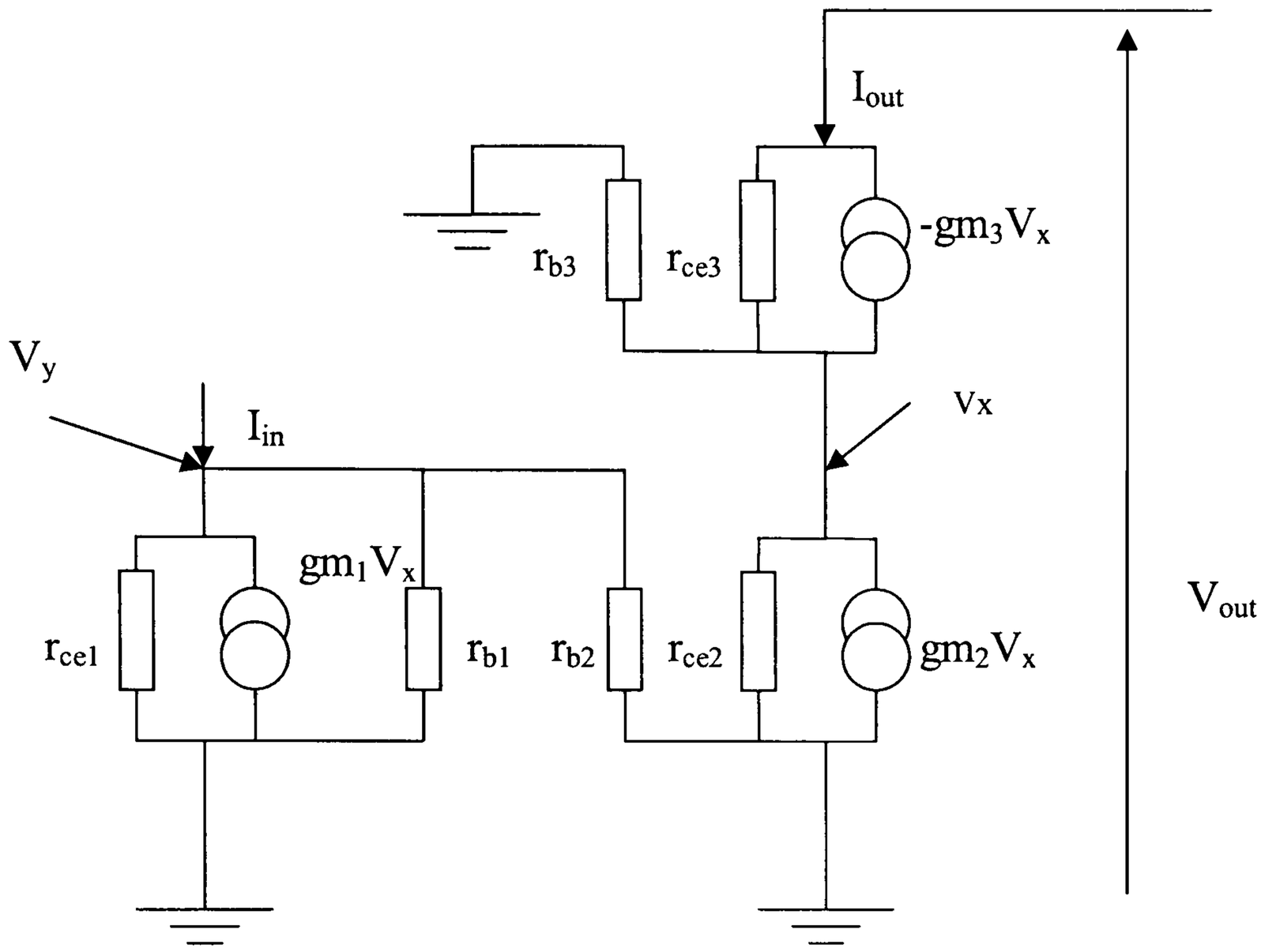

Figure AP.2.1 The cascode current mirror small signal model

$I_{in} = 0$ (For AC small Signal);

so:

$$I_{out} + i_{b3} = gm_2.V_y + \frac{V_x}{r_{ce2}}$$

$$I_{out} = \frac{V_{out} - V_x}{r_{ce3}} - gm_3.V_x \qquad \textbf{(APP-1)}$$

and:

$$I_{out}.r_{ce3} = V_{out} - V_x - gm_3.r_{ce3}.V_x$$

$$V_x(1 + gm_3.r_{ce3}) = V_{out} - V_x - I_{out}.r_{ce3}$$

$$V_x = \frac{V_{out} - I_{out}.r_{ce3}}{(1 + gm_3.r_{ce3})} \qquad \textbf{(APP-2)}$$

looking at transistor M2:

$$I_{out} + i_{b3} = gm_2.V_y + \frac{V_x}{r_{ce2}}$$

$$I_{out} + \frac{gm_3.V_x}{\beta_3} = gm_2.V_y + \frac{V_x}{r_{ce2}}$$

re-arranging:

$$gm_2.\beta_3.r_{ce2}.V_y = I_{out}.\beta_3.r_{ce2} - gm_3.r_{ce2}.V_x - \beta_3.V_x$$

$$V_y = I_{out}.\beta_3.r_{ce2} + \frac{V_x(gm_3.r_{ce2} + \beta_3)}{gm_2.\beta_3.r_{ce2}} \quad \textbf{(APP-3)}$$

from (APP-3):

$$V_y.gm_2.\beta_3.r_{ce2} = I_{out}.\beta_3.r_{ce2} + V_x(gm_3.r_{ce2} + \beta_3)$$

$$V_x = \frac{I_{out}.\beta_3.r_{ce2} + V_y.gm_2.\beta_3.r_{ce2}}{(gm_3.r_{ce2} + \beta_3)}$$

let V_y=0 (AC: As It comes from an ideal source.)

so:

$$V_x = \frac{I_{out}.\beta_3.r_{ce2}}{(gm_3.r_{ce2} + \beta_3)} \quad \textbf{(APP-4)}$$

from (APP-2), (APP-4)

$$\frac{V_{out} - I_{out}.r_{ce3}}{(1 + gm_3.r_{ce3})} = \frac{I_{out}.\beta_3.r_{ce2}}{(gm_3.r_{ce2} + \beta_3)}$$

$$\frac{V_{out}}{I_{out}} = R_{out} = r_{ce3} + \frac{\beta_3.r_{ce2}(1 + gm_3.r_{ce3})}{(gm_3.r_{ce2} + \beta_3)}$$

(APP 2.1.2) The Wilson Current Mirror.

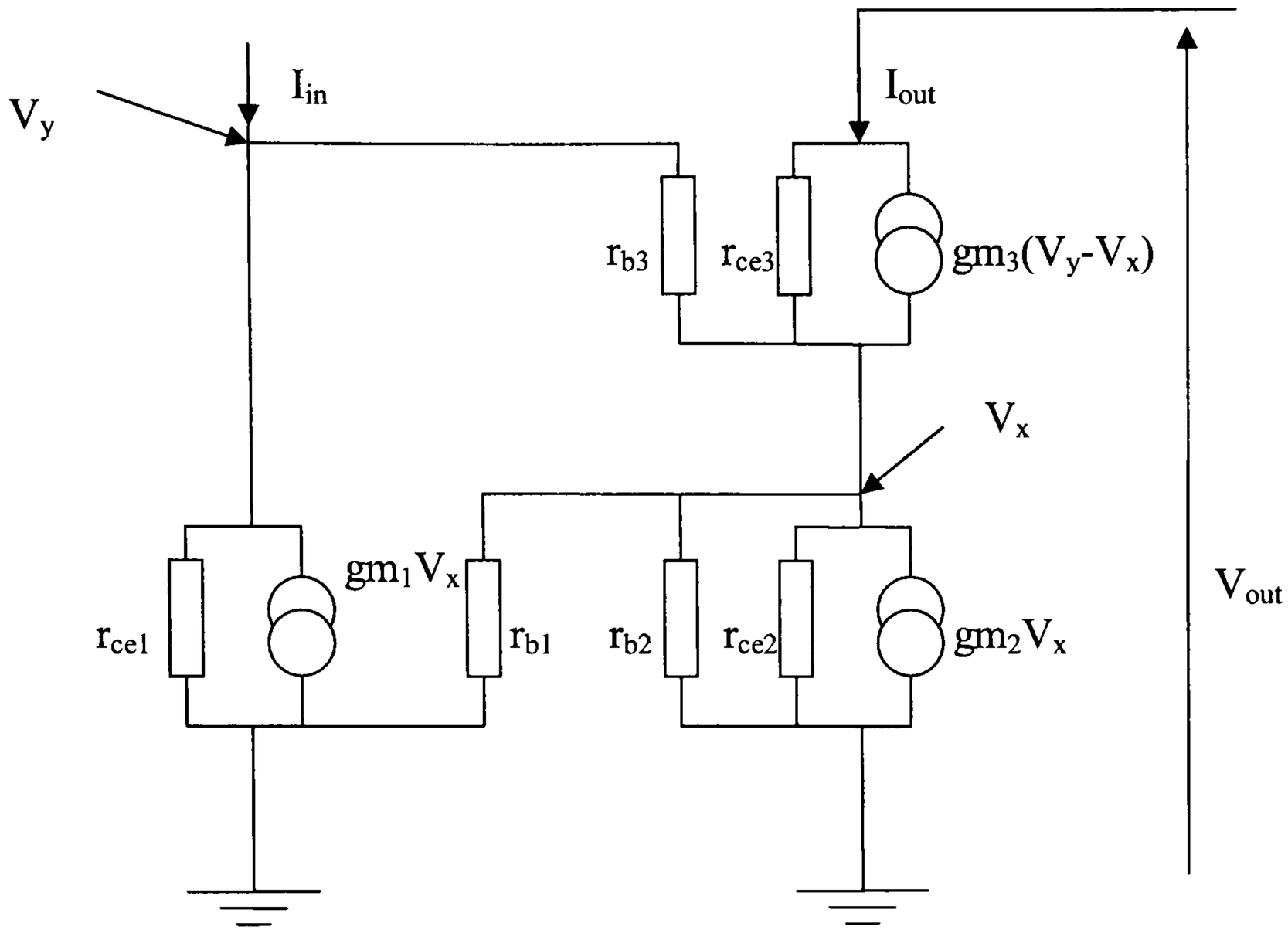

Figure AP.2.2 The Wilson Current Mirror small signal model

$$I_{out} = gm_3(V_y - V_x) + \frac{(V_{out} - V_y)}{r_{ce3}} \qquad \textbf{(APP-5)}$$

$$I_{in} + i_{b3} = \frac{V_y}{r_{ce1}} + gm_1.V_x + i_{b3} \qquad \textbf{(APP-6)}$$

$$i_{b3} + I_{out} = I_x + gm_2.V_x + \frac{V_x}{r_{ce2}} \qquad \textbf{(APP-7)}$$

$$I_x = \frac{gm_1.V_x}{\beta_1} + \frac{gm_2.V_x}{\beta_2} \qquad \textbf{(APP-8)}$$

from (APP-6) In=0 (AC small Signal)

$$\frac{V_y}{r_{ce1}} + gm_1.V_x = -i_{b3} \qquad \textbf{(APP-9)}$$

and:

$$ib_3.\beta_3 = gm_3(V_y - V_x) \qquad \textbf{(APP-10)}$$

from (APP-9) and (APP-10)

$$\frac{V_y}{r_{ce1}} + gm_1.V_x = \frac{gm_3.V_x}{\beta_3} - \frac{gm_3.V_y}{\beta_3}$$

re-arranging:

$$V_y = (\frac{gm_3.r_{ce1} - gm_1.\beta_3.r_{ce1}}{(\beta_3 + gm_3.r_{ce1})}).V_x$$

let $Bgy = (\frac{gm_3.r_{ce1} - gm_1.\beta_3.r_{ce1}}{(\beta_3 + gm_3.r_{ce1})})$

so:

$$Vy = Bgy.Vx \qquad \textbf{(APP-11)}$$

from (APP-10) and (APP-11)

$$i_{b3} = \frac{gm_3(V_y - V_x)}{\beta_3}$$

$$i_{b3} = \frac{gm_3.V_x(Bgy - 1)}{\beta_3} \qquad \textbf{(APP-12)}$$

from (APP-7),(APP-8),(APP-12)

$$\frac{gm_3.V_x(Bgy - 1)}{\beta_3} + I_{out} = \frac{gm_3.V_x}{\beta_1} + \frac{gm_2.V_x}{\beta_2} + gm_2.V_x + \frac{V_x}{r_{ce2}}$$

re-arranging:

$$V_x = \frac{\beta_3.\beta_2.\beta_1.r_{ce2}}{(gm_1.\beta_2.\beta_3.r_{ce2} + gm_2.\beta_1.\beta_3.r_{ce2} + gm_2.\beta_1.\beta_2.\beta_3.r_{ce2} + \beta_1.\beta_2.\beta_3 - gm_3.\beta_1.\beta_2.r_{ce2}(Bgy - 1))}.I_{out}$$

let $Bgx = \frac{\beta_3.\beta_2.\beta_1.r_{ce2}}{(gm_1.\beta_2.\beta_3.r_{ce2} + gm_2.\beta_1.\beta_3.r_{ce2} + gm_2.\beta_1.\beta_2.\beta_3.r_{ce2} + \beta_1.\beta_2.\beta_3 - gm_3.\beta_1.\beta_2.r_{ce2}(Bgy - 1))}$

so:

$$V_x = Bgx.I_{out} \qquad \textbf{(APP-13)}$$

from (APP-13),(APP-12),(APP-5)

$$I_{out} = gm_3(Bgy.V_x - V_x) + \frac{(V_{out} - V_x)}{r_{ce3}}$$

re-arranging:

$$\frac{V_{out}}{I_{out}} = R_{out} = r_{ce3} + gm_3.Bgy.Bgx.r_{ce3} + Bgx.gm_3.r_{ce3} + Bgx$$

(APP 2.1.3) The Improved Wilson Current Mirror.

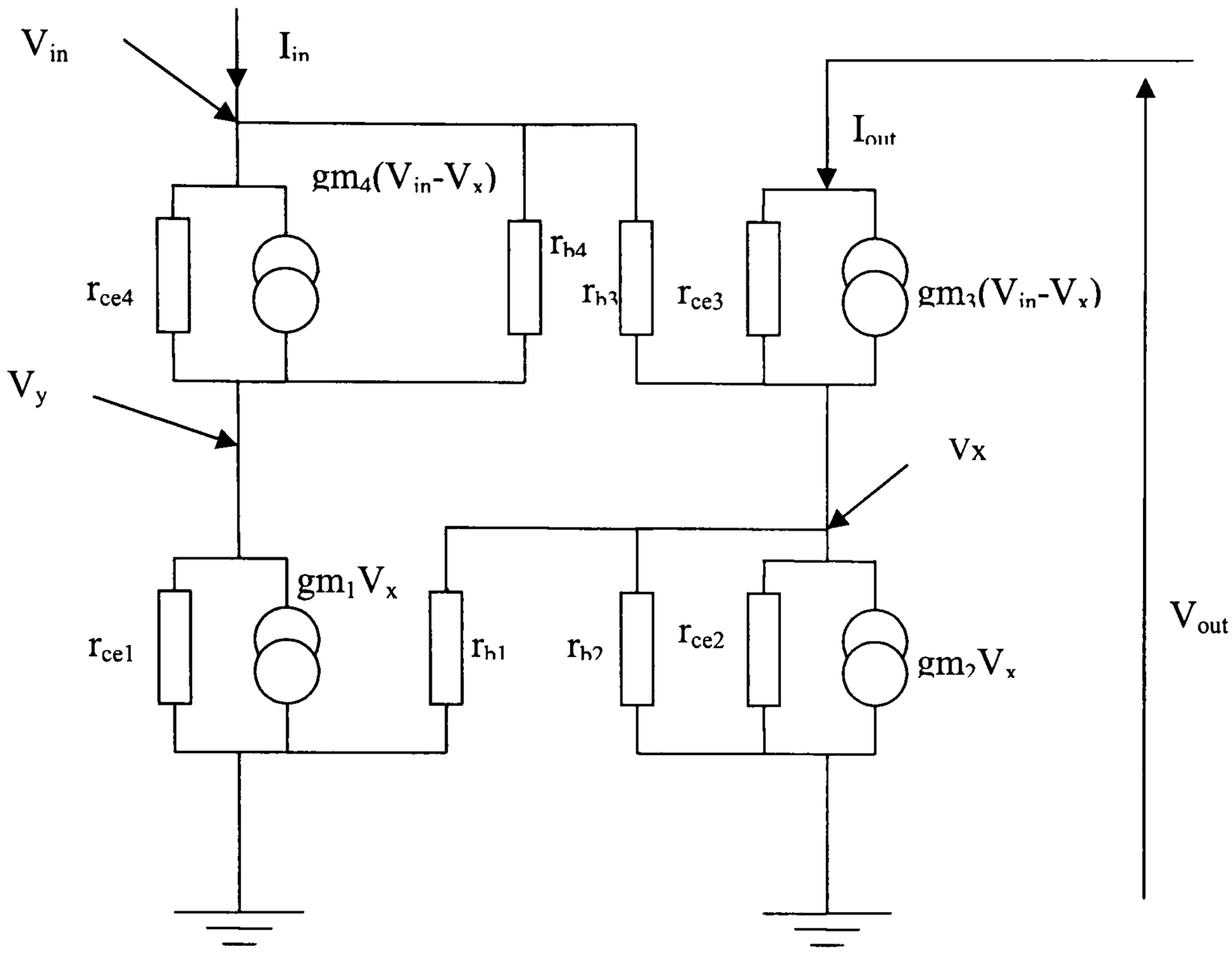

Figure AP.2.3 The Improved Wilson Current Mirror Small Signal Model

$$-i_{b3} = \frac{V_{in} - V_y}{Rd1} \qquad \textbf{(APP-14)}$$

where:

$$Rd1 = \frac{r_{ce1}.\beta_1}{(\beta_1 + gm_1.r_{ce1}.\beta_1 + gm_1.r_{ce1})} \qquad \textbf{(APP-14a)}$$

also:

$$I_{out} = \frac{V_{out} - V_x}{r_{ce3}} + gm_3(V_{in} - V_x)$$

$$I_{out}.r_{ce3} = V_{in} - V_x + gm_3.r_{ce3}.V_{in} - gm_3.r_{ce3}.V_x \qquad \textbf{(APP-15)}$$

and:

$$I_{d4} = I_{out} + i_{b3} - i_{b2} \qquad \textbf{(APP-16)}$$

from (APP-14a)

$$\frac{V_y - V_{in}}{Rd1} = \frac{gm_3(V_{in} - V_x)}{\beta_3}$$

$$V_{in} = \frac{V_y.\beta_3 + gm_3.Rd1.V_x}{\beta_3 + gm_3.Rd1}$$

let: $V_{in} = Bin(V_y.\beta_3 + gm_3.Rd1.V_x)$ **(APP-17)**

where:

$$Bin = \frac{1}{\beta_3 + gm_3.Rd1}$$

also:

$$\frac{V_y}{r_{ce2}} + gm_2.V_x = -i_{b3}$$ **(APP-18)**

from (APP-14),(APP-18)

$$\frac{V_y - V_{in}}{Rd1} = \frac{V_y}{r_{ce2}} + gm_2.V_x$$

re-arranging and substituting (APP-17) into (APP-14),(APP-18)

$$V_y = (\frac{gm_2.Rd1.r_{ce2} - Bin.gm_3.Rd1.r_{ce2}}{Bin.\beta_3.r_{ce2} - r_{ce2} - Rd1}).V_x$$

let:

$$By = (\frac{gm_2.Rd1.r_{ce2} - Bin.gm_3.Rd1.r_{ce2}}{Bin.\beta_3.r_{ce2} - r_{ce2} - Rd1})$$

so:

$$V_y = By.V_x$$ **(APP-19)**

from (APP-16)

$$V_x = (I_{out} + i_{b3} - i_{b2})Rd4$$ **(APP-20)**

where

$$Rd4 = \frac{r_{ce4}.\beta_4}{(\beta_4 + gm_4.r_{ce4}.\beta_4 + gm_4.r_{ce4})}$$ **(APP-20a)**

substituting (APP-16),(APP-17) into (APP-20)

$$V_x = (I_{out} + \frac{Bin.By.\beta_3.V_x}{Rd1} + Bin.gm_3.V_x - \frac{By.V_x}{Rd1} - gm_2.V_x)Rd4$$

re-arranging:

$$V_x = \frac{I_{out}.Rd1.Rd4}{(Rd1 + By.Rd4 + gm_2.Rd1.Rd4 - Bin.By.\beta_3.Rd4 - Bin.gm_3.Rd1.Rd4)}$$

let:

$$Bx = \frac{Rd1.Rd4}{(Rd1 + By.Rd4 + gm_2.Rd1.Rd4 - Bin.By.\beta_3.Rd4 - Bin.gm_3.Rd1.Rd4)}$$

so:

$$V_x = Iout.Bx \qquad \textbf{(APP-21)}$$

from (APP-15),(APP-20),(APP-21)

$$I_{out}.r_{ce3} = V_{out} - I_{out}.Bx + gm_3.r_{ce3}(Bin.By.Bx.\beta_3.I_{out} + Bin.Bx.gm_3.Rd1.I_{out}) - gm_3.Bx.r_{ce3}.I_{out}$$

re-arranging:

$$\frac{V_{out}}{I_{out}} = R_{out} = r_{ce3} + Bx + gm_3.r_{ce3}.Bx(1 - Bin.By.\beta_3 - Bin.gm_3.Rd1)$$

(APP 2.1.4) The Regulated Cascode Current Mirror.

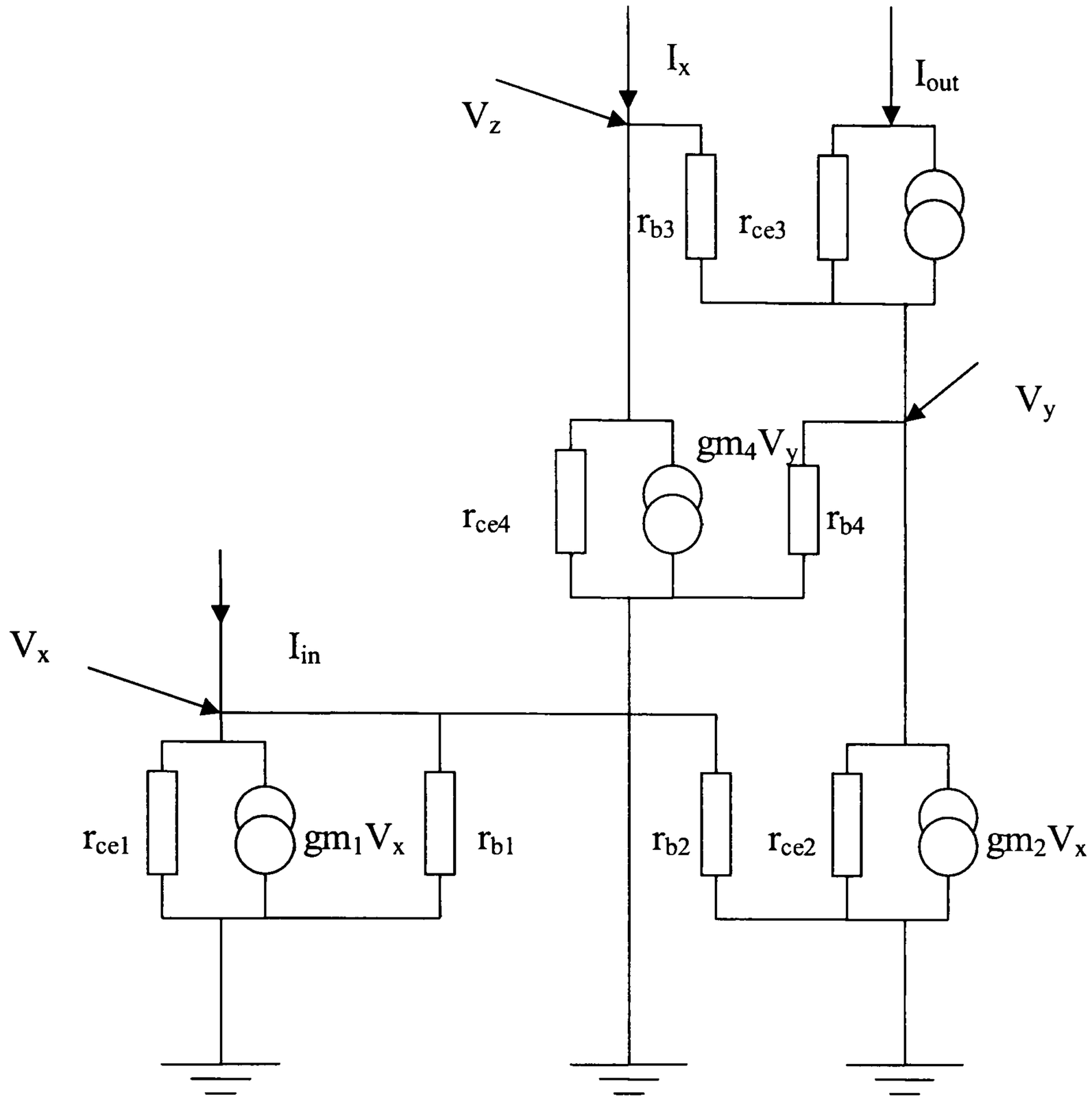

Figure AP.2.4 The regulated cascode current mirror small signal model

$$I_{in} = \frac{V_x}{r_{ce1}} + gm_1.V_x + \frac{gm_1.V_x}{\beta_1} + \frac{gm_2.V_x}{\beta_2} \qquad \textbf{(APP-22)}$$

$$I_x = i_{b3} + \frac{V_z}{r_{ce4}} + gm_4.V_y \qquad \textbf{(APP-23)}$$

$$I_2 = I_{out} + i_{b3} - i_{b4} \qquad \textbf{(APP-24)}$$

$$I_2 = \frac{V_y}{r_{ce2}} + gm_2.V_x \qquad \textbf{(APP-25)}$$

$$I_{out} = \frac{V_{out} - V_y}{r_{ce3}} + gm_3(V_z - V_y) \qquad \textbf{(APP-25a)}$$

assuming an ideal current source:

$I_{in} = 0,$ $V_x = 0$

also

$i_{b1} = i_{b2} = 0$ as $V_x = 0$

from (APP-22),(APP-23)

$$0 = \frac{gm_3.V_z}{\beta_3} - \frac{gm_3.V_y}{\beta_3} + gm_4.V_y + \frac{V_z}{r_{ce4}}$$

re-arranging

$$V_z = (\frac{gm_3.r_{ce4} - gm_4.\beta_3.r_{ce4}}{gm_3.r_{ce4} + \beta_3}).V_y$$

let $V_z = Bgz.V_y$ **(APP-26)**

where:

$$Bgz = \frac{gm_3.r_{ce4} - gm_4.\beta_3.r_{ce4}}{gm_3.r_{ce4} + \beta_3}$$

from (APP-24),(APP-25)

$$\frac{V_y}{r_{ce2}} = I_{out} + \frac{gm_3(V_z - V_y)}{\beta_3} - \frac{gm_4.V_y}{\beta_4}$$

substituting in (APP-26) and re-arranging

$$V_y = \frac{r_{ce2}.\beta_3.\beta_4.I_{out}}{\beta_4.\beta_3 - gm_3.Bgz.\beta_4.r_{ce2} + gm_3.\beta_4.r_{ce2} + \beta_3.gm_4.r_{ce2}}$$

let $V_y = Bgy.I_{out}$ **(APP-27)**

where:

$$Bgy = \frac{r_{ce2}.\beta_3.\beta_4}{\beta_4.\beta_3 - gm_3.Bgz.\beta_4.r_{ce2} + gm_3.\beta_4.r_{ce2} + \beta_3.gm_4.r_{ce2}}$$

from (APP-25a),(APP-26),(APP-27)

$$I_{out} = \frac{V_{out} - Bgy.I_{out}}{r_{ce3}} + gm_3(Bgz.Bgy.I_{out} - Bgy.I_{out})$$

so:

$$\frac{V_{out}}{I_{out}} = R_{out} = r_{ce3} + Bgy - gm_3.Bgz.Bgy.r_{ce3} + gm_3.Bgy.r_{ce3}$$

(APP 2.2) The MATLAB Source Files.

(APP 2.2.1) The Cascode Current Mirror.

```
%Wilson Current Mirror output impedance calculator
%Please refer to Wilson current mirror document.

%Set up plots for graph
plot_decade = 10;       % Define first Beta point
plot_points_per_dec = 20        % points per decade
plot_step = 0;          % Reset for first plot point
max_beta  = 10000      % To maximum beta value

%Set up Results matrix
%with first value
index = 1

%initialise
%Beta_First_Point = plot_decade
Beta_First_Point = 50
Beta_Point = plot_decade

while (Beta_Point <= max_beta)
% Update new Beta
  if (plot_step == 0)                % plot first point
    Beta_Point = plot_decade;
    plot_step = plot_step + 1;
  elseif (plot_step < plot_points_per_dec)
    % Avoid calculating below the decade plot point
    if (plot_step*((1/plot_points_per_dec)*plot_decade*10) <=
plot_decade)
      plot_step = plot_step + round(plot_points_per_dec/10);
    end
    Beta_Point = plot_step*((1/plot_points_per_dec)*plot_decade*10);
    plot_step = plot_step + 1;
  else
    plot_decade = plot_decade*10;  % jump to next decade
    plot_step = 1;
    Beta_Point = plot_decade;
  end


%Transconductance
gm1 = 10e-3; %A/V;
gm2 = 10e-3; %A/V;
gm3 = 10e-3; %A/V;

%Beta VAlues
B1 = Beta_Point
B2 = Beta_Point;
B3 = Beta_Point;

%rds/rce values
rce1 = 10e3; %Ohms
rce2 = 10e3; %Ohms
rce3 = 10e3; %Ohms

%Output inpedence
Absolute_Rout = rce3 + (B3*rce2*(1+(gm3*rce3))/((gm3*rce2)+B3))

%Store Results
```

```
results(index,1) = Beta_Point;
results(index,2) = Absolute_Rout;
index = index + 1;

end    % Simulation end

%plot results
semilogx(results(:,1),results(:,2),'-')
Xlabel ('Beta')
YLabel ('Output Resistance (ohms)')
title ('Output resistance of Cascode Mirror wrt Beta')
%gset logscale x 10    % set x-axis to log base 10
%gplot [Beta_First_Point:max_beta] results with lines
```

(APP 2.2.2) The Wilson Current Mirror.

```
%Wilson Current Mirror output impedance calculator
%Please refer to Wilson current mirror document.

%Set up plots for graph
plot_decade = 10;       % Define first Beta point
plot_points_per_dec = 20        % points per decade
plot_step = 0;          % Reset for first plot point
max_beta  = 10000      % To maximum beta value

%Set up Results matrix
%with first value
index = 1

%initialise
Beta_First_Point = plot_decade
Beta_Point = plot_decade

while (Beta_Point <= max_beta)
% Update new Beta
  if (plot_step == 0)                % plot first point
    Beta_Point = plot_decade;
    plot_step = plot_step + 1;
  elseif (plot_step < plot_points_per_dec)
    % Avoid calculating below the decade plot point
    if (plot_step*((1/plot_points_per_dec)*plot_decade*10) <=
plot_decade)
      plot_step = plot_step + round(plot_points_per_dec/10);
    end
    Beta_Point = plot_step*((1/plot_points_per_dec)*plot_decade*10);
    plot_step = plot_step + 1;
  else
    plot_decade = plot_decade*10;  % jump to next decade
    plot_step = 1;
    Beta_Point = plot_decade;
  end


%Transconductance
gm1 = 10e-3; %A/V;
gm2 = 10e-3; %A/V;
gm3 = 10e-3; %A/V;

%Beta VAlues
B1 = Beta_Point
B2 = Beta_Point;
B3 = Beta_Point;

%rds/rce values
rce1 = 10e3; %Ohms
rce2 = 10e3; %Ohms
rce3 = 10e3; %Ohms

%Intermidiate values
%Vy = Bgy.Vx
Bgy = ((gm3*rce1)-(gm1*B3*rce1))/(B3+(gm3*rce1));

%Vx = Bgx.io
BgxVy = gm3*B1*B2*rce2*(Bgy-1);
```

```
Bgx =
(B1*B2*B3*rce2)/((gm1*B2*B3*rce2)+(gm2*B1*B3*rce2)+(gm2*B1*B2*B3*rce2
)+(B1*B2*B3)-BgxVy);

%Output inpedence
Absolute_Rout = rce3 - (gm3*Bgy*Bgx*rce3) + (Bgx*gm3*rce3) + Bgx

%Store Results
results(index,1) = Beta_Point;
results(index,2) = Absolute_Rout;
index = index + 1;

end    % Simulation end
```

```
%plot results
semilogx(results(:,1),results(:,2),'-')
Xlabel ('Beta')
YLabel ('Output Resistance (ohms)')
title ('Output resistance of Wilson Mirror wrt Beta')
%gset logscale x 10    % set x-axis to log base 10
%gplot [Beta_First_Point:max_beta] results with lines
```

(APP 2.2.3) The Improved Wilson Current Mirror.

```
%Wilson Current Mirror output impedance calculator
%Please refer to Wilson current mirror document.

%Set up plots for graph
plot_decade = 10;       % Define first Beta point
plot_points_per_dec = 20        % points per decade
plot_step = 0;          % Reset for first plot point
max_beta  = 10000      % To maximum beta value

%Set up Results matrix
%with first value
index = 1

%initialise
Beta_First_Point = plot_decade
Beta_Point = plot_decade

while (Beta_Point <= max_beta)
% Update new Beta
  if (plot_step == 0)                % plot first point
    Beta_Point = plot_decade;
    plot_step = plot_step + 1;
  elseif (plot_step < plot_points_per_dec)
    % Avoid calculating below the decade plot point
    if (plot_step*((1/plot_points_per_dec)*plot_decade*10) <=
plot_decade)
      plot_step = plot_step + round(plot_points_per_dec/10);
    end
    Beta_Point = plot_step*((1/plot_points_per_dec)*plot_decade*10);
    plot_step = plot_step + 1;
  else
    plot_decade = plot_decade*10;  % jump to next decade
    plot_step = 1;
    Beta_Point = plot_decade;
  end


%Transconductance
gm1 = 10e-3; %A/V;
gm2 = 10e-3; %A/V;
gm3 = 10e-3; %A/V;
gm4 = 10e-3; %A/V;

%Beta VAlues
B1 = Beta_Point
B2 = Beta_Point;
B3 = Beta_Point;
B4 = Beta_Point;

%rds/rce values
rce1 = 10e3; %Ohms
rce2 = 10e3; %Ohms
rce3 = 10e3; %Ohms
rce4 = 10e3; %Ohms

%Intermidiate values
%Diode Equations
rd1=rce1*B1/(B1+(gm1*rce1*B1)+(gm1*rce1))
rd4=rce4*B4/(B4+(gm4*rce4*B4)+(gm4*rce4))
```

```
%Bin
Bin = 1/(B3+(gm3*rd1))

%Bgy
Bgy = ((gm2*rd1*rce2)-(Bin*gm3*rd1*rce2))/((Bin*B3*rce2)-rce2-rd1)

%Bgx
Bgx= (rd1*rd4)/(rd1+(Bgy*rd4)+(gm2*rd1*rd4)-(Bin*Bgy*B3*rd4)-
(Bin*gm3*rd1*rd4))

%Output inpedence
Absolute_Rout = rce3 + Bgx + (gm3*rce3*Bgx*(1-(Bin*Bgy*B3)-
(Bin*gm3*rd1)))

%Store Results
results(index,1) = Beta_Point;
results(index,2) = Absolute_Rout;
index = index + 1;

end   % Simulation end

%plot results
semilogx(results(:,1),results(:,2),'-')
Xlabel ('Beta')
YLabel ('Output Resistance (ohms)')
title ('Output resistance of Improved Wilson Mirror wrt Beta')
%gset logscale x 10   % set x-axis to log base 10
%gplot [Beta_First_Point:max_beta] results with lines
```

(APP 2.2.4) The Regulated Cascode Current Mirror.

```
%Regulated Cascode Current Mirror output impedance calculator
%Please refer to Wilson current mirror document.

%Set up plots for graph
plot_decade = 10;       % Define first Beta point
plot_points_per_dec = 20        % points per decade
plot_step = 0;          % Reset for first plot point
max_beta  = 1000000      % To maximum beta value

%Set up Results matrix
%with first value
index = 1

%initialise
Beta_First_Point = plot_decade
Beta_Point = plot_decade

while (Beta_Point <= max_beta)
% Update new Beta
  if (plot_step == 0)                % plot first point
    Beta_Point = plot_decade;
    plot_step = plot_step + 1;
  elseif (plot_step < plot_points_per_dec)
    % Avoid calculating below the decade plot point
    if (plot_step*((1/plot_points_per_dec)*plot_decade*10) <=
plot_decade)
      plot_step = plot_step + round(plot_points_per_dec/10);
    end
    Beta_Point = plot_step*((1/plot_points_per_dec)*plot_decade*10);
    plot_step = plot_step + 1;
  else
    plot_decade = plot_decade*10;  % jump to next decade
    plot_step = 1;
    Beta_Point = plot_decade;
  end

%Transconductance
gm1 = 10e-3; %A/V
gm2 = 10e-3; %A/V
gm3 = 10e-3; %A/V
gm4 = 10e-3; %A/V

%Beta VAlues
B1 = Beta_Point;
B2 = Beta_Point;
B3 = Beta_Point;
B4 = Beta_Point;

%rds/rce values
rce1 = 10e3; %Ohms·
rce2 = 10e3; %Ohms
rce3 = 10e3; %Ohms
rce4 = 10e3; %Ohms

%Intermidiate values
%Vy = Bgz.Vy
Bgz = ((gm3*rce4) -(gm4*B3*rce4))/((gm3*rce4) + B3);

%Vy = Bgy.io
```

```
Bgy = (rce2*B4*B3)/((B3*B4) - (gm3*Bgz*B4*rce2) + (gm3*B4*rce2) +
(B3*gm4*rce2));

%Output inpedence                                                    .
Absolute_Rout = rce3 + Bgy - (gm3*Bgz*Bgy*rce3) + (gm3*Bgy*rce3)

%Store Results
results(index,1) = Beta_Point;
results(index,2) = Absolute_Rout;
index = index + 1;
```

```
end   % Simulation end

%plot results
semilogx(results(:,1),results(:,2),'-')
Xlabel ('Beta')
YLabel ('Output Resistance (ohms)')
title ('Output resistance of Regulated Cascode Mirror wrt Beta')
%gset logscale x 10   % set x-axis to log base 10
%gplot [Beta_First_Point:max_beta] results with lines
```

CHAPTER 3

The Voltage Follower

3.1 Introduction.

The source follower is an integral part of the current conveyor design, and is effectively the Y to X node section of the current conveyor as per Figure 1-3 (Chapter One). For the current conveyor to work properly **[3-1]** the gain from Y (input) to X the output must be as close as possible to unity. This was easier to achieve with the original BJT designs **[3-2]** as BJTs have a much higher gm than their CMOS counterparts.

Therefore an accurate source follower is difficult to design using CMOS transistors due to their inherent low gm values compared with BJT equivalents, and so a nonconventional follower had to be designed to give a gain close to unity, as the gain of a simple common drain follower is much less than unity, for reasons which will be shown later on in this chapter.

This chapter will deal voltage follower which makes up part of the Current Conveyor, as explained in Chapter One, section 1.1, 'The Current Conveyor Explained'.
The chapter starts by looking at the advantages and disadvantages of a typical source follower, and expands the analysis by looking at the effects of source resistance on the gain of the source follower. This chapter then moves onto introducing current solutions of voltage followers that are used in CMOS devices to date. Finally the chapter will introduce the proposed voltage follower used in the new CMOS current conveyor.

3-2 The CMOS source follower gain analysis and problems.

To see what type of gain could be obtained from a source follower, the following analysis was performed. The diagram below shows a typical source follower using a CMOS device. Virtually the same analysis could be used on the BJT equivalent.

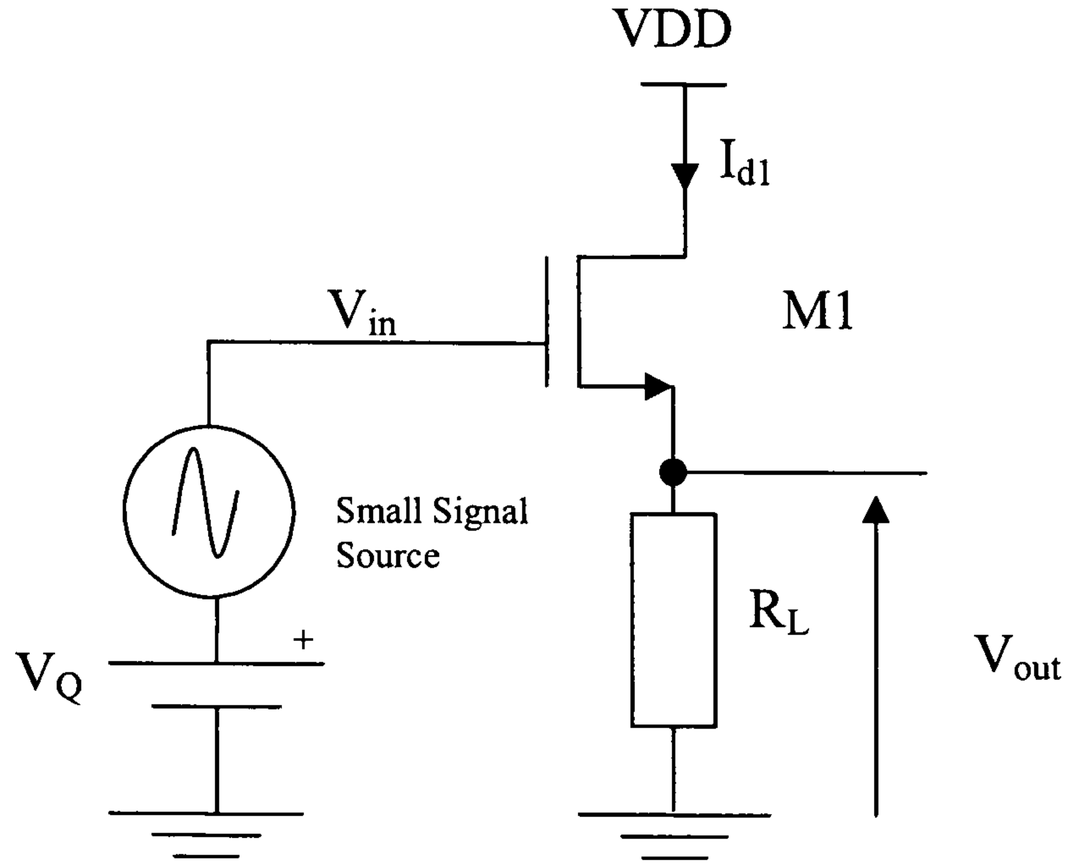

Figure 3-1: Typical source follower using CMOS device.

From this a low frequency small signal model can be drawn as shown below:

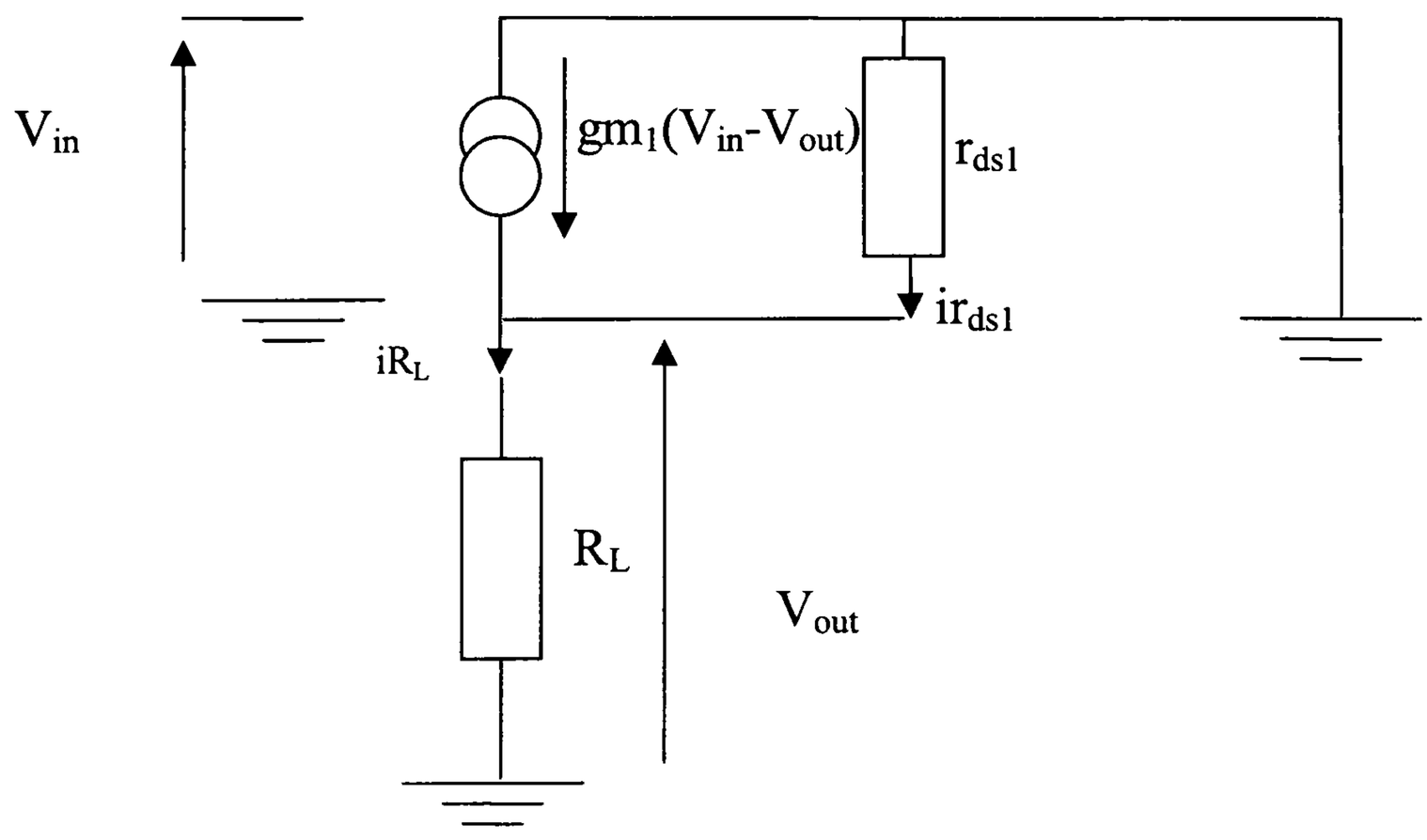

Figure 3-2: Low frequency small signal equivalent model of the source follower.

From Figure 3-2 the following equation can be derived for the low frequency voltage gain of this simple source follower circuit,

$$Av = \frac{1}{1+\frac{(g_L + g_{ds1})}{gm_1}} \approx 1-(\frac{g_L + g_{ds1}}{gm_1}) \qquad (3.1)$$

where Av is the voltage gain, g_L conductance of the load resistor R_L, g_{ds1} is the drain/source conductance of the CMOS device M1, and gm_1 is the transconductance of the device M1.

From Equation 3.1 the following are needed for a good voltage follower; firstly the value of g_{ds1} must be as small as possible so that $g_{ds1} << g_L$ i.e. drain/source resistance (r_{ds}) of the transistor must as large as possible; and secondly the transconductance (gm) must be as large as possible so that $g_L << gm_1$ so making $(\frac{g_L + g_{ds1}}{gm_1})$ as small as possible and therefore making the gain of the voltage follower (Av) close to the desired value of unity. BJTs have a higher gm then CMOS devices which enables a single stage emitter follower to operate with Av approximately equal to one. However, the equivalent source follower in CMOS is not as good. This is because CMOS transistors suffer from low values of transconductance (gm) and Drain/Source resistance (rds). The latter is due to poor channel modulation effects, and these effects are getting worse with continual shrinkages in process technology **[3-3]**.

To demonstrate the effects of using this type of circuit, a test circuit was simulated with spice using AC analysis and using Figure 3-1, the following results were obtained shown in Tables 3-1 and 3-2 on the next page.

The following equations were used to determine the intrinsic gm_1', using the DC operating points extracted from the simulation:

$$gm_1' = 2.\sqrt{\beta_1 . Ids_1(DC)} \qquad (3.2)$$

where:

$$Ids_1(DC) = I_{d1}(DC) - Ir_{ds1}(DC) \qquad (3.3)$$

I_{d1}(DC) refers to the simulated DC bias drain current of M1.

where:

$$Ir_{ds1}(DC) = (V_{d1} - V_{s1}) * g_{ds1} \qquad (3.4)$$

V_{d1} and V_{s1} refer to the DC bias voltage conditions for the drain and source of M1 respectfully. The drain/source conductance ($g_{ds1)}$ was also extracted from the DC bias conditions of the simulation.

The following transistors were used in this test.

1) TSMC 0.18μm process **[3-4]**; Gate Length (L1) = 0.18μm;
Gate Width (W1) = 10μm.
2) TSMC 0.18μm process **[3-4]**; Gate Length (L1)= 0.18μm;
Gate Width (W1) = 5μm.

β_1 for both CMOS transistors used, was derived from the following equation:

$$\beta_1 = \frac{\mu_o C_{ox} . W1}{2.L1} \qquad (3.5)$$

where $\mu_o = 0.044$ m^2/V

and $C_{ox} = 0.0084$ F/m^2

Other Simulator parameters:

V_{supply} =1.2V; V_{in} (small signal) =50mV Peak; $R_L = 1K\Omega$

The simulation results are shown in Tables 3-1 and 3-2, the results to the diagram shown in the AC small signal model in Figure 3.2.

Table 3-1: Source follower gain Table for L=0.18µm and W=10µm

V_Q (V)	g_{ds1} (Ω^{-1})	ir_{ds1} (A)	gm_1' (A/V)	Theoretical Gain (Av)	Simulated Gain (Av)
1.2	20.4u	15.69u	4.13m	0.802	0.655
1	16.9u	15.18u	3.43m	0.771	0.63
0.9	15.3u	14.69u	3.04m	0.750	0.612
0.75	12.8u	13.43u	2.38m	0.701	0.566

Table 3-2: Source follower gain Table for L=0.18µm and W=5µm

V_Q (V)	g_{ds1} (Ω^{-1})	ir_{ds1} (A)	gm_1' (A/V)	Theoretical Gain (Av)	Simulated Gain (Av)
1.2	19.5u	16.28u	2.75m	0.836	0.655
1	15.7u	14.90u	2.26m	0.749	0.63
0.9	14u	14.04u	1.99m	0.703	0.612
0.75	11.3u	12.23u	1.52m	0.631	0.56

From Tables 3-1 and 3-2 above, it can be seen that the simulated gain is consistently less than the expected calculated gain from Equation 3.1 in this chapter. The likely effect is the presence of source resistance **[3-5],** this parameter along with its counterpart the drain resistance (Rd) are significant in RF amplifier design where such things as inductance also has to be taken into account when matching into transmission lines such as designing low noise amplifiers (LNA). Section 3-3 will deal with the extraction of this parameter.

3.3 Extraction of Equivalent Rs.

From Section 3.2 (Equation 3.1) it could be seen that the theoretical gain (Av) was greater than that measured, and this suggests the presence of extra source resistance (Rs). This section will deal with extracting this parameter and determining its value as accurately as possible.

By using the small signal model in Figure 3-2 (Section 3.2), but now adding the source resistance (R_s), the following small signal model can be derived as shown in Figure 3-3 below:

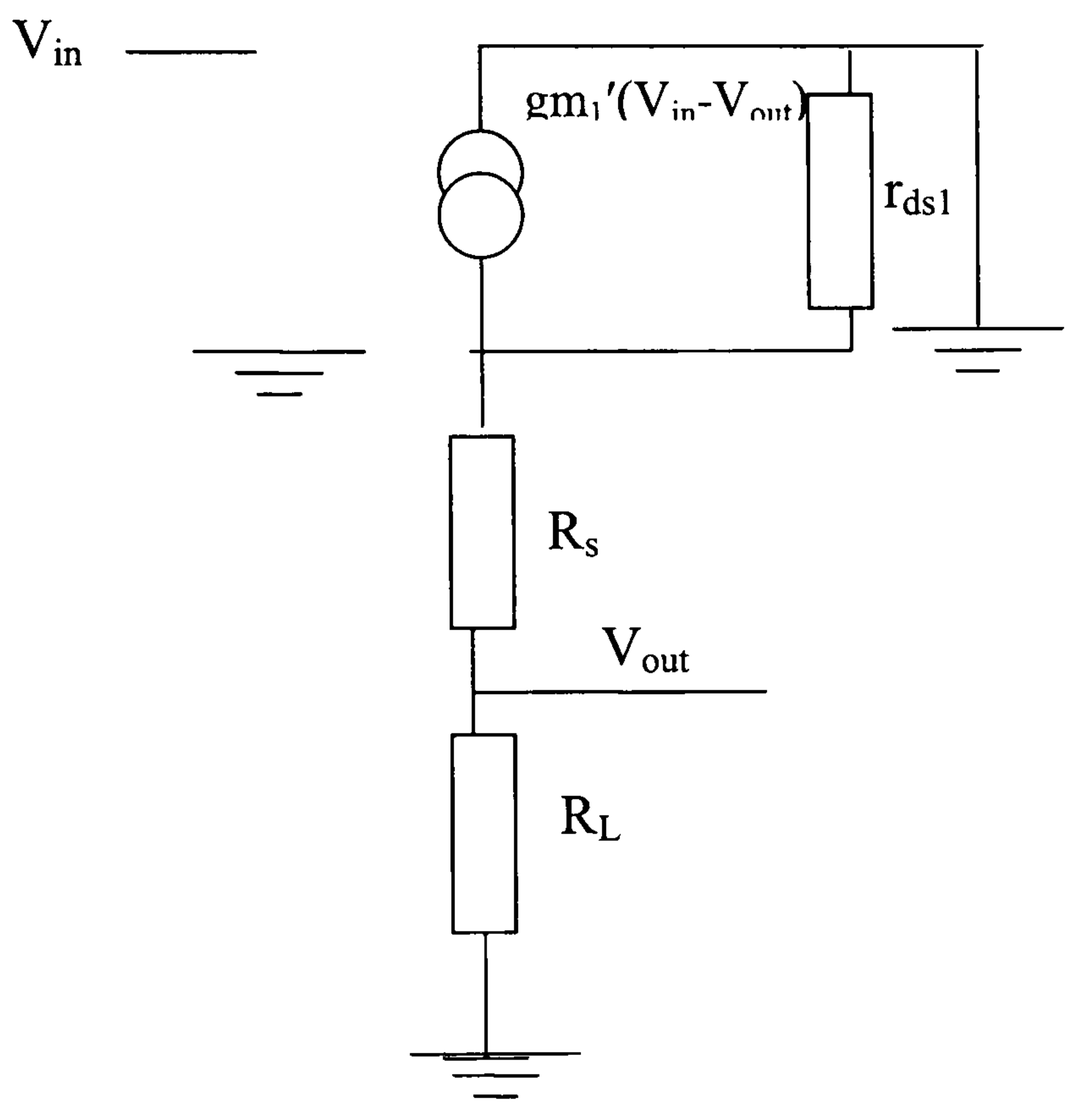

Figure 3-3: Small signal equivalent model of the follower with the added source resistance (R_s).

From Figure 3-3 the following Equation 3.6 can be derived shown below (a more detailed analysis of this is shown in appendices at the end of this chapter):

$$R_s = \frac{(gm_1'.R_L - G(1 + gm_1'.R_L)}{G.gm_1'} \qquad (3.6)$$

where 'G' is the gain obtained from simulation.

Note: Referring to Figure 3-1, the drain current of M1 (I_{d1}) would normally be calculated using Equation 3.7, and the transconductance of M1 (gm_1) would be calculated by using Equation 3.2 (Section 3.2) using I_{d1} from equation 3.7.

$$Id = \frac{W\mu_o C_{ox}}{2L}(V_{gs} - V_{th})^2(1 + \lambda V_{ds}) \qquad (3.7)$$

This assumes that the source resistance (R_s) is small compared with the value of $1/gm_1$, but as R_s plays a significant part in these calculations it can cannot be used in this case. So the simulated drain current I_{d1}(DC) must be used to obtain the intrinsic gm (gm_1').

Using the data from Tables 3-1 and 3-2 (Section 3.2) the following results were obtained shown below in Tables 3-3 and 3-4.

Table 3-3: Estimated value of source resistance (R_s) for L=0.18µm and W=10µm

V_Q (V)	gm_1 (A/V)	Theoretical Gain (Av)	Estimated R_s (Ω)
1.2	4.13m	0.655	291
1	3.43m	0.63	304
0.9	3.04m	0.612	314
0.75	2.38m	0.566	358

Table 3-4: Estimated value of source resistance (R_s) for L=0.18µm and W=5µm

V_Q (V)	gm_1 (A/V)	Theoretical Gain (Av)	Estimated R_s (Ω)
1.2	2.75m	0.655	370
1	2.26m	0.63	357
0.9	1.99m	0.612	357
0.75	1.52m	0.566	375

The calculated values of the source resistance of M1 (R_s) shown in Tables 3-1 and 3-2 are a very close to each other. The inaccuracies in the results are due to estimates made from the simulated evaluation of parameters such as the drain/source conductance (g_{ds1}) for the given transistor. As these parameters are difficult to measure especially with small geometry devices as the transition into the saturation region from the linear region is not so well defined.

But it can be seen that the source resistance (R_s) is around 300-350Ω for both transistor widths simulated. This at first did not add up as it would be expected that if the width of the transistor was to double, the source resistance (R_s) would be expected to halve as the area of the source would double. On further investigation it was discovered that the TSMC 0.18μm standard design kit **[3-4]** does not include the appropriate Bsim3 parameters **[3-6]** needed to calculate the active areas of source properly. Therefore the value of source resistance (R_s) defaults to the resistance value of the minimum active area allowed under the process design rules. Therefore the worst case value of resistance for the source resistance (R_s) is calculated for the model, in this case 300-350Ω. The extra parameters needed to calculate source resistance (R_s) will have to be added to the model in future development to take into account the effects of this rising value, due to newer processes having smaller geometry devices leading to higher source resistances (R_s).

3.4 The proposed CMOS source follower for the current conveyor.

As previously explained the major problem with using a standard CMOS follower (as shown in Figure 3-1), is that it suffers from a low value of transconductance (gm) and poor Early voltage ($1/\lambda$) which in turn affects the drain/source conductance (g_{ds}) figure of the transistor used in the follower, this equates to poor gain (Av) as the gain for a voltage follower heavily relies on these two parameters to be as large as possible, as shown Equation 3.1.

Figure 3-4 shows the effects of the gain (Av) of a source follower for different values of load resistance (R_L) and varying widths of the source follower's transistor. The gain (Av) can be related back to transconductance (gm) by using Equation 3.1, where the transconductance (gm) is derived using Equation 3.8 below, this equation neglects the Early effect, and assumes that the drain/source conductance is zero.

$$gm = \frac{W\mu_o C_{ox}}{L}(V_{gs} - V_{th}) \qquad (3.8)$$

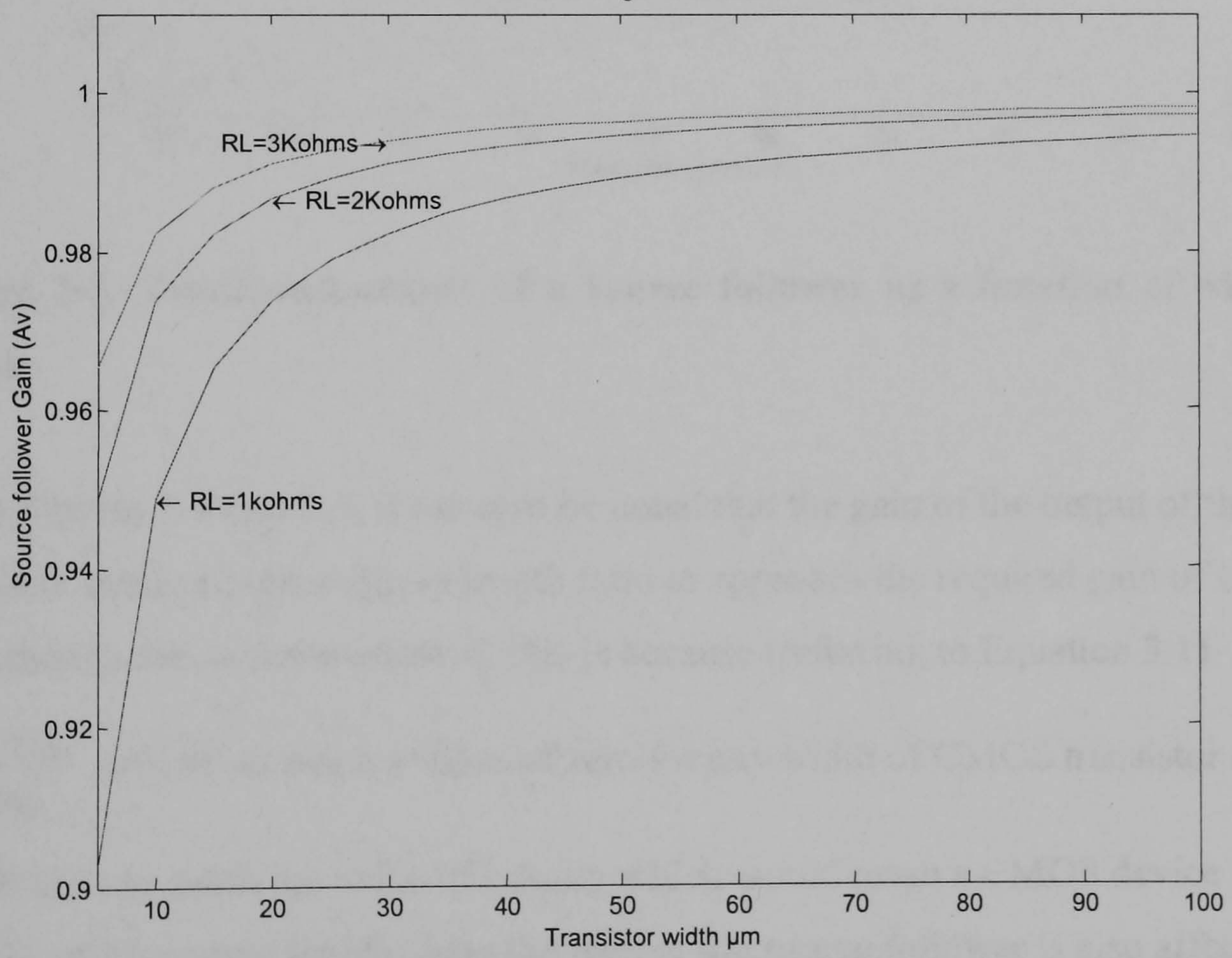

Figure 3-4: The effects on the gain of a source follower with varying transistor widths for different loads resistances (R_L), with L = 0.1µm.

Figure 3-4 shows the effects of gain of the source follower, for different transistor widths using a fixed gate length of 0.1μm. From equation 3.8 it can be seen that the width of the transistor is directly proportional to the transconductance (gm) of the transistor as shown in Figure 3-5 below:

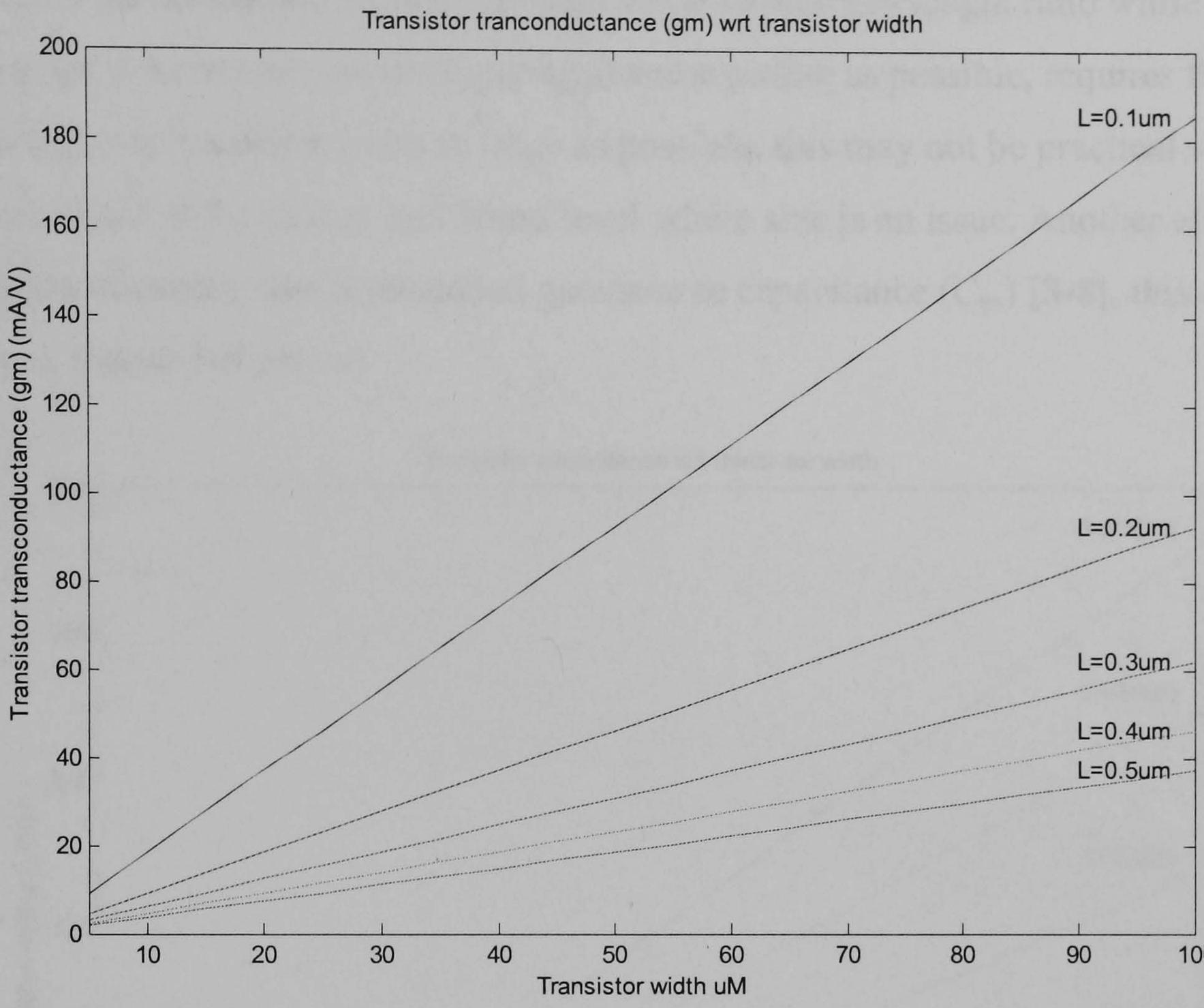

Figure 3-5: Transconductance of a source follower as a function of width and length.

From Figures 3-4 and 3-5, it can also be noted that the gain of the output of the transistor needs a high width to length ratio to approach the required gain of unity even though this is never attained, this is because (referring to Equation 3.1)

$\frac{g_L + g_{ds1}}{gm_1}$ will never reach a value of zero for any width of CMOS transistor as gm_1 would have to reach the value of infinity which would mean a CMOS device of infinite width or zero length. Also the gain of the source follower is also affected by the load resistance R_L which means that the gain of the source follower is dependant on the load attached to the follower, for a good source follower the gain should be independent of the load R_L.

It can also be shown **[3-7]** that the channel modulation effect (λ), is inversely proportional to the length of the transistor of the source follower, this means that the length of the transistor must be as large as possible to reduce the effect of the drain/source conductance (g_{ds}), which also contributes to the loss of gain in the source follower. This means that to keep the high value of width to length ratio while keeping the drain/source conductance (g_{ds}) value as low as possible, requires the source follower transistor to be as large as possible, this may not be practical when designing both at the silicon and board level where size is an issue. Another effect of increasing transistor size is the added gate/source capacitance (C_{gs}) **[3-8],** this effect is shown in Figure 3-6 below:

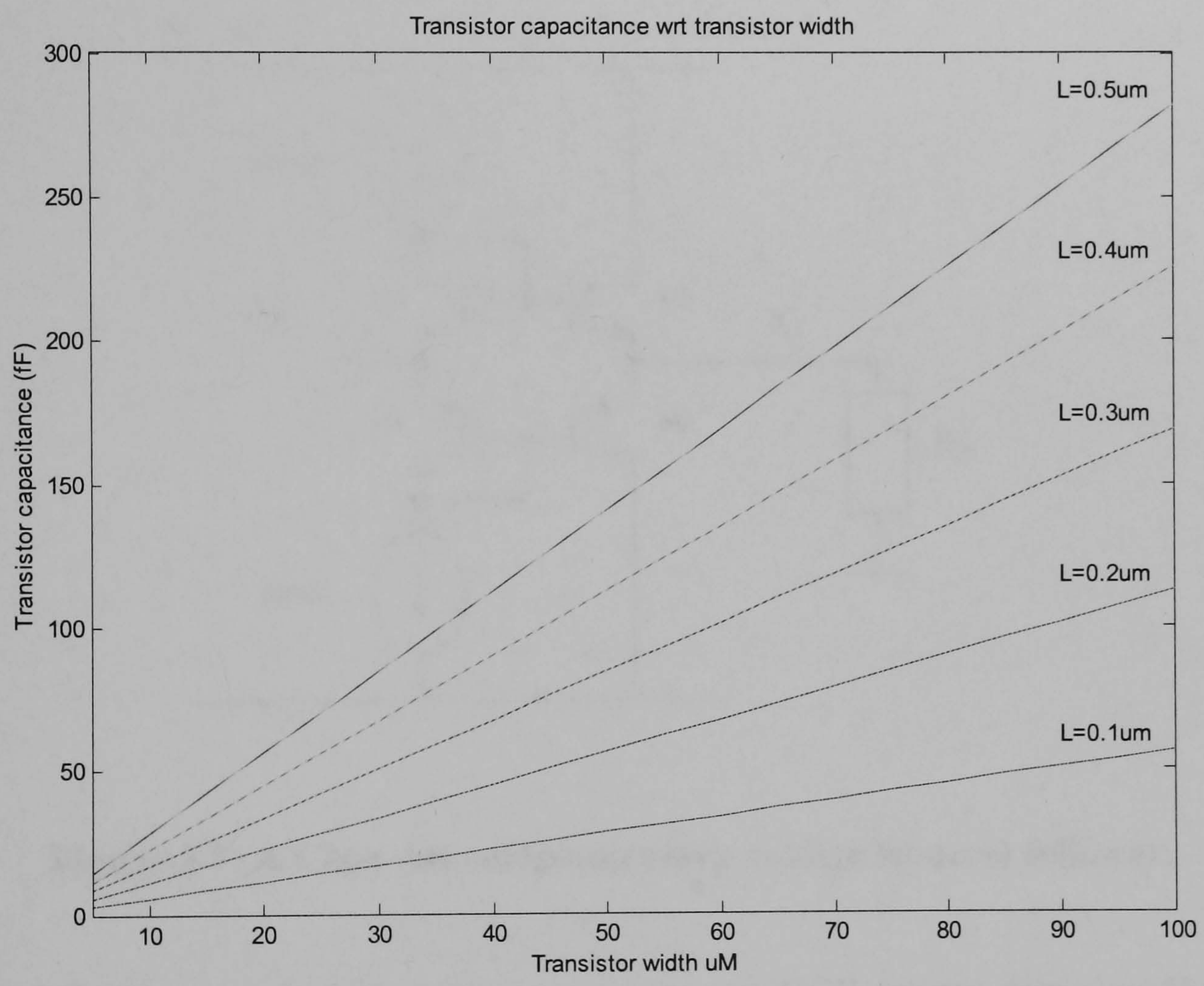

Figure 3-6: The effects of capacitance of a source follower as a function of width and length.

It can be seen from Figure 3-5 that the gate/source capacitance (C_{gs}), increases with transistor width as well as transistor length, so as these values are increased the effect is to increase capacitance and reduce the bandwidth of the device.

Then the added effect of the source resistance (R_s) shown in Section 3.3 (Table 3-2), which shows a simulated gain of 0.63, with a TSMC 0.18μm **[3-4]** with a load of $1k\Omega$ and a gate bias voltage of 1V, against its theoretical gain of 0.75, adds another 12% loss to the output gain (Av). This would mean that unlike the BJT equivalent, this circuit architecture though simple in its nature, could not be used practically in an equivalent CMOS circuit for such a device as the current conveyor. Therefore alternative architectures were considered for the source follower **[3-9] , [3-10], [3-11], [3-12],** to obtain a voltage gain as close to unity a, or in the possible, or in the case of the current conveyor nodes Y to X.

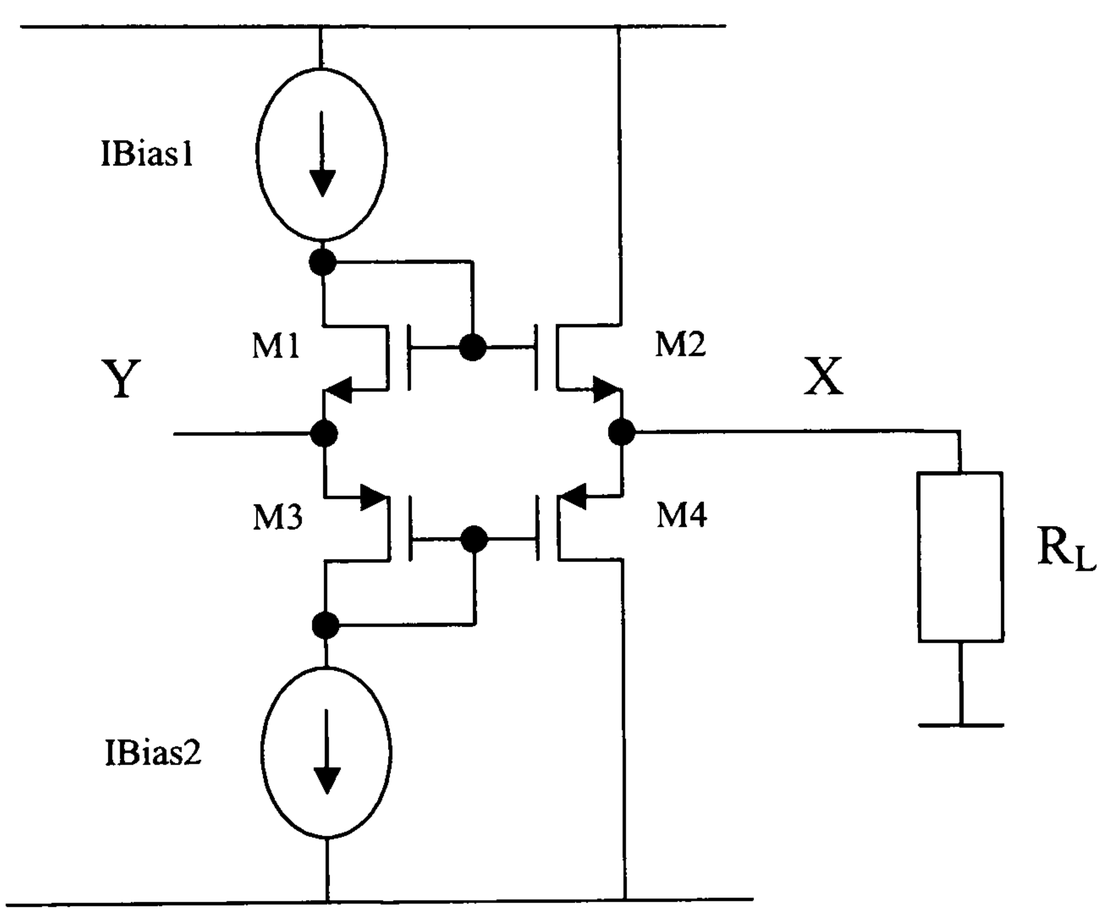

Figure 3-7: A Class AB complementary voltage (source) follower.

Figure 3-7 shows an example of an input stage of a CCII current conveyor **[3-9], [3-10],** where Node X tracks Node Y as a voltage follower by means of transistors M1 to M4 which make up the translinear loop **[3-13]**. The disadvantage with this structure is that for the input stage (node Y) to track the output stage (node X) means that M1 must match precisely to M2 and M3 to M4, along with the IBias currents IBias1 and IBias2 being a symmetrical design. In practice this is hard to achieve even using techniques such as common centroid transistor layout, but even if they were to match precisely the input and output loads probably would not. This would mean that the mirrors IBias1 and IBias2 would have slightly different operating points adding to

voltage errors between the input and output of this circuit. Note that the power supplies are not shown, this is because Figure 3-7 can operate at varying positive and negative voltages and not just between a positive supply and ground. Actually from a small signal analysis this circuit behaves as a conventional signal stage source follower.

Another type of symmetrical source follower used in current conveyors **[3-11]** is shown in Figure 3-8 below:

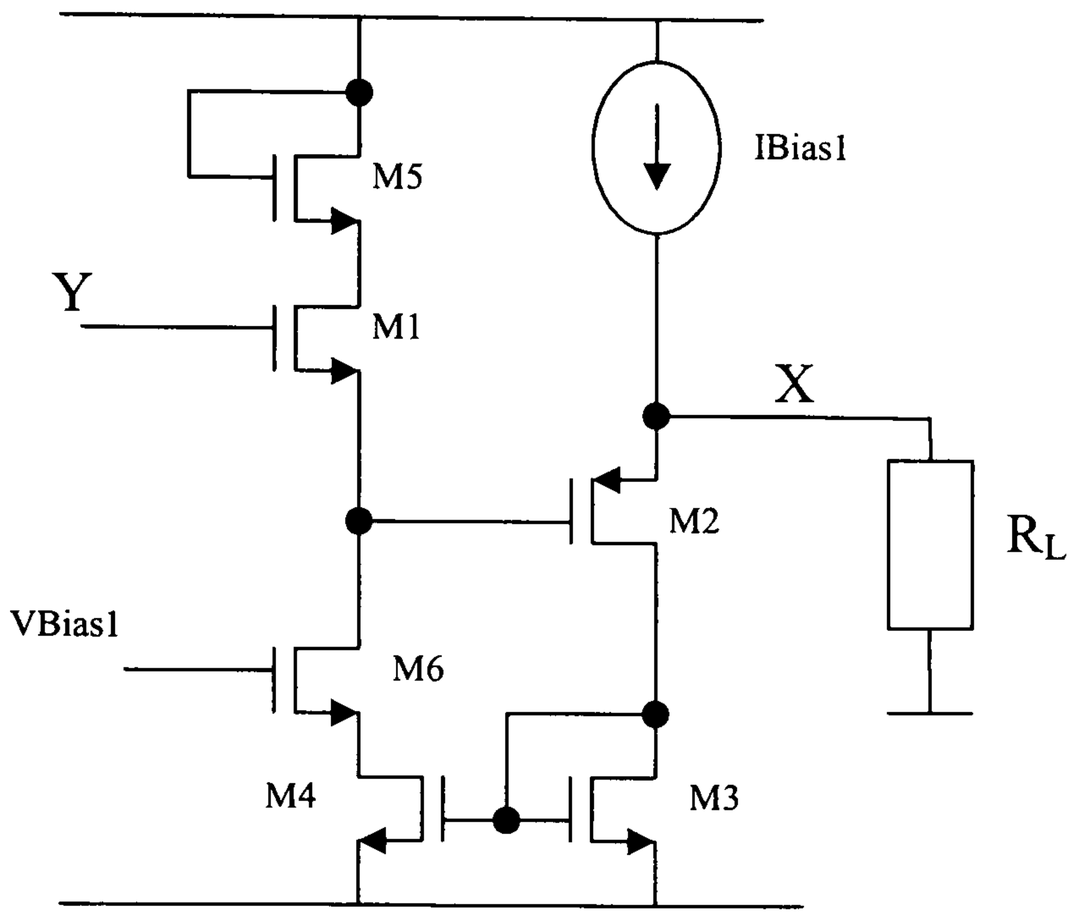

Figure 3-8: A source follower input stage of a second generation current conveyor.

Figure 3-8 shows another input stage of a second generation current conveyor (CCII), Ibias1 provides the biasing current for the input stage and M5 is to compensate for the voltage drop of IBias1 in the circuit to keep it symmetrical, M2, M3, M4 and M6 make up the current mirror so that current through M1 matches that through M2. Transistor M1 acts as a source follower and drives M2 as the currents between M1 and M2 match then as long as the transconductance of M1 gm_1 matches that of M2 gm_2 then the voltage at node X should match the input voltage at node Y. The disadvantage of this circuit is that transistor M1 transconductance must match that of transistor M2 so that the circuit remains symmetrical under DC conditions, the circuit also relies on having two source follower stages and as the voltage gain of M1 is then

multiplied by the voltage gain of M2 this compounds the inevitable gain loss through the source follower stages as previously shown.

Another method is to use an operational amplifier with a unity feedback **[3-12]** as shown in Figure 3-8 below:

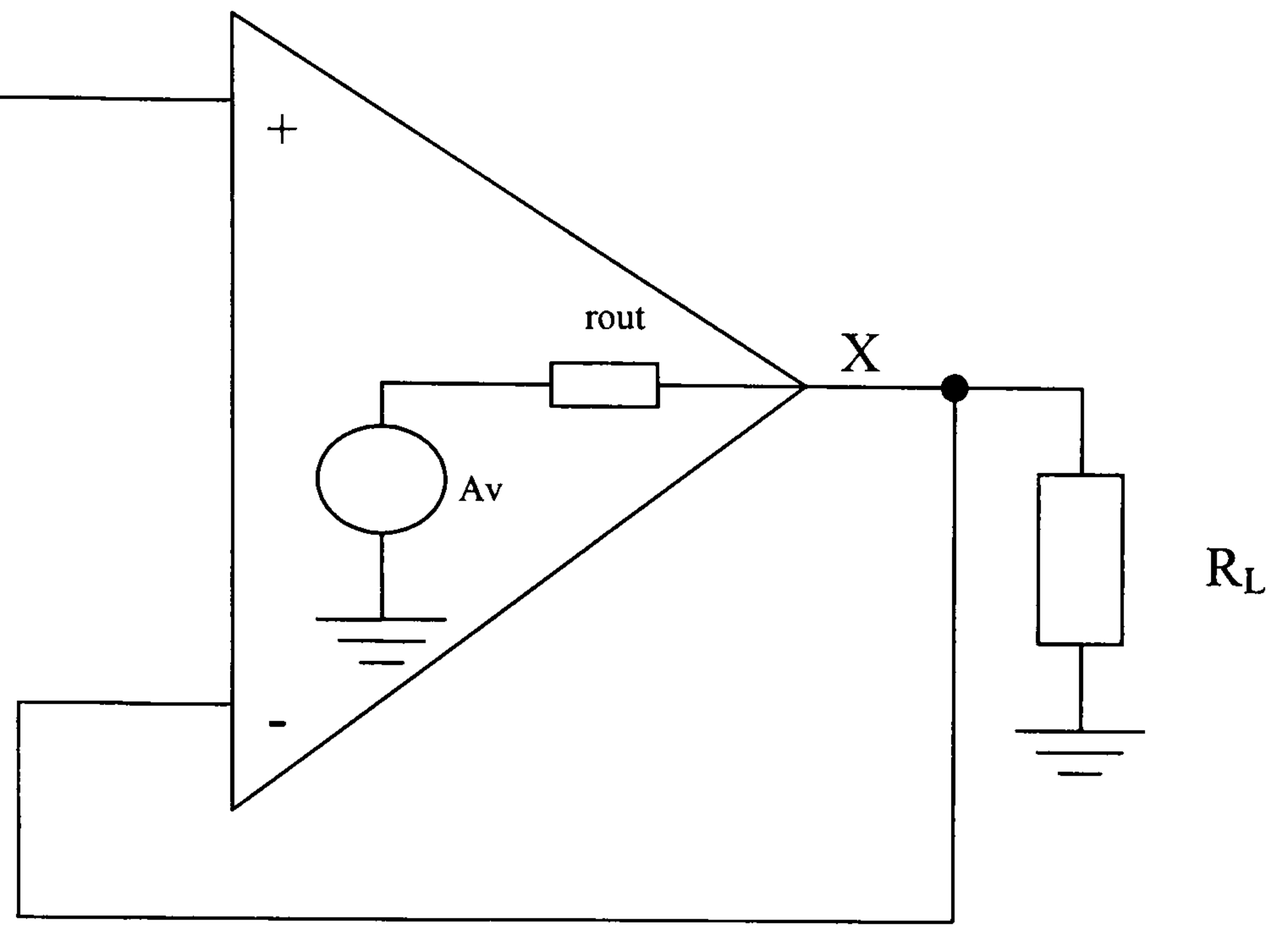

Figure 3-9: The current conveyor source follower block diagram.

Using Figure 3-9 as an input stage of the current conveyor would give a closer to unity gain almost independent of the output load than the single transistor source follower. The actual output impedance of the voltage follower (r_{out}) can be shown to be equal to $\frac{r_{out}}{Av}$ so if the gain is significantly high enough $r_{out} << R_{L,}$ so making the output resistance seen at node X close to that of $R_{L,}$ this in turn makes the output voltage gain of the voltage follower stage close to the desired value of unity. The problem with this design is that the gain-bandwidth of the follower would be limited by the bandwidth of the operational amplifier, and the component count for a current conveyor would be much greater than that of a typical operational amplifier, it would give no advantage at all in building a device based on this type of architecture.

This concept can be used by taking away the compensation capacitor of the amplifier the next part of this section will explain.

Figure 3-9 can be used as the voltage follower stage of the current conveyor giving a gain of approximately unity, as this type of circuit is ideal as it can track the output X close to that of input Y while providing the necessary current needed for the output resistance R_L.

But as previously explained if an operational amplifier was to be used it would be limited by its gain-bandwidth product, so by taking out this limitation by eliminating the compensation capacitor then the bandwidth can be extended considerably.

The problem with doing this is that the roll-off of the amplifier is now defined by the CMOS transistors themselves and it is difficult to predict whether the loop will become unstable. However, because the feedback loop is always fixed at unity this can be easily simulated and therefore the behaviour predicted and catered for in the final design. An example of this is shown in Figure 3-10 below:

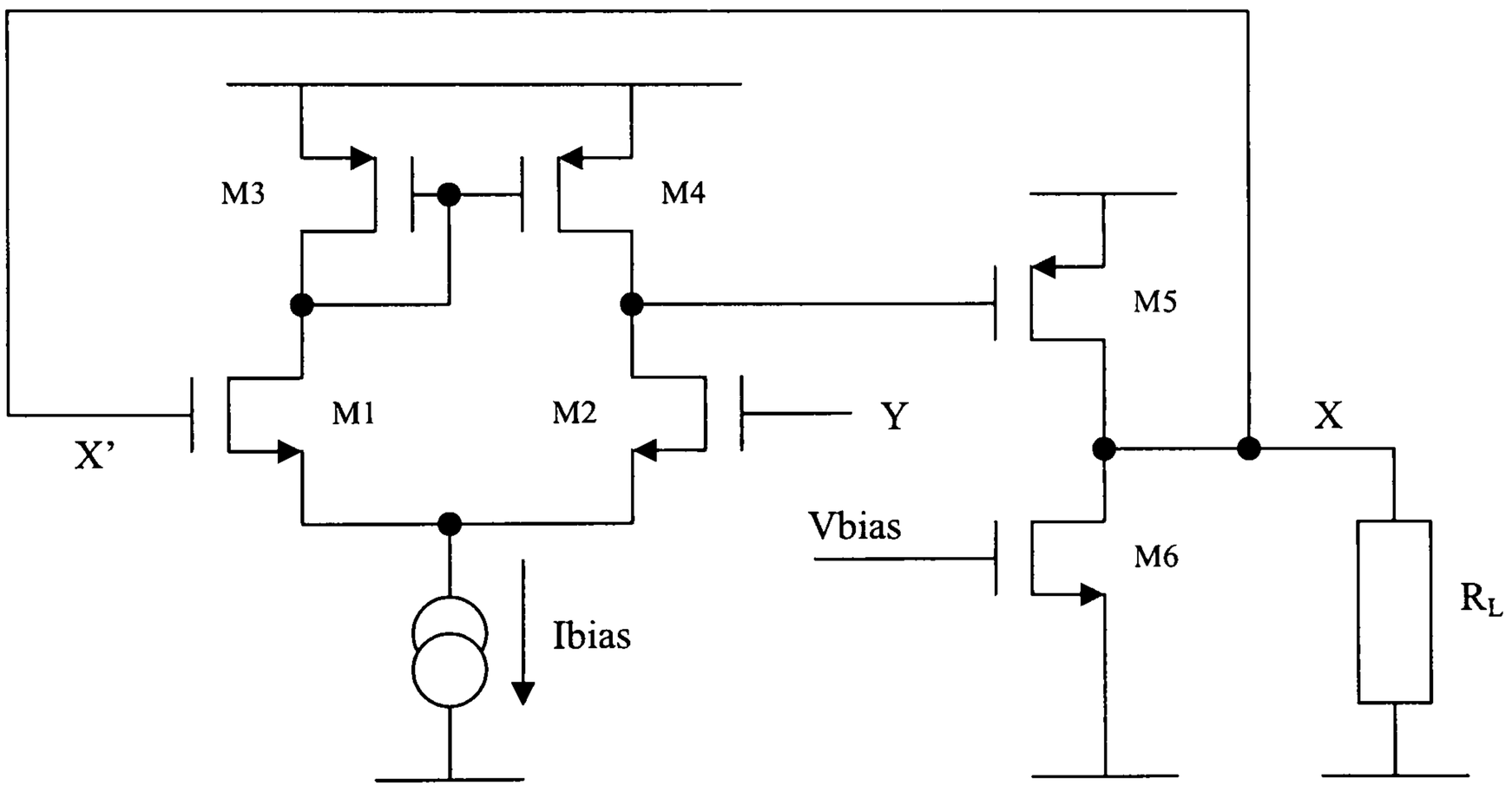

Figure 3-10: A source follower using a 2 stage CMOS unbuffered amplifier.

From Figure 3-10 it can be seen that output X is fed back to one of the long tail pairs inputs (X') the other input to the long tail pair is Y. As input Y changes the current through M1 and M2 differs as M3 and M4 is a current mirror there is a current difference between M2 and M4 this imbalance is addressed by pulling current from or to the gate/source capacitance Cgs of device M5, until the output X' matches that of

Y. The bandwidth limit is now only limited by the transistors used in the 2 stage unbuffered amplifier. This option will significantly improve the bandwidth of the voltage follower input stage of the current conveyor over using a compensated operational amplifier **[3-9].**

3.5 Review of results.

Firstly looking at a standard source follower implementation in Section 3-2 it can be seen from Tables 3-1 and 3-2 that the output gain is much below the unity needed to make the ideal source follower for the CMOS implementation of the current conveyor, and that not only is there a problem with the low transconductance values (gm) and channel modulation effect associated with CMOS transistors, but there is also a problem with the source resistance of these transistors. This is becoming more apparent with smaller the geometry transistors **[3-3]**.

From the results in Section 3-3 it can be seen that R_s has a major effect on the gain of a source follower. The results show a 5% spread in the value of R_s which is probably due to the measurement inaccuracies of the value of R_{ds} when simulated. It is also worth mentioning that the value of R_s will affect the value of the calculated gm as the true V_{gs}' used to calculate gm is in fact smaller than the measured V_{gs} due to the existence of R_s.

Also from the results in Tables 3-3 and 3-4 it would be expected that by doubling the width from 5μm to 10μm, the source resistance (R_s) should be halved. This was not the case and the simulated results highlighted that the values were similar in value. After further investigation it was found that the design kit used **[3-4]** based its calculations on a minimum source/drain area of a CMOS transistor, and without the addition of parameters to the CMOS transistor model ie. the Source/Drain perimeter values **[3-6],** source resistance (R_s) will almost always be incorrect. Actually the only time a transistor would have an accurate source resistance (R_s) value during simulation is when it uses minimum width and length parameters, as stated in the TSMC 0.18μm design rules **[3-4]**. This will mean there will almost always be a mismatch between real silicon and simulation when measuring such things as transconductance (gm), unless the correct parameters for drain and source area are added to the appropriate BSIM model **[3-6].**

Several methods were reviewed in Section 3-4 for improving the gain of the source follower, this included increasing the dimensions of the transistor to reduce the effects of source resistance (R_s) and increasing parameters such as transconductance (gm) to improve the overall gain. These were proved to be impractical as it would increase the size of the design and would affect such parameters as the overall bandwidth of the source follower. Other circuits reviewed included using translinear loops **[3-13]**, these would be a better approach and are used in some CMOS current conveyors **[3-10]**, but they have the disadvantage of needing precisely matched transistors and are susceptible to external loading.

Finally the type of circuit proposed in Figure 3-10 would give the best overall solution for the following reasons; (i) the output gain is independent of the output load; and (ii) it is not bandwidth limit as per the reviewed circuit which uses an operational amplifier **[3-4]**. Its only drawback is that it is uncompensated leading to possible problems of instability. However, as the gain is fixed the effects of its feedback can be simulated to find out how stable the design is. The circuit shown in Figure 3-10 is the basic circuit that will be used as the voltage follower building block in the current conveyor that is presented in the next chapter.

3.6 References.

[3-1] C. Toumazou, J. Lidgey & Alison Payne, 'Current-Conveyor Basics and Applications', Current Mode Circuits Techniques in Analog High Frequency Design, Tutorial book at IEEE sponsored International conference on Electronic Circuits and Systems, July 1994, Chapter 5.1, pp 49-67.

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[3-9] S.B. Salem, M. Fakhfak, D. Masmoudi, M. Loulou, 'A high performace CMOS CCII and high frequency applications', Analog Integrated Circuit Signal Processing, June 2006.

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[3-11] M. Kumar, 'Low-Voltage Current Mode Analog Cells', Seminar report, Electrical & Electronic Department, IIT Bombay, November 2002.

[3-12] I.G. Finvers, B.J. Maundy, I.A. Omole, P. Aronhime, 'On the Design of CMOS Current Conveyors', People Maundy Publications, University of Calgary, 'www2.enel.ucalgary.ca/People/bmaundy/Publications/cmos.pdf'.

[3-13] C. Toumazou, J. Lidgey & A. Payne, 'Translinear Circuits', current mode circuits Techniques in Analog High Frequency Design, Tutorial book at IEEE sponsored International conference on Electronic Circuits and Systems, July 1994, Chapter 3, pp. 9-23.

[3-14] K.Laker, W.Sansen, 'Design of Analog Integrated Circuits and Systems', McGraw Hill International Editions, First Edition, 1994, pp. 8-9.

APPENDIX 3

APP 3.1 Detailed analysis of the extraction of the CMOS source resistance.

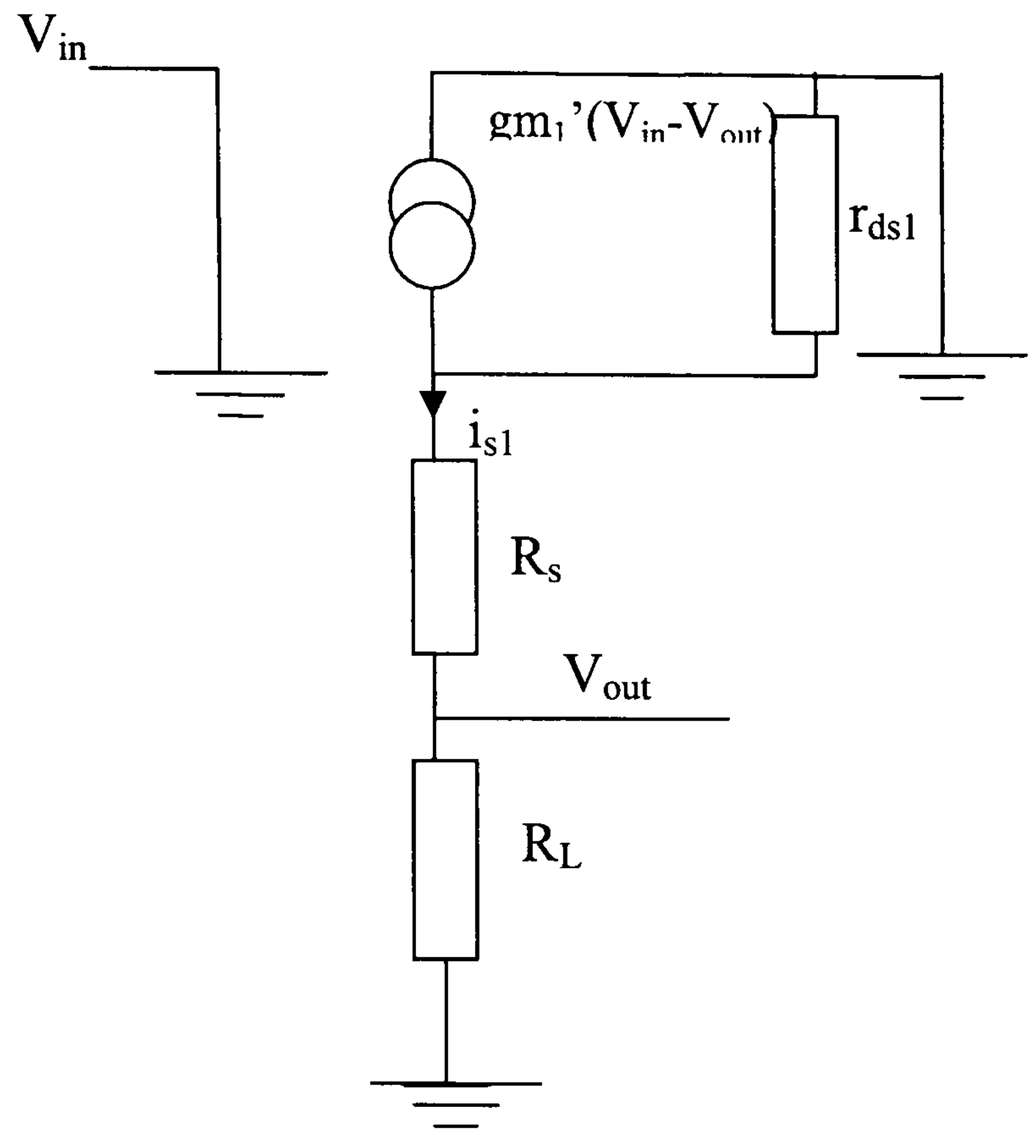

Figure AP.3.1 : Small signal equivalent model of the source follower with the added source resistance (Rs).

This analysis is used to extract the value of the source resistance (R_s), from the transistor model used **[3-5]** for simulating the source follower used in this chapter.

This analysis relates to Section 3.2: Extraction of Equivalent source resistance (R_s).

Assuming $r_{ds1} >> 1/gm_1'$

then:

$$i_{s1} = \frac{(V_{in} - V_{out})}{(1/gm_1') + R_s} \qquad \textbf{(APP.1)}$$

also:

$$i_{s1} = \frac{V_{out}}{R_L} \qquad \textbf{(APP.2)}$$

therefore from (APP.1) and (APP.2):

$$\frac{V_{out}}{R_L} = \frac{(V_{in} - V_{out})}{(1/gm_1') + R_s}$$

re-arranging:

$$V_{in}.gm_1'.R_L = V_{out}(1 + R_s + gm_1' + gm_1'.R_L)$$

so:

$$gm_1'.R_L = Av(1 + R_s + gm_1' + gm_1'.R_L) \qquad \textbf{(APP.3)}$$

where $Av = \frac{V_{out}}{V_{in}}$

re-arranging (APP.3) gives:

$$R_s = \frac{(gm_1'.R_L - Av(1 + gm_1'.R_L))}{Av.gm_1'}$$

APP 3.2 The MATLAB Source Files.

APP 3.2.1 The source follower gain scripts.

```
%Transistor calculator for Gain (Av) for a source follower
clear

%Set up plots for graph
Trans_max = 5;          % How many
plot_points = 20        % Number of points per line
Length_step = 0.1;      % legnth step in um
Max_Width  = 100;       % To Max Width um

% TSMC 0.18um process parameters
tox = 4.08e-9           % Oxide thickness
eoxer = 3.45e-11        % permiabilty of silicon
Cox = (eoxer/tox)*1e15    % Unit capacitance fF/m2
uo = 0.04387662

%Setup initial conditions
Trans_count = 1;
Loop_init = 1;
Width_step = Max_Width/plot_points;
index = 1;       % Used as point matrix counter
Vgs = 1
Vt = 0.5


while (Trans_count <= Trans_max)
% First time around the loop
if (Loop_init == 1)          % plot first Transistor point
  Lgth = Length_step;             % in um
  Wdth = Width_step;              % in um
  Loop_init = 0;
  Rl = 1e3;
else
  % Next transistor
  if (Wdth >= Max_Width)
      Rl = Rl +1e3;
      Wdth = Width_step;
      index = 1;                  % Reset matrix index
      Trans_count = Trans_count + 1;
  else
      Wdth = Wdth + Width_step;
      index = index + 1;
  end
end

% Beta calculation
Beta = uo*Cox*Wdth/(2*Lgth);

%Calculate Capacitance
gm = 2*Beta*(Vgs-Vt)*1e-15;    %into correct units (A/V)

%Calculate Gain Av
gl = 1/Rl
Av = 1/(1+(gl/gm))

%Calculate Graph Indexing
GraphIndex1 = ((Trans_count - 1)*2) + 1;
```

```
GraphIndex2 = ((Trans_count - 1)*2) + 2;

%Store Results
results(index,GraphIndex1) = Wdth;
results(index,GraphIndex2) = Av;

end   % While loop ** Simulation end **

%plot results
%plot(results(:,1),results(:,2),'-');
plot(results(:,1),results(:,2),results(:,3),results(:,4),results(:,5)
,results(:,6));
%results(:,7),results(:,8),results(:,9),results(:,10),'-');
axis([5 100 0.9 1.01]);
text(10,results(2,2),['\leftarrow
RL=1kohms'],'VerticalAlignment','middle','HorizontalAlignment','left'
);
text(20,results(4,4),['\leftarrow
RL=2Kohms'],'VerticalAlignment','middle','HorizontalAlignment','left'
);
text(30,results(6,6),[' RL=3Kohms
\rightarrow'],'VerticalAlignment','middle','HorizontalAlignment','rig
ht');
%text(40,results(8,8),['RL=4Kohms'],'VerticalAlignment','bottom','Hor
izontalAlignment','left');
%text(50,results(10,10),['RL=5Kohms'],'VerticalAlignment','bottom','H
orizontalAlignment','left');

Xlabel ('Transistor width uM');
YLabel ('Source follower Gain (Av)')
title ('Source follwer gain wrt transistor width')
%gset logscale x 10    % set x-axis to log base 10
%gplot [Beta_First_Point:max_beta] results with lines
```

APP 3.2.2 The source follower transconductance scripts.

```
%Transistor calculator for gm on a CMOS transistor
clear

%Set up plots for graph
Trans_max = 5;          % How many
plot_points = 20        % Number of points per line
Length_step = 0.1;      % legnth step in um
Max_Width  = 100;       % To Max Width um


% TSMC 0.18um process parameters
tox = 4.08e-9           % Oxide thickness
eoxer = 3.45e-11        % permiabilty of silicon
Cox = (eoxer/tox)*1e15    % Unit capacitance fF/m2
uo = 0.04387662

%Setup initial conditions
Trans_count = 1;
Loop_init = 1;
Width_step = Max_Width/plot_points;
index = 1;      % Used as point matrix counter
Vgs = 1
Vt = 0.5


while (Trans_count <= Trans_max)
% First time around the loop
  if (Loop_init == 1)          % plot first Transistor point
    Lgth = Length_step;              % in um
    Wdth = Width_step;               % in um
    Loop_init = 0;
  else
    % Next transistor
    if (Wdth >= Max_Width)
        Lgth = Lgth + Length_step;
        Wdth = Width_step;
        index = 1;                  % Reset matrix index
        Trans_count = Trans_count + 1;
    else
        Wdth = Wdth + Width_step;
        index = index + 1;
    end
  end

% Beta calculation
Beta = uo*Cox*Wdth/(2*Lgth);

%Calculate Capacitance
gm = 2*Beta*(Vgs-Vt)*1e-12;    %into correct units (mA/V)

%Calculate Graph Indexing
GraphIndex1 = ((Trans_count - 1)*2) + 1;
GraphIndex2 = ((Trans_count - 1)*2) + 2;

%Store Results
results(index,GraphIndex1) = Wdth;
results(index,GraphIndex2) = gm;

end    % While loop ** Simulation end **
```

```
%plot results
%plot(results(:,1),results(:,2),'-');
plot(results(:,1),results(:,2),results(:,3),results(:,4),results(:,5)
,results(:,6),results(:,7),results(:,8),results(:,9),results(:,10),'-
');
axis([5 100 0 200])
text((Max_Width-
2),results(20,2),['L=0.1um'],'VerticalAlignment','middle','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,4),['L=0.2um'],'VerticalAlignment','middle','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,6),['L=0.3um'],'VerticalAlignment','middle','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,8),['L=0.4um'],'VerticalAlignment','middle','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,10),['L=0.5um'],'VerticalAlignment','middle','Horizonta
lAlignment','right');

Xlabel ('Transistor width uM');
YLabel ('Transistor transconductance (gm) (mA/V)')
title ('Transistor tranconductance (gm) wrt transistor width')
%gset logscale x 10    % set x-axis to log base 10
%gplot [Beta_First_Point:max_beta] results with lines
```

APP 3.2.3 The source follower capacitance scripts.

```
%Capacitance calculator for Cgs on a CMOS transistor
clear

%Set up plots for graph
Trans_max = 5;          % How many
plot_points = 20        % Number of points per line
Length_step = 0.1;      % legnth step in um
Max_Width  = 100;       % To Max Width um


% TSMC 0.18um process parameters
tox = 4.08e-9           % Oxide thickness
eoxer = 3.45e-11        % permiabilty of silicon
Cox = (eoxer/tox)*1e15   % Unit capacitance fF/m2

%Setup initial conditions
Trans_count = 1;
Loop_init = 1;
Width_step = Max_Width/plot_points;
index = 1;      % Used as point matrix counter


while (Trans_count <= Trans_max)
% First time around the loop
  if (Loop_init == 1)          % plot first Transistor point
    Lgth = Length_step;             % in um
    Wdth = Width_step;              % in um
    Loop_init = 0;
  else
    % Next transistor
    if (Wdth >= Max_Width)
        Lgth = Lgth + Length_step;
        Wdth = Width_step;
        index = 1;                  % Reset matrix index
        Trans_count = Trans_count + 1;
    else
        Wdth = Wdth + Width_step;
        index = index + 1;
    end
  end

%Calculate Capacitance
Cgs = (2/3)*Cox*Wdth*1e-6*Lgth*1e-6;

%Calculate Graph Indexing
GraphIndex1 = ((Trans_count - 1)*2) + 1;
GraphIndex2 = ((Trans_count - 1)*2) + 2;

%Store Results
results(index,GraphIndex1) = Wdth;
results(index,GraphIndex2) = Cgs;

end   % While loop ** Simulation end **

%plot results
%plot(results(:,1),results(:,2),'-');
plot(results(:,1),results(:,2),results(:,3),results(:,4),results(:,5)
,results(:,6),results(:,7),results(:,8),results(:,9),results(:,10),'-
');
```

```
axis([5 100 0 300]);
text((Max_Width-
2),results(20,2),['L=0.1um'],'VerticalAlignment','bottom','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,4),['L=0.2um'],'VerticalAlignment','bottom','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,6),['L=0.3um'],'VerticalAlignment','bottom','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,8),['L=0.4um'],'VerticalAlignment','bottom','Horizontal
Alignment','right');
text((Max_Width-
2),results(20,10),['L=0.5um'],'VerticalAlignment','bottom','Horizonta
lAlignment','right');

Xlabel ('Transistor width uM');
YLabel ('Transistor capacitance (fF)')
title ('Transistor capacitance wrt transistor width')
%gset logscale x 10   % set x-axis to log base 10
%gplot [Beta_First_Point:max_beta] results with lines
```

CHAPTER 4

The CMOS current conveyor

4.1 Introduction.

Previous chapters have shown that the current conveyor is a very useful building block that can be used to implement many analogue functions **[4-1],[4-2]**. This chapter combines the two elements (i) the current follower from Chapter Two, and (ii) the voltage follower from Chapter Three, to build a new type of CMOS current conveyor.

Taking the results and design concepts from Chapters Two and Three and combining them a new CCII+ and a CCII- will be designed and simulated, with the view of utilising the best possible design concepts, to improve the performance of the current conveyor in the areas of voltage gain, current gain and PSRR over current implementations of the CMOS current conveyor.

This chapter will first review the most common design of the current conveyor replacing the usual BJT devices with CMOS, and then will combine the new voltage follower described in Chapter Three, with several examples of the current followers discussed in Chapter Two.

In the final part of the chapter a way of converting the CCII+ into a CCII- is described, thus giving designers a more versatile use for the current conveyor as the CCII- mimics the operation of a CMOS device. However, this option offers a much lower source resistance than that of a standard CMOS device, so overcoming problems in voltage gain that is seen in such configurations as standard CMOS source followers.

4.2 The Proposed CMOS CCII+ Circuit.

A current conveyor consists of a voltage follower (described in Chapter Three) and a current follower (described in Chapter Two) **[4-3]**. These two blocks can be combined as shown in Figure 4-1 below:

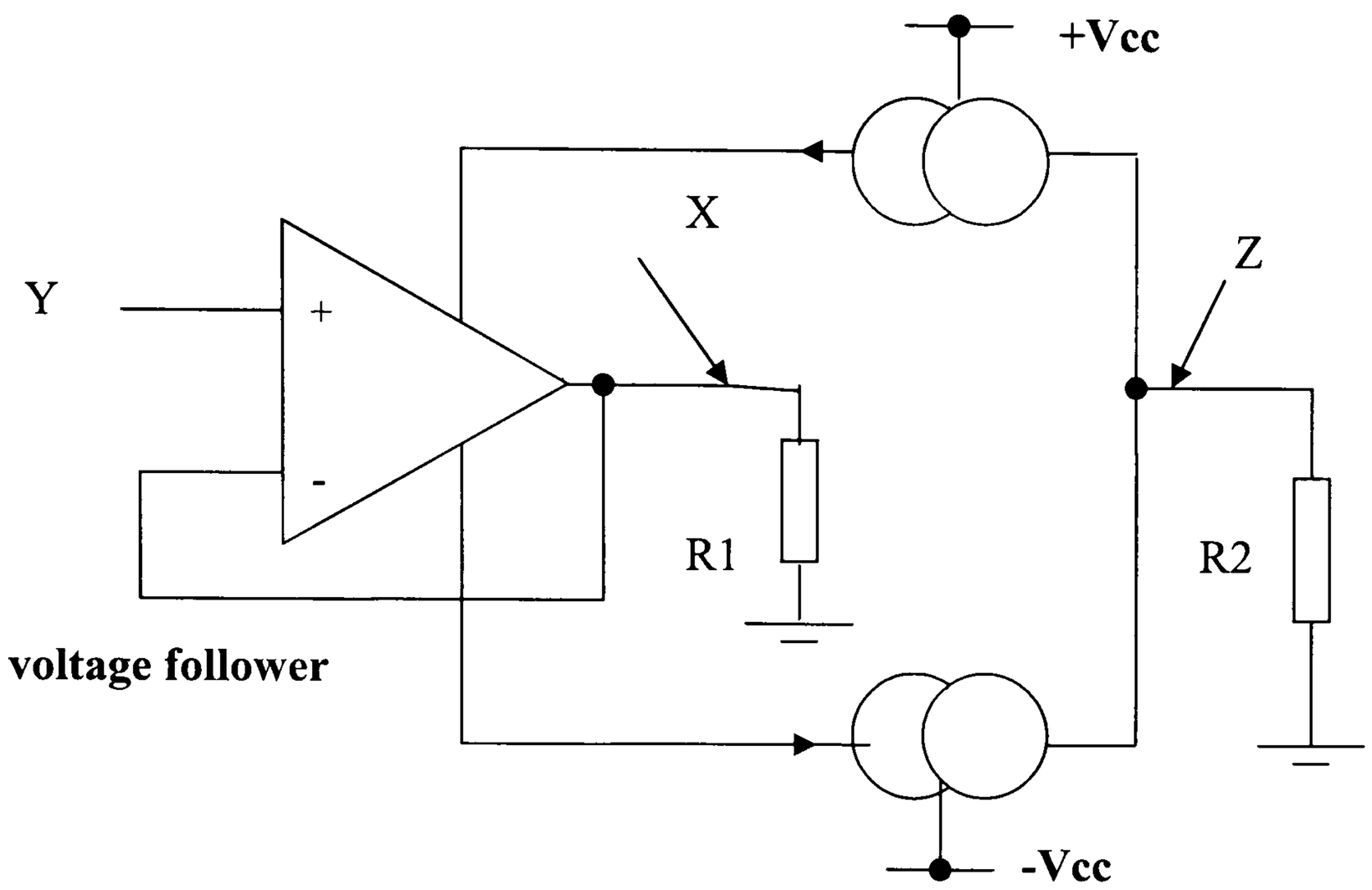

Figure 4-1 : Block Diagram of the CCII+

Figure 4-1 shows a basic overview of a CCII+. Note: the direction of the current in a current follwer determines whether the device is a CCII+ or CCII- **[4-4];** for a CCII+ the current through R1 should be in the same direction as R2; for a CCII- the current. For an ideal current conveyor node the voltage at 'X' should track the input voltage at node 'Y' the current through R1 should match that of R2, giving an overall gain from node 'Y' to 'X' of unity; and a gain from node 'Y' to 'Z' of R2/R1.

There are several types of current conveyors both using BJTs and CMOS devices **[4-6],[4-7],[4-8],[4-9,[4-10]**. This section will highlight a couple of examples of the current conveyor based on the source follower stages shown in Chapter Three (Section 3.4 'The proposed CMOS source follower for the current conveyor').

The first example of a current conveyor uses the translinear loop in the voltage follower stage shown below **[4-8]:**

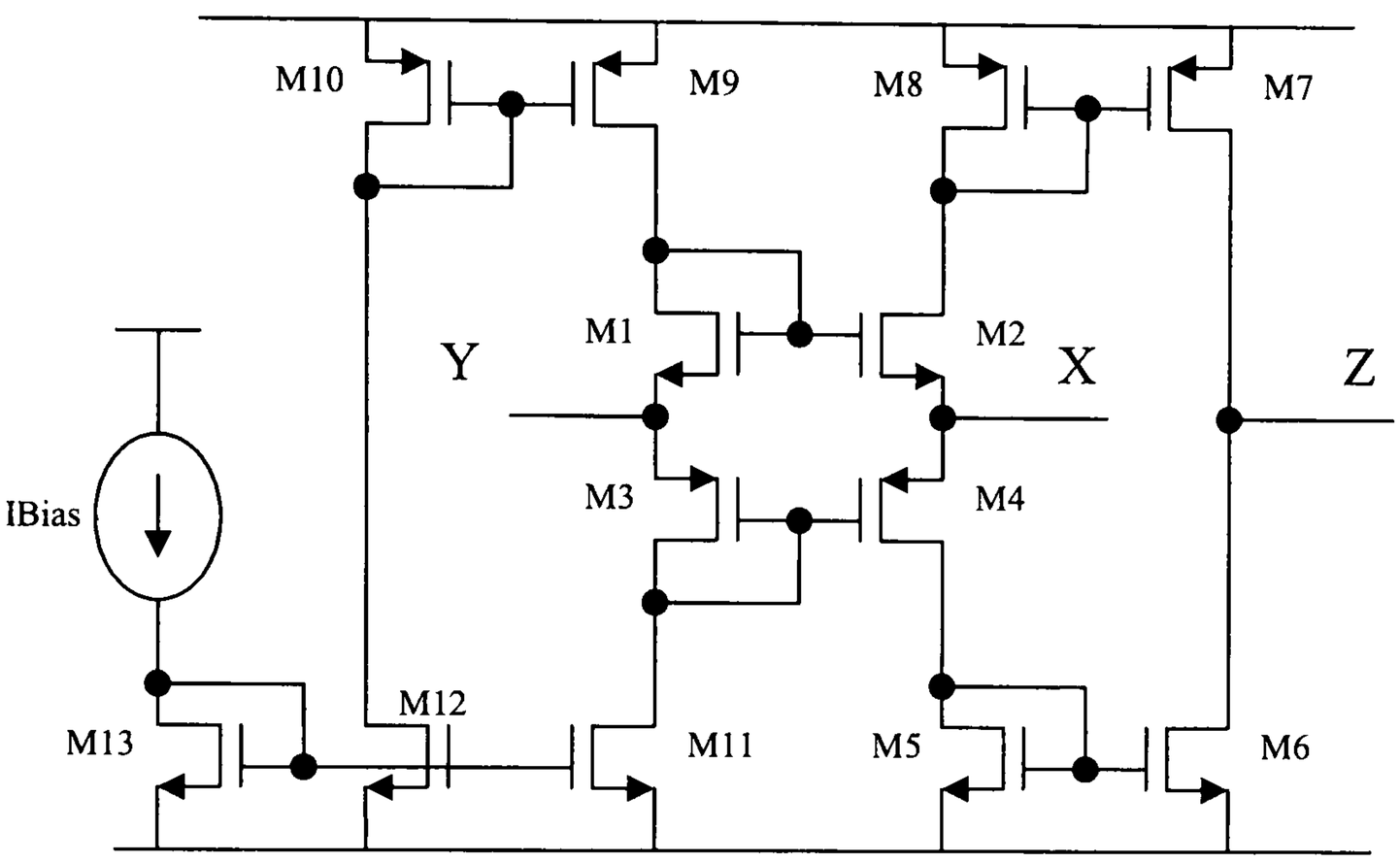

Figure 4-2 : A current conveyor using translinear loops.

Figure 4-2 gives an example of how a current conveyor can be made up by using translinear loops, transistors M1 to M4 make up a class AB complementary pair voltage follower that allows the output node X of the source follower to track the input node Y, M9 to M11 sets up the bias current (using IBias) to bias the current conveyor. M5,M6,M7 and M8 mirrors the current from node X to node Z and is the current follower of the current conveyor. The problem with this implementation of the current conveyor is that it is difficult to match the transistors and the biasing between node X and node Y especially when the output loading of node X being low impedance will be different to that of node Y high impedance if the standard CCII matrix is to be satisfied **[4-2].**

Another implementation of a current conveyor **[4-3]** is shown in Figure 4-3 is shown below:

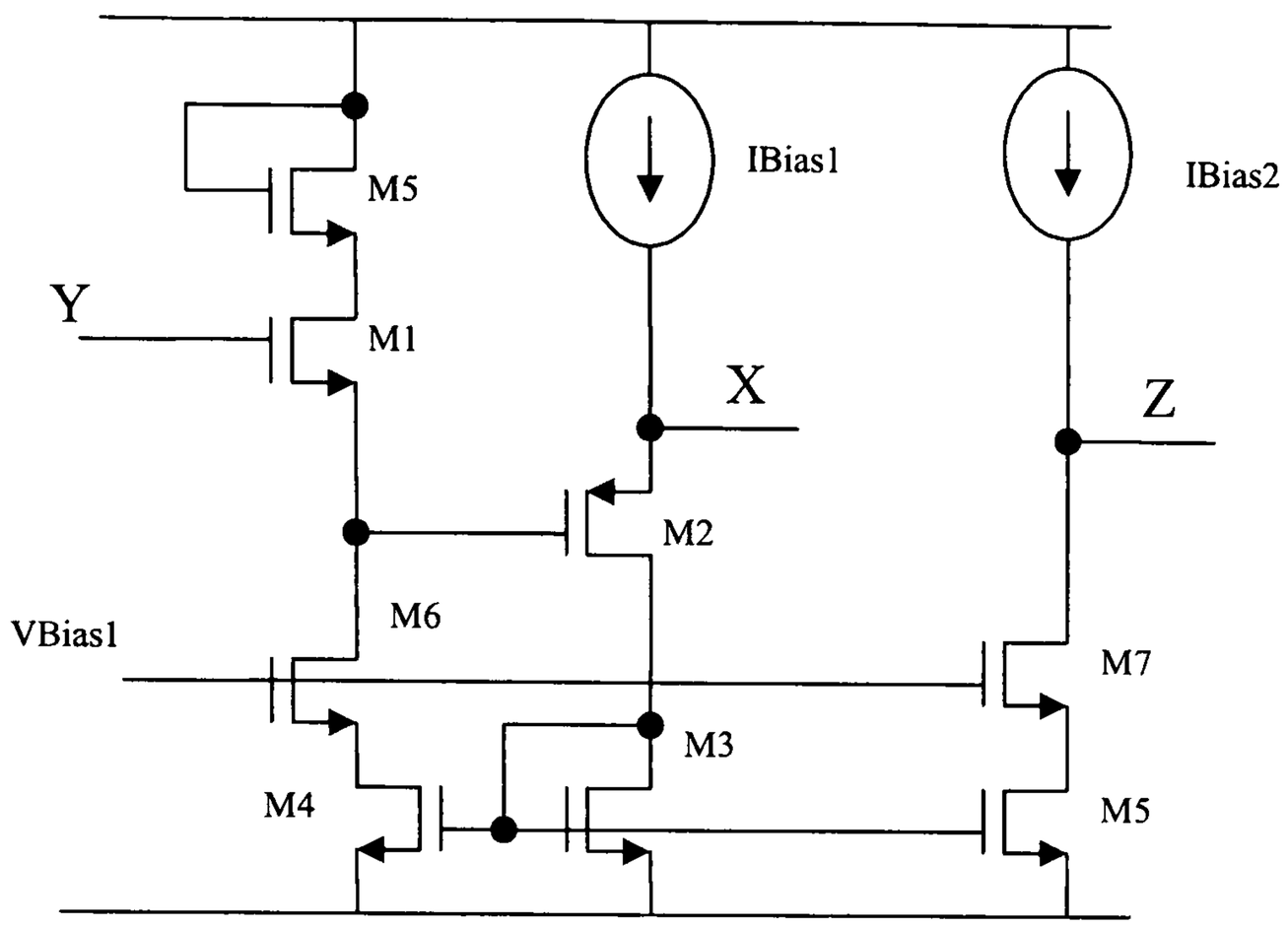

Figure 4-3 : A second generation current conveyor using a source follower input (node Y).

Figure 4-3 shows a second generation current conveyor with a source follower input M1. M2 is another source follower but uses a PMOS device and buffers the node X from node Y and as long as the transconductance of M1 (gm_1) matches the transconductance of (gm_2) then the voltage seen at the output of node X should match the voltage seen at node Y. Ibias1 should match Ibias2 as well as M7 matching M6 and M5 matching M4 and M3, this is to allow the current to be mirrored to node Z. Again the design is reliant on the transistors being precisely matched, and as transistor M1 is an NMOS device and M2 is a PMOS device it is difficult to match the transconductance of the devices as the surface mobility figures are different for NMOS and PMOS devices **[4-12]**. Also as explained in Chapter Three (section 3.4) this type of circuit uses two voltage follower gain stages between node Y and X which means that it is more important that the voltage gain of the voltage followers M1 and M2 are as close as possible to that of unity, as the gain error will be compounded as the output voltage gain between nodes Y and X is the multiple of the gains of the voltage followers M1 and M2.

After reviewing previously published CCIIs it was found that the best option was to build a current conveyor around the voltage follower shown in Figure 3-5 in Chapter Three which is a CMOS unbuffered amplifier. This solution has the advantage of offering a larger bandwidth than that of an OTA voltage follower type current conveyor, as it is not limited by the compensation capacitor of the OTA, but unlike other CMOS current conveyor architectures it also offers the same PSRR of the OTA type current conveyor. An example of the current conveyor using these voltage following techniques is shown in Figure 4-4 below:

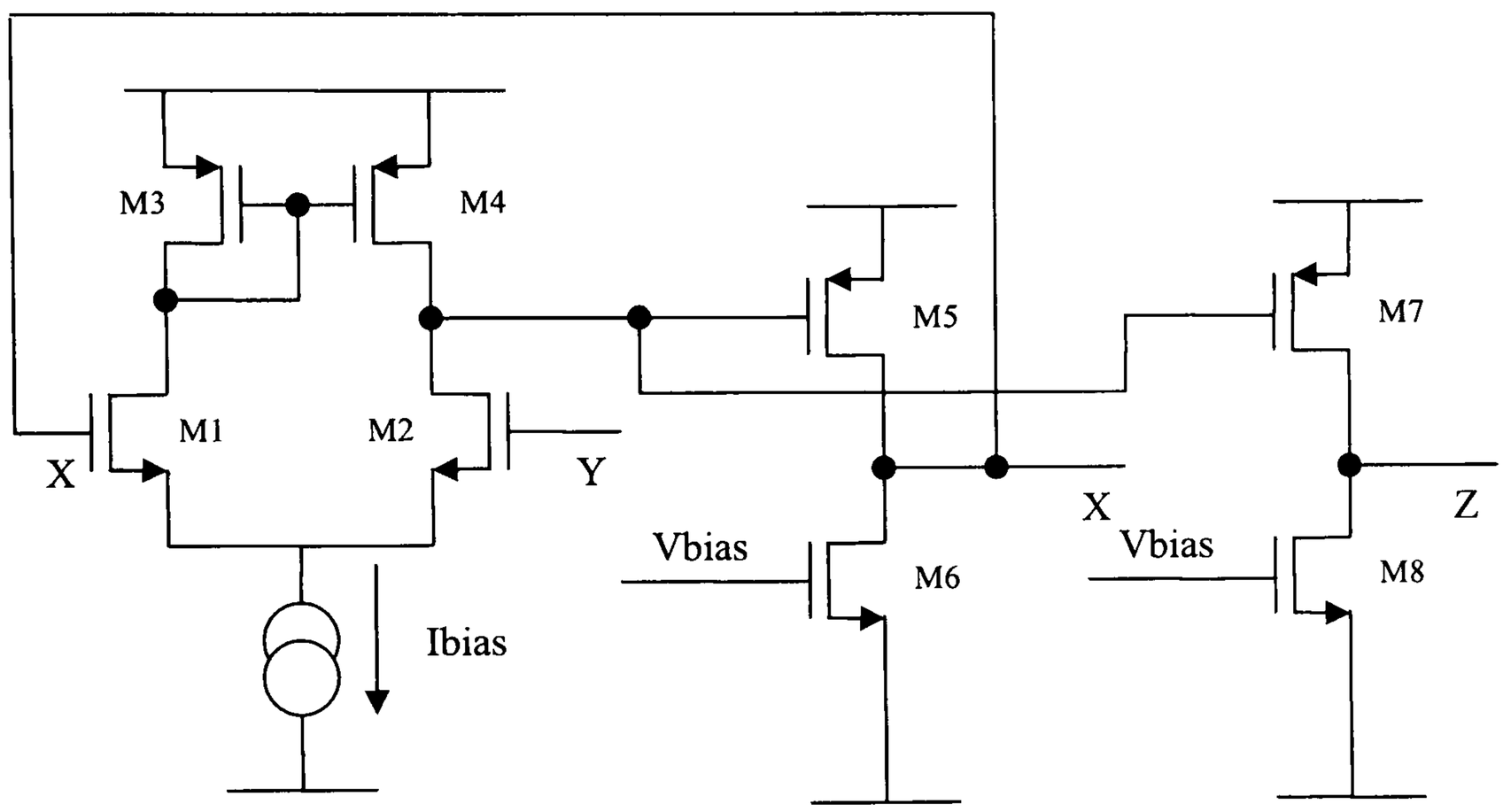

Figure 4-4: The proposed second generation current conveyor using a simple current mirror.

In Figure 4-4 transistors M1 to M6 make up the voltage follower as discussed in Section 3.4 in Chapter Three; transistors M5 and M7 is a single current mirror (current follower), that mirrors the output current from node X to node Z. M6 and M8 form a second current mirror used to subtract the DC bias current from M7.

This chapter will deal with several examples of current conveyor based on the architecture shown in Figure 4-4 by substituting M5 to M8 with versions of current mirrors discussed in Chapter Two. These versions of current conveyor will be simulated using the transistor models from the TSMC 0.18um process **[4-11],** and the results recorded.

4.3 The benchmark version of the current conveyor in CMOS.

4.3.1 Design.

To show the design improvements in the proposed current conveyor shown in Figure 4-4, it was decided to bench mark the design against a simplified version of the more popular design used in a lot of BJT current conveyors **[4-5]**. Figure 4-5 below shows the CMOS equivalent circuit:

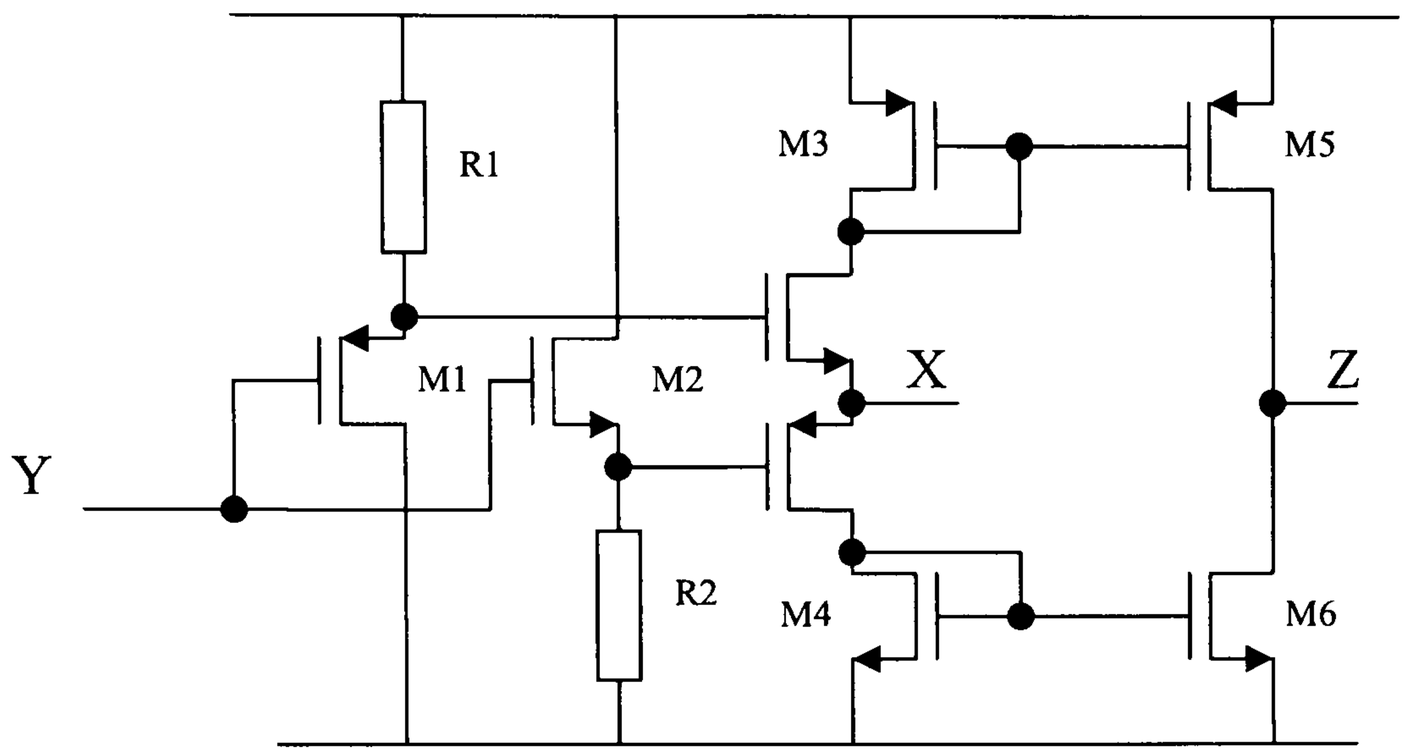

Figure 4-5: The benchmark version of the current conveyor in CMOS.

Figure 4-5 shows the current conveyor **[4-2]** used to benchmark the other designs described in this chapter. Transistors M3 and M4 make up the voltage follower and transistor M5 and M6 make up the current follower. Transistors M1 and M2 are used to eliminate the dead band region of the voltage follower so the voltage follower stage behaves as a class AB amplifier **[4-13].**

4.3.2 Simulation Results.

Using Figure 4-5 the following test circuit was drawn up as shown in Figure 4-6 below:

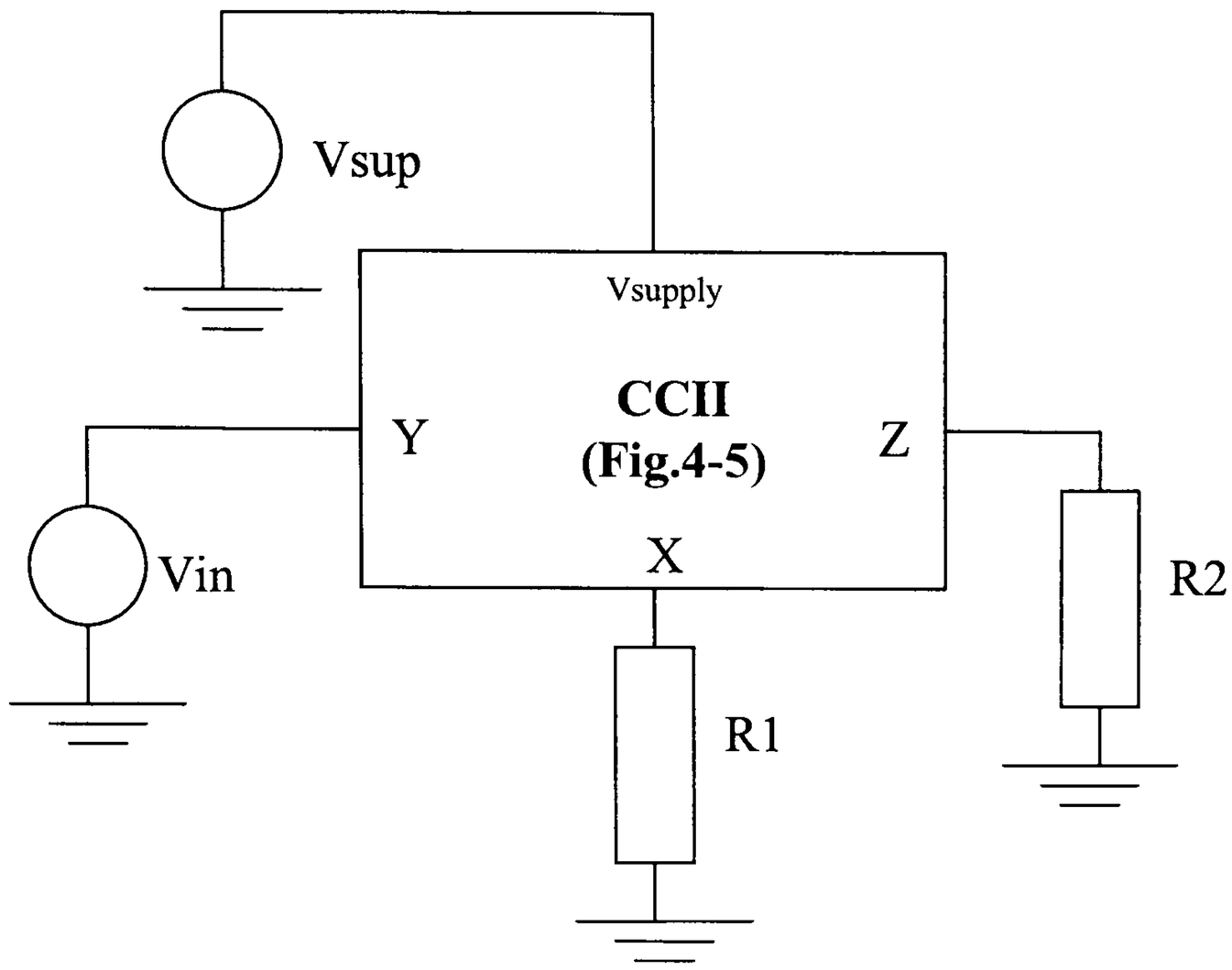

Figure 4-6: The test bench for the CMOS implementation of the benchmark CCII.

Figure 4-6 was tested using SPICE and the transistor models came from the TSMC 0.18μm design kit **[4-11]**:

The following parameters were used:

Resistors: $R1 = R2 = 1K\Omega$.

CMOS transistor dimensions:

NMOS: Width = 20μm; Length = 0.4μm;

PMOS: Width = 40μm; Length = 0.4μm;

Stimulus for Figure 4-6 (The test bench):

Vsup = 1.8V (DC); Vsup = 0V (AC); (for gain tests)

Vsup = 1.8V (DC) ; Vsup = 50mV (AC); (for PSRR test)

Vin = 0.9V (DC); Vin = 50mV (AC); (for gain tests)

Vin = 0.9V (DC); Vin= 0V (AC); (for PSRR test)

For gain test1: R1 = 1KΩ; R2 = 1KΩ

For gain test2: R1 = 1KΩ; R2 = 2KΩ

For Power Supply Rejection (PSRR) test: R1 = 1KΩ; R2 = 1KΩ

The test results looked specifically at the gain and the Power Supply Rejection Ratio (PSRR), which are the two main factors when considering the overall design of the current conveyor.

Results from gain test1

Figure 4-7 below shows the gain of X with respect to Y for the current conveyor this should be as close to unity as possible.

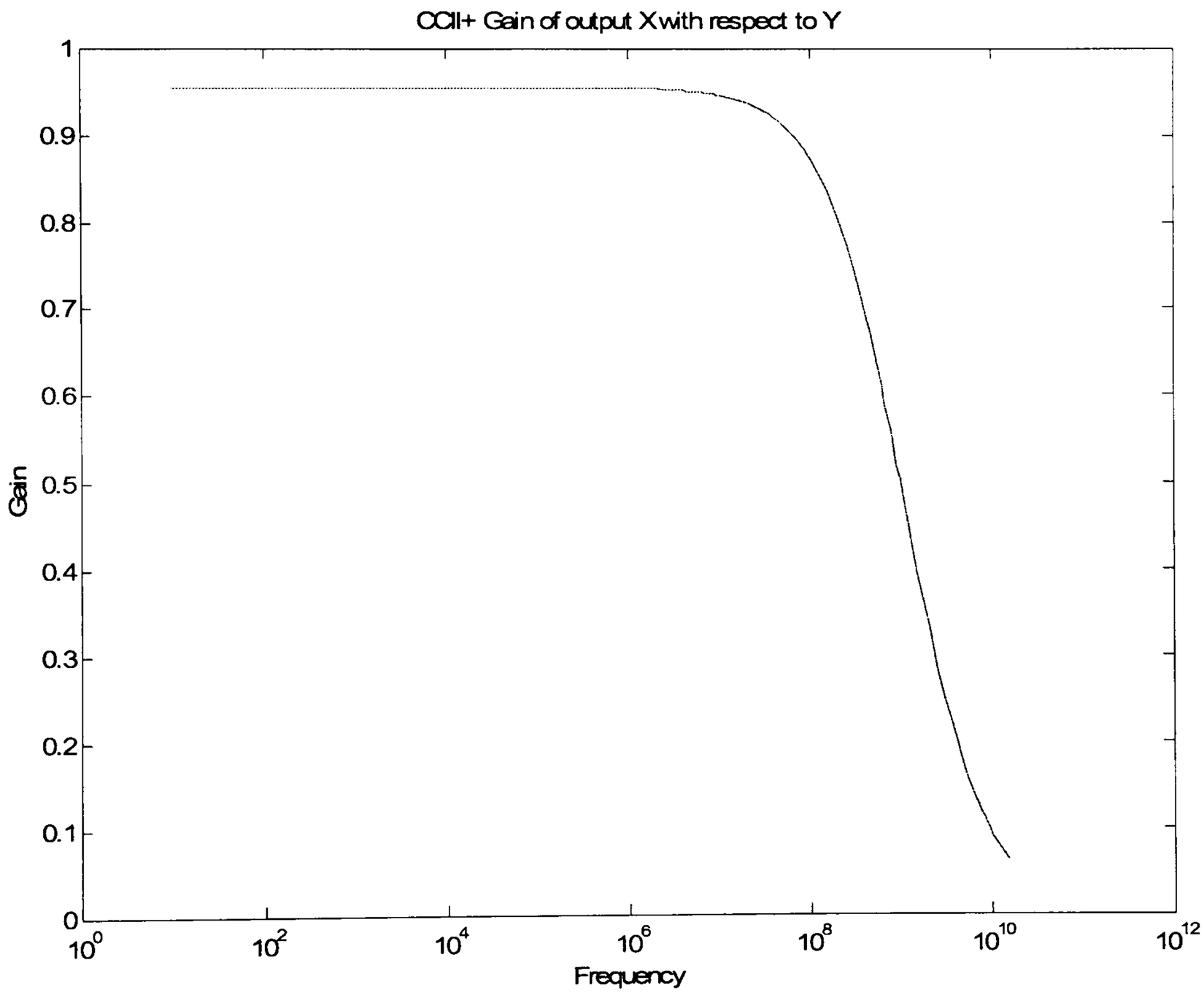

Figure 4-7: Gain of X with respect to Y for the CMOS implementation of the benchmark CCII.

The gain test1 summary of results:

Gain from Y to X = 0.955.

This shows a voltage gain error of 4.5% against the ideal voltage gain of 1. This figure is poor for a voltage follower and the results shown later in this chapter will show that a marked improvement in this figure can be achieved with the new current conveyor.

Bandwidth 3dB point = 1.059GHz, with a transistor f_T of 80GHz.

Equivalent Thevenin (r_{out}) of node X = 47.1 Ω.

Figure 4-8 shows the gain response of Z with respect to Y with the ideal gain equal to unity as R1 = 1KΩ and R2 = 1KΩ.

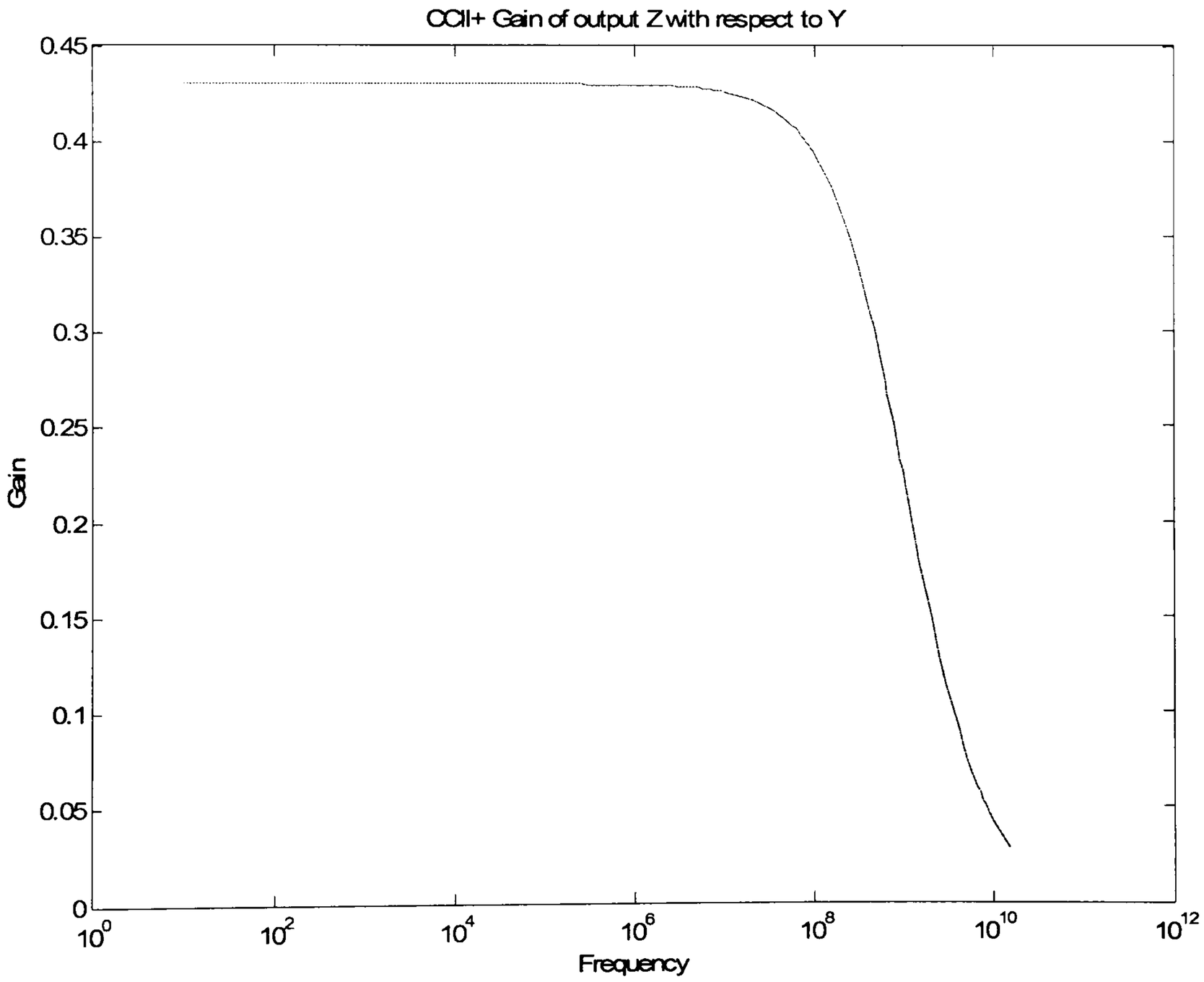

Figure 4-8: Gain of Z with respect to Y for the CMOS implementation of the benchmark CCII.

The gain test1 summary of results:

Gain from Y to Z = 0.43. The gain error between Y and Z is 57% as the expected gain was unity, which shows that this circuit architecture is extremely poor example of a current follower.

Bandwidth 3dB point = 1.059GHz.

Equivalent Thevenin (r_{out}) of node Z = 750 Ω.

Results from gain test2

Figure 4-9 below shows the gain response of X with respect to Y for the benchmark current conveyor this again should be as close to unity as possible:

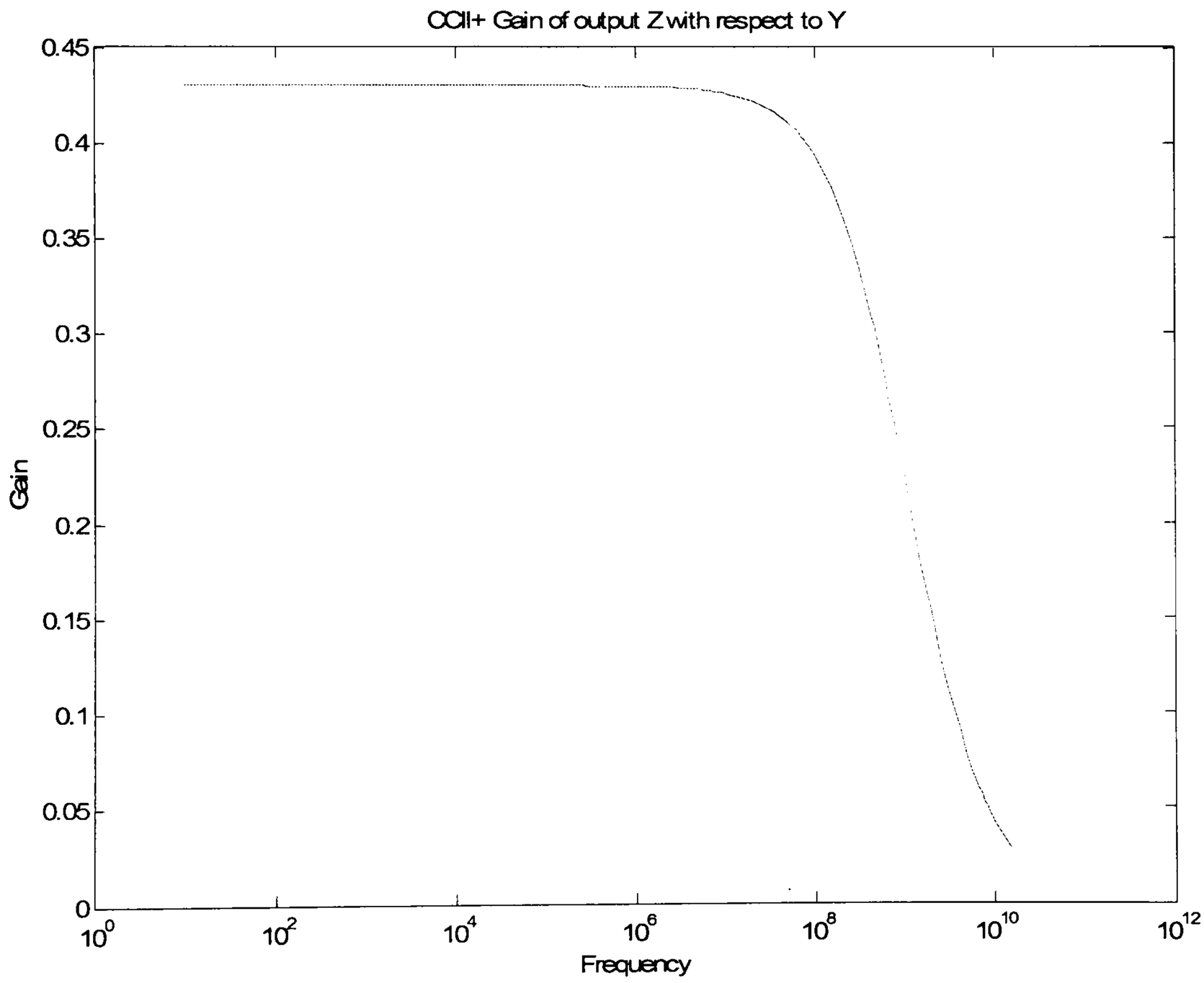

Figure 4-9: Gain of X with respect to Y for the CMOS implementation of the benchmark CCII.

The gain test2 summary of results:

Gain from Y to X = 0.81. Again the gain error is poor when changing the gain of the current conveyor, this time the error is 19.0%. This change in error from gain test 1, is due to the change in the biasing conditions of the circuit under test due to the new load on node Z.

Bandwidth 3dB point = 977MGHz. With a transistor f_T of 80GHz.

Equivalent Thevenin (r_{out}) of node X = $234\,\Omega$.

Figure 4-10 shows the gain response of Z with respect to Y with the R1 = $1K\Omega$ and R2 = $2K\Omega$, which should provide a voltage gain of 2:

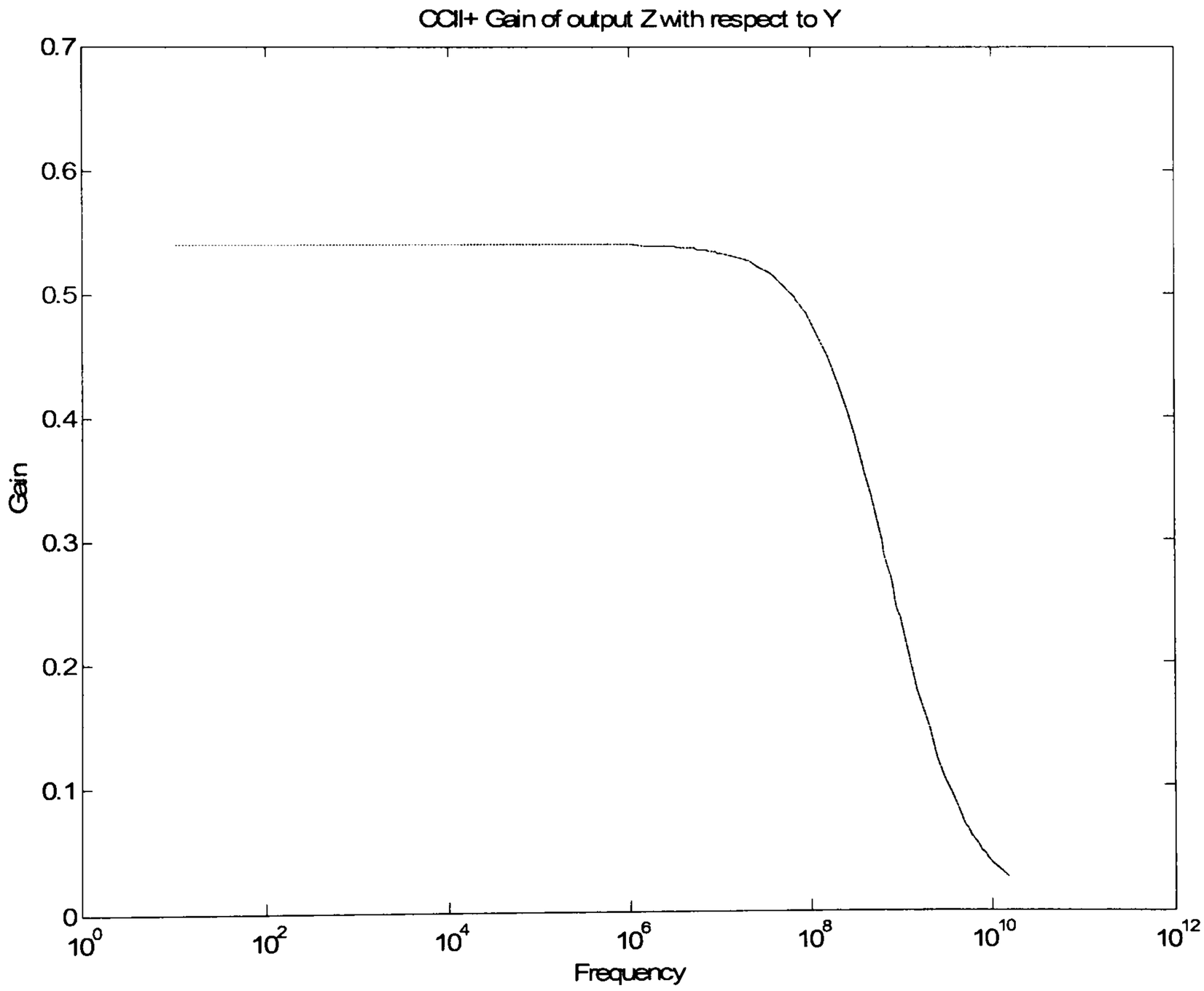

Figure 4-10: Gain of Z with respect to Y for the CMOS implementation of the benchmark CCII.

The gain test2 summary of results:

Gain from Y to Z = 0.54. This error has now been compounded and is now equal to 73%. The reason for this is that the biasing conditions, due to the change of load on node Z of the circuit under test, have now changed to such a degree that the current follower cannot; one mirror the proper value of current; and two the transistors do not have enough transconductance to drive the output.

Bandwidth 3dB point = 741MHz.

Equivalent Thevenin (r_{out}) of node Z = 740 Ω.

Results from Power Supply Rejection Ratio (PSRR) test

Figure 4-11 below shows the PSRR for the benchmark current conveyor. The definition of PSRR is 20log(Vout(AC)/Vsup(AC)) **[4-14]**, and this aim is to keep this figure should be kept as low as possible. The power supply rejection was measured on node 'Z' of the benchmark CCII:

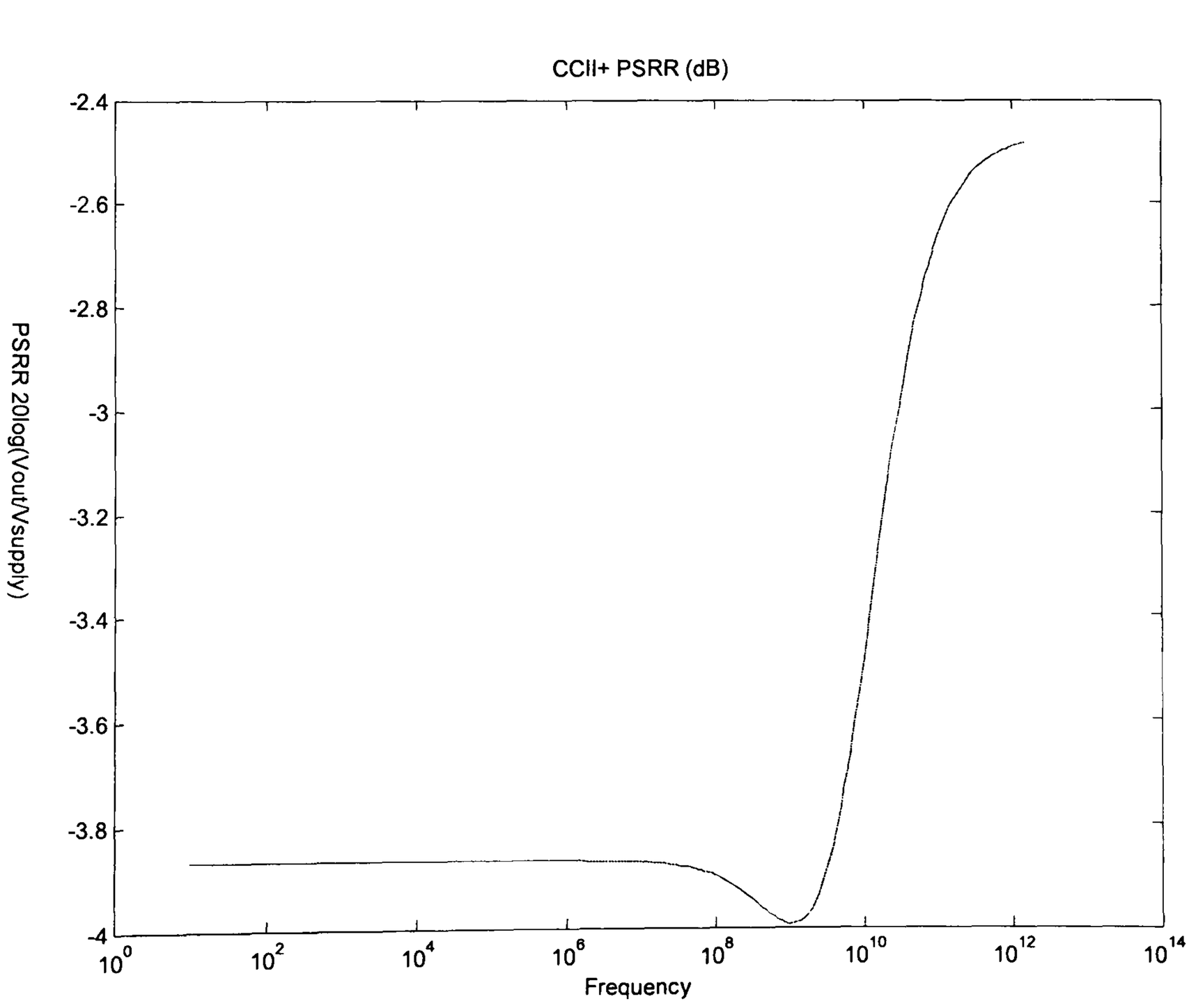

Figure 4-11: PSRR for the CMOS implementation of the original BJT CCII+.

The PSRR test summary of results:

PSRR = -3.87dB; falling to -4.51dB at 1.34GHz; rising eventually to -2.4dB at 11GHz. This is extremely poor and is due to the fact that this type of circuit has no ability to track changes in the power supply, i.e. most of the supply noise is fed directly to node X and Z because the power supply acts as a small signal input source on the current follower transistors M3 to M6 on Figure 4-5.

4.3.3 Summary of simulation of the benchmark CCII.

From the results in 4.3 it can be seen that the CMOS implementation of the benchmark CCII is unsatisfactory, as the output gain response of X with respect to Y is not close to the desired value of unity, also the gain between nodes X and Z does not reflect the expected output gain of R2/R1 (referring to Figure 4-6) as stated in the theory **[4-2]** and in Chapter One, and the impedance levels of node X and node Z are not good enough.

There is virtually no Power Supply Rejection Ratio (PSRR), this is due to the fact there is no relationship between any of the nodes X,Y and Z, and therefore no way of tracking the movements of X and Z to that of Y due to changes in supply voltage, as X, Y, Z, are totally independent of each other. Also the benchmark CCII suffers from having a low output impedance on nodes X and Z, due to the CMOS transistors having low values of transconductance (gm), and a low equivalent voltage. This has the effect of reducing the gain as the low impedance combines with the load impedances (R1,R2) and reduces the overall impedance of node X and Z. It is possible to improve the factors previously described, and improving the overall performance of this circuit, such as increasing the length of the transistors which will have the effect of improving the Early voltage of the device, and widening the transistors to improve their transconductance (gm). But the overall architecture for a CMOS benchmark current conveyor CCII is poor and that is why the architectures described in Section 4.4 based on what was discussed in Chapters Two and Three will give a much improved performance without the need of increasing the dimensions of the CMOS transistors.

4.4 Design of a new current conveyor (CCII +).

4.4.1 A Simple current mirror CCII+.

4.4.1.1 Design.

Applying the theories from Chapters Two and Three Figure 4-12 below shows the new current conveyor using a simple current mirror described in Section 2.4.1 (Chapter Two):

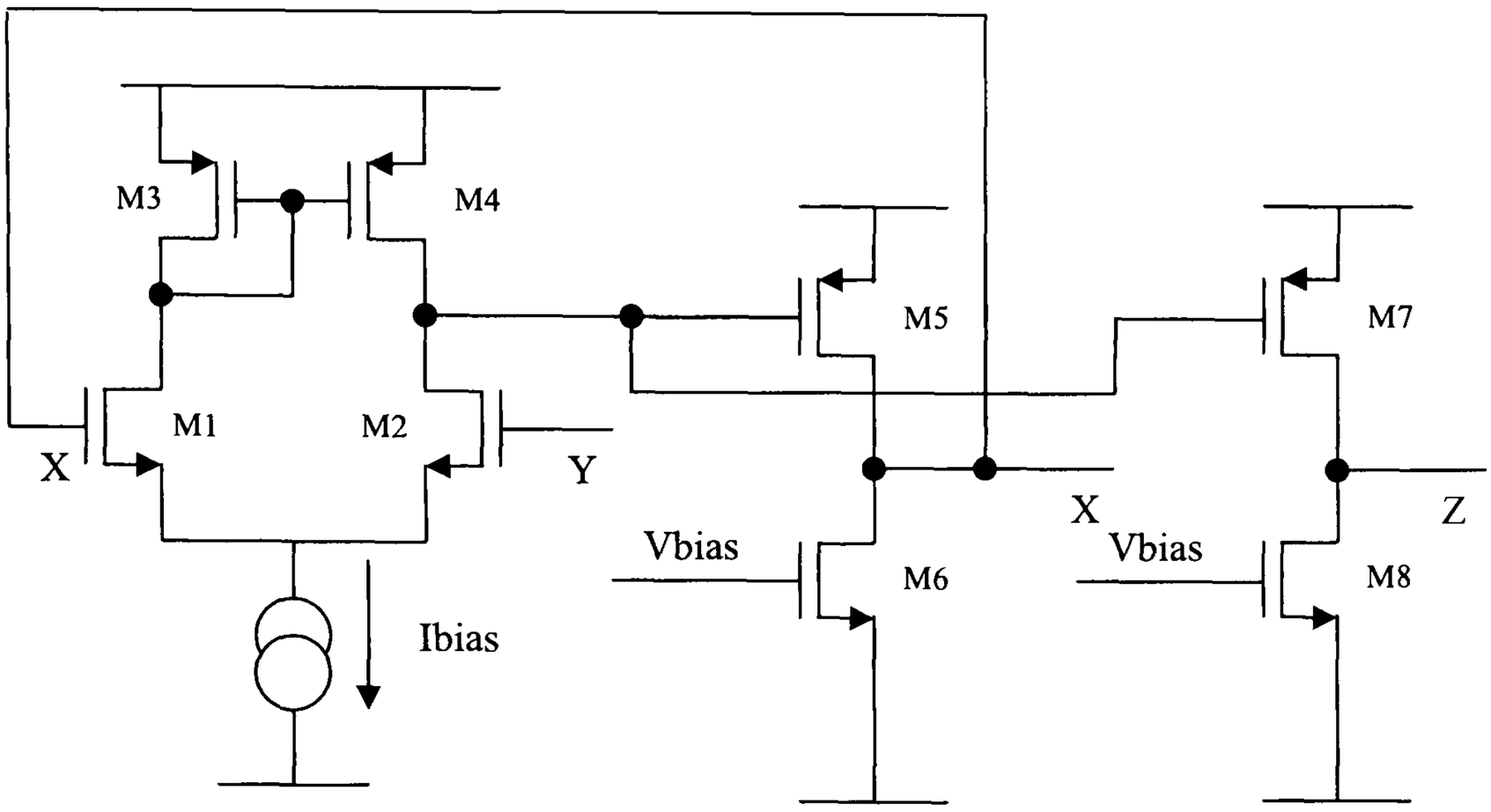

Figure 4-12: The proposed current conveyor (CCII+) using a simple current mirror.

Figure 4-12 shows the current conveyor (CCII+) which is a practical realisation of the circuit of Figure 4-1. The voltage follower, described in Chapter Three, is made up of transistors M1 to M6. The bias current (Ibias) is set to a nominal value which sets up the transconductance (gm) of the long tail pair M1 and M2. M5 and M6 provide the output of the voltage follower, and the gate of M5 is tied to the gate of M7 which with M8 makes up the current follower. Because there is feedback the output X can track Y, and as the gate of transistor M5 which is used to drive the output of the voltage follower, also is connected the gate of M7 used to drive the output of the current follower stage. This means that the output current of Z matches that of X assuming that the dimensions of M5 matches that of M7 and M6 matches M8. The only requirement is that the same power supply must be connected to all devices in this design, Thus will improving the overall Power Supply Rejection Ratio (PSRR) of this

circuit. It should be noted too that the long tailed pair bias current (Ibias) is primarily responsible for giving the CCII a very good PSRR.

4.4.1.2 Simulation Results.

Using Figure 4-12 the following test circuit was drawn up as shown in Figure 4-13 below:

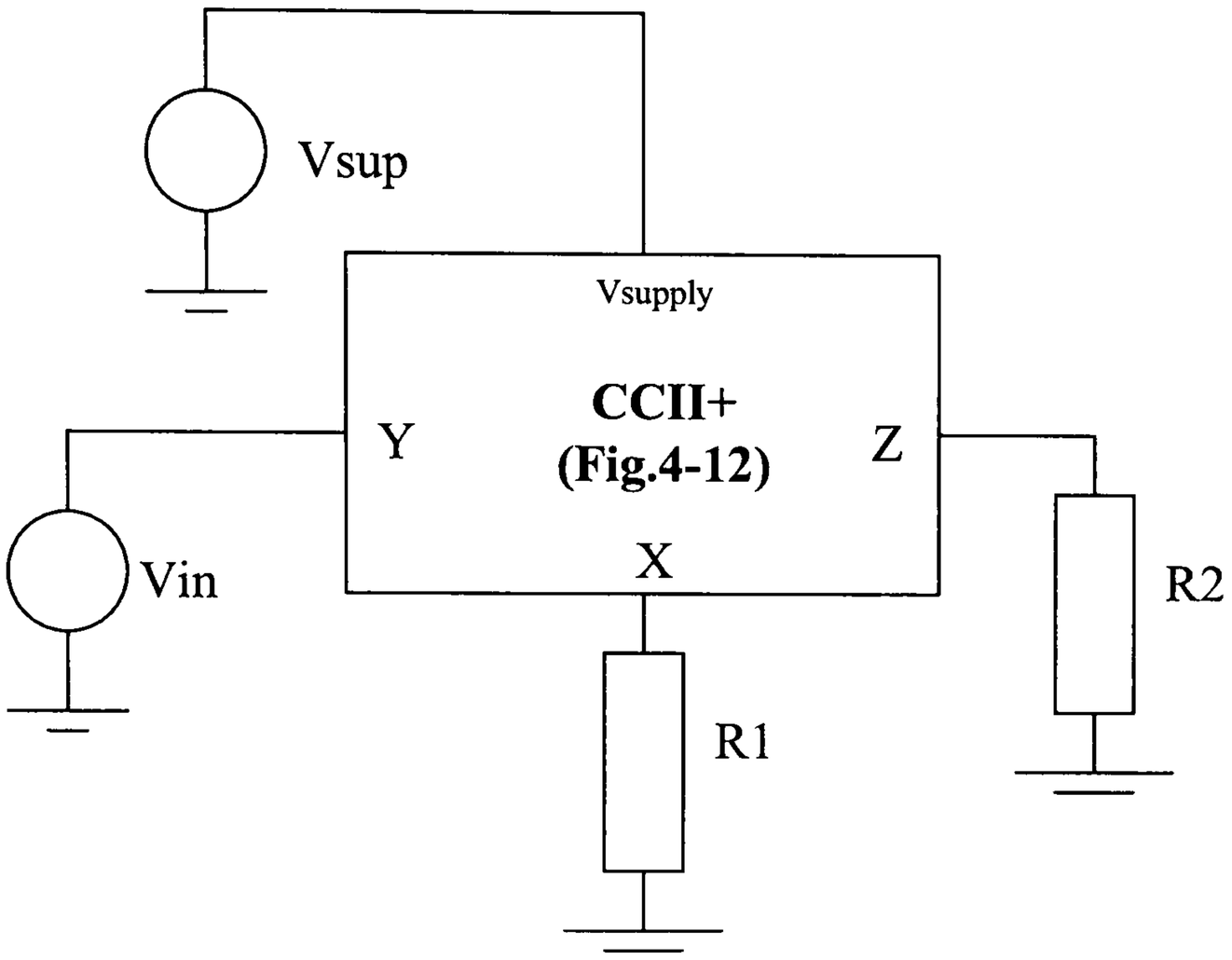

Figure 4-13: The test bench for the proposed current conveyor (CCII+) using a simple current mirror.

Figure 4-13 was tested using Eldo spice and the transistor models came from the TSMC 0.18μm design kit **[4-11]**:

The following parameters were used:

For Figure 4-12 (New CCII+ using a simple current mirror):

Resistors: $R1 = R2 = 1K\Omega$.

CMOS transistor dimensions:

NMOS: Width = 20μm; Length = 0.4μm;

PMOS : Width = 40μm; Length = 0.4μm;

Stimulus for Figure 4-13 (The test bench):

Vbias = 0.45V (DC); Ibias = 50μA (DC);

Vsup = 1.8V (DC); Vsup = 0V (AC); (For gain tests)

Vsup = 1.8V (DC); Vsup = 50mV (AC); (For PSRR test)

Vin = 0.9V (DC); Vin = 50mV (AC); (For gain tests)

Vin = 0.9V (DC); Vin= 0V (AC); (For PSRR test)

For gain test1:

R1 = 1KΩ; R2 = 1KΩ

For gain test2:

R1 = 1KΩ; R2 = 2KΩ

For Power Supply Rejection (PSRR) test:

R1 = 1KΩ; R2 = 1KΩ

The test results looked specifically at the gain and the Power Supply Rejection Ratio (PSRR), which are the two main factors when considering the overall design of the CCII+.

Results from gain test1

Figure 4-14 below shows the gain of X with respect to Y for the current conveyor this should be as close to unity as possible:

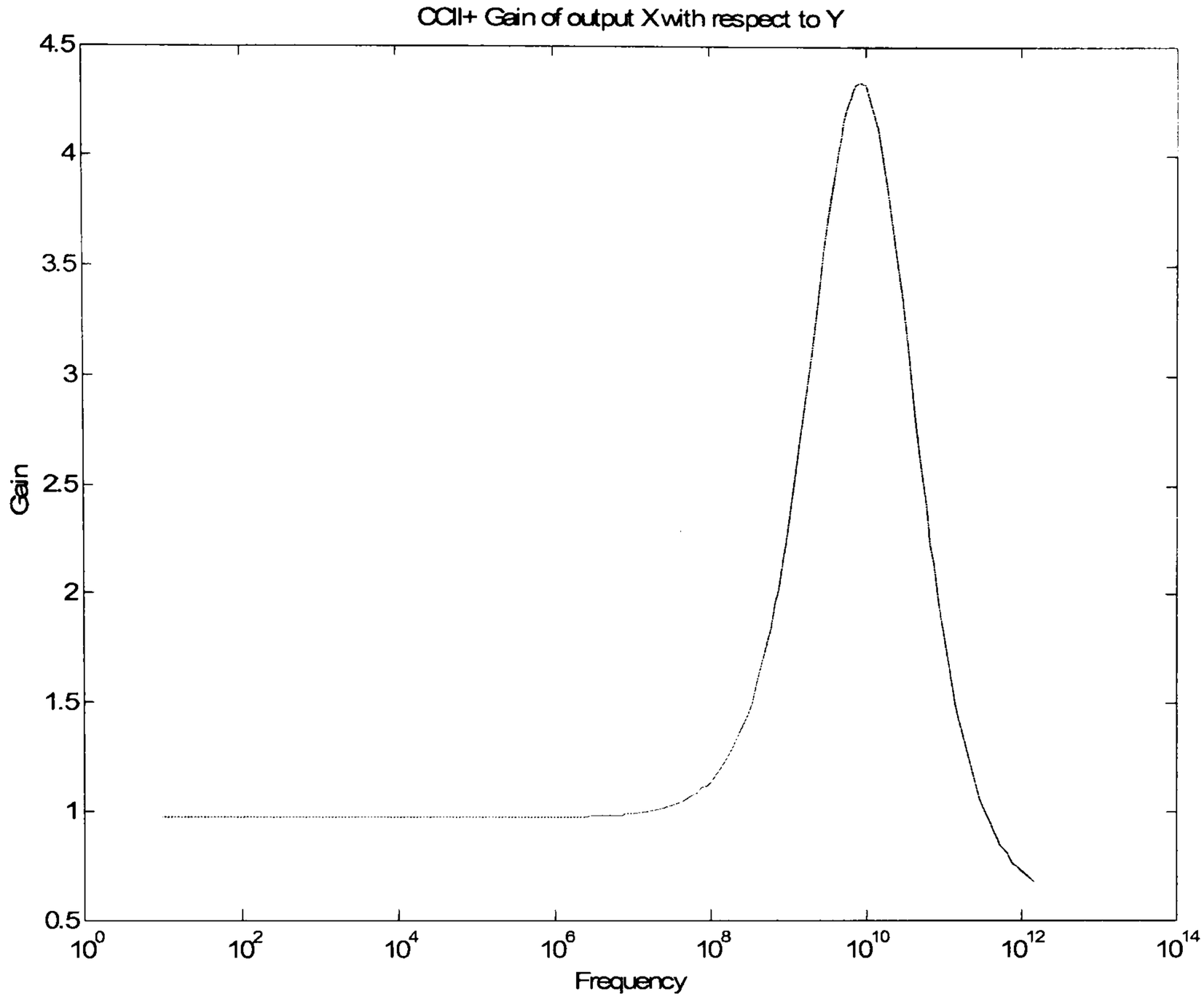

Figure 4-14: Gain of X with respect to Y for the proposed CCII+ using a simple current mirror.

The gain test1 summary of results:

Gain from Y to X = 0.9996; (peaking at a gain of 4.4 at 4.365GHz). This shows a voltage gain error of 0.04% against the ideal voltage gain of 1, this figure shows that the gain error has reduce to 1% of that of the benchmark current conveyor shown in Figure 4-5.

Equivalent Thevenin (r_{out}) of node X = 0.4Ω. This impedance is around 1% of the benchmark current conveyor in Figure 4-5.

Figure 4-15 shows the gain response of Z with respect to Y with the ideal gain equal to unity as $R1 = 1K\Omega$ and $R2 = 1K\Omega$.

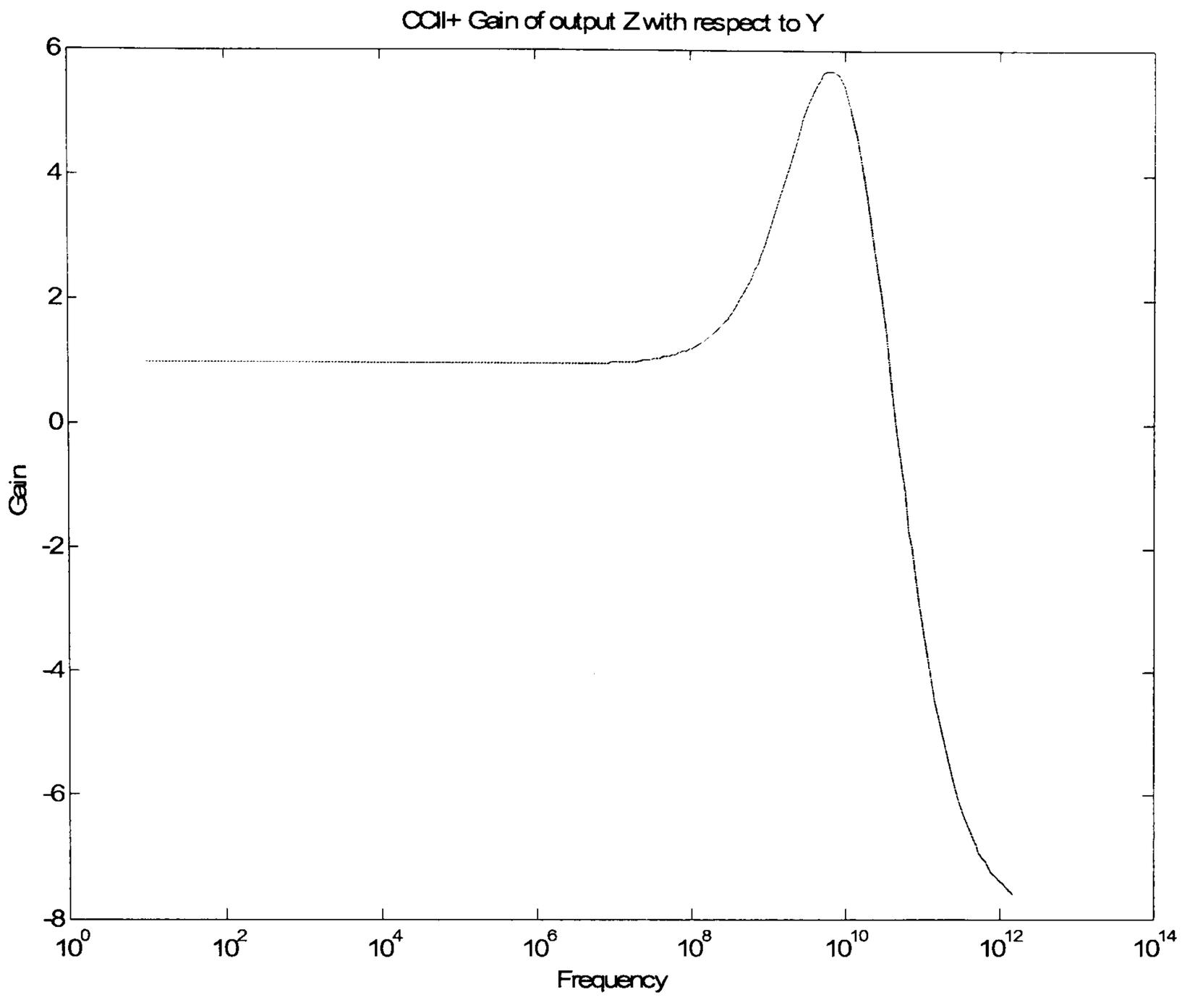

Figure 4-15: Gain of Z with respect to Y for the proposed CCII+ using a simple current mirror.

The gain test1 summary of results:

Gain from Y to Z = 0.972; (peaking at a gain of 5.9 at 4.365GHz). This shows a significant improvement in the gain accuracy over the benchmark CCII, the gain error is 2.8% compared to 57%, it will be shown how this again can be improved upon later on in this chapter. The bandwidth has now been increased to 4.365GHz compared to that of 1.059GHz for the benchmark CCII, this shows a vast improvement.

Equivalent Thevenin (r_{out}) of node $Z = 34.7K\Omega$. This compares to an impedance of 740Ω for the benchmark CCII shown in figure 4-5, a significant improvement.

Results from gain test2

Figure 4-16 below shows the gain of X with respect to Y for the current conveyor (CCII+) this again should be as close to unity as possible:

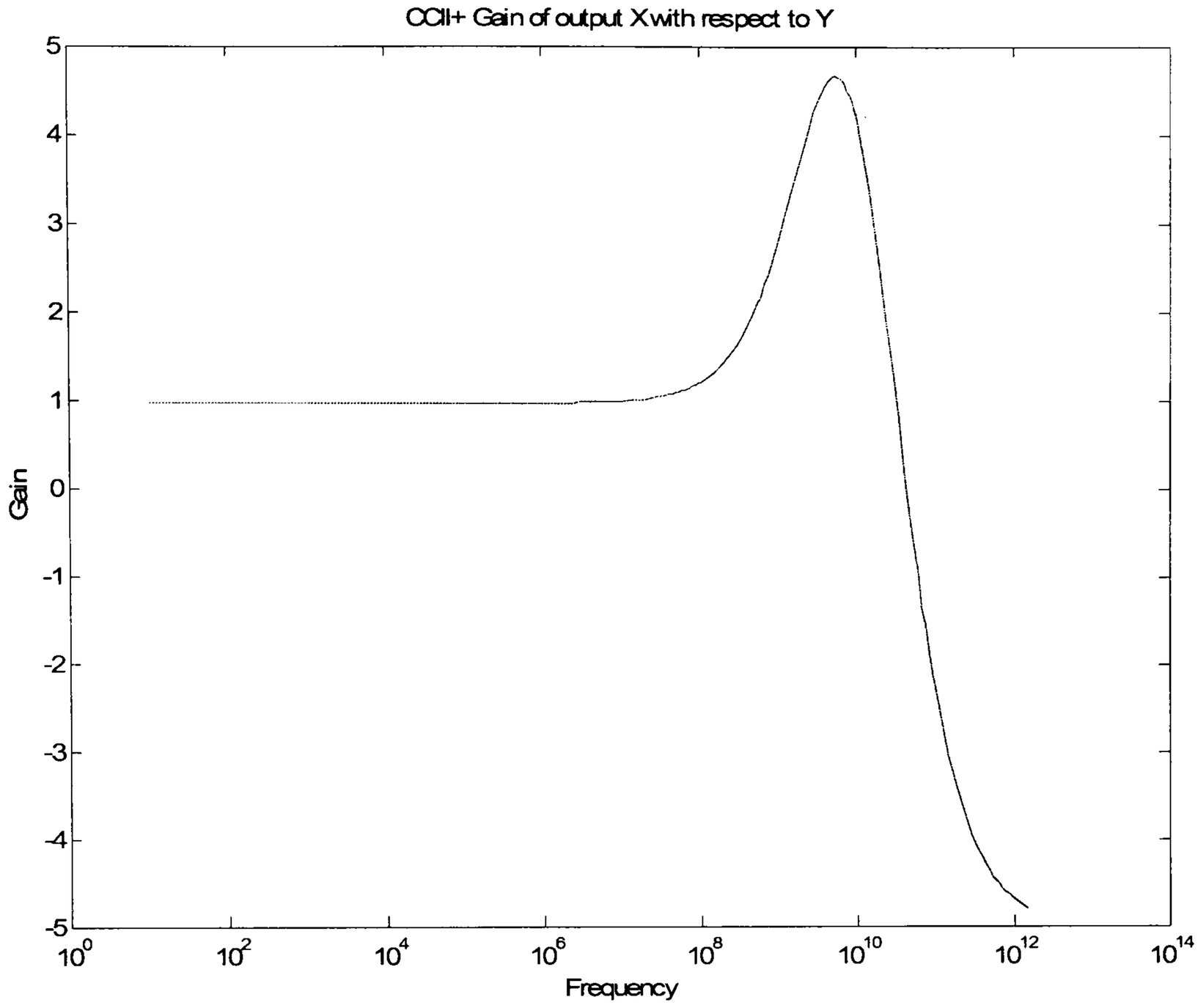

Figure 4-16: Gain of X with respect to Y for the proposed CCII+ using a simple current mirror.

The gain test2 summary of results:

Gain from Y to X = 0.972; (peaking at a gain of 4.8 at 4.12GHz). This shows a gain error of 2.8% and is a marked improvement on the benchmark CCII which showed a gain error of 19.0%. Again this will be improved upon later on in this chapter.

Equivalent Thevenin (r_{out}) of node X = $28\,\Omega$. This compares to an impedance of $234\,\Omega$ for the benchmark CCII current conveyor shown in Figure 4-5, a significant improvement.

Figure 4-17 shows the gain response of Z with respect to Y with R1 = 1KΩ and R2 = 2KΩ, which should provide a voltage gain of 2:

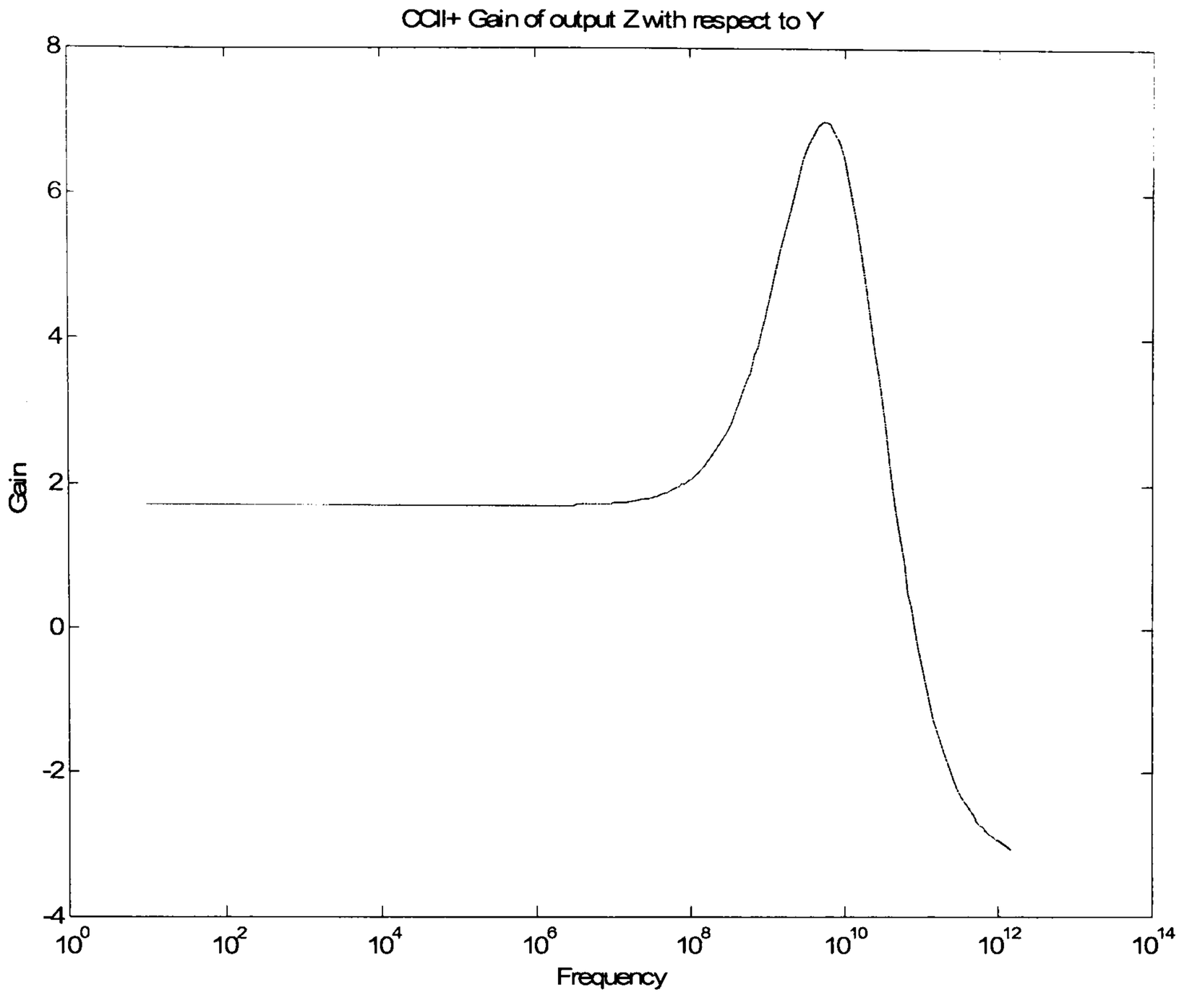

Figure 4-17: Gain of Z with respect to Y for the proposed CCII+ using a simple current mirror.

The gain test2 summary of results:

Gain from Y to Z =1.707; (peaking at a gain of 4.8 at 4.12GHz). This shows a improvement in the gain accuracy compared to that of the benchmark CCII, the gain error is 14.6% compared to 73%, this is still poor and needs improvement. The bandwidth has now been increased to 4.12GHz compared to that of 741MHz for the benchmark CCII, showing a vast improvement.

Equivalent Thevenin (r_{out}) of node Z = 11.7KΩ. This compares to an impedance of 740Ω for the benchmark CCII current conveyor shown in Figure 4-5, a marked improvement.

Results from Power Supply Rejection Ratio (PSRR) test

Figure 4-18 below shows the PSRR for the current conveyor (CCII+). The definition of PSRR is 20log(Vout(AC)/Vsup(AC)) **[4-14]**, and this aim is to keep this figure should be kept as low as possible. The power supply rejection was measured on node 'Z' of the CCII+:

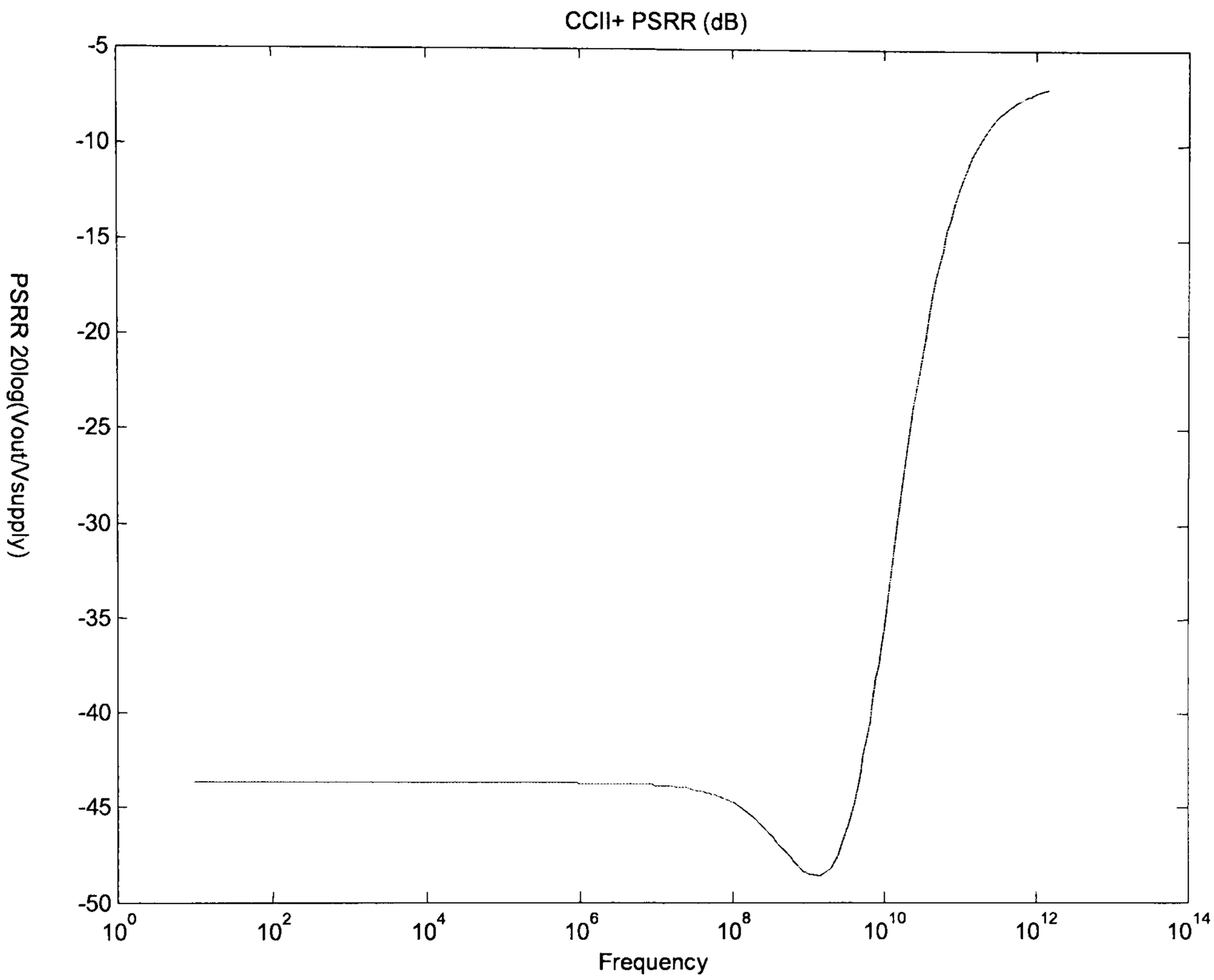

Figure 4-18: PSRR for the new simple current mirror CCII+.

The PSRR test summary of results:

PSRR = -43.7dB; falling to -48.1dB at 1.04GHz; rising eventually to -4.3dB at 4.65GHz.

Note: The ideal long tail pairs bias current contributes to the high value of PSRR, in practice this figure will be lower as a practical biasing circuit would also be affected by the power supply.

Again the collapse of PSRR above 1GHz is due to the device capacitance linking the power supply directly into the signal path. This is seen on virtually all circuits at varying frequencies and is unavoidable but is seldom a practical problem.

4.4.1.3 Summary of the analysis of the CCII of Figure 4-12.

From these results it can be seen that the gain of X with respect to Y is much improved and actually when R1=R2 at 1KΩ the gain was the required unity, and Y to Z is much closer the required gain of unity that of 0.972 compared with 0.955, seen in the previous benchmark design in Section 4.3. But the design again suffers from an insufficiently high Thevenin output impedance on node the Z, as can be seen from the results in gain test 2 where the gain is much below the expect value of 2 at 1.707. This can be improved upon and the examples in the next section will show current mirror architectures which will do this.

Also from the results it can be seen that the Power Supply Rejection (PSRR) has improved by a factor of 40dB to -43dB from the benchmark design this means that the noise from the power supply has been reduced by a factor of 100. This is due the fact that the voltage follower of the current conveyor can now track the power supply as there is feedback present. Therefore any changes in supply are fed back to the input of the voltage follower, and the output of the follower can then correct its output accordingly. The current follower will do the same as long as the power supply to the voltage follower is the same as the power supply to the current follower.

Another factor to be taken into account is now there is gain peaking whereas the output from the original BJT type CCII+ did not have this. This is due to the uncompensated voltage follower in this design when feedback is applied to it there will be a point of instability **[4-15]**. This is not a problem as the circuit has fixed unity feedback and this can be then compensated for by adding the appropriate low pass filtering to the output stages (nodes X and Z) to make sure that the roll off occurs before the point of instability if required.

4.4.2 A cascode current mirror CCII +.

4.4.2.1 Design.

Applying Chapters Two and Three Figure 4-19 below shows the new current conveyor using a cascode current mirror described in Section 2.4.2 (Chapter Two):

:

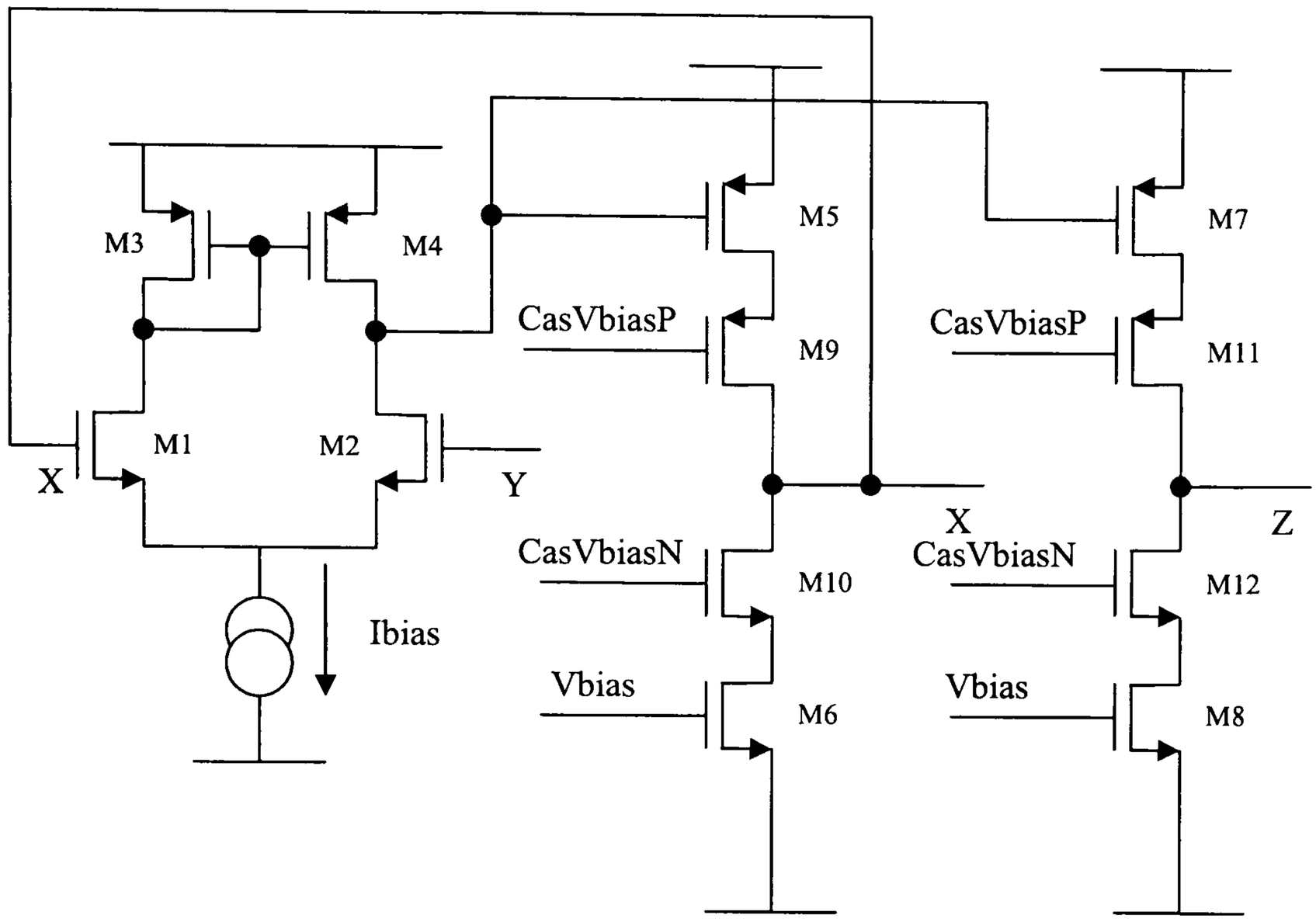

Figure 4-19: The New CCII+ using a cascode current mirror.

Referring to Figure 4-12, Figure 4-19 shows the current conveyor (CCII+) which works in the same way as Figure 4-12, except transistors M9 to M12 have been added. These are the cascode transistors and are biased by fixed voltages CasVbiasN and CasVbiasP, these transistors are used to increase the Thevenin equivalent impedance by a factor of around 80 (based on the results in chapter Two) specifically on node Z and therefore improving the voltage gain of the current conveyor under test. As well as transistors M5 to M8 matching in size as explained in Section 4.4.1.1, transistors M9 to M12 must also match to provide symmetry in the circuit and to allow current to be mirrored from node X to node Z with a unity current gain.

4.4.2.2 Simulation Results.

Using Figure 4-19 the following test circuit was drawn up as shown in Figure 4-17 below:

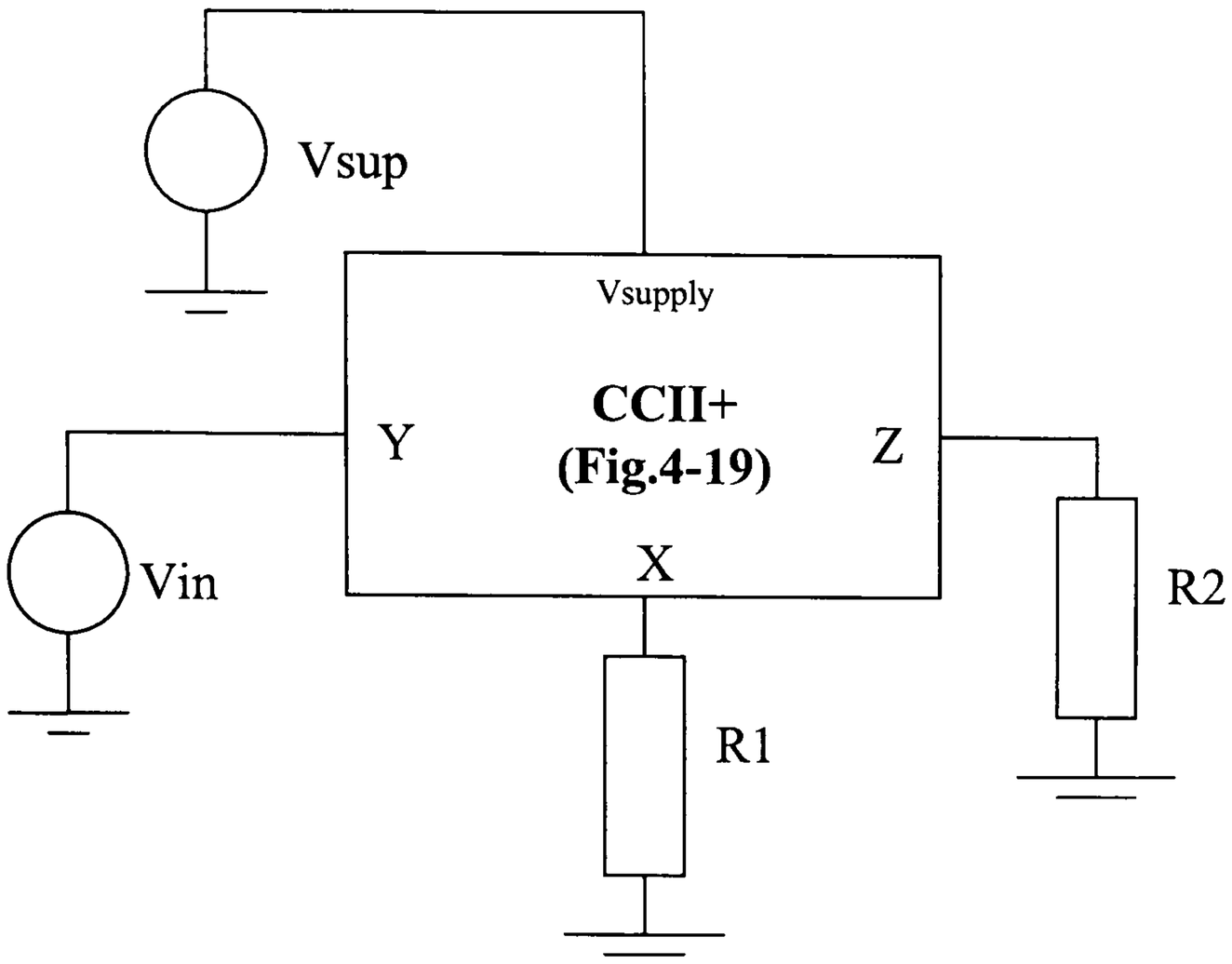

Figure 4-20: The test bench for the proposed current conveyor (CCII+) using a cascode current mirror.

Figure 4-20 was tested using Eldo spice and the transistor models came from the TSMC 0.18μm design kit **[4-11]**:

The following parameters were used:

Resistors: $R1 = R2 = 1K\Omega$.

CMOS transistor dimensions:

NMOS: Width = 20μm; Length = 0.4μm;

PMOS: Width = 40μm; Length = 0.4μm;

Stimulus for Figure 4-20 (The test bench):

Vbias = 0.45V (DC); Ibias = 50μA (DC);

CasVbiasN = 0.6V (DC); CasVbiasP = 1.2V (DC);

Vsup = 1.8V (DC); Vsup = 0V (AC); (For gain tests)

Vsup = 1.8V (DC); Vsup = 50mV (AC); (For PSRR test)

Vin = 0.9V (DC); Vin = 50mV (AC); (For gain tests)

Vin = 0.9V (DC); Vin= 0V (AC); (For PSRR test)

For gain test1:

R1 = 1KΩ; R2 = 1KΩ

For gain test2:

R1 = 1KΩ; R2 = 2KΩ

For Power Supply Rejection (PSRR) test:

R1 = 1KΩ; R2 = 1KΩ

The test results looked specifically at the gain and the Power Supply Rejection Ratio (PSRR), which are the two main factors when considering the overall design of the CCII+.

Results from gain test1

Figure 4-21 below shows the gain of X with respect to Y for the current conveyor (CCII+) this should be as close to unity as possible:

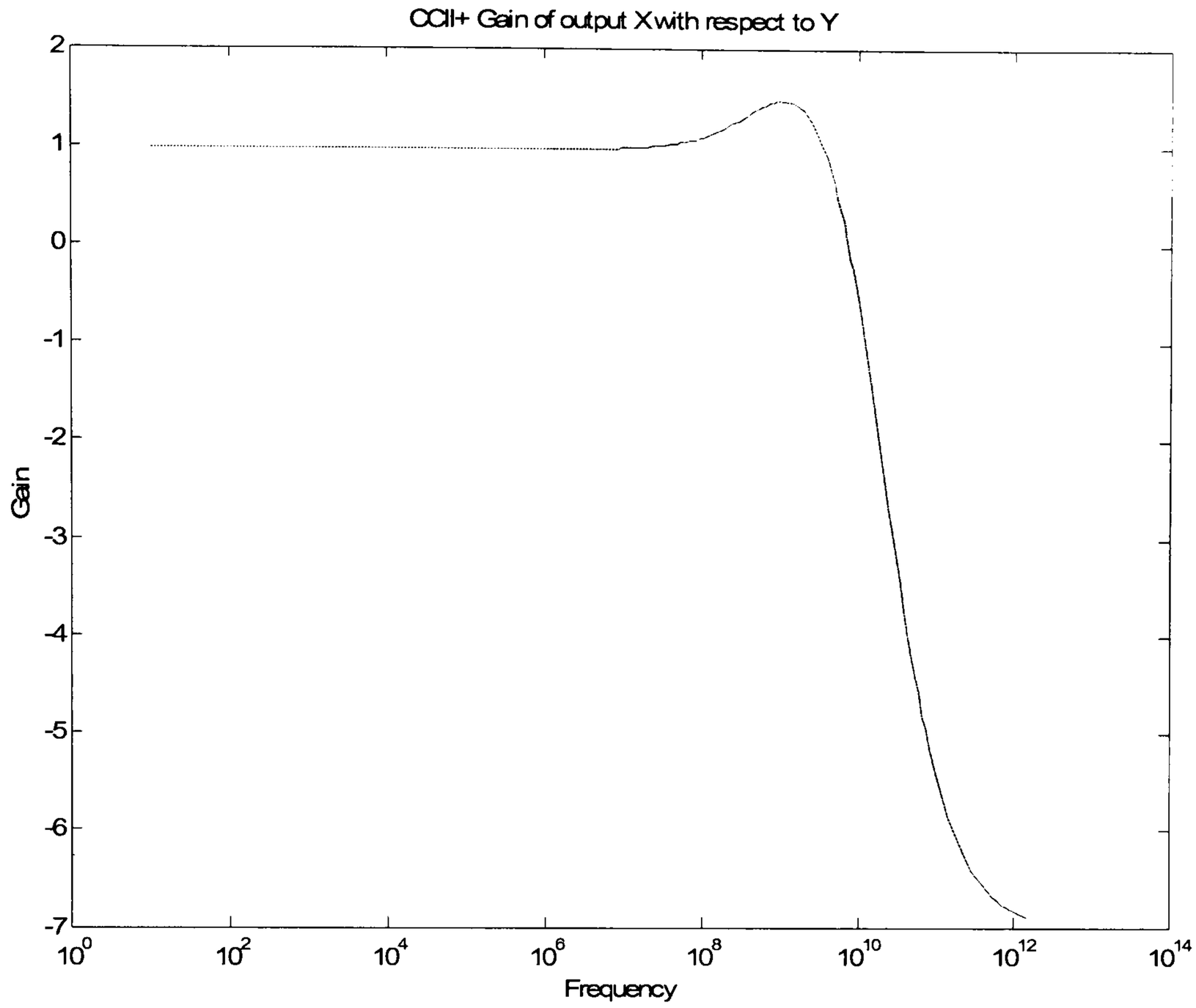

Figure 4-21: Gain of X with respect to Y for the proposed CCII+ using a cascode current mirror.

The gain test1 summary of results:

Gain from Y to X =1; (peaking at a gain of 1.3 at 1.047GHz). The output gain error seen is now negligible but it can be seen that the bandwidth has reduced from that of 4.365GHz. This is due to the extra capacitance seen on node X due to the extra transistors needed for the cascode current mirrors.

Equivalent Thevenin (r_{out}) of node X is now negligible.

Figure 4-22 shows the gain response of Z with respect to Y with the ideal gain equal to unity as $R1 = 1K\Omega$ and $R2 = 1K\Omega$:

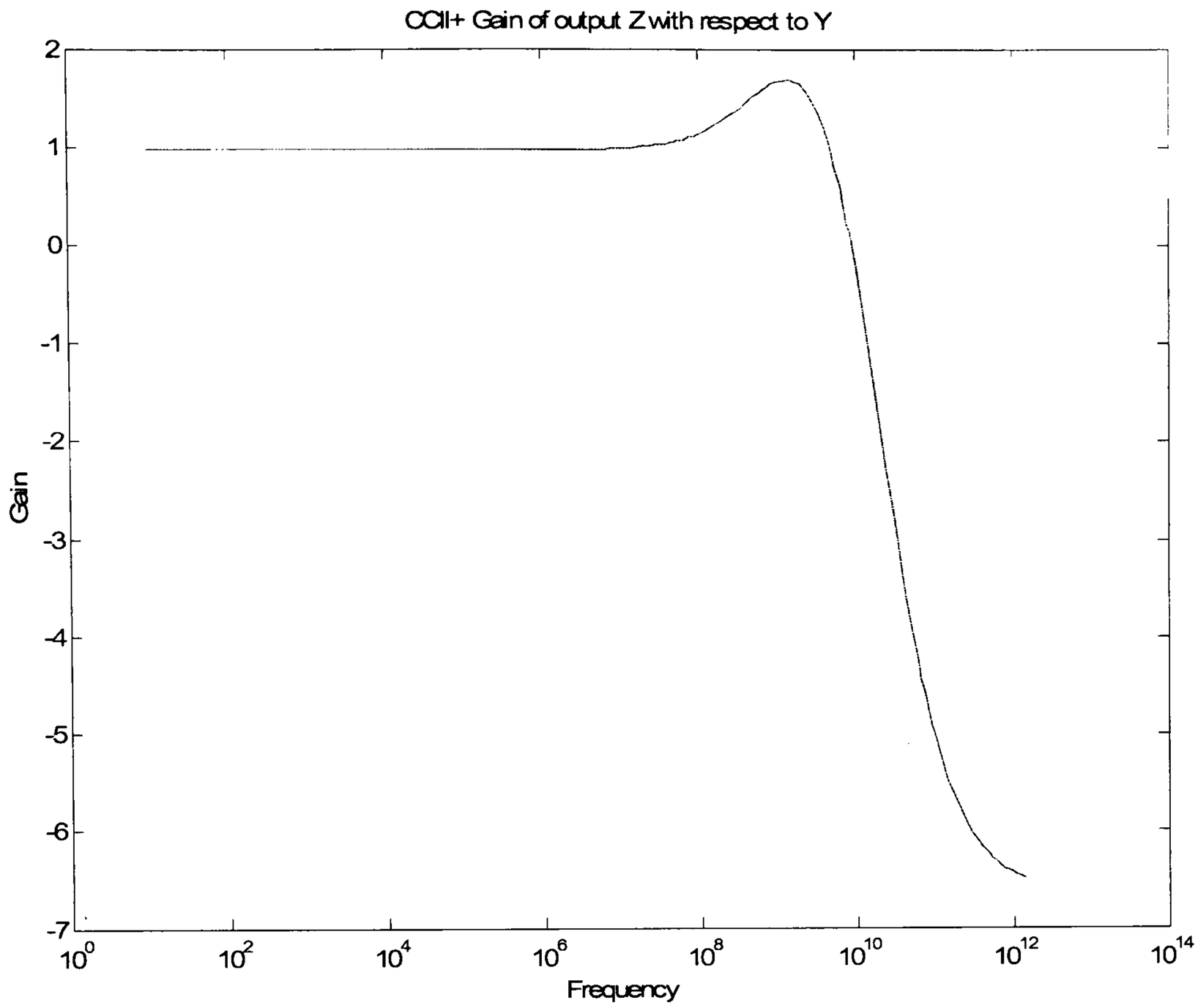

Figure 4-22: Gain of Z with respect to Y for the proposed CCII+ using a cascode current mirror.

The gain test1 summary of results:
Gain from Y to Z =0.993; (peaking at a gain of 1.6 at 1.047GHz). The gain error between node Y and Z is now 0.7%, compared to and error of 2.8% using the CCII+ using a simple current mirror a marked improvement.

Equivalent Thevenin (r_{out}) of node $Z = 141K\Omega$. This compares to an impedance of $34.7K\Omega$ from the new simple current mirror current conveyor.

Results from gain test2

Figure 4-23 below shows the gain of X with respect to Y for the current conveyor (CCII+) this again should be as close to unity as possible:

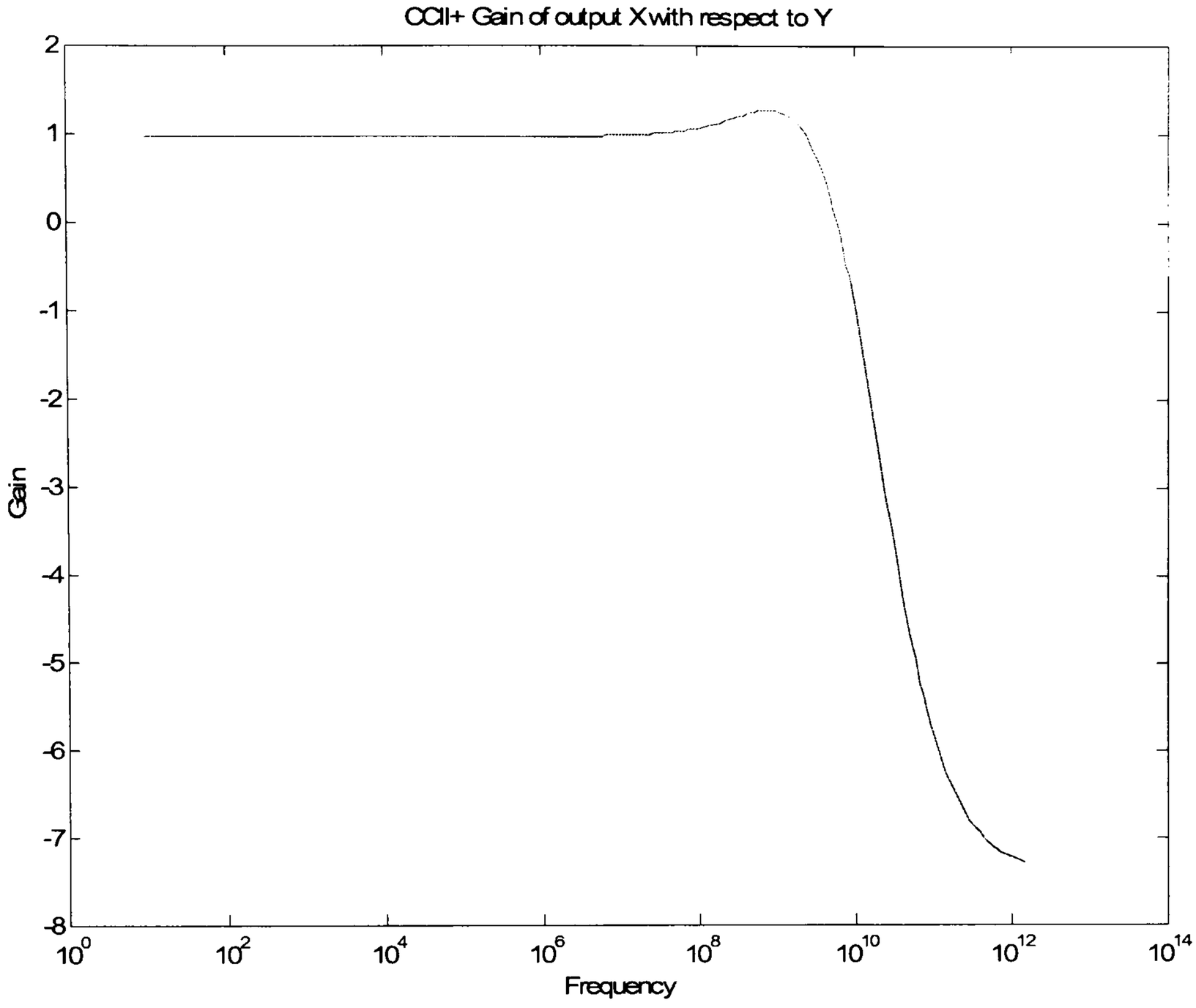

Figure 4-23: Gain of X with respect to Y for the proposed CCII+ using a cascode current mirror.

The gain test2 summary of results:
Gain from Y to X =0.992; (peaking at a gain of 1.2 at 1.07GHz). The gain error between node Y and Z is now 0.8%, compared to and error of 2.8% using the CCII+ using a simple current mirror a marked improvement.

Equivalent Thevenin (r_{out}) of node X = $8\,\Omega$. This compares to an impedance of $28\,\Omega$ from the new simple current mirror current conveyor.

Figure 4-24 shows the gain response of Z with respect to Y with the gain equal to R2/R1, where R1 = 1KΩ and R2 = 2KΩ, the gain should equal 2:

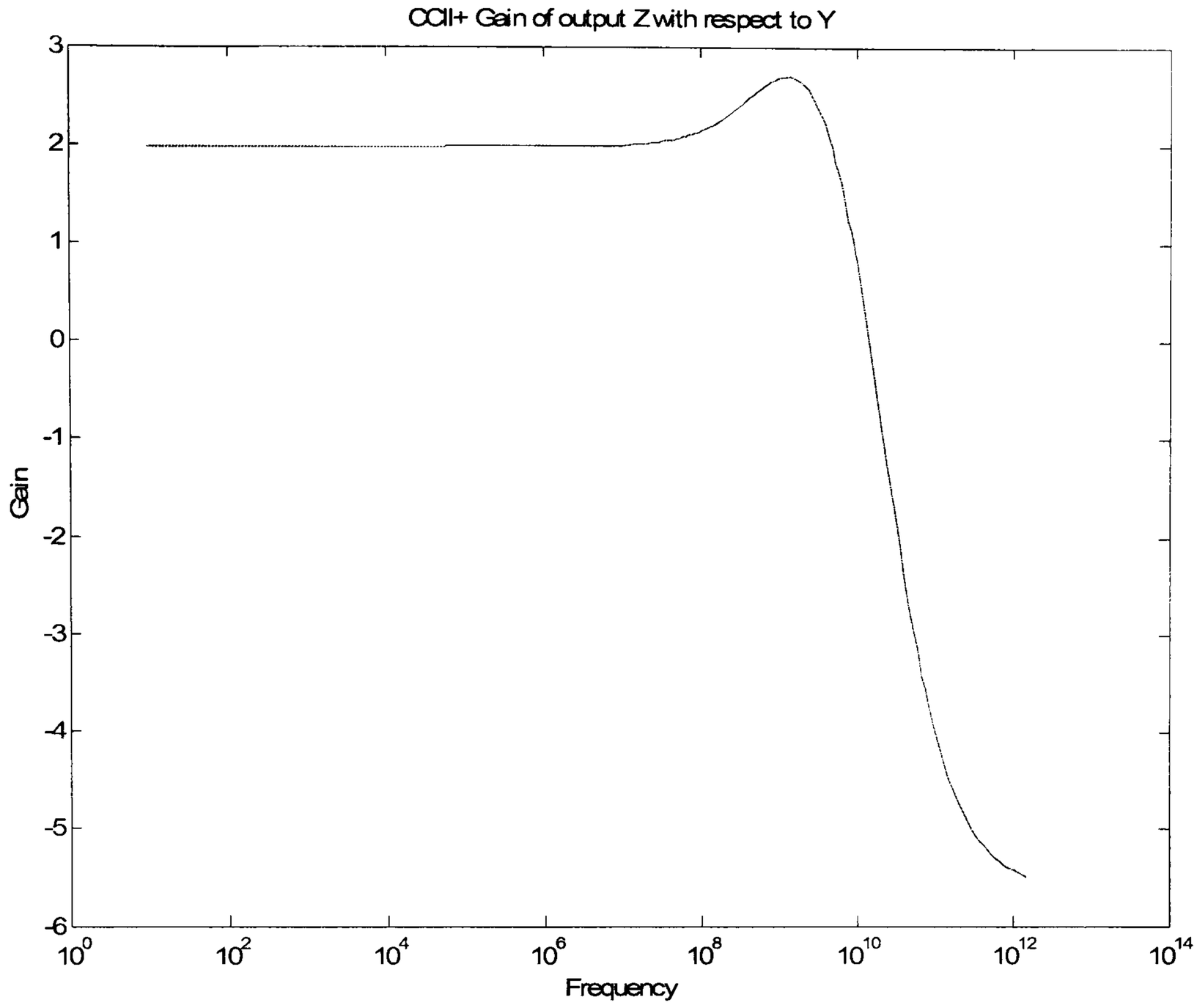

Figure 4-24: Gain of Z with respect to Y for the proposed CCII+ using a cascode current mirror.

The gain test2 summary of results:
Gain from Y to Z = 1.985; (peaking at a gain of 2.4 at 741MHz). Giving a voltage gain error of 0.75% compared to that of 14.6% using a simple current mirror current conveyor in the previous section.

Equivalent Thevenin (r_{out}) of node Z = 132KΩ. This compares to an impedance of 11.7KΩ from the new simple current mirror current conveyor.

Results from Power Supply Rejection Ratio (PSRR) test

Figure 4-25 below shows the PSRR for the current conveyor (CCII+) the definition of PSRR is 20log(Vout(AC)/Vsup(AC)) **[4-14]**, and this aim is to keep this figure as low as possible, the power supply rejection was measured on node 'Z' of the CCII+:

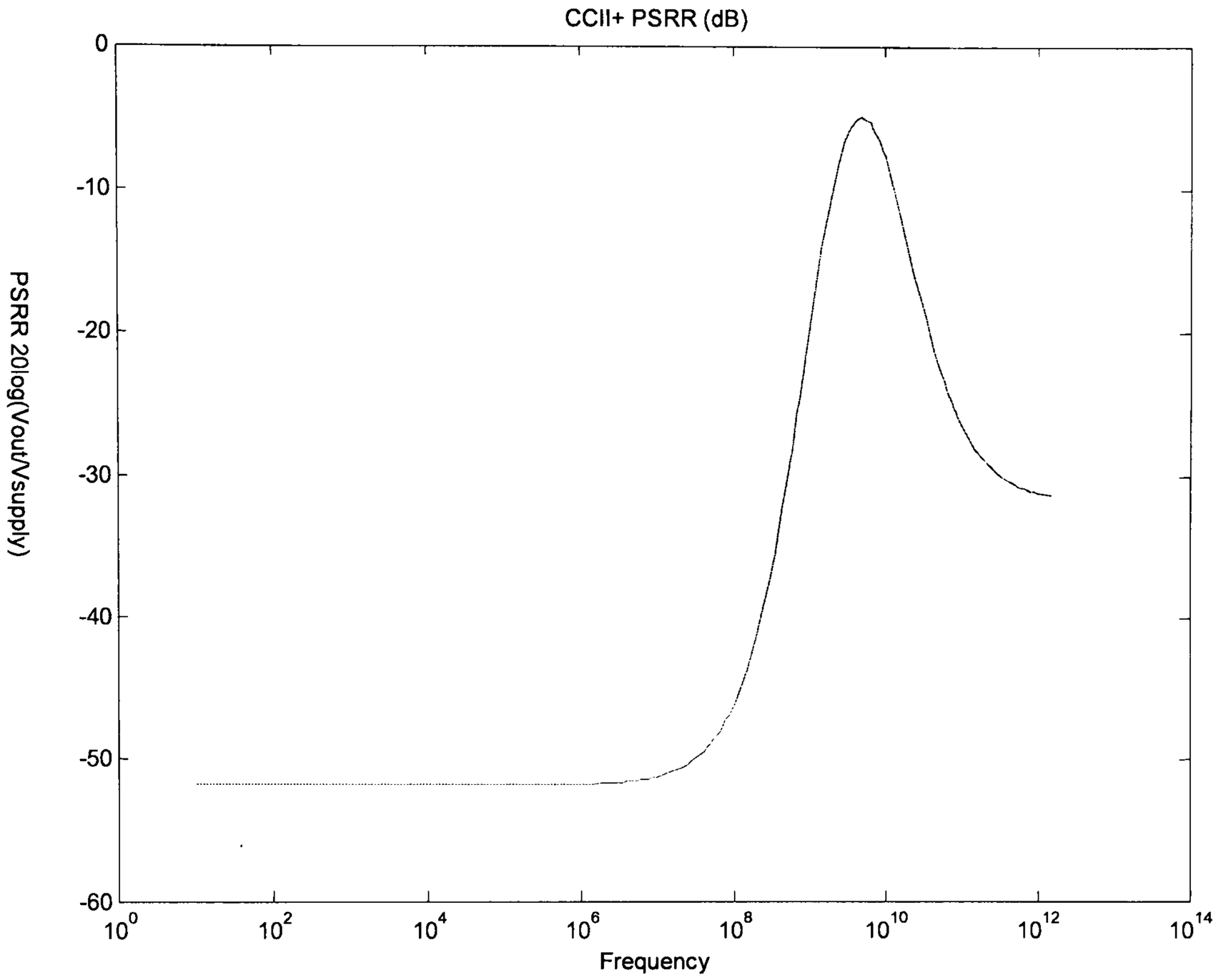

Figure 4-25: PSRR for the CMOS implementation of the proposed cascode CCII+.

The PSRR test summary of results:

PSRR = -51.8dB; rising eventually to -6.9dB at 1.2GHz.

Again the collapse of PSRR above 1.2GHz is due to the device capacitance linking the power supply directly into the signal path. This is seen on virtually all circuits at varying frequencies and is unavoidable but is seldom a practical problem. The PSRR has improved by around 10dB from that of the simple current mirror as the cascode offers a higher output impedance than that of the mirror, which means that any voltage change in the power supply will in turn produce a fraction of current change seen at the output of the current mirror (follower), compared with that of the simple current mirror.

4.4.2.3 Summary of the analysis of the CCII of Figure 4-19.

From the results shown it can be seen that there is a marked improvement over the design shown in Section 4.4.1.1 the simple current mirror version of the proposed current conveyor, in the outputs of X and Z with respect to Y. The unity gain required between Y and X is very close to unity for the two gain tests and the output of Z worst case is 99% of its required value. This is due to the improved output impedance shown at node X and Y due to the cascoding of the current follower as explained in Chapter Two. So as resistors R1 and R2 combine with the parallel impedances seen at node X and Y respectively, the approximate impedance seen at node X and Y are close to the values of R1 and R2.

The Power Supply Rejection Ratio (PSRR) is also improved by a factor 10dB compared with the previous section going to -51dB, this is due to the improvement in output impedance compared with that of the simple current mirror this type of mirror (as shown in Chapter Two). Also this makes the circuit less prone to changes in power supply due to the current sink biasing of the long tailed pair stage. In addition the improvement in the figure over the simple current mirror current conveyor is due to the increased equivalent impedance, seen between the power supply and node X and Y offered by the cascode current mirror architecture.

4.4.3 A regulated cascode current mirror CCII +.

4.4.3.1 Design.

Applying Chapters Two and Three Figure 4-26 below shows the new current conveyor using a regulated cascode current mirror described in Section 2.4.5 (Chapter Two):

:

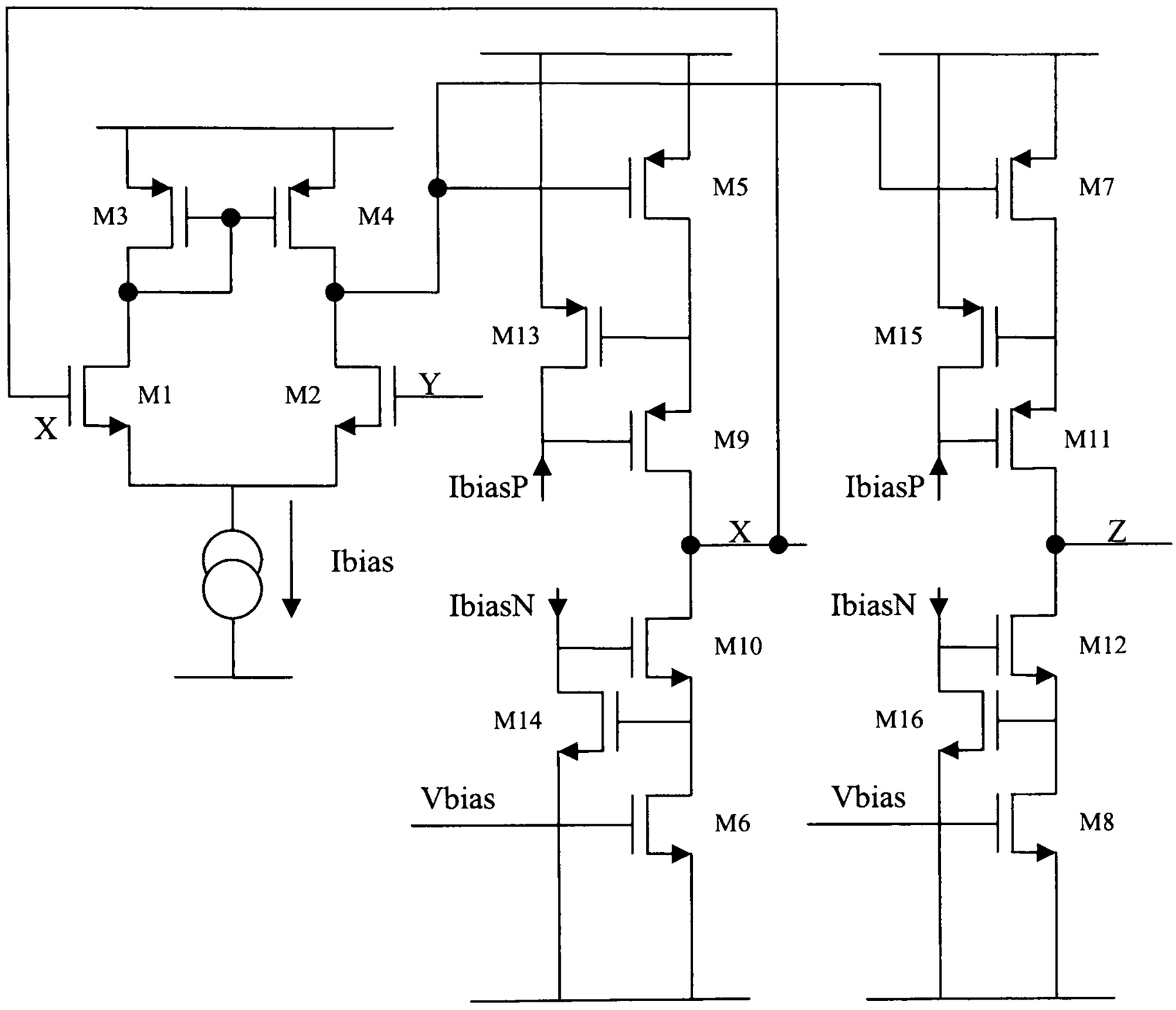

Figure 4-26: The proposed current conveyor (CCII+) using a regulated cascode current mirror.

Referring to Figure 4-12, Figure 4-19 shows the current conveyor (CCII+) which works in the same way as Figure 4-12, except transistors M9 to M16 have been added. These are the regulated cascode transistors shown in Section 2.4.5, and are biased by fixed currents IbiasN and IbiasP, these transistors are used to improve the impedance specifically on node Z. Again it is important for current gain of the current follower to be equal to unity, that transistors M5 matches with M7, M6 matches with M8, M10 matches with M12, M9 matches with M11, M13 matches with M15 and M14 matches with M16.

4.4.3.2 Simulation Results.

Using Figure 4-26 the following test circuit was drawn up as shown in Figure 4-27 below:

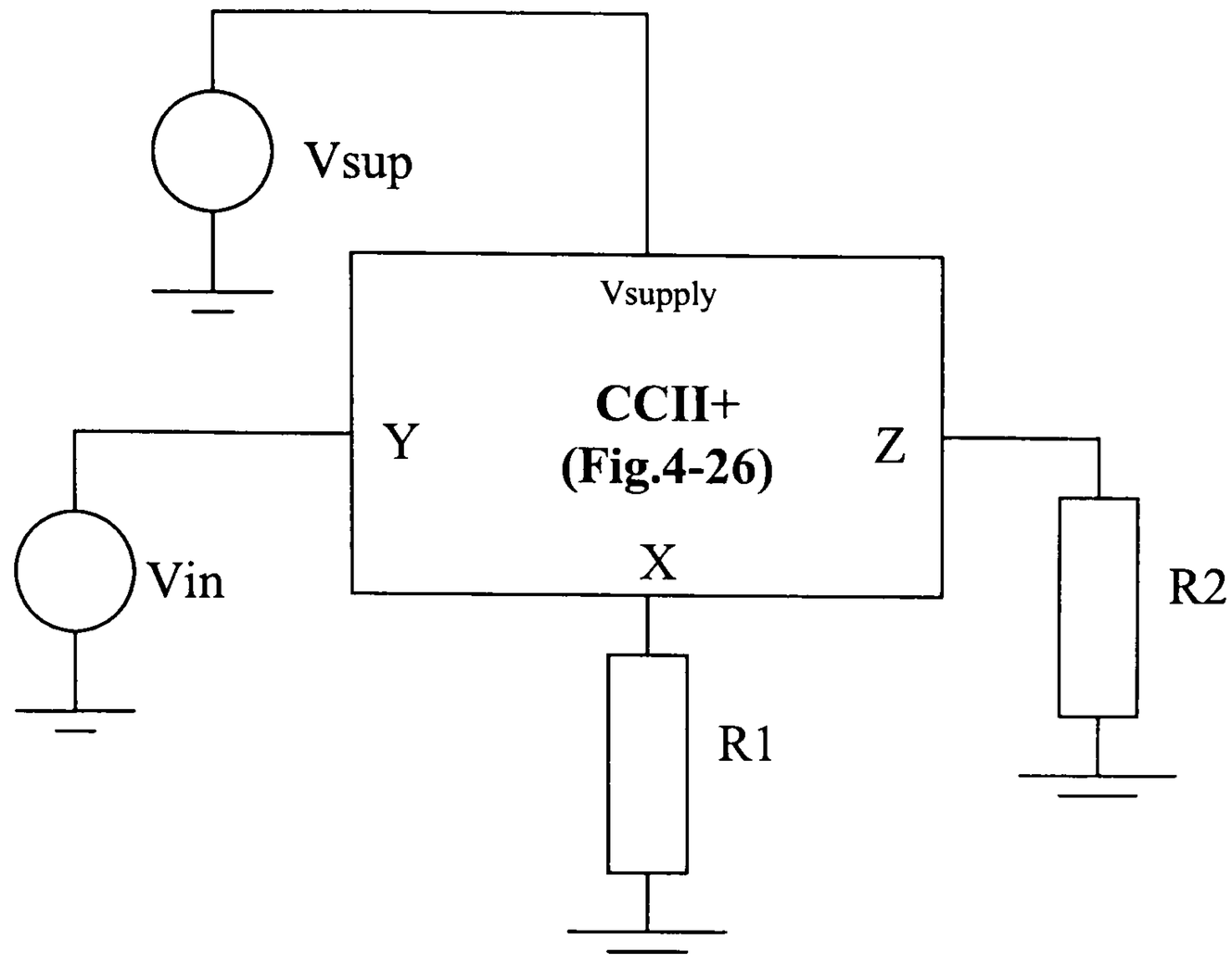

Figure 4-27: The test bench for the proposed CCII+ using a regulated cascode current mirror.

Figure 4-27 was tested using Eldo spice and the transistor models came from the TSMC 0.18μm design kit **[4-11]**:

The following parameters were used:

Resistors: $R1 = R2 = 1K\Omega$.

CMOS transistor dimensions:

NMOS: Width = 20μm; Length = 0.4μm;

PMOS: Width = 40μm; Length = 0.4μm;

Stimulus for Figure 4-27 (The test bench):

Vbias = 0.45V (DC); Ibias = 50μA (DC);

IbiasN = 50μA (DC); IbiasP = 50μA (DC);

Vsup = 1.8V (DC); Vsup = 0V (AC); (For gain tests)

Vsup = 1.8V (DC); Vsup = 50mV (AC); (For PSRR test)

Vin = 0.9V (DC); Vin = 50mV (AC); (For gain tests)

Vin = 0.9V (DC); Vin= 0V (AC); (For PSRR test)

For gain test1:

R1 = 1KΩ; R2 = 1KΩ

For gain test2:

R1 = 1KΩ; R2 = 2KΩ

For Power Supply Rejection (PSRR) test:

R1 = 1KΩ; R2 = 1KΩ

The test results looked specifically at the gain and the Power Supply Rejection Ratio (PSRR), which are the two main factors when considering the overall design of the CCII+.

Results from gain test1

Figure 4-28 below shows the gain of X with respect to Y for the current conveyor (CCII+) this should be as close to unity as possible:

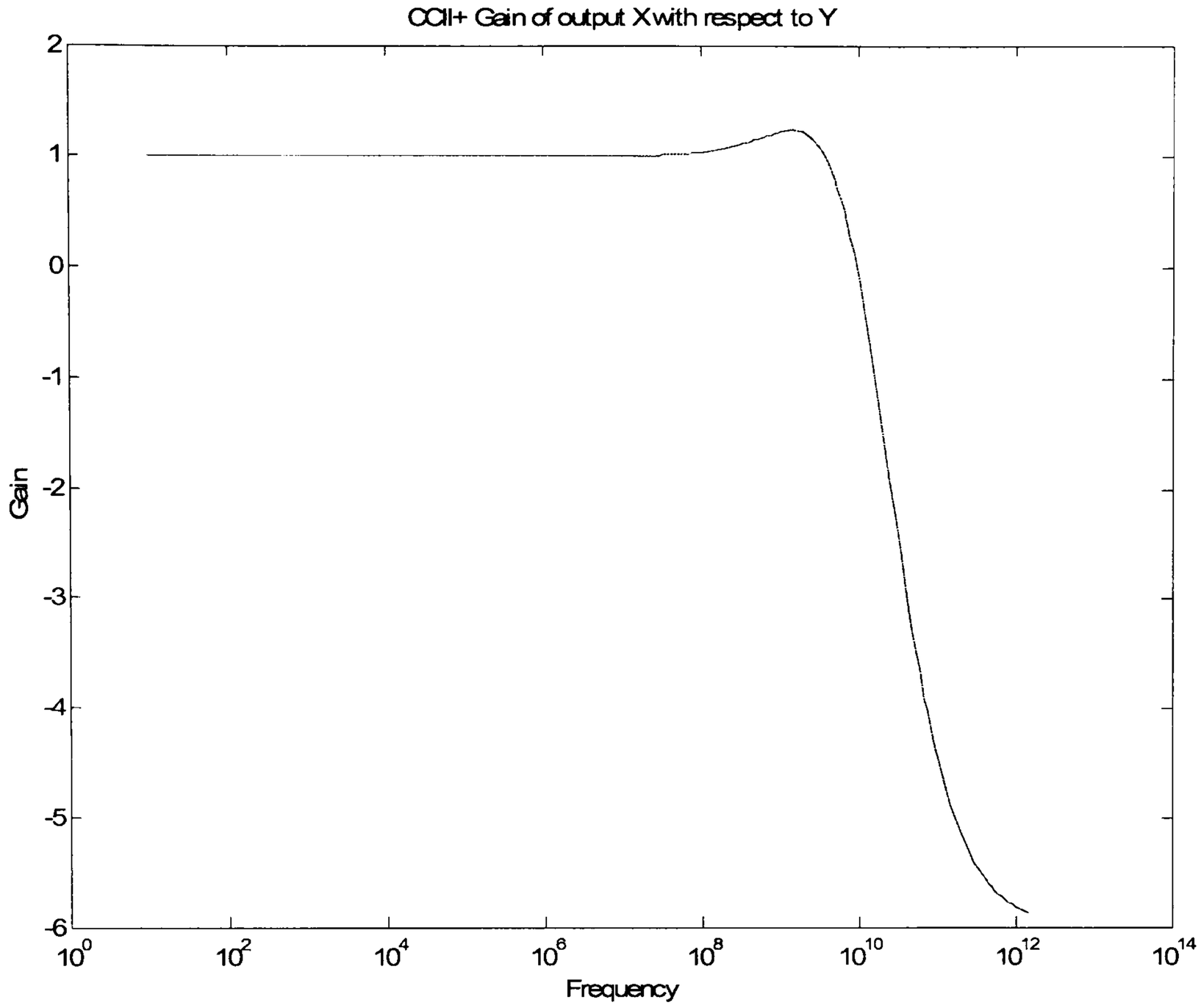

Figure 4-28: Gain of X with respect to Y for the proposed CCII+ using a regulated cascode current mirror.

The gain test1 summary of results:

Gain from Y to X =1; (peaking at a gain of 1.19 at 745MHz). The output gain error seen is now negligible but it can be seen that the bandwidth has reduced from that of 1.047GHz, this is due to the extra capacitance seen on node X due to the extra transistors needed for the regulated cascode current mirrors.

Equivalent Thevenin (r_{out}) of node X is again is negligible.

Figure 4-29 shows the gain of Z with respect to Y with the gain equal to R2/R1, where R1 = 1KΩ and R2 = 1KΩ, the gain should equal unity:

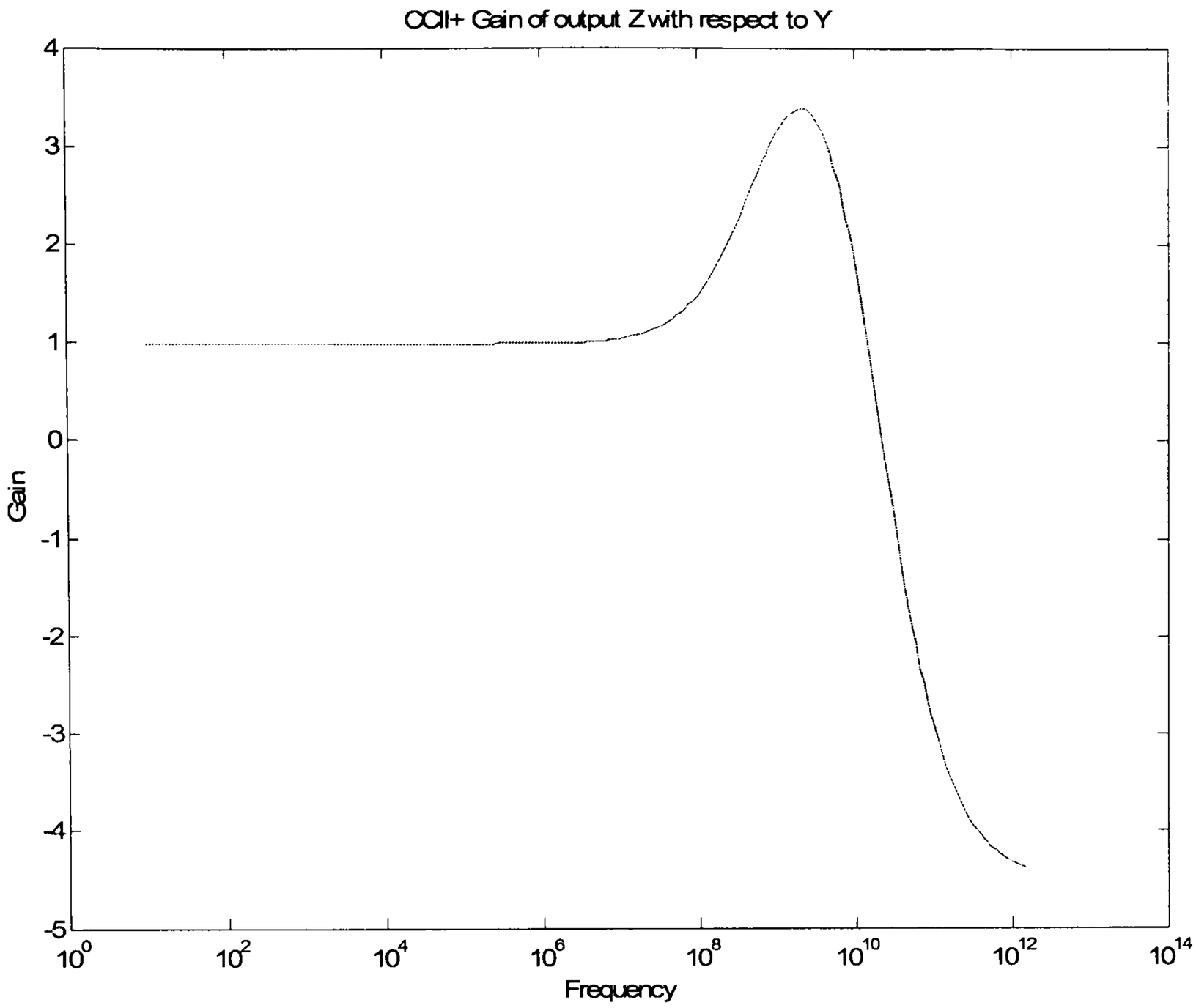

Figure 4-29: Gain of Z with respect to Y for the proposed CCII+ using a regulated cascode current mirror.

The gain test1 summary of results:
Gain from Y to Z =0.992; (peaking at a gain of 3.3 at 724MHz). The gain error between node Y and Z is now 0.8%, compared to and error of 0.7% using the CCII+ using a cascode current mirror this is around the same value.

Equivalent Thevenin (r_{out}) of node Z = 124KΩ. This compares to an impedance of 141KΩ from the new cascode current mirror current conveyor.

Results from gain test2

Figure 4-30 below shows the gain of X with respect to Y for the current conveyor (CCII+) this again should be as close to unity as possible:

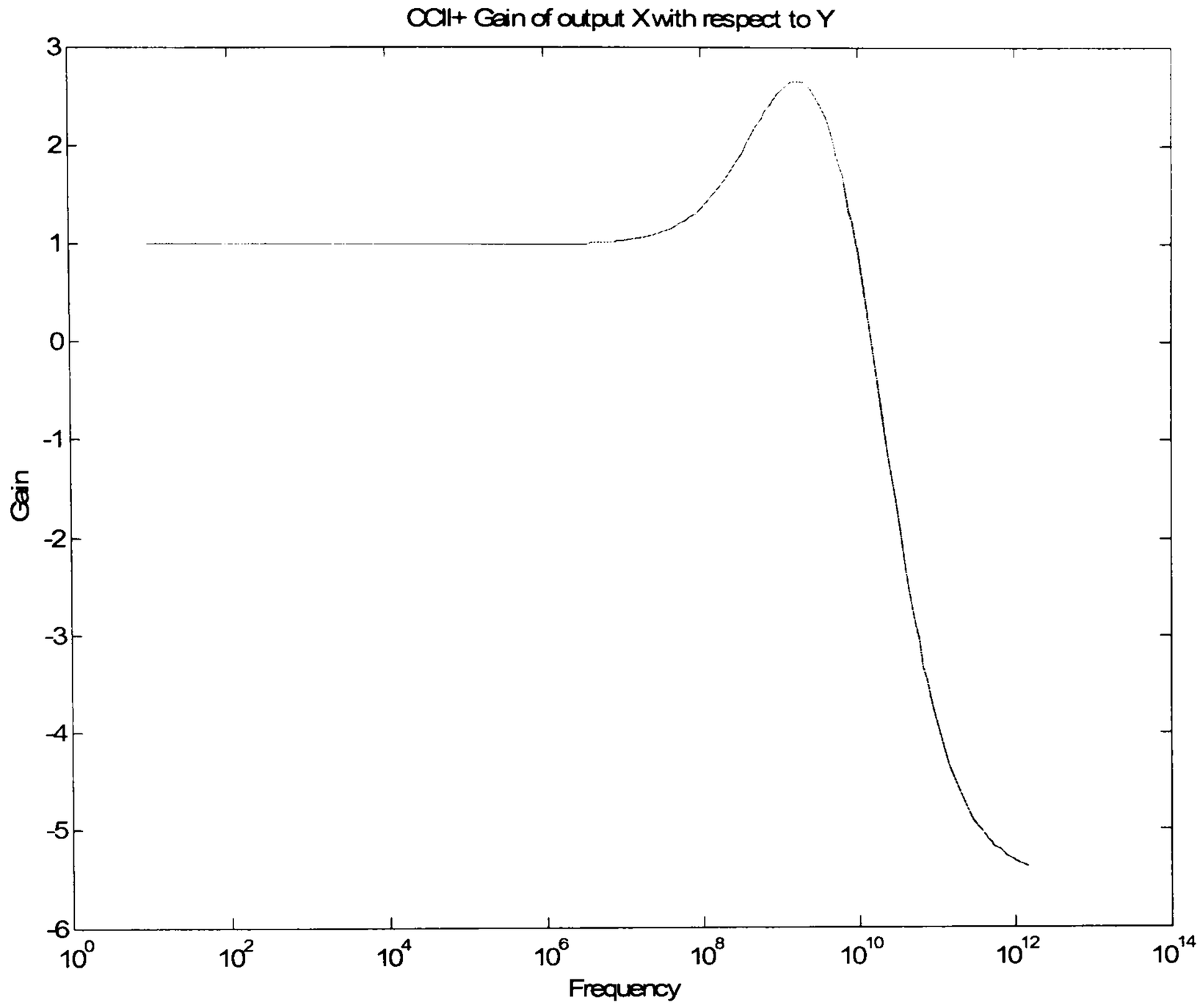

Figure 4-30: Gain of X with respect to Y for the proposed CCII+ using a regulated cascode current mirror.

The gain test2 summary of results:
Gain from Y to X =0.993; (peaking at a gain 2.4 of at 741MHz). The gain error between node Y and Z is now 0.7%, compared to and error of 0.8% using the CCII+ using a cascode current mirror the difference is negligable.

Equivalent Thevenin (r_{out}) of node X = $7\,\Omega$. This compares to an impedance of $8\,\Omega$ from the new cascode current mirror current conveyor.

Figure 4-31 shows the gain response of Z with respect to Y with the gain equal to R2/R1, where R1 = 1KΩ and R2 = 2KΩ, the gain should equal 2:

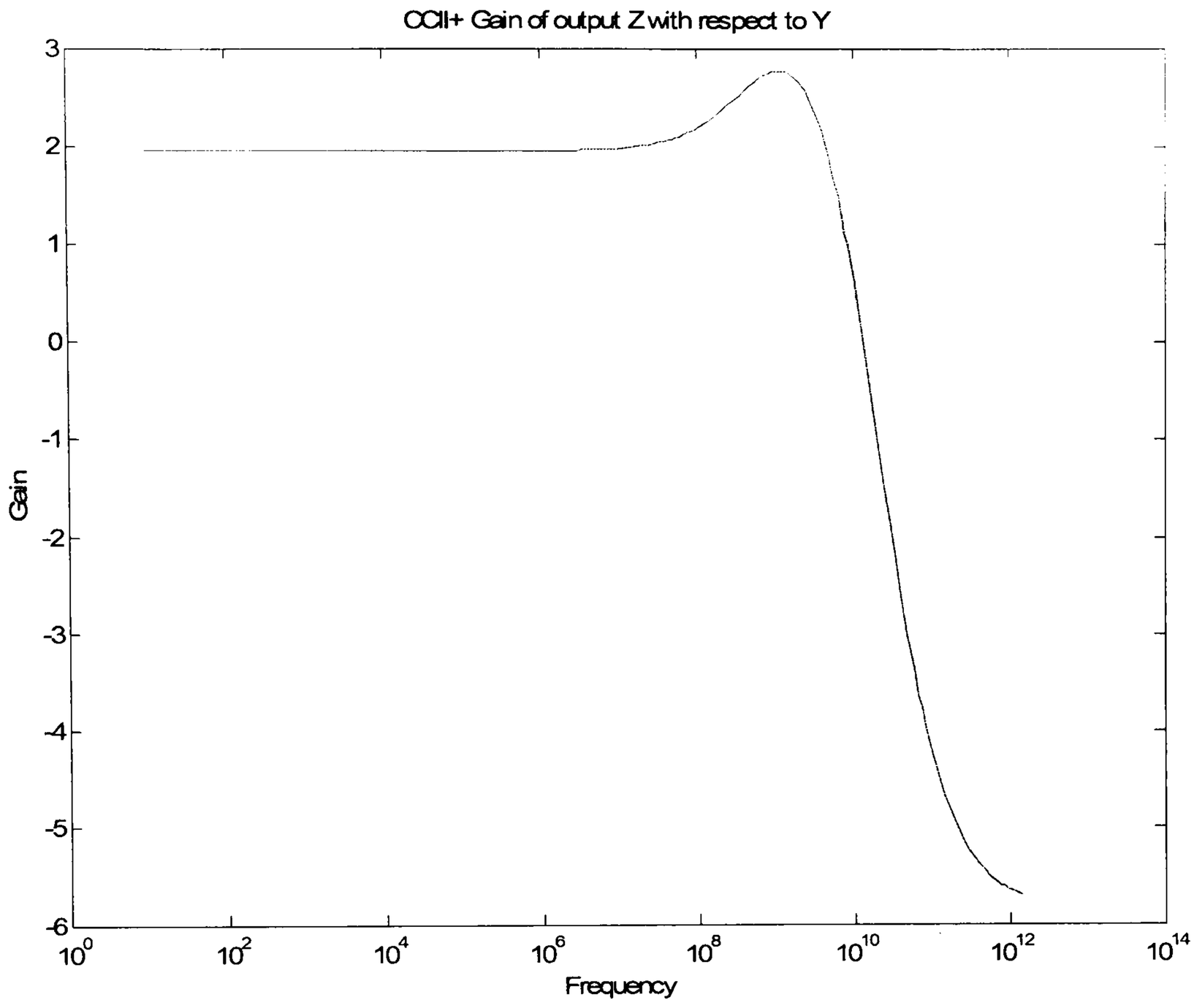

Figure 4-31: Gain of Z with respect to Y for the proposed CCII+ using a regulated cascode current mirror.

The gain test2 summary of results:
Gain from Y to Z = 1.957; (peaking at a gain of 2.7 at 707MHz). Giving a voltage gain error of 1.25% compared to that of 0.75% using a cascode current mirror current conveyor in the previous section.

Equivalent Thevenin (r_{out}) of node Z = 45KΩ. This compares to an impedance of 132KΩ from the new cascode current mirror current conveyor.

Results from Power Supply Rejection Ratio (PSRR) test

Figure 4-32 below shows the PSRR for the current conveyor (CCII+) the definition of PSRR is 20log(Vout(AC)/Vsup(AC)) **[4-14]**, and this aim is to keep this figure as low as possible, the power supply rejection was measured on node 'Z' of the CCII+.

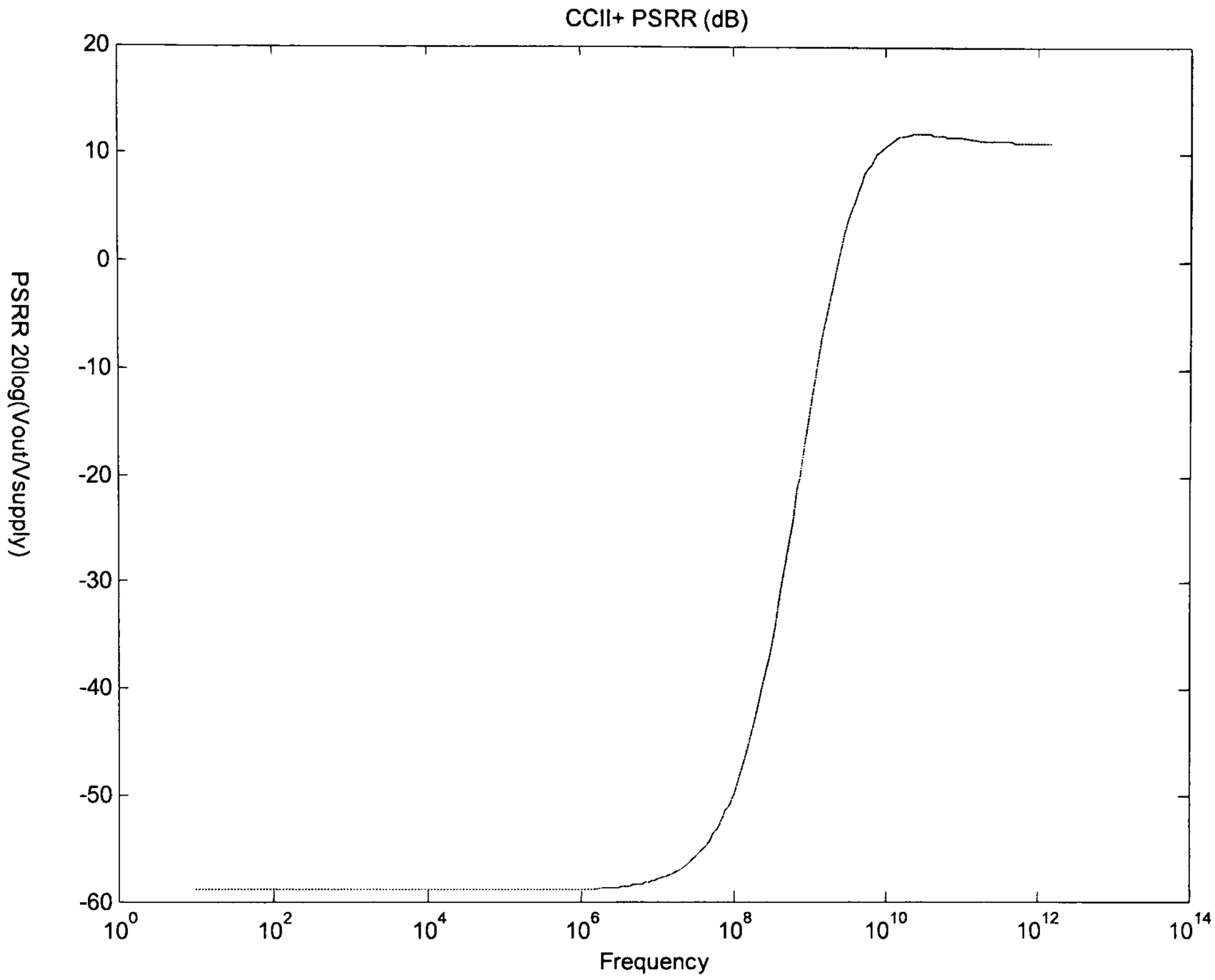

Figure 4-32: PSRR for the CMOS implementation of the proposed regulated cascode CCII+.

The PSRR test summary of results:

PSRR = 58.97dB; rising eventually to 5.6dB at 767MHz.

Again the collapse of PSRR above 767MHz is due to the device capacitance linking the power supply directly into the signal path. This is seen on virtually all circuits at varying frequencies and is unavoidable but is seldom a practical problem. The PSRR has improved by around 8dB from that of the cascode current mirror as the regulated cascode offers a higher output impedance than that of the mirror, which again means that any voltage change in the power supply will in turn produce a fraction of current change seen at the output of the current mirror (follower), compared with that of the simple current mirror and cascode current mirror.

4.4.3.3 Summary of the analysis of the CCII of Figure 4-26.

This CCII+ architecture improves the Power Supply Rejection Ratio (PSRR) from that of the cascode CCII+ version shown in Section 4.4.2 by a factor of around 8dB to close to 60dB, the overall improvement on the gain is small though gain test2 which has an expected gain of two dropped slightly with this design over the cascode CCII+. This was probably due the slight change in the operating conditions of the transistors being used due to the change in the load on node Z.

It is also worth noting that for both the cascode and regulated cascode versions of the CCII+ power supply head room is a problem due to the fact that the Drain/Source voltage (V_{ds}) of the current mirror must be at least a Vt higher than that of a simple current mirror to remain in the saturation region and this factor must be taken into account when designing the current conveyor using either of these techniques. It would be possible to employ folded cascode techniques, however this was not explored.

4.5 The Proposed CMOS CCII- circuit addition.

4.5.1 Design Concept

This section will describe the extra CMOS devices which can take the new CCII+ described in Section 4.4 and convert that into a CCII-. This section will use the design in Section 4.4.1. (A simple current mirror CCII+) to explain the design process more easily, but any type of new conveyor can use this technique as long as the current mirrors remain symmetrical as previously explained in Section 4.4.

The starting point will be the circuit shown in Figure 4-33 below.

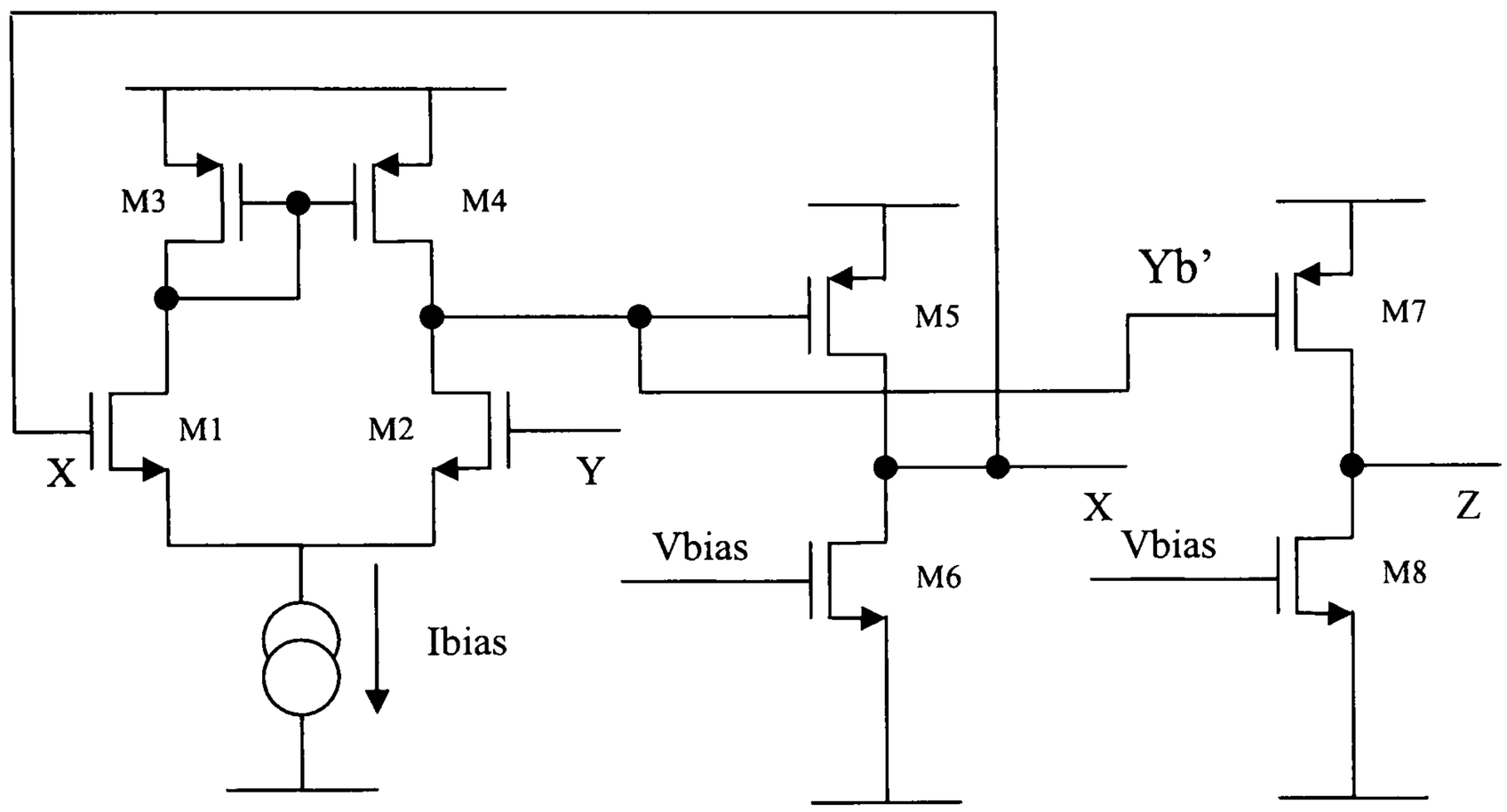

Figure 4-33: The New CCII+ using a simple current mirror.

Then taking the bias point Yb' shown in Figure 4-33, simply add the extra connections as shown below (Figure 4-34):

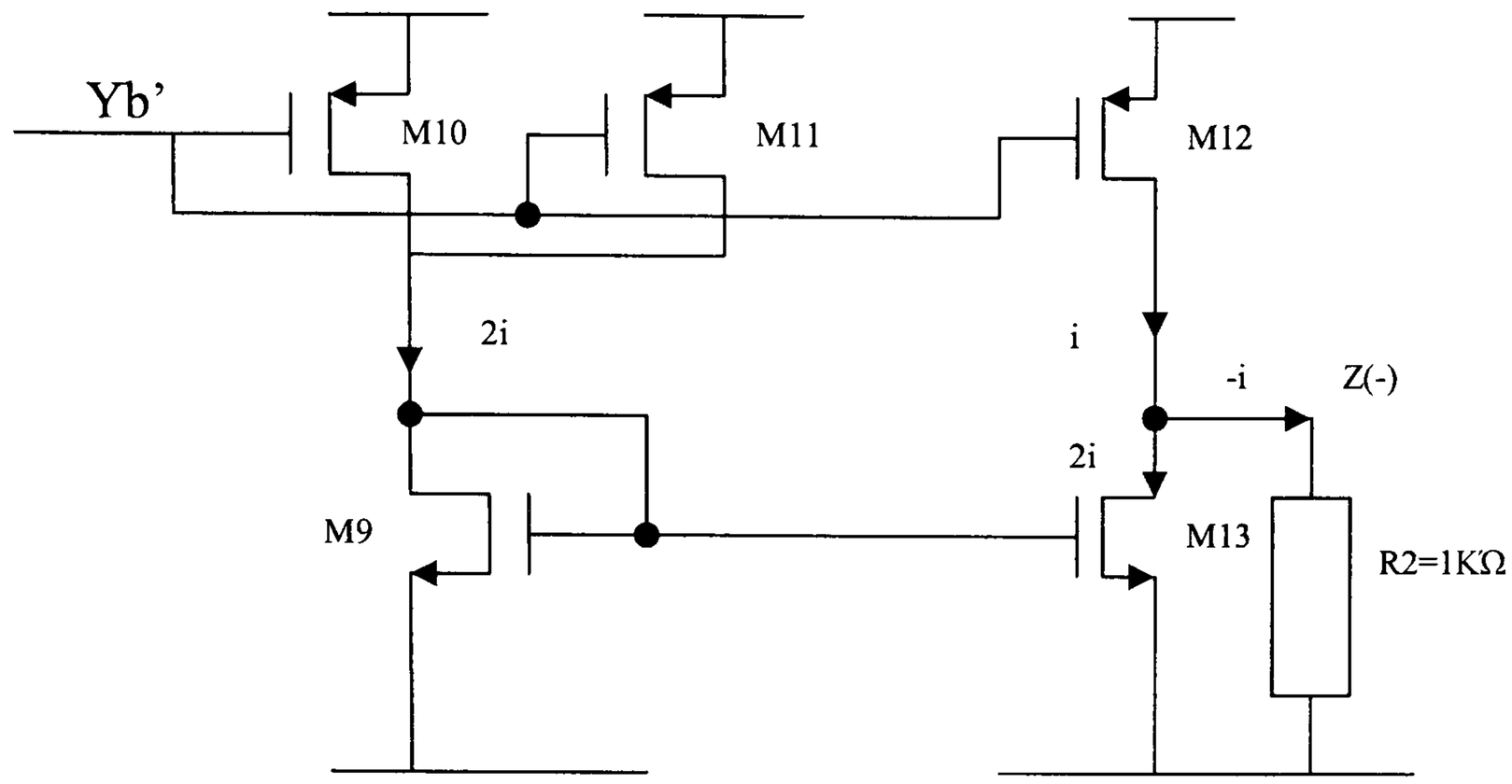

Figure 4-34: New CCII – output addition.

From Figure 4-34 if all transistor dimensions are the same and match those of Figure 4-33, if Yb' the bias point from Figure 4-33 is taken then a current '2i' is generated fro M10 and M11 this is mirrored by M9 to give a current of '2i' through M13. M12 provides a current of 'i' and giving a current of '-i' through Z(+) giving a true CCII- output. The only problem is that the Z(-) know has a '-i' DC term now instead of '+i' term, so a '2i' DC term needs to be added to the output of Z(+) to compensated for the '-i' DC term. Figure 4-35 in the next section shows the addition needed.

4.5.2 Solving the DC Bias Problem

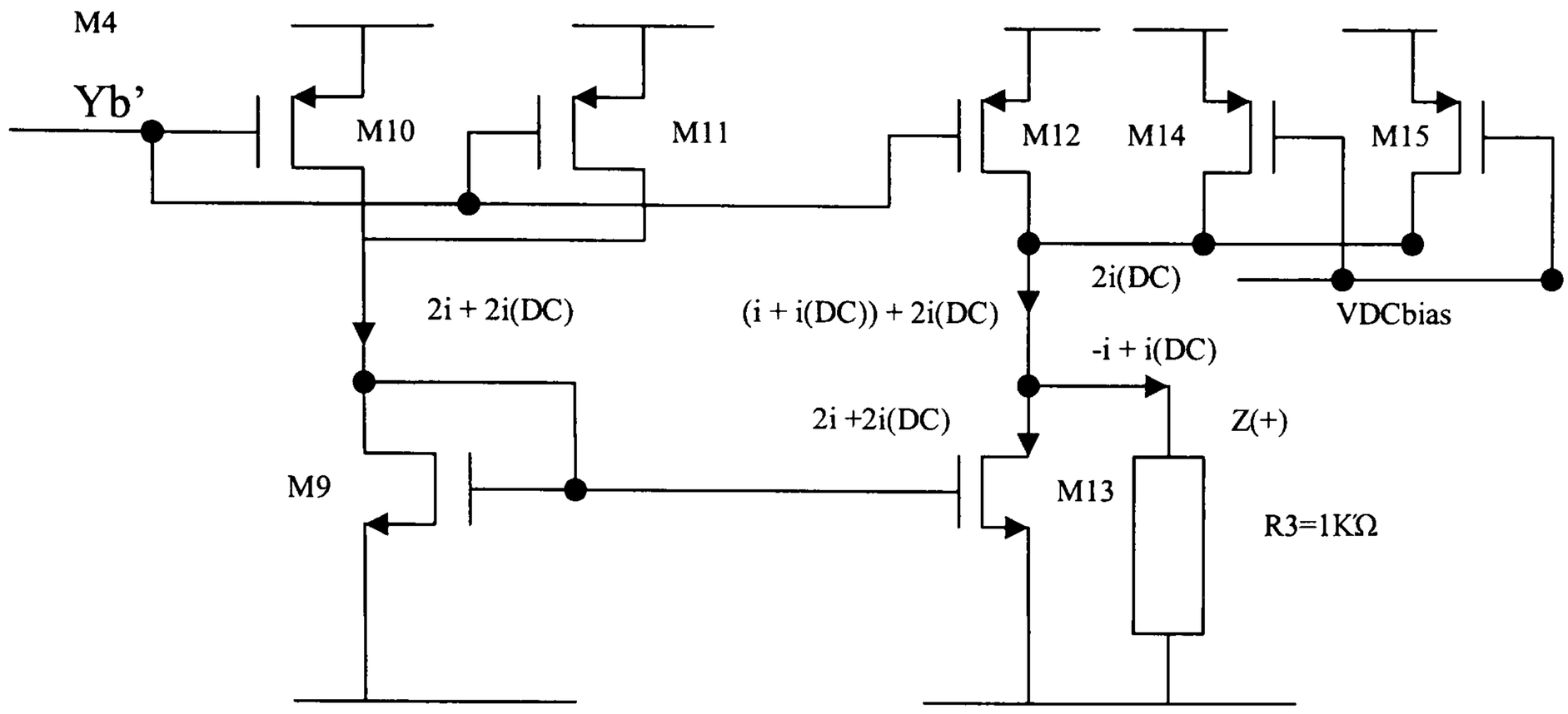

Figure 4-35: New CCII - output with added DC bias

From Figure 4-35 transistors M14 and M15 must provide the appropriate current to compensate for the DC current taken by M13, (note that M14 and M15 must match M12). Making the current through R3 equal to 'i(DC) – i'. But note that R3 and R2 must match any mismatch in their values will mean that their output DC values will be different. Notice there is an extra VDCbias voltage that is needed this is described in subsection 4.5.2.1.

4.5.2.1 The VBias Circuit

To create the necessary and appropriate voltage VDCbias to maintain the DC currents in M14 and M15 then VDCbias (Figure 4-36) must have the same DC value as Node Yb' (Figure 4-34 and Figure 4-35). To do this simply mimic the front end stage and take the DC value of the input signal as the input bias voltage into this stage (VinDC). As shown in Figure 4-36 below.

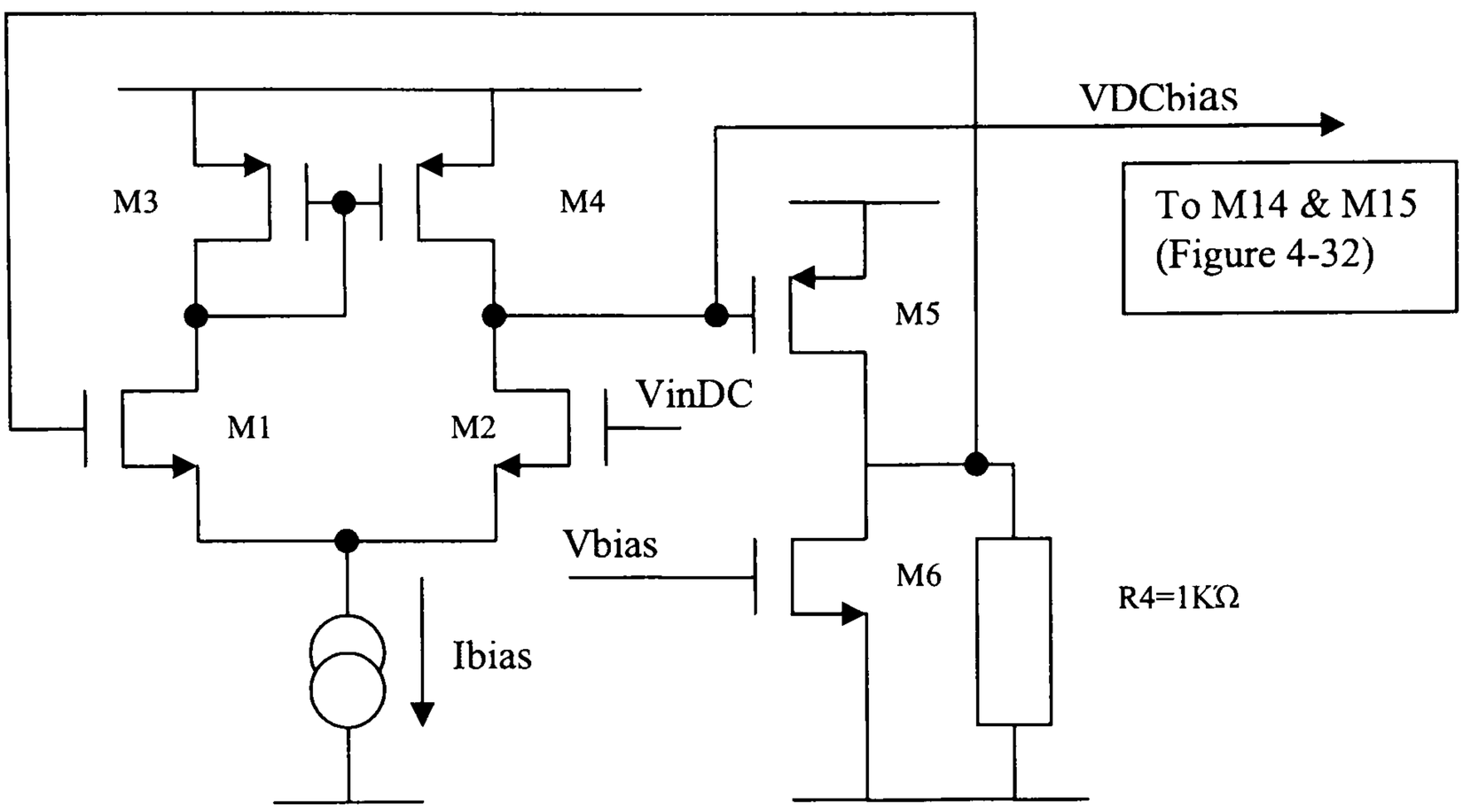

Figure 4-36: Vbias Circuit for the DC compensation circuit (Figure 4-35)

The only problem is another resistor (R4) is needed and this must again match R2 and R3.

4.6 Review of Results.

From section 4.1 it could be seen that the original BJT bench mark CCII architecture would not work well as the gain of the source follower stage (from Y to X). Also it did not perform well due to the inherent low values of transconductance (gm) and Early voltage ($1/\lambda$).

There are two requirements for a good current conveyor **[4-2]** a good voltage follower with a voltage gain close to unity, and a good current follower with a current gain of close to unity, with a CCII+ having an inverse current gain of close to -1. This chapter shows that both of these can be achieved by using the architecture shown in Chapter Three for the voltage follower and using the different current mirror architectures shown in Chapter Two for the current follower part of the CCII.

From the results in this chapter the best architectures are that of the cascode and regulated cascode current mirror current conveyors. Both the gain tests showed gains are close to the required ideal gains, and power supply rejection (PSRR) had a much improved value much better than the original benchmark CCII **[4-2]** tested and these were close to -60dB.

The disadvantages of these circuits are the supply overheads needed to keep the mirrors in saturation and the extra bias circuitry needed to bias the current mirrors correctly, all adding to the transistor count of the circuits.

This chapter also shows how to turn a CCII+ current conveyor into a CCII- this though adds considerable amounts of transistors to the design, but allows the designer the flexibility of designing an accurate equivalent CMOS transistor device if needed.

One of the application areas for the CCII is within a current feedback operational amplifier. In Chapter Five the different current conveyors described in this chapter are used to build current feedback operational amplifiers, and their relative performances evaluated.

4.7 References

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[4-13] P.Allen, D.R.Holdberg, 1st Edition, 'CMOS Analog Circuit Design', Oxford University Press 1987, pp. 74-77.

[4-14] K.Laker, W.Sansen, 'Design of Analog Integrated Circuits and Systems', McGraw Hill International Editions, First Edition, 1994, pp. 562-575.

[4-15] K.Laker, W.Sansen, 'Design of Analog Integrated Circuits and Systems', McGraw Hill International Editions, First Edition, 1994, pp 172-219.

CHAPTER 5

CMOS Current Feedback Op-Amp based on the new CMOS CCII+

5.1 Introduction

There are many applications for the current conveyor such as active filter design, gain stages etc. **[5-1],[5-2],** and the current conveyor can be useful when designing filters for mobile communications due to there inherent wide bandwidths and smaller component count compared with typical filter active filter designs using operation amplifiers **[5-3],[5-4]**. These applications are well documented so this chapter will not deal with them, but what this chapter will concentrate on is applying the current conveyor architectures discussed in Chapter Four, to the CFOA **[5-5],[5-6],[5-7]**. The CFOA offers better slew rates and bandwidths than their voltage feedback counterparts, the conventional operational amplifier. They are also not constrained by the gain-bandwidth product that conventional operational amplifiers are, which means that they can be used where higher bandwidth is required.

This Chapter will deal with two best performing versions of the new CCII+ described in Chapter Four, to build two new types of CFOA:

1) Using a cascode current mirror CCII+.
2) Using a regulated cascode current mirror CCII+.

Each design will be described and the simulation results presented.

5.2 The current feedback operational amplifier

The current feedback operational amplifier has in the past been built using bipolar technology **[5-8],** due to their inherent higher values of transconductance and Early voltage over their CMOS counterparts. Up to now it has been difficult to offer an equivalent CFOA in CMOS.

New versions of CFOAs can now be built using the new current conveyors described in Chapter Four using conventional CMOS technology **[5-9].** This will offer increased performance in areas such as bandwidth and PSRR which other CMOS designs cannot currently deliver.

The CFOA consists of a CCII+ connected to a voltage (source) follower output stage as shown in Figure 5-1 below **[5-8]**:

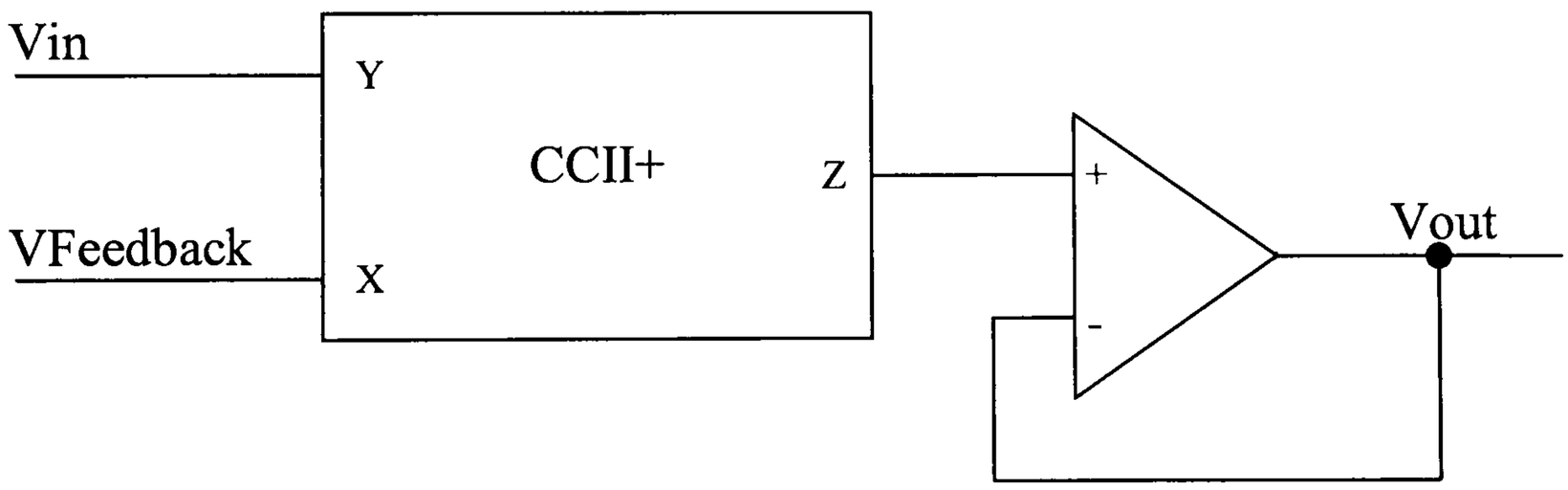

Figure 5-1: A block diagram of the CFOA.

From Figure 5-1, the CFOA uses the high impedance Y node of the CCII+ as the positive input. The low impedance X node is used as the feedback into the amplifier, hence the name current feedback as it is current that is feedback to the inverting input and not voltage as is the case for the conventional operational amplifier **[5-5]**. Node Z of the CCII+ is connected to the input of a source follower amplifier, thereby generating a high open loop voltage gain for the complete amplifier.

Figure 5-2 below shows a CFOA setup as a closed loop non inverting amplifier:

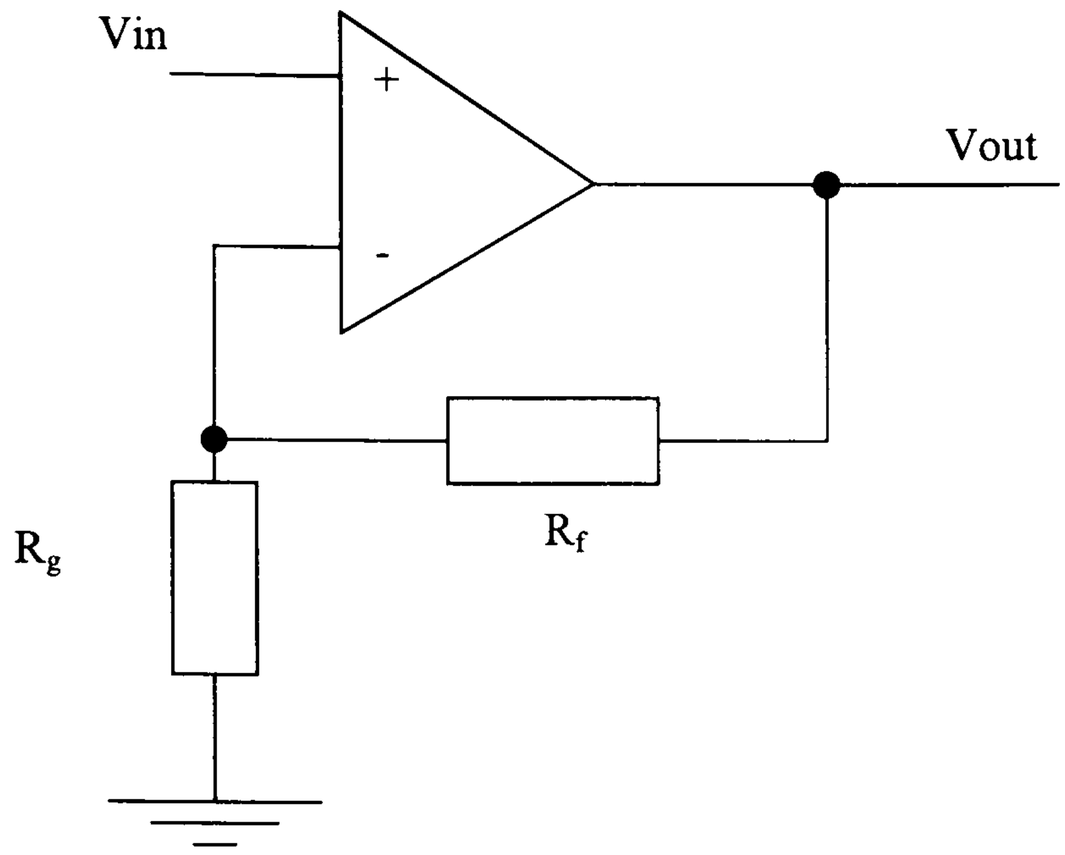

Figure 5-2: A CFOA set up as a closed loop non inverting amplifier.

This non–inverting amplifier has a gain of $(R_f+R_g)/R_g$, but unlike a conventional voltage operational amplifier the CFOA is not limited by a gain-bandwidth product. Actually the CFOA closed loop bandwidth is limited by the combination of the feedback resistor (R_f) and the equivalent capacitance seen between node Z and ground (C_o), as shown in Equation 1 (f_p being the dominant pole of the amplifier) below **[5-5]**. This assumes that the feedback resistor R_f is much larger than the input resistance at node X:

$$f_p = \frac{1}{2\pi C_o R_f} \qquad \textbf{(5.1)}$$

Therefore this amplifier is capable of a much wider bandwidth than a conventional voltage feedback operational amplifier as it is not limited by a gain-bandwidth product. As the bandwidth does not depend on R_g and the bandwidth controlled by R_f.

This chapter will deal with two types of CFOAs based on the current conveyors described in Chapter Four.

5.2.1 Using a cascode current mirror

5.2.1.1 Design.

This amplifier is based on the cascode current mirror conveyor described in Section 4.4.2 and is shown in Figure 5.3 below:

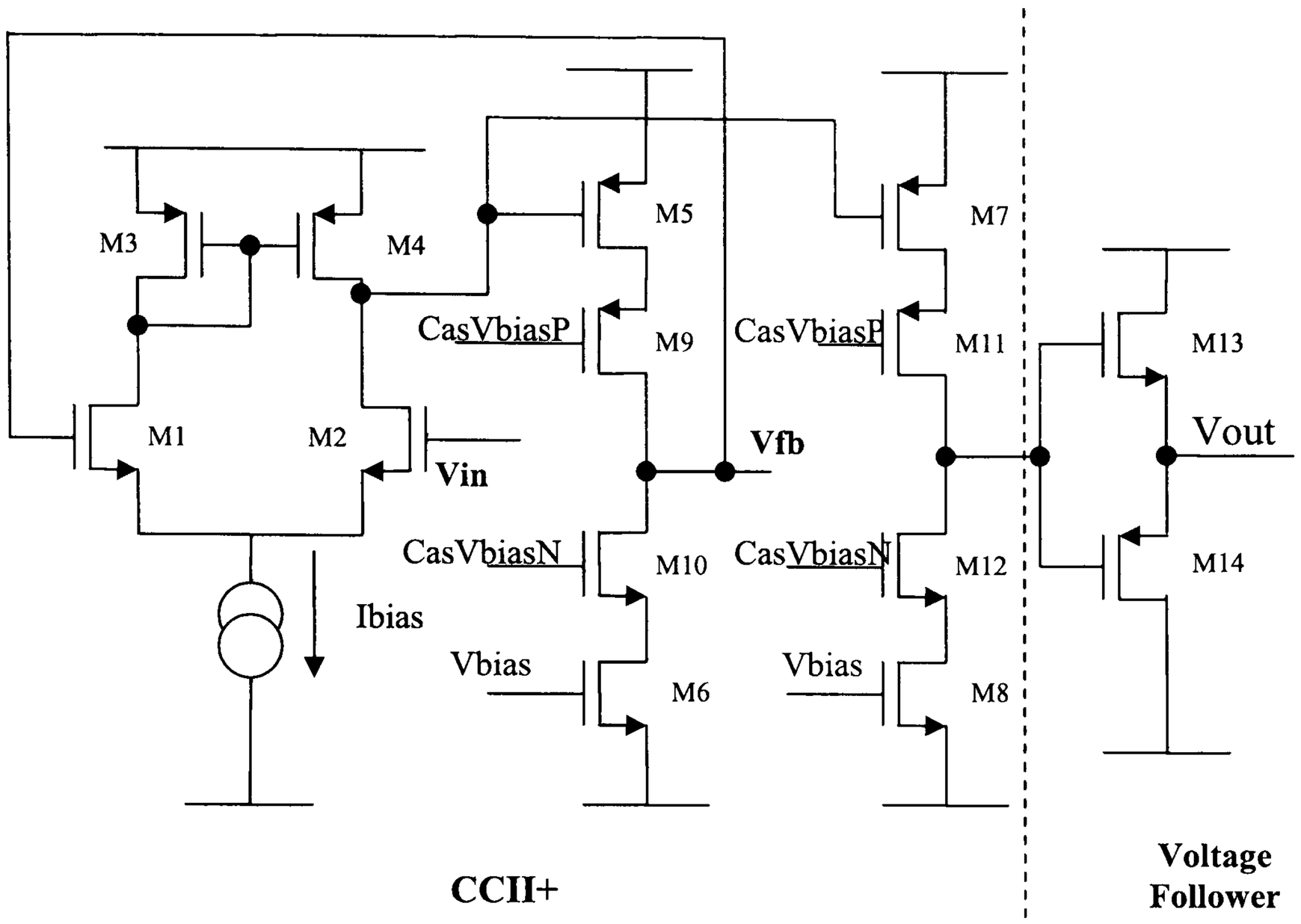

Figure 5-3: A CFOA using a cascode current mirror CCII+.

From Figure 5-3 it can be seen that the transistors M1 to M12 make up the cascode current mirror current conveyor (CCII+), and the source follower is made up of transistor M13 and M14 for the purpose of this simulation, to keep the component count down the minimum and reduce the effect on the overall bandwidth that would be incurred if a more complex source follower was used.

The transistor dimensions used in the design were as follows:

NMOS: Width = 20μm; Length = 0.4 μm;

PMOS: Width = 40 μm; Length = 0.4 μm;

This circuit simulation results are shown in the next section.

5.2.1.2 Simulation.

The Figure 5-4 shows the test bench used to measure the following parameters specified in the tests listed below for the cascode CFOA shown in Figure 5-3. This was tested using TMSC 0.18 μm process models **[5-9]**.

1. AC small signal gain test.
    a. $R_f = 250\,\Omega$; $R_g = 250\,\Omega$.
    b. $R_f = 300\,\Omega$; $R_g = 300\,\Omega$.
    c. $R_f = 500\,\Omega$; $R_g = 500\,\Omega$.
    d. $R_f = 500\,\Omega$; $R_g = 250\,\Omega$.
    e. $R_f = 1K\,\Omega$; $R_g = 500\,\Omega$.
2. AC small signal power supply rejection test.
    a. $R_f = 300\,\Omega$; $R_g = 300\,\Omega$.
3. Transient slew rate test.
    a. $R_f = 300\,\Omega$; $R_g = 300\,\Omega$.

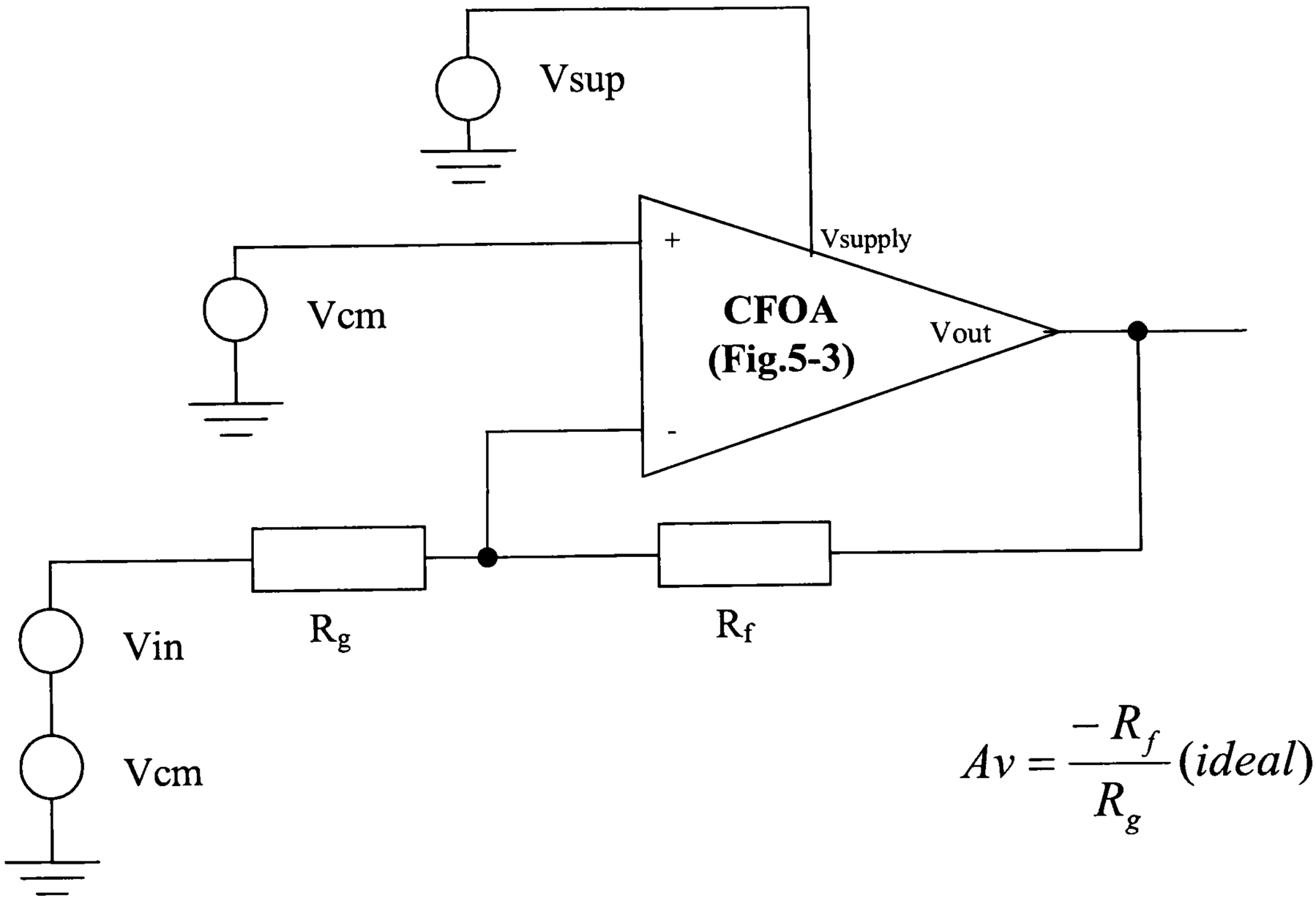

Figure 5-4: Test bench for the CFOA using a cascode current mirror.

The following test conditions were supplied for each test

1. AC small signal gain test.

Vin = 50mV (AC); 1.5V (DC) ; Vbias = 0.45V (DC); Ibias = 50μA (DC);
CasVbiasN = 0.6V (DC); CasVbiasP = 1.2V (DC); Vsupply = 3V; Vcm = 1.5V.

2. AC small signal power supply rejection test.

Vin = 50mV (AC); 1.5V (DC); Vbias = 0.45V (DC); Ibias = 50 μA (DC);
CasVbiasN = 0.6V (DC); CasVbiasP = 1.2V (DC); Vsupply = 3V. Vcm = 1.5V.

3. Transient slew rate test.

Vin = 100mV pulse with a period of 50ns with a rise fall time of 0.1ns.
Vbias = 0.45V (DC); Ibias = 50 μA (DC); CasVbiasN = 0.6V (DC);
CasVbiasP = 1.2V (DC); Vsupply = 3V. Vcm = 1.5V.

Results for each simulated test:

1. AC small signal gain test.

1.a Gain test.

Ideal gain = -1; simulated gain = -0.998; Gain Error = 0.2%.
simulated bandwidth = 389MHz.

1.b Gain test.

Ideal gain = -1; simulated gain = -0.997; Gain Error = 0.3%.
simulated bandwidth = 167MHz.

1.c Gain test.

Ideal gain = -1; simulated gain = -0.996; Gain Error = 0.4%.
simulated bandwidth = 100MHz.

1.d Gain test.

Ideal gain = -2; simulated gain = -1.992; Gain Error = 0.4%.
simulated bandwidth = 286MHz.

1.e Gain test.

Ideal Gain = -2; simulated gain = -1.984; Gain Error = 0.8%.
simulated bandwidth = 68MHz.

2.a AC small signal power supply rejection test.

Figure 5-5 below shows a graph of the power supply rejection ratio (PSRR) in decibels (dB) for the cascode CFOA.

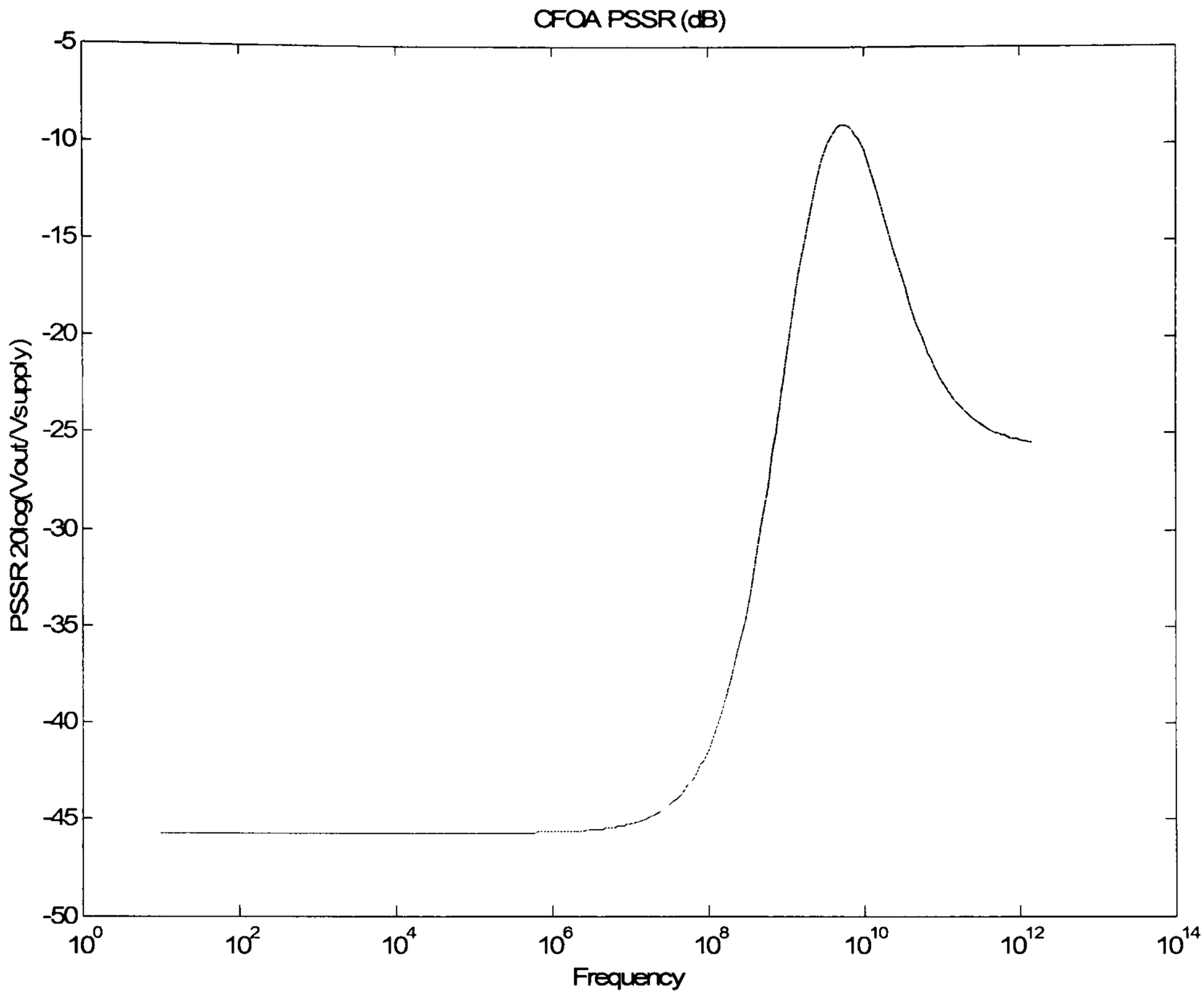

Figure 5-5: PSSR for the CMOS implementation of the cascode CFOA.

The PSRR test summary of results:

Simulated PSSR = -45.72dB; Rising eventually to -7.6dB at 1.3GHz.

3.a Transient slew rate test.

Simulated slew rate (Rising edge) = 8.2KV/μs.

Simulated slew rate (Falling edge) = 922V/ μs.

The difference in the rising and falling edge slew rates is due to the fact that the current conveyor PMOS devices are driving the NMOS source follower to turn it on and PMOS source follower to turn it off. As the PMOS devices have a much lower surface mobility than the NMOS devices it will take longer to drive using a PMOS device than an NMOS device. This in turn gives the differences seen in slew rates **[5-10].**

5.2.2 Using a regulated cascode current mirror

5.2.2.1 Design.

This CFOA is based on the CCII+ that uses a regulated cascode current mirror described in Section 4.4.3 and is shown in Figure 5-6 below:

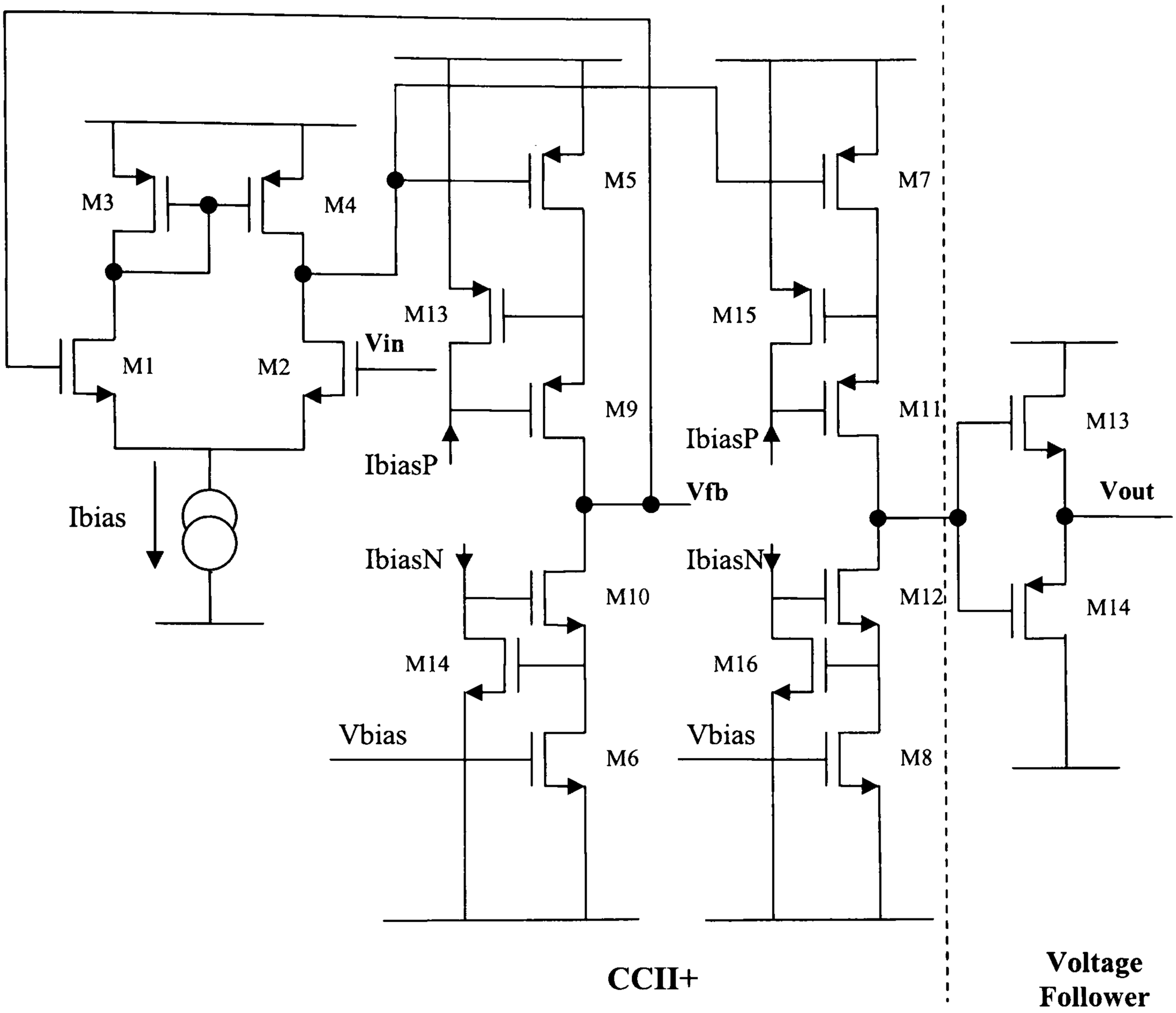

Figure 5-6: A CFOA using a regulated cascode current mirror.

From Figure 5-6 it can be seen that the transistors M1 to M12 make up the cascode current mirror current conveyor (CCII+), and the source follower is made up of transistor M13 and M14.

The transistor dimensions used in the design were as follows:

NMOS: Width = 20μm; Length = 0.4 μm;

PMOS: Width = 40 μm; Length = 0.4 μm;

This circuit simulation results are shown in the next section.

5.2.2.2 Simulation.

The Figure 5-7 shows the test bench used to measure the following parameters specified in the tests listed below for the cascode CFOA shown in Figure 5-6. This was tested using TMSC 0.18 μm process models **[5-9]**.

1. AC small signal gain test..
    a. $R_f = 250\,\Omega$; $R_g = 250\,\Omega$.
    b. $R_f = 300\,\Omega$; $R_g = 300\,\Omega$.
    c. $R_f = 500\,\Omega$; $R_g = 500\,\Omega$.
    d. $R_f = 500\,\Omega$; $R_g = 250\,\Omega$.
    e. $R_f = 1\mathrm{K}\,\Omega$; $R_g = 500\,\Omega$.
2. AC small signal power supply rejection test.
    f. $R_f = 300\,\Omega$; $R_g = 300\,\Omega$.
4. Transient slew rate test
    b. $R_f = 300\,\Omega$; $R_g = 300\,\Omega$.

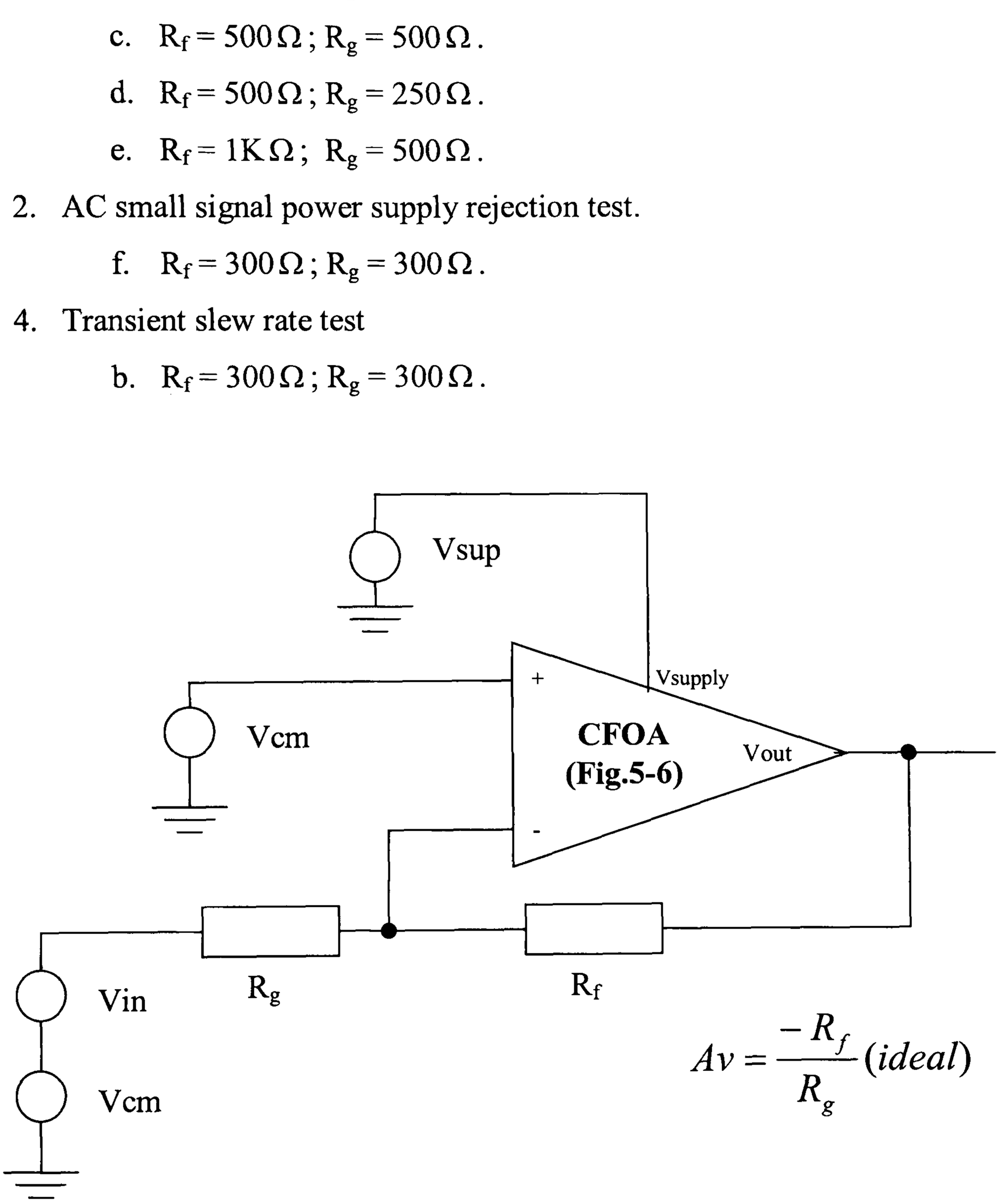

Figure 5-7: Test bench for the CFOA using a regulated cascode current mirror.

The following test conditions were supplied for each test

1. AC small signal gain test.

Vin = 50mV (AC); 1.5V (DC) ; Vbias = 0.45V (DC); Ibias = 50 μA (DC);
IbiasN = 50 μA (DC); IbiasP = 50 μA (DC); Vsupply = 3V. Vcm = 1.5V.

2. AC small signal power supply rejection test.

Vin = 50mV (AC); 1.5V (DC); Vbias = 0.45V (DC); Ibias = 50 μA (DC);
IbiasN = 50 μA (DC); IbiasP = 50 μA (DC); Vsupply = 3V. Vcm = 1.5V.

3. Transient slew rate test.

Vin = 100mV pulse with a period of 50ns with a rise fall time of 0.1ns.
Vbias = 0.45V (DC); Ibias = 50 μA (DC); IbiasN = 50 μA (DC);
IbiasP = 50 μA (DC); Vsupply = 3V. Vcm = 1.5V

Results for each simulated test:

1. AC small signal gain test.

1.a Gain test.

Ideal Gain = -1; Measured Gain = -0.12; Gain Error = 88%.

Measured Bandwidth = 100MHz.

(Gain Collapsed due to low feedback resistance).

1.b Gain test.

Ideal Gain = -1; Measured Gain = -0.999; Gain Error = 0.1%.

Measured Bandwidth = 120MHz.

1.c Gain test.

Ideal Gain = -1; Measured Gain = -0.949; Gain Error = 5.1%.

Measured Bandwidth = 100MHz.

1.d Gain test.

Ideal Gain = -2; Measured Gain = -1.99; Gain Error = 0.5%.

Measured Bandwidth = 234MHz.

1.e) Gain test.

Ideal Gain = -2; Measured Gain = -1.962; Gain Error = 1.9%.

Measured Bandwidth = 60MHz.

2.a AC small signal power supply rejection test..

Figure 5-8 below shows a graph of the power supply rejection ratio (PSRR) in decibels (dB) for the regulated cascode CFOA.

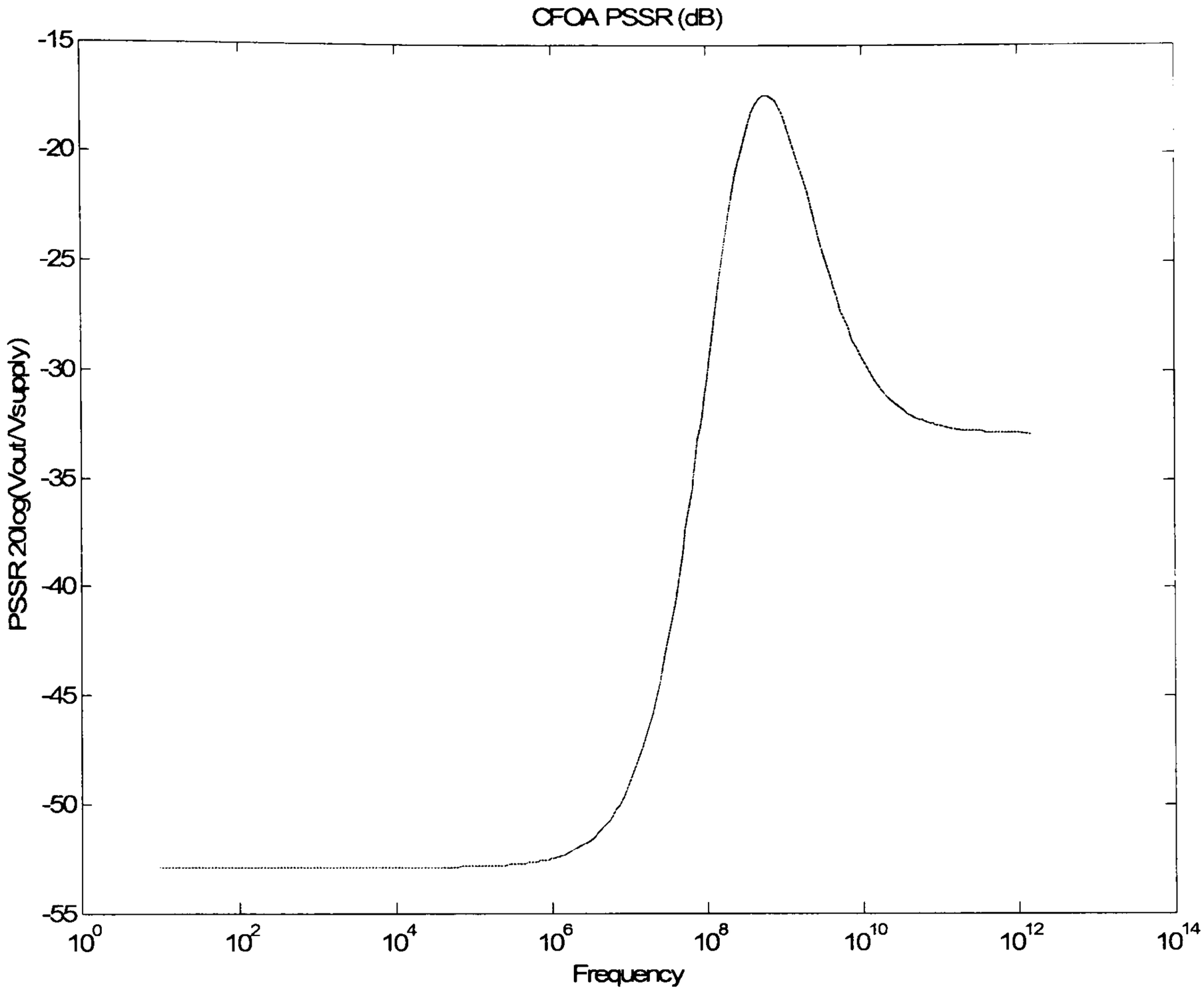

Figure 5-8: PSSR for the CMOS implementation of the regulated cascode CFOA.

The PSRR test summary of results:

Simulated PSSR = -52.9dB; Rising eventually to -16dB at 136MHz.

3.a Transient slew rate test.

Simulated slew rate (Rising edge) = 1.5KV/μs.

Simulated slew rate (Falling edge) = 1.1KV/μs.

Again the difference in slew rates is due to the fact that the current conveyor PMOS devices are driving the NMOS source follower to turn it on and PMOS source follower to turn it off. As the PMOS devices have a much lower surface mobility than the NMOS devices it will take longer to drive using a PMOS device than an NMOS device. This in turn gives the differences seen in slew rates **[5-10]**.

5.3 Summary of Results.

This chapter introduces the new type of CFOA built up using the two best performing new current conveyors described in Chapter Four **[5-5]**,**[5-8]**, the cascode and regulated cascode CCII+. Overall the output gain for the cascode CFOA show gain errors of less than 1%. The regulated cascode CFOA showed larger errors for some of the gain tests. This was due to the feedback collapsing as there was not enough current drive to maintain the feedback through the feedback resistor (R_f) which this design was not capable of delivering. This could be easily fixed if this design was optimized.

It was shown that the cascode and regulated cascode CFOAs had similar bandwidths, which meant that the equivalent capacitance seen on node Z was similar in value for both types of CFOA. The only anomaly in the results was when using the 250Ω resistors for the unity gain test. This was due to the regulated cascode CFOA voltage gain collapsing, caused by the reduced current drive of the CFOA. This would have the effect of reducing the bandwidth of the CFOA as the current driving into the equivalent capacitor seen on node Z was dramatically reduced. It can be also seen that the bandwidth of the amplifier is also affected by the size of the feedback resistor as per Equation 5.1, so as the resistance of the feedback resistor increases the bandwidth drops. It is also noted that the bandwidth is not proportional to the size increase of the feedback resistor. This is due to the fact that the output resistance of the amplifier combines with the feedback resistor (R_f) **[5-5]**.

The CFOAs offered a good level of PSRR, due to the internal voltage feedback of the voltage follower in the new current conveyors as explained in Chapter Three. The cascode CFOA had a PSRR 46dB, but the best was the regulated cascode design with a PSRR figure of 53dB because of its better immunity to power supply noise as explained in Chapter Two. These figures can be improved on by optimizing the design.

The slew rate had faster rise times than fall times for both the CFOAs, this is due to the fact that the architectures use a PMOS driver on the output of the current conveyor CCII+ which in turn drives the voltage follower. As the surface mobility is a lot smaller than that of an NMOS device, the current drive into the follower is worse

when the PMOS is driving. The regulated cascode CFOA offered the best symmetrical rise and fall time around 1.1-1.5KV/μs.

5.4 References

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CHAPTER 6

Conclusions

The current conveyor can be used in many applications from low frequency as LED or backlight drivers for mobile phones, television etc. where it is important to maintain a fixed current through diodes to prevent them from blowing, to high frequency applications where the current conveyors can be used in mixers for up and down converters in anything from radios to mobile phones.

The aim of this thesis was to develop a new type of CMOS current conveyor which could offer improvements in, (i) voltage gain by reducing the gain losses of the voltage follower stage and making the voltage gain as independent as possible of output load, (ii) current gain accuracy by looking at ways of increasing the output impedance, and (iii) improvements in PSRR. These would be compared to other CMOS architectures **[6-1], [6-2],[6-3]**. The thesis is aimed at CMOS type current conveyors, because the CMOS process technologies are more readily available than the BJT equivalents, due to their cost performance and popularity in today's semiconductor industry **[6-4]**.

The thesis approaches the current conveyor by dividing it up into its constituent blocks, the current follower which is dealt with in Chapter Two, and the voltage follower which is looked at in Chapter Three. The results from Chapters Two and Three are then combined to build several version of the new current conveyor in Chapter Four. Chapter Five looks at build a new current feedback operational amplifier from these new types of current conveyor.

Looking in more detail Chapter Two shows how by using analysis and simulation methods different techniques can increase the output impedance of the current followers (mirrors), and therefore reducing the PSRR of the current follower stage.

The analysis was divided into two areas. The first was to look at the behavioural differences in the output impedance between using CMOS and BJT transistors in current mirrors using an analytical approach, and highlighted the advantages and disadvantages of using CMOS devices over that of BJTs. This meant that a new generic low frequency small signal model had to be produced to work with both types of transistors. The second area of this chapter dealt with simulating the current mirrors using CMOS transistors from the TSMC 0.18μm process. From both the analysis and simulations it was found that the best types of current followers were the cascode types, which offered the higher values of output impedance, especially the regulated cascode which had the highest of the impedances 1000 times greater than that of a simple current mirror. It was also shown that the Wilson type of current follower (mirror) had problems mirroring current with smaller gate length CMOS devices. This was due to the fact that a Wilson mirror like any other mirror does not copy the current through the drain source resistance component of the transistor. The Wilson current mirror does not have equal drain source voltages across its input and output transistors, so current is inevitably lost through the input drain source resistance due to the voltage differences. This can be a significant percentage for the smaller gate length devices, as the channel modulation effect is higher and so the drain source resistance tends to be lower. It was found that the improved Wilson mirror offered a more balance approach, so that the voltages across the drain source of the input and output transistors were more closely matched and therefore the current gain was closer to the desired value of unity.

Chapter Three reviewed several types of voltage followers used in CMOS current conveyors. It also looks at the effects of transistor dimensions on gain and bandwidth. It was found that the simple source follower could not be used due to its poor value of voltage gain. This is due to the low value of transconductance that CMOS devices offer over that of their BJT equivalents, which means that large geometry transistors would have to be used to compensate for this. Overall this would have the effect of reducing the bandwidth as the size increase would affect the capacitance at the gate source of the device. The simulations also highlighted the effects of voltage gain due to the presence of the CMOS transistors source resistance, which reduced the overall gain of the voltage follower. The chapter dealt with the extraction of the source resistance and found it to be around 300-350Ω. It was also noted that the standard

process design kit used from TSMC **[6-5]** did not take into account the drain source areas of the transistor, and therefore the drain source resistance defaulted to the maximum value based on the smallest transistor of the design kit, these parameters need to be added into future design kits to prevent this from happening again. Other designs were also reviewed, including a class AB complementary follower and a balanced two stage voltage follower. But overall it was found that the best design was the two stage un-buffered amplifier with unity feedback and gain which offered the best combination of PSSR, gain and bandwidth.

There are two basic elements to a good current conveyor a low output impedance stage voltage follower discussed in Chapter Two, and a high output impedance current follower discussed in Chapter Three. These two elements are combined in Chapter Four to present several types of new current conveyors. The best overall option for the voltage follower was found to be a two stage un-buffered amplifier with unity feedback. This solution has the advantage of offering a larger bandwidth than that of an OTA voltage follower type current conveyor, as it is not limited by the compensation capacitor of the OTA, but unlike other CMOS current conveyor architectures it also offers the same PSRR of the OTA type current conveyor. The new current conveyors performance was measured against a benchmark version of the current conveyor which was a simplified version of the more popular bipolar design. It was found that all the new current conveyors performed better than the benchmark version of the current conveyor both in gain accuracy and PSRR. It was also found that the best conveyors were using the cascode type current mirrors as these had the least overall voltage gain errors and the best PSRR figures. This was due to the inherent high output impedance values that they offered compared to that of a simple current mirror, the disadvantage of these devices is the extra power supply headroom needed to operate them. It was also noted that the regulated cascode current conveyor offered the best PSRR a figure of around 59dB, while the cascode current conveyor offered the better bandwidth option of the two cascode current conveyor solutions.

Chapter 5 uses the two best performing current conveyors from Chapter 4, the new cascode current conveyor, and the new regulated cascode current conveyor to build two new CFOAs. These designs were simulated and the results compared. It was found that the CFOA with the cascode type current conveyor offered the best type of

voltage gain simulated accuracy with less than 1% error. The regulated cascode type CFOA suffered from a lack of current drive which caused the feedback to collapse during the unity gain test using resistor values of $250\,\Omega$, optimising the design would remedy this problem. It was found that the cascode type CFOA also had the greater bandwidth that of up to 400MHz. The regulated cascode offered the better PSRR that of -53dB compared to that of -46dB of the cascode type CFOA, this shows that the regulated CFOA has a higher immunity to the power supply due to its higher output impedance over the cascode type CFOA.

Overall it was found that the best type of current conveyor was one that was built with an un-buffered amplifier voltage follower stage, and a cascode type current follower stage, as this offered the best voltage gain and PSSR characteristics.

6.1 Further work

Most of the work of this thesis was to look at the architectures of the existing current conveyors and highlighted improvements for CMOS type devices using existing processes in this case the TSMC 0.18um process **[6-4]**. Further work can be done on looking at ways of improving the efficiency of these current conveyors by reducing the current consumption especially under DC bias conditions.

This thesis briefly looked at the CMOS current feedback operational amplifiers and this is a definite area for further research, looking at other architectures, the initial work shows a good PSSR and good overall gain bandwidth figures are initially around 400MHz for the cascode version. This can be improved dramatically with more work.

6.2 References

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