# High-Speed Low-Voltage Line Driver for SerDes Applications

By

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In Collaboration With
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## Abstract

The driving factor behind this research was to design & develop a line driver capable of meeting the demanding specifications of the next generation of SerDes devices. In this thesis various line driver topologies were analysed to identify a topology suited for a high-speed low-voltage operating environment.

This thesis starts of by introducing a relatively new high-speed communication Device called SerDes. SerDes is used in wired chip-to-chip communications and operates by converting a parallel data stream in a serial data stream that can be then transmitted at a higher bit rate, existing SerDes devices operate up to 12.5Gbps. A matching SerDes device at the destination will then convert the serial data stream back into a parallel data stream to be read by the destination ASIC. SerDes typically uses a line driver with a differential output. Using a differential line driver increases the resilience to outside sources of noise and reduces the amount of EM radiation produced by transmission.

The focus of this research is to design and develop a line driver that can operate at 40Gbps and can function with a power supply of less than 1V. This demanding specification was decided to be an accurate representation of future requirements that a line driver in a SerDes device will have to conform to.

A suitable line driver with a differential output was identified to meet the demanding specifications and was modified so that it can perform an equalisation technique called pre-distortion. Two variations of the new topology were outlined and a behavioural model was created for both using Matlab Simulink. The behavioural model for both variants proved the concept, however only one variant maintained its performance once the designs were implemented at transistor level in Cadence, using a 65nm CMOS technology provided by Texas Instruments.

The final line driver design was then converted into a layout design, again using Cadence, and RC parasitics were extracted to perform a post-layout simulation. The post layout simulation shows that the novel line driver can operate at 40Gbps with a power supply of 1V – 0.8V and has a power consumption of 4.54mW/Gbps. The Deterministic Jitter added by the line driver is 12.9ps.

# List of principal symbols and acronyms

| | |
|---|---|
| *SerDes* | Serialiser / Deserialiser |
| *ZTC* | Zero Temperature Coefficient |
| *PCI-E* | Peripheral Component Interconnect Express |
| *SATA* | Serial Advanced Technology Attachment |
| *SAS* | Serially Attached Small Computer System Interface |
| *IC* | Itegrated Circuit |
| *ASIC* | Application Specific Integrated Circuit |
| *PLL* | Phased-locked loop |
| *I/O* | Input / Output |
| *Gbps* | Gigabit per Second |
| *Tx* | Transmitter |
| *Rx* | Receiver |
| *RC* | Resistor and Capacitor |
| *ISI* | Inter-Symbol Interference |
| *TI* | Texas Instruments |
| *CML* | Common Mode Logic |
| *LVPECL* | Low-Voltage Positive Emitter Coupled Logic |
| *LVDS* | Low-Voltage Differential Signalling |
| *HPF* | High Pass Filter |
| *PRBS* | Pseudo-Random Bit Sequence |
| $G_m$ | Transconductance |
| $g_m$ | Transconductance of a CMOS device |
| $Av$ | Voltage gain |
| $\beta$ | Transconductance parameter |
| $V_T$ | Threshold Volatge of a CMOS device. |
| $V_A$ | Early Voltage |
| $f_T$ | Transistor unity-gain frequency |
| $f_{-3dB}$ | Closed-loop -3dB frequency |

| | |
|---|---|
| $I_D$ | Drain current. |
| $\lambda$ | CMOS transistor channel modulation effect. |
| $C_{ox}$ | Gate oxide capacitance for a CMOS device |
| $C_{gs}$ | Intrinsic Gate-Source capacitance |
| $C_{gd}$ | Intrinsic Gate-Drain capacitance |
| $C_{db}$ | Intrinsic Drain-Body capacitance |
| $r_o$ | Small-signal output resistance of a CMOS device |
| $m$ | Current mirror transfer ratio |
| *CMOS* | Complementary Metal Oxide Silicon. |
| *MOSFET* | Metal–Oxide–Semiconductor Field-Effect Transistor |
| *THD* | Total Harmonic Distortion |
| *TIA* | Transimpedance Amplifier |

## Contents

# Chapter 1

# Introduction

## 1.1 Motivation for Thesis

The conventional method of conveying electronic data at high data rates is to use parallel rather than serial transmission [1]. However, as the data rates continue to increase into the gigabit range, parallel transmission becomes problematic due to multi-path synchronisation difficulties as well as being expensive to implement [2]. The industry is resolving the problem by introducing high-speed serial technology. For example there are several different industry standards, including PCI-E (Peripheral Component Interconnect Express), SATA (Serial Advanced Technology Attachment), and SAS (Serially Attached Small Computer System Interface) which are all inter-computer serial communication protocols that have been developed from parallel predecessors [1,3].

A circuit that is used to convert parallel data to serial data for serial data transmission and then receive the serial data and convert it back to parallel data is referred to as a Serialiser / Deserialiser, which is abbreviated to SerDes [4,5]. It can either be a stand-alone device or integrated into an Application Specific Integrated Circuit (ASIC). Its function is to convert the input parallel data stream into an output serial data stream for transmission. On the receiver end a SerDes is used to reconvert the incoming serial data stream back into parallel output data. The further features included in a SerDes device are clock recovery/generation for synchronisation, channel equalisation, error correction and data encoding [6].

SerDes can be found in wireless routers[4], fibre optic communication systems, mobile phones and base stations, super computers[7], liquid crystal displays, anywhere that a high speed link is needed with very low data errors[8]. For example super computers are given mammoth tasks to accurately predict global weather and climate change[2] which involves large amounts of data to be transmitted between processor clusters at high speeds with low error rates. SerDes is used to allow the clusters of processors to communicate at data rates up to 10Gb/s with bit error rates of $10^{-12}$ [3,4,9].

The bit error rate (BER) of $10^{-12}$ was chosen as it is stated in the IEEE 802.3 standard [10]. This value was chosen by the 802.3 standard as a target BER because it was measurable. However as data rates increased the minimum measurable BER also decreased and today a BER of $10^{-15}$ is measurable.

This research program is sponsored by Texas Instruments, (TI), and the work is focused on the development of high speed inter-computer communication electronics. This is a particular strength of TI with their UK Design Centre at Northampton being responsible for these circuit and system developments. The likely destination for the results of this research will be for high speed communication links between processors within a super-computer.

The primary aims of this thesis are to i) critically review and investigate the challenges facing SerDes as speeds reach 40Gbps while maintaining the bit error rate of $10^{-12}$, ii) design and develop a novel transmitter to help overcome the challenges of high speed communications. Key parameters such as chip area, power consumption, and maximum speed will be used as figures of merit for comparison purposes in evaluation of different designs.

## 1.2 Main Objectives

There are many aspects to SerDes design including the transmitter, receiver, phased-locked loop (PLL) and mixed signal routing. Each comes with its own challenges and a design team of experts is required to overcome them. Due to the complexity of high speed data transmission I will be focusing my efforts on the transmitter, which in the case of SerDes is called a 'line driver'.

The main objective of this research is to design a novel line driver to meet the "future proof" specification of:

- A supply rail (VDD) of 1V
- Operating frequency = 40Gbps
- Chip area = 200$\mu m^2$, which is defined by the area available for the line driver on a test chip supplied by Texas Instruments.
- Transistor technology = CMOS 65nm, which can be readily migrated to smaller geometry processes.

Due to deep sub-micron technology devices and power consumption requirements the rail voltage of 1V is becoming more and more prevalent. Furthermore, due to power distribution losses on the die, the rail voltage can be as low as 0.85V by the time it reaches the transmitter.

The typical challenges of high speed data transmission will be identified and a range of relevant techniques will be reviewed that have been developed to address these challenges.

To achieve these demanding specifications a detailed study of existing line driver topologies will be undertaken to identify which design techniques can be applied to the high-speed low-voltage environment.

## 1.3 Thesis Outline and Structure

This thesis is seven chapters in total. Following this introductory chapter, Chapter 2 introduces the concept of the SerDes device including why it is needed for high speed data transmission and operating principles. Also in Chapter 2 the line driver and its role within SerDes is examined in detail.

In Chapter 3 the performance of four existing different driver topologies are critically reviewed and compared with the aim of identifying which type would fit the tight performance specifications (1.2 above) that the novel driver has to achieve. In addition Chapter 3 also contains the device parameters of all transistors used in this research. Having completed the ground work discussed in Chapter 3, a driver topology suitable for low-power high-speed transmission has been identified along with its strengths and weaknesses.

The thesis contains two MOSFETs from different companies. The more advanced of the two is the Texas Instruments 65nm "model". This 65nm model is specifically for low voltage circuits where a typical power supply is 1V. This transistor will be used in the novel Chapters of this thesis where supply voltages will be 0.8V – 1V. At 2V the gate oxide breaks down thus a second transistor with a thicker gate oxide is needed for the high voltage applications, i.e. applications with supply voltages greater than 2V.

The second model to be used is the IBM T68A 130nm MOSFET. This transistor will be used in the critical review chapter where higher supply voltages are used to meet the standards specifications. The focus of Chapter 4 is on the design and development of a novel SerDes line driver. Using an adapted Low-Voltage-Differential Signaling (commonly referred to as LVDS) architecture I have designed a novel line driver, named Composite-LVDS (C-LVDS), which can adjust its gain depending on the frequency of the input data, performing a form of equalisation on the transmitter end. Two versions of C-LVDS are presented and verified mathematically in a behavioral model designed in Matlab before the transistor level model is designed in Cadence. Also in Chapter 4, different ways in which the driver can detect its operating frequency are identified, and then used to adjust the transmitter gain.

The layout floor-plan will be presented in Chapter 5 and will provide all the rules and layout techniques used to achieve this level of performance. Chapter 5 also contains one of the most important and realistic simulations possible in Cadence, called a RC Post-Layout simulation. This simulation contains all the parasitic resistances and capacitances, hence the term 'RC', which will be added by the metal traces used in the routing of the devices.

Finally Chapter 6 will wrap up the thesis with any conclusions that can be drawn about the novel line driver, C-LVDS, as well as any future work to be carried out.

## 1.4 Original Work

There have been several areas of original work throughout this thesis, a summary is shown below:

- In Chapter 2 I investigated the use of a device called SerDes. Typical noise factors are described and analysed. Common types of channel equalisation are also investigated.

- In Chapter 3 I investigated various line driver topologies. I characterised two geometries of CMOS MOSFETs, 130nm and 65nm, which were then analysed to ensure performance at 40Gbps and various levels of VDD.

- In Chapter 3 I critically analyse four popular line driver topologies:
    1. Common Mode Logic (CML).
    2. Low-Voltage Positive Emitter Coupled Logic (LVPECL).
    3. H-Bridge.
    4. Low-Voltage Differential Signaling (LVDS).

- In Chapter 4 I investigated how channel equalisation can improve performance at 40Gbps. My novel line driver topology is introduced as Composite-LVDS (C-LVDS) which comprises of LVDS style drivers employing a pre-distortion channel equalisation technique, two further variants of C-LVDS are designed and the high speed performance of both circuits is analysed in this chapter.

- In Chapter 5 I continue the development of C-LVDS by designing a mask set for use in Photolithography.

- Chapter 5 continues with a Monte Carlo analysis that I performed on the final design of my novel line driver with the added parasitics that I extracted from the layout.

- Chapter 6 concludes the thesis with a discussion of the final design of my novel line driver. I discuss future work and possible applications of C-LVDS.

Two Papers have been produced from this research. The first paper, found in Appendix 1, contains preliminary results and findings and was published in the Analog Signal Processing Conference Proceedings in 2008. The second paper, found in Appendix 2, contains full results and findings and has been submitted to the ISCAS 2010 Conference.

## 1.5 References


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[9] M. Ishida, et al, "A Method for Testing Jitter Tolerance of SerDes Receivers Using Random Jitter," in Proc. Int. Engr. Consortium DesignCon 2007, January 2007.

# Chapter 2

# Overview of Serialiser Deserialiser

## 2.1 Introduction

SerDes stands for Serialiser / Deserialiser and is a relatively new device for converting parallel links into high speed serial links. SerDes is an I/O interface to be added between two devices using a parallel data stream, where its job would be to convert the parallel data stream into a serial data stream and back to parallel at the other side of the channel, shown in Figure 2.1. SerDes can be a separate device, or it can be integrated directly into the Application Specific Integrated Circuit (ASIC) replacing the conventional parallel I/O device[1]. This integrated solution had a profound effect on the SerDes device as it has made it possible to move a lot of the digital architecture involved into the ASIC.

This parallel to serial conversion is important as for a given number of links the data that can be transferred between chips goes up from 1Gbps/link to 10Gbps/link and reduces the link count by a factor of 10, or alternatively allows ten times as much data to be transferred between chips. The typical data transfer rate of a super computer is in the Tb/s region, therefore 100 10Gb/s links are needed for each Tb.

### 2.1.1 SerDes Architecture

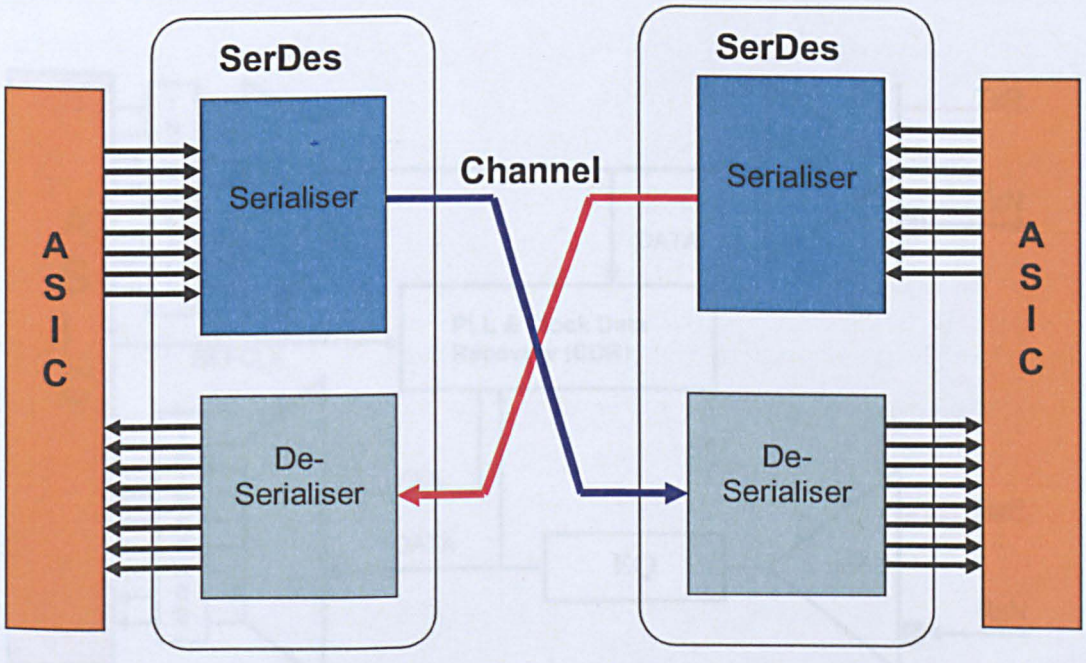


*Figure 2.1 – SerDes Overview [1]*

Figure 2.1 shows that the ASIC transmits and receives a parallel data stream. However the data is transmitted over a transmission line in a serial manner.

A simplified block diagram of the SerDes architecture is shown in Figure 2.2, which was adapted from [1,2,3]. Starting on the left of the diagram is the ASIC which is the device that is sending and receiving the data, usually to another ASIC. This data is intercepted by the SerDes device using a sample and hold latch, commonly referred to a D-Type flip-flop.

The latch can be used to redefine signal voltage levels for use by the multiplexer. A clock signal (REFCLK) is provided by the ASIC to be used for the timing of the multiplexer. The multiplexer converts the parallel data into a serial data stream, but before the signal is transmitted a clock signal needs to be added to the data for synchronisation of the receiver. The clock signal is derived by using a PLL to multiply the REFCLK signal provided by the ASIC.

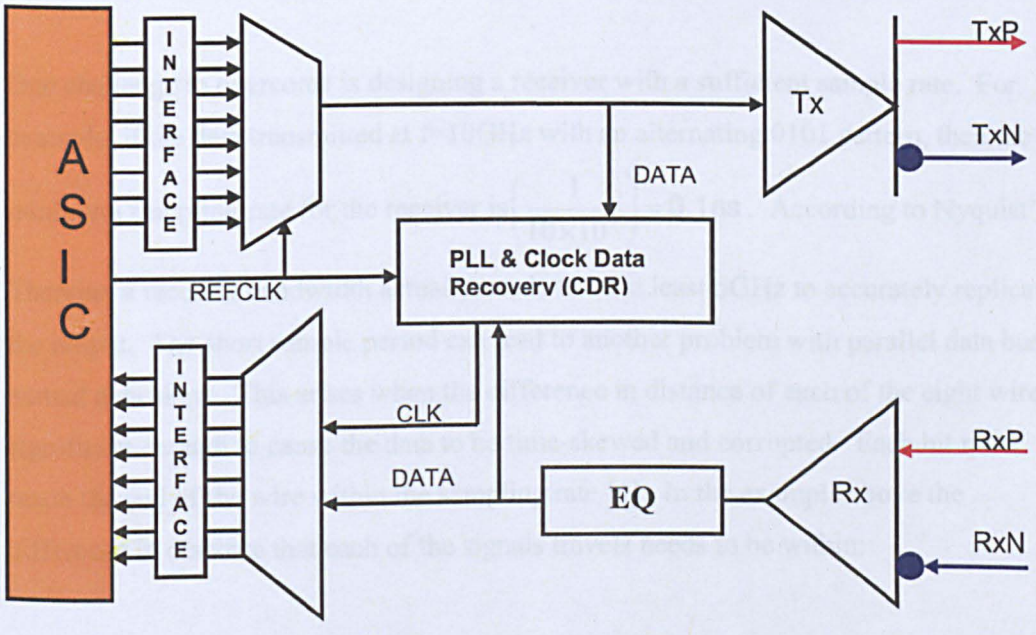


*Figure 2.2 – Simplified SerDes Block Diagram*

Once the clock signal has been added to the data it is transmitted using a line driver which uses the differential signalling method, indicated by TxP and TxN.

SerDes has the ability for full duplex transmission as it also contains a receiver, which receives the differential signal using a differential receiver. An equalizer (EQ) is used to equalize the signal to improve Bit Error Rate (BER)[2]. The synchronization clock is extracted from the data using a Clock and Data Recovery (CDR) circuit which provides the clock for the de-multiplexer. Finally the data is run through a latch to redefine the voltage levels for the ASIC.

### 2.1.2 Challenges facing SerDes

Converting data from parallel to serial for high speed transmission may seem counter intuitive as for many years parallel has always been seen as the faster method of sending data. Although this is still true at low frequency transmission, to achieve data rates in the gigabit range the introduction of SerDes provides a cost effective and practical alternative approach.

One challenge to overcome is designing a receiver with a sufficient sample rate. For example, if the data transmitted at f=10GHz with an alternating 0101 pattern, then the minimum sampling rate for the receiver is $\left(\frac{1}{10\times10^{9}}\right)=0.1\text{ns}$. According to Nyquist's Theorem a receiver bandwidth actually needs to be at least 5GHz to accurately replicate the output. The short sample period can lead to another problem with parallel data buses named data skew. This arises when the difference in distance of each of the eight wires is significant enough to cause the data to be time-skewed and corrupted. Each bit must reach the end of the wire within the sampling rate [1]. In the example above the difference in distance that each of the signals travels needs to be within:

$$v_o = \frac{1}{\sqrt{\omega_o \varepsilon_o}}$$

$$v_{(line)} = \frac{1}{\sqrt{\omega_o \varepsilon_r \varepsilon_o}} = \frac{v_o}{\sqrt{\varepsilon_r}}$$

for $\varepsilon_r = 4$

$$v_{(line)} = \frac{v_o}{2}$$

$$v_o = c = 3_{\times 10}{}^{8}\, m/s = 30cm/ns$$

$$v_{(line)} = \frac{v_o}{2} = 15cm/ns$$

where:

$v_o$ = velocity of an electron in freespace.

$\varepsilon_o$ = vacuum permittivity

$\varepsilon_r$ = relative permittivity

$\omega_o$ =resonance frequency

Assuming the receiver has a 5% tolerance to skew then the time maximum time variance tolerance becomes 5% of the period = 0.005ns.

$$\therefore \Delta l = \frac{v_o}{2} \times 0.005ns$$

$$= \underline{\underline{0.75mm}}$$

By using serial transmission architecture the data skew problem is greatly reduced as only two wires in a differential pair need to be matched and the cost of the system is reduced as less pins/wires/traces are needed for transmission.

Another problem faced by SerDes devices operating at high speeds is signal degradation due to the bandwidth limitation of the channel's electrical properties, the skin effect and dielectric loss, at high frequencies[4].

The problem of the skin effect arises due to the nature of the transmission lines attenuation properties in relation to speed. Consider the bit pattern 1010110011. The first four bits represent the maximum bit rate while the final six bits will appear as half the maximum frequency. An example transmission line bandwidth is shown in Figure 2.3. In this case the maximum bit rate is 1Gbps, this means the last six bits will have an effective data rate of 0.5Gbps. According to Figure 2.3 the attenuation for the first part of the data is greater than the second, and the through delay also varies.

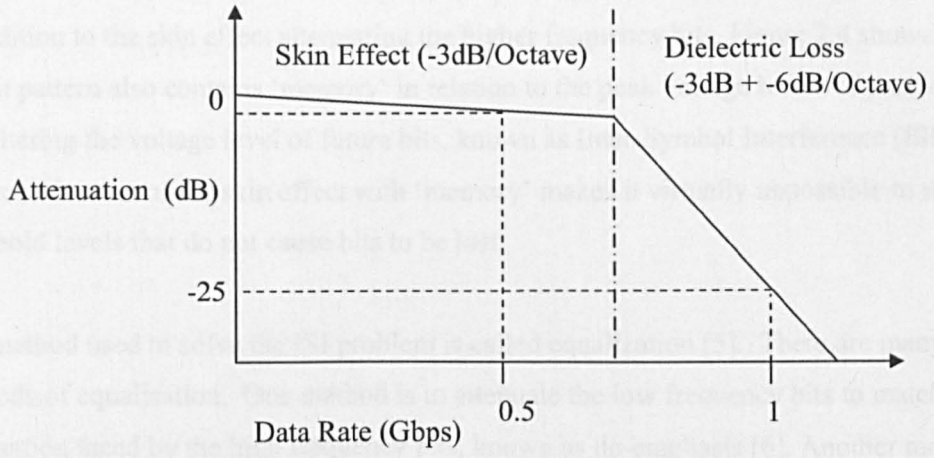


*Figure 2.3 – Example attenuation characteristics of a theoretical transmission line*

The input and output waveforms can be compared to see how the skin effect and dielectric loss alters the transmitted signal, as shown in Figure 2.4 which was obtained through Cadence using a Pseudo-Random Bit Sequence (PRBS) generator driving a single pole RC filter. It can be clearly seen that the high frequency bits have been greatly attenuated compared with the low frequency bits and no longer reach the threshold levels of the receiver.

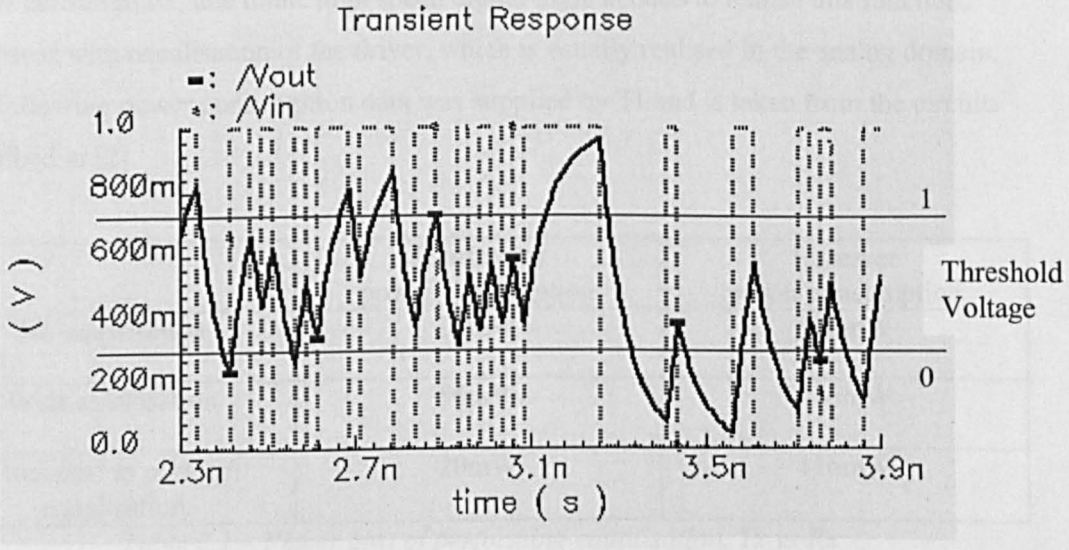


*Figure 2.4 – Transmitted signal vs received signal over a transmission line*

In addition to the skin effect attenuating the higher frequency bits, Figure 2.4 shows how the bit pattern also contains 'memory' in relation to the peak voltage levels of previous bits altering the voltage level of future bits, known as Inter-Symbol Interference (ISI). The combination of the skin effect with 'memory' makes it virtually impossible to set threshold levels that do not cause bits to be lost.

The method used to solve the ISI problem is called equalization [5]. There are many methods of equalisation. One method is to attenuate the low frequency bits to match the attenuation faced by the high frequency bits, known as de-emphasis [6]. Another method would be to boost the high frequency bits to overcome the attenuation of the channel, known as pre-emphasis [6]. Pre-emphasis and De-emphasis can be performed by the transmitter and are discussed in more detail later in this chapter.

One more method of equalisation is called Decision Feedback Equalisation (DFE) and can only be performed by the receiver [2]. This method works by the receiver looking at n previous bits in the pattern and predicting what the voltage level of the next bit will be. The receiver will then adjust its threshold voltage accordingly. This method is very complex [7] and can only be performed by the receiver making it costly in terms of power consumption, due to the high speed digital logic needed to realise this function, compared with equalisation of the driver, which is usually realised in the analog domain. The following power consumption data was supplied by TI and is taken from the circuits described in [2]

| | Transmitter power consumption | Receiver power consumption |
|---|---|---|
| No equalisation | 36mW | 100mW |
| With equalisation | 56mW | 216mW |
| Total cost to perform equalisation | 20mW | 116mW |

*Table 2.1 – Power cost of performing equalisation, Tx vs Rx*

Clearly from the data in Table 2.1 it can be seen that engineering effort is best concentrated on the transmitter where greater power efficiency can be achieved.

## 2.2 Role of the Line Driver in SerDes

### 2.2.1 Introduction

The role of the line driver is to prepare a digital signal for transmission over a transmission line for extended distances and to increase the reliability (BER target 1 x $10^{-15}$) of transmission of the digital signal. There are many types of line driver architectures that may be considered for this, which will be discussed in Chapter 3. Digital signals are made up of many harmonics to make a square wave, however over long distances and at high speeds the higher harmonic components suffer greater attenuation distorting the signal[8].

The SerDes line driver is essentially an amplifier designed to send the digital signal down a transmission line interconnecting two or more electronic devices together. The primary roles are (i) to condition the signal to compensate for the non-ideal characteristics of the transmission line and (ii) to launch the signal with a low output impedance as closely matched to that of the transmission line as possible.

### 2.2.2 Differential Signaling

Differential signaling is commonly used in areas that are prone to large amount of common-mode noise, such as mains interference and ground offsets, and car electronic systems like CAN Bus [9]. Differential signaling is set up by using two transmission lines in parallel and in close physical proximity to each other. The data is then sent down both lines by a dual output transmitter where the outputs are in anti-phase [10]. To recover the data the receiver then takes the difference between the two signals and any common-mode interference/noise is cancelled. Figure 2.5 shows how differential signaling can be used to remove noise spikes created by Electro-Magnetic Interference (EMI).

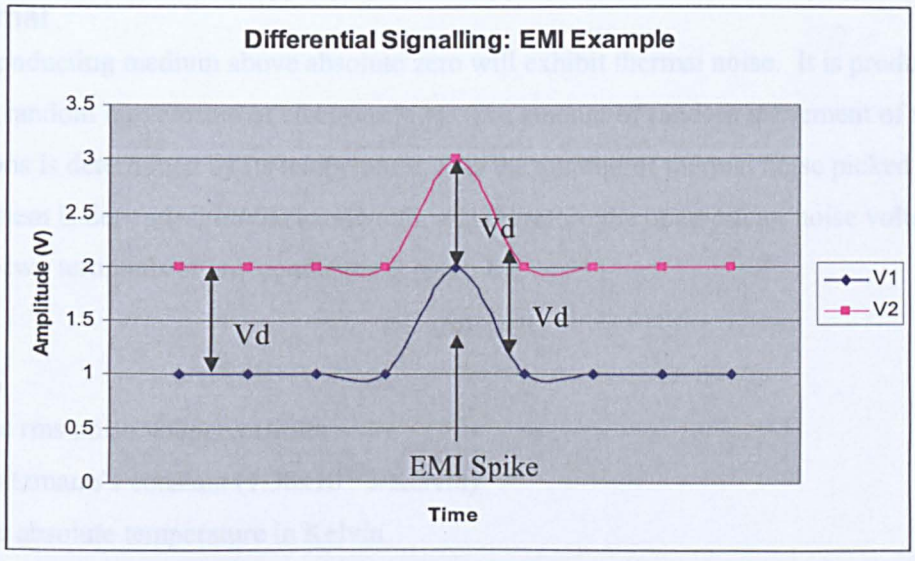


*Figure 2.5 – Removing EMI with differential signaling*

Although the EMI spike has caused a voltage level increase, both transmission lines were affected equally, therefore the voltage difference (Vd) between them stays the same.

Less EMI is created by the differential signals compared with single ended signal due to the fact that the signals are of opposite polarity, resulting in a cancellation of the magnetic field caused by the electrons flowing through the wire [11].

Another benefit of differential signaling is due to the signal not being referenced to ground, whereas in single ended signaling it is. This means that the transmitter and receiver may operate on different grounds without causing signal level errors [11].

### 2.2.3 Noise

Three types of noise that are common to transmission systems, due to the nature of active devices [12], namely (i)Thermal (or Johnson-Nyquist noise), (ii) Shot and (iii) 1/f noise (or Pink noise). A fourth noise component common to SerDes in particular is called Jitter [3]. The origins of each type of noise will be discussed below, leading to relevant equations that define them.

## Thermal

Any conducting medium above absolute zero will exhibit thermal noise. It is produced by the random movements of electrons [13]. The amount of random movement of the electrons is determined by its temperature, also the amount of thermal noise picked up by the system is dependent on the bandwidth, and therefore the open-circuit noise voltage across two terminals of any conductor is given by:

$$V = \sqrt{4kTRB} \tag{2.1}$$

where,

V = the rms noise voltage in volts

k = Boltzmann's constant ($1.38 \times 10^{-23}$J/Kelvin)

T = the absolute temperature in Kelvin

R = the resistance of the conductor in ohms

B = the bandwidth in hertz.

## Shot

Shot noise is produced by the particle like nature of a flow of electrons. As the flow of current is made up of individual electrons there are moments in time where the amount of electrons flowing fluctuates, causing minor changes in the current, which is seen as noise [13]. Shot noise is found using the formula,

$$I_n^2 = 2qI_{dc}B \tag{2.2}$$

where,

$I_n^2$ = the mean square noise current

q = the electron charge ($1.6 \times 10^{-19}$coulombs)

$I_{dc}$ = the direct current in amperes

B = the bandwidth in hertz.

## 1/f

This type of noise is found in all active devices [12]. Its origins vary but are mainly caused by 'traps' made up from impurities in the silicon where carriers are stored and released at random times.

This type of noise is also known as Flicker noise and is dependent on a flow of direct current. It displays a spectral density in the form of

$$\overline{I^2} = K_1 \frac{I^a}{f^b} \Delta f \tag{2.3}$$

where,

$\Delta f$ = bandwidth at frequency f

I = direct current

$K_1$ = constant for particular device

a = constant in the range 0.5 to 2

b = constant of about unity.

## Jitter

Jitter is considered to be the most important form of noise in terms of SerDes and is regularly used in terms of merit for components destined for SerDes. Jitter is noise in the time domain [14], therefore its effects are best seen in the transient response of the system. Figure 2.6 was produced in Cadence by the author to show how jitter can be seen in an 'eye-diagram'.

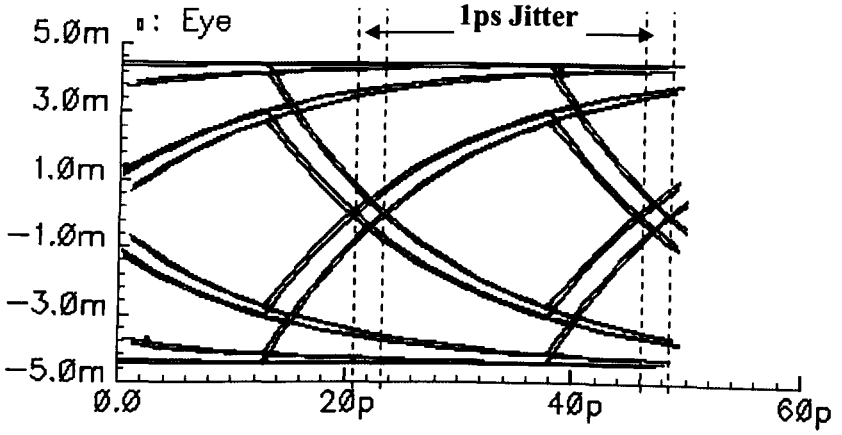


*Figure 2.6 – Simulated eye-diagram showing jitter noise*

From the eye-diagram above it can be noted that the pulse does not always cross the zero crossing point at the same point in time. This spread is called Jitter.

Jitter can be caused at any stage of the system, but the largest contributors are from the PLL, inter-symbol interference and impedance mismatching [15]. Because of this the Total Jitter (TJ) can be split into 2 main groups, namely (i) Deterministic Jitter, (ii) Random Jitter [16].

Deterministic Jitter (DJ) is predictable by definition and covers Data Dependent Jitter (DDJ) and Phase Jitter (PJ) [17]. DJ can be caused by clock noise, power supply noise, process variations and Inter Symbol Interference (ISI). DJ is bounded in nature and therefore has a maximum value.

Random Jitter (RJ) is random by definition. It can take Gaussian distribution form however other forms also may be observed. Random Jitter is usually caused by device noise i.e. Shot, Flicker and Thermal noise are the common contributors to RJ [18]. RJ is unbounded in nature and hence the peak value depends on the length of time over which it is measured. This noise is the main cause of the bit error rate of SerDes links.

### 2.2.4 Channel Characteristics and Equalisation

As SerDes is designed for wired transmission the "Channel", Figure 2.7, consists of the "package", which is the capacitance and resistance associated with the signal leaving the package. The transmission line which can be the wire, the track or the backplane and the associated parasitics of each, ending with another package which represents the receiver's physical package properties.

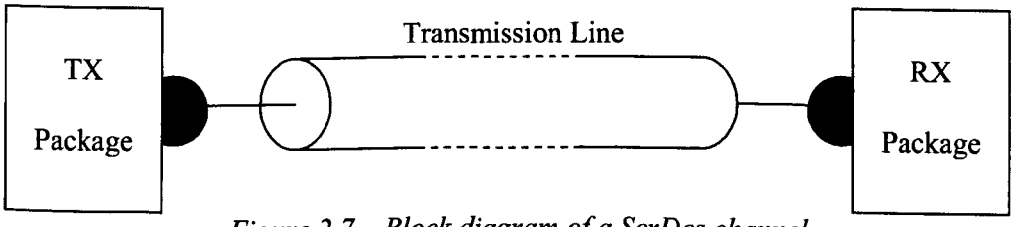


*Figure 2.7 – Block diagram of a SerDes channel*

It is important to be able to include the extra parasitics associated with the channel into the simulation as it will give more accurate physical limitations to the simulation. As the transmission line is the biggest limiter of performance lots of research is done on improving its properties and so it can be assumed that there will be sufficient improvements to transmission line technology that the transmission line will be a suitable medium for the target speeds. As a rule of thumb the worst case scenario would be -25dB of signal attenuation at 20GHz which is the equivalent of about 8 inches of PCB made out of FR4 material or 16inches of PCB made out of Rogers material.

However to keep simulations as accurate as possible TI have created S-Parameter files that accurately simulate the channel and are adaptable to future improvements of process technologies. Due to complicated legal issues these S-Parameter files have to remain on TI's servers therefore a lumped approximation is needed for simulations of the IBM transistor models which are run locally.

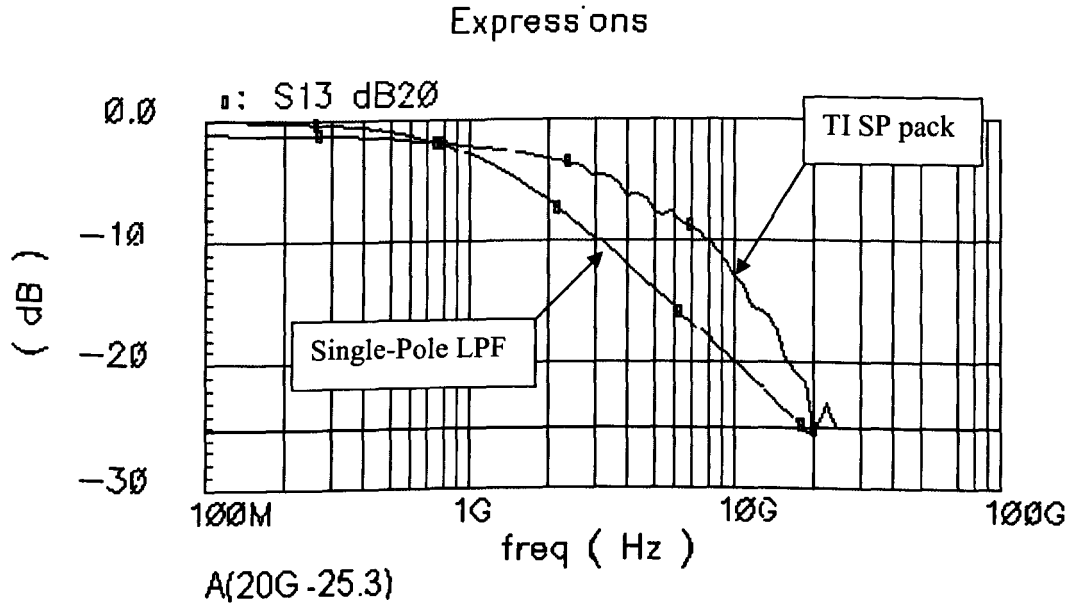


*Figure 2.8 – Simulated SerDes channel characteristics*

The channel, whose characteristics are shown in Figure 2.8, effectively behaves as a low pass filter and as a first order approximation can be considered as a single pole RC filter [19], Figure 2.9. It is known that the resistance of the transmission line is 50Ω and using $f = \frac{1}{2\pi RC}$ an appropriate capacitance can be selected for the appropriate frequency. For comparison the LPF attenuation characteristic is also shown in Figure 2.8.

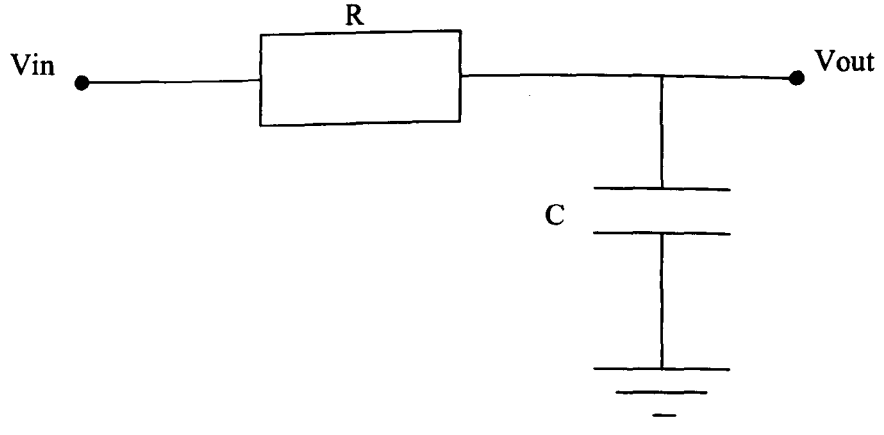

*Figure 2.9 – Lumped sum approximation of a channel*

De-emphasis is a method that is used to balance the attenuation of the channel, which is a form of equalisation. It works by purposely attenuating the low frequency components of the signal by adding a high pass filter to the low pass filter which gives an attenuation curve similar to the one in Figure 2.10

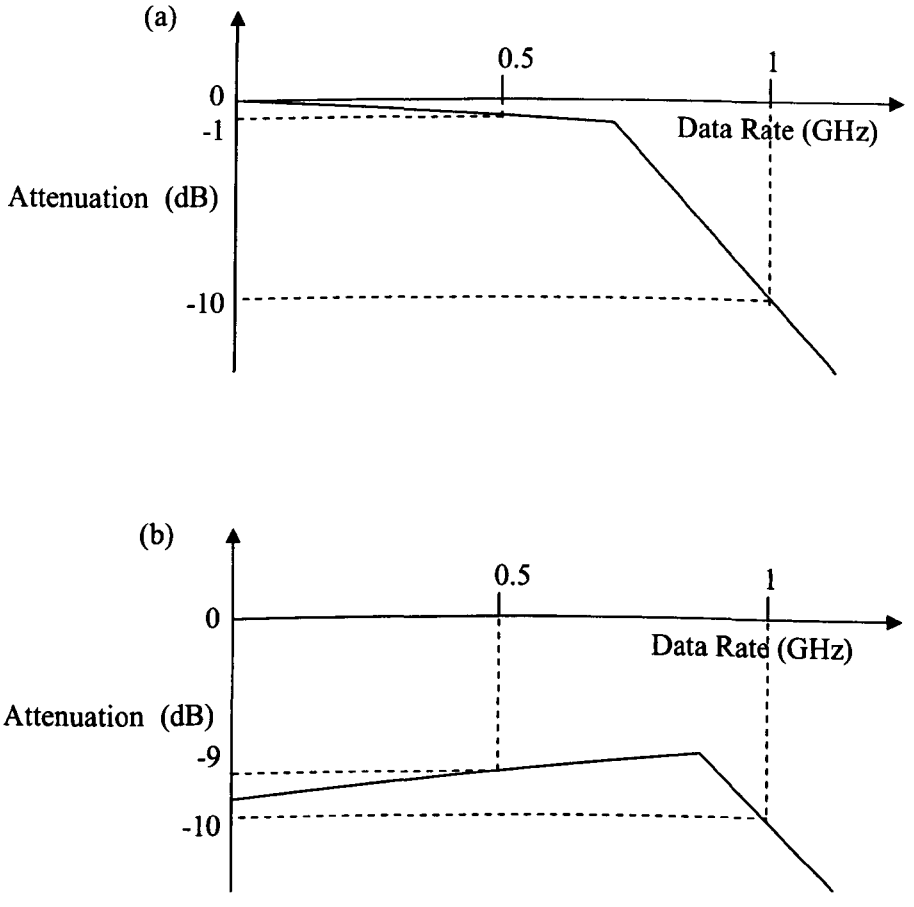


*Figure 2.10 – Attenuation curves of transmission line, channel attenuation (a), result of de-emphasis (b)*

It can be seen from Figure 2.10 that the difference in attenuation between the 0.5GHz signal and the 1GHz signal has been greatly reduced by using de-emphasis. This form of equalization has a profound effect on increasing signal integrity and is widely used in modern communication systems.

Pre-emphasis is essentially the opposite of de-emphasis wherein instead of attenuating low frequencies the high frequencies are boosted to compensate for the high frequency losses of the channel. Figure 2.11 shows how pre-emphasis can be used to increase the bandwidth of the transmission line. This makes for a more efficient use of power, by not wasting power by attenuating the low frequencies, however this technique is not widely adopted as the transistors need to be overdriven during high frequency cycles.

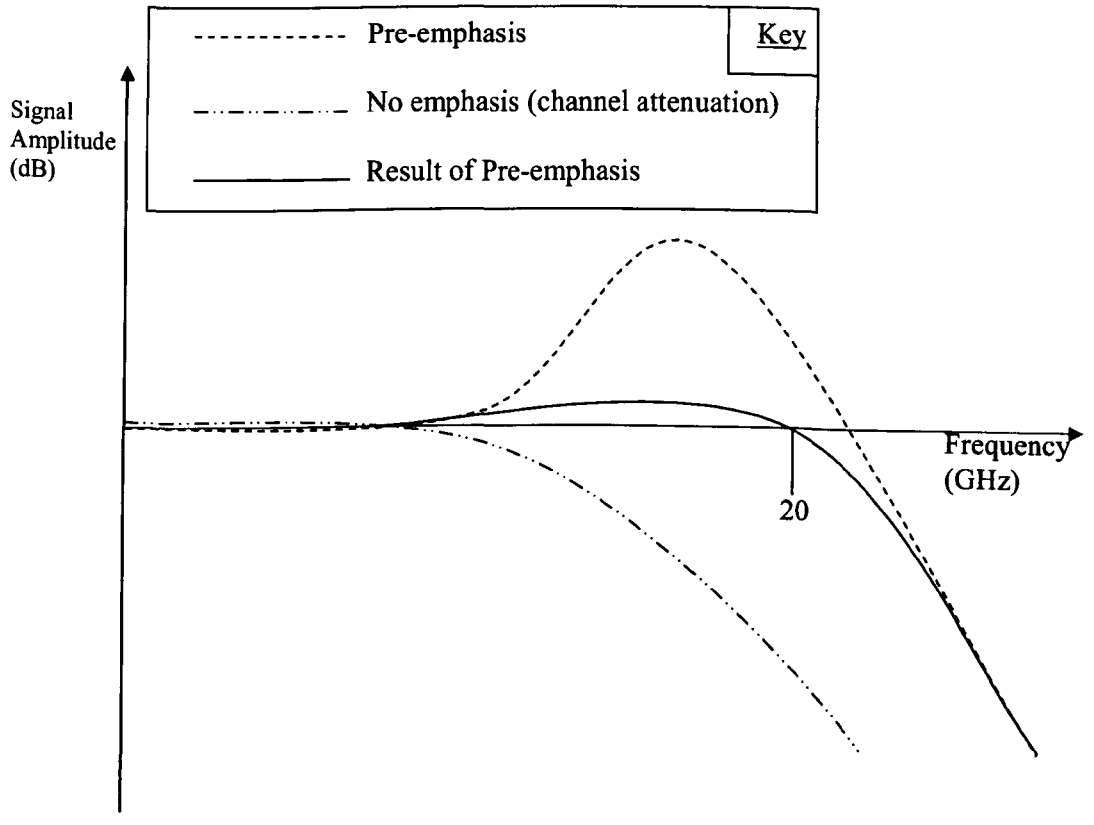


*Figure 2.11 –Pre-emphasis*

The next chapter will review various line driver architectures with the aim to identify which architecture is best suited to the high-speed low-voltage environment.

## 2.3 References


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# Chapter 3

# Critical Review of Line Driver Topologies

## 3.1 Introduction

In this chapter, four of the most frequently used line drivers will be presented and critically analysed. This will provide a sound knowledge base of existing line driver architectures to enable the development of two new line drivers that are presented in Chapter 4.

To ensure an accurate comparison can be made, each circuit in this chapter will be tested under the same conditions. The input signal will be a differential signal in all cases, generated by two voltage pulse generators in anti-phase. A differential signal is used to increase the resilience of the driver to noise by only amplifying the voltage difference between the two signals, as explained in Chapter 2. Any noise from previous stages will appear equally on both inputs and therefore the difference between the outputs will remain essentially the same. Similarly the drivers will all use a differential output stage, which will protect the transmitted signal from noise such as electromagnetic interference applied to the transmission line by using the same principle [1]. Also all circuits will be simulated under ideal conditions where all parasitics are ignored, and it will be assumed that the driver will have perfect impedance match with the transmission line with zero capacitance load.

In addition all circuits presented in this chapter are tested to determine how well they each conform to the respective governing standards, which are summarised in Table 3.1.

| Parameter | CML | LVPECL | LVDS |
|---|---|---|---|
| $V_{OH}$ | VDD | 2.3V | 1.425 |
| $V_{OL}$ | VDD – 0.8V | 1.6V | 1.075 |
| $V_{OD}$ | 800mV | 700mV | 350mV |
| $V_{CM}$ | VDD – 0.4V | 1.95V | 1.25V |
| $R_T$ | 50Ω | 50Ω | 100Ω |

*Table 3.1 – Standard Specifications*

Key:

VDD = Positive Power Supply

CML = Current Mode Logic

LVPECL = Low-Voltage Positive Emitter Coupled Logic

LVDS = Low-Voltage Differential Signalling

$V_{OH}$ = Output Voltage (High)

$V_{OL}$ = Output Voltage (Low)

$V_{OD}$ = Differential Output Voltage Swing

$V_{CM}$ = Common Mode Voltage

RT = Termination Resistance

CML is a style of interface but for the purpose of this comparison the CML standard is taken from the requirements of Clause 47 of the IEEE 802.3 standard which defines the physical layer of the XAUI interface [2]. LVPECL's standard can be found in TIA's ANSI/TIA/EIA-613 [3]. Finally the LVDS standard can be found in ANSI/TIA/EIA-644-A [4]. It should be noted that all of the standards, except for CML, shown in Table 3.1 require power supply voltage levels above 1.6V. Therefore these circuits will be simulated in Cadence Capture using the IBM T68A 130nm CMOS transistor which is rated to work at these voltage levels.

## 3.2 Device Parameters

To determine the primary design equations for the various line driver topologies it is necessary to extract the main device parameters from the simulation model, namely:

- $V_T$, threshold voltage.
- $I_D$ - $V_{DS}$ curves.
- $\lambda$, channel length modulation parameter.
- $f_T$, transition frequency.
- $\mu nCox$, a product of electron mobility and capacitance of oxide per unit length.

The following section will put the IBM model under various tests designed to extract the above mentioned parameters.

The threshold voltage can be obtained by applying an increasing DC voltage between gate and source of a MOSFET and observing when the transistor conducts significantly [5], an easy method to ensure that the results are consistent is to use a linear extrapolation back to the zero crossing of the y axes. Figure 3.1 shows the circuit and Figure 3.2 shows the results of the $V_T$ test. Looking at the curve in Figure 3.2 it can be seen that $I_D$ increases significantly at $V_{GS} = 0.45V$, hence $V_T = 0.45V$.

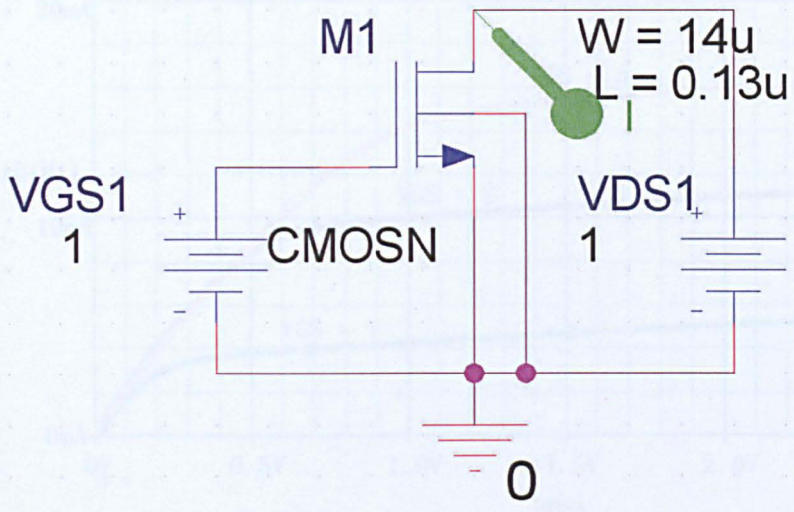


*Figure 3.1 – Test circuit to find $V_T$*

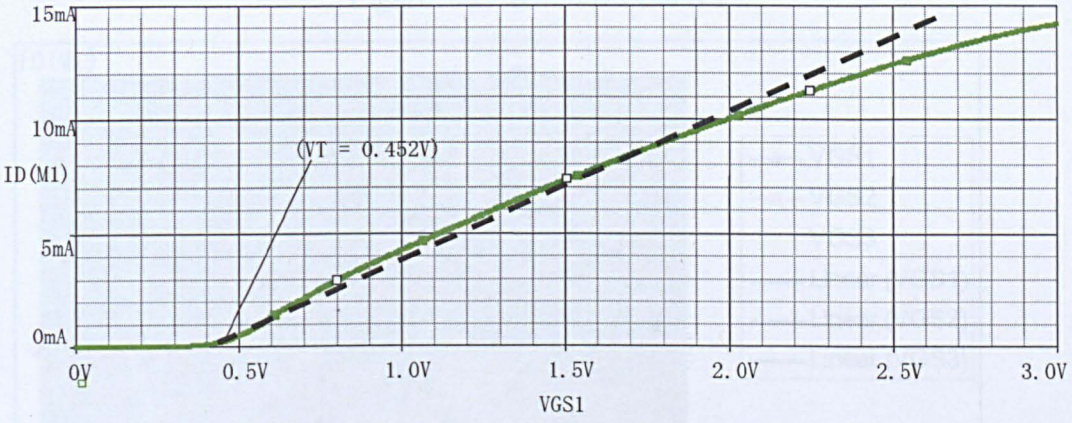


*Figure 3.2 –Results of $V_T$ Test*

Using the same circuit in Figure 3.1 $I_D \sim V_{DS}$ curves can be obtained by running a parametric $V_{GS}$ with a DC sweep of $V_{DS}$ [6]. The results obtained are shown in Figure 3.3. Normally the λ parameter can be obtained by extrapolating the (almost) horizontal area of the curve. However, one effect of such short channel MOSFETs is that the extrapolations no longer converge on a single voltage, as shown in Figure 3.4.

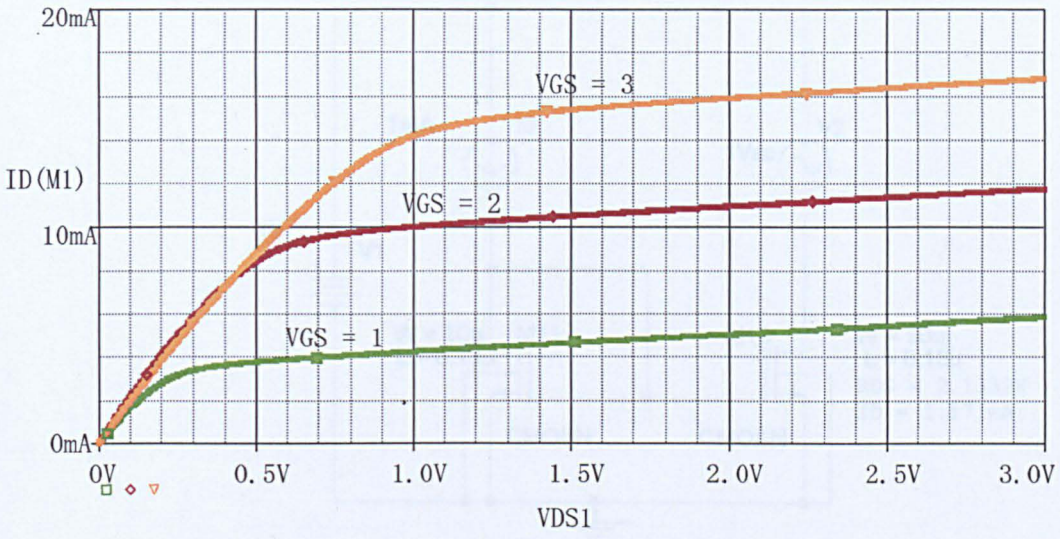


*Figure 3.3 – ID – VDS Curves*

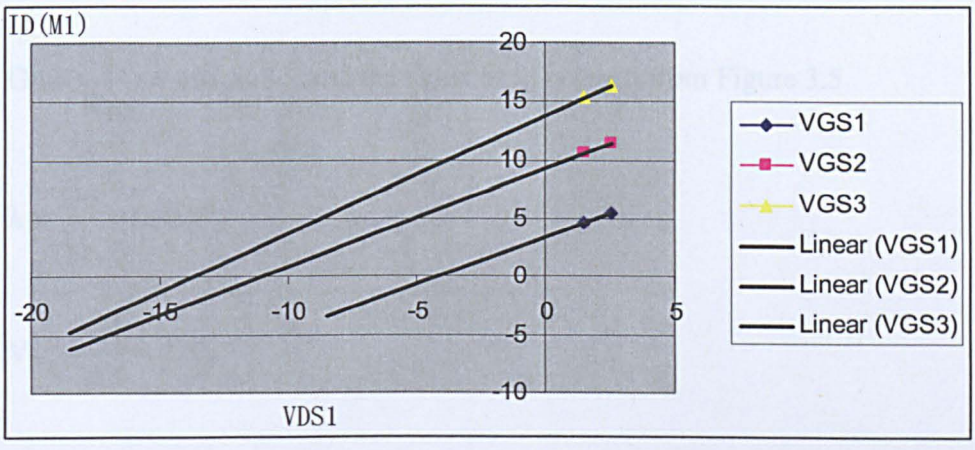


*Figure 3.4 – The effect of channel length modulation on the Early Voltage*

From Figure 3.4 it can be seen that the early voltage ($V_A$) [7] changes with different levels of $V_{GS}$. Therefore $\lambda$ needs to be calculated by different means. From device physics we know that $Go \approx \lambda \times I_D$ [8], where Go = output conductance, therefore using a simple current mirror, Figure 3.2.5, the output conductance (Go) can be calculated for a known drain current ($I_D$).

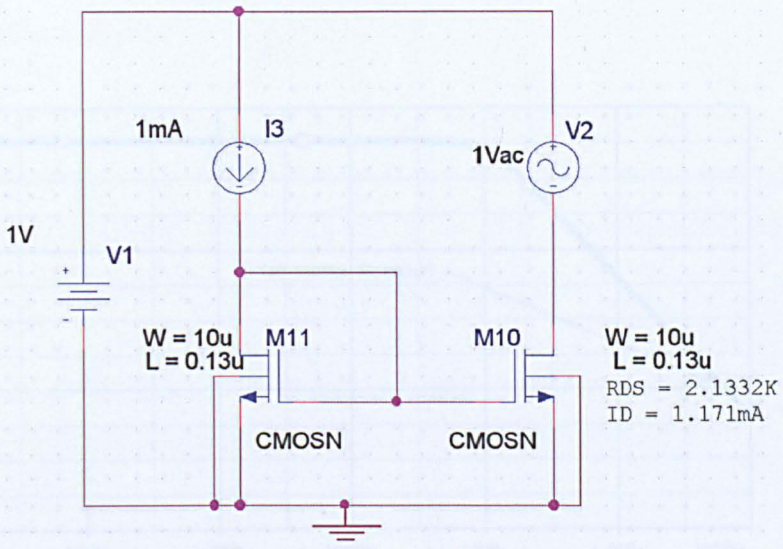


*Figure 3.5 – Simple Current Mirror to calculate $R_{DS}$*

$$Go = \frac{1}{R_{DS}} = 468.8uS \quad \text{,and the value of } I_D \text{ is taken from Figure 3.5} \tag{3.1}$$

$$\lambda = \frac{Go}{I_D} = 0.4V^{-1} \tag{3.2}$$

$$V_A = \frac{1}{0.4} = 2.5V$$

The $f_T$ is a measure of the maximum useful frequency of the transistor when used as an amplifier [8], the $f_T$ of the MOSFET is found by using the circuit in Figure 3.6. The impedance of the drain is measured in an AC sweep and $f_T$ is the frequency where the impedance is unity (0dB), Figure 3.7, measured to be 40THz.

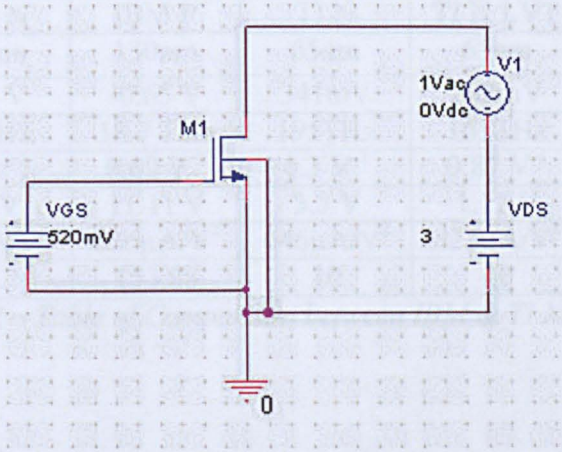


*Figure 3.6 - $f_T$ Schematic*

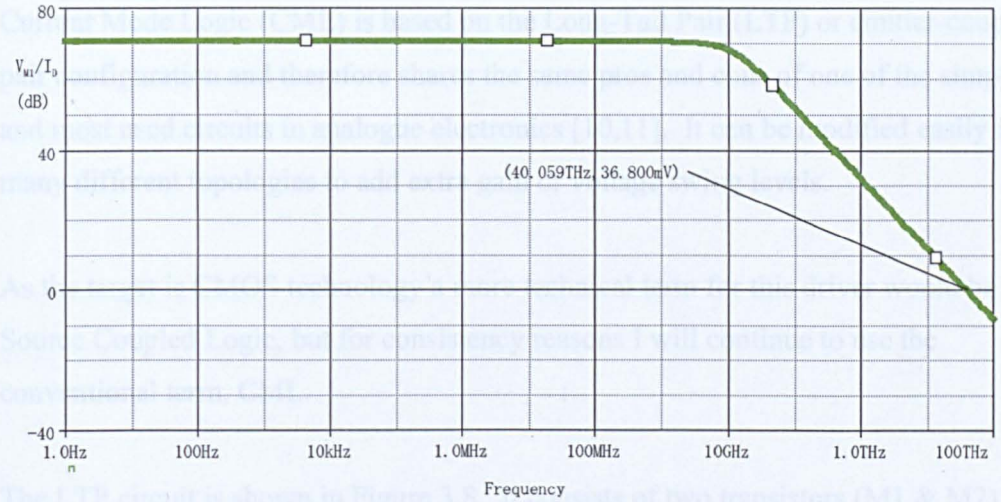


*Figure 3.7 – Transition Frequency (FT)*

And finally, the μxCox parameter can be found by calculation [9], using the equation:

$$I_D = \frac{\mu xCox}{2}\frac{W}{L}(V_{GS} - V_T)^2 \tag{3.3}$$

$\therefore$ where μx = μn or μp (nMOS or pMOS)

$$\mu xCox = \frac{2I_D}{\frac{W}{L}(V_{GS} - V_T)^2} \tag{3.4}$$

These parameters were also found for the P-channel and N-channel IBM transistors as well as the TI transistors, two of which are the standard 65nm transistor, and two special transistors with a low $V_T$. These results are shown in Table 3.2 for comparison and reference purposes.

| Parameter | IBM N | IBM P | TI N | TI N LVT | TI P | TI P LVT |
|---|---|---|---|---|---|---|
| L(min) | 130nm | 130nm | 65nm | 65nm | 65nm | 65nm |
| $V_T$ | 0.45 V | -0.65 V | 341mV | 292mV | -375mV | -312mV |
| $f_T$ | 40 THZ | 18.7 THz | 195THz | 163THz | 96.5THz | 95THz |
| λ | 0.4 $V^{-1}$ | 0.09 $V^{-1}$ | 0.3 $V^{-1}$ | 0.87 $V^{-1}$ | 0.93 $V^{-1}$ | 0.44 $V^{-1}$ |
| $V_A$ | 2.5 V | 11.11 V | 3.3 V | 1.15 V | 1.1 V | 2.27 V |
| μxCox | 186μA/$V^2$ | 226μA/$V^2$ | 646μA/$V^2$ | 823μA/$V^2$ | 554μA/$V^2$ | 476μA/$V^2$ |
| W/L | 107.7 | 153.85 | 10 | 10 | 20 | 20 |

*Table 3.2 – Table of Comparison between IBM & TI MOSFETS*

## 3.3 Current Mode Logic

Current Mode Logic (CML) is based on the Long-Tail Pair (LTP) or emitter-coupled pair configuration and therefore shares the same pros and cons of one of the simplest and most used circuits in analogue electronics [10,11]. It can be modified easily into many different topologies to add extra gain or voltage swing levels.

As the target is CMOS technology a more technical term for this driver would be Source Coupled Logic, but for consistency reasons I will continue to use the conventional term, CML.

The LTP circuit is shown in Figure 3.8. It consists of two transistors (M1 & M2) each loaded by a resistor (RL1 & RL2) on the drain. Another transistor (M3) is used to provide the bias currents for the transistors.

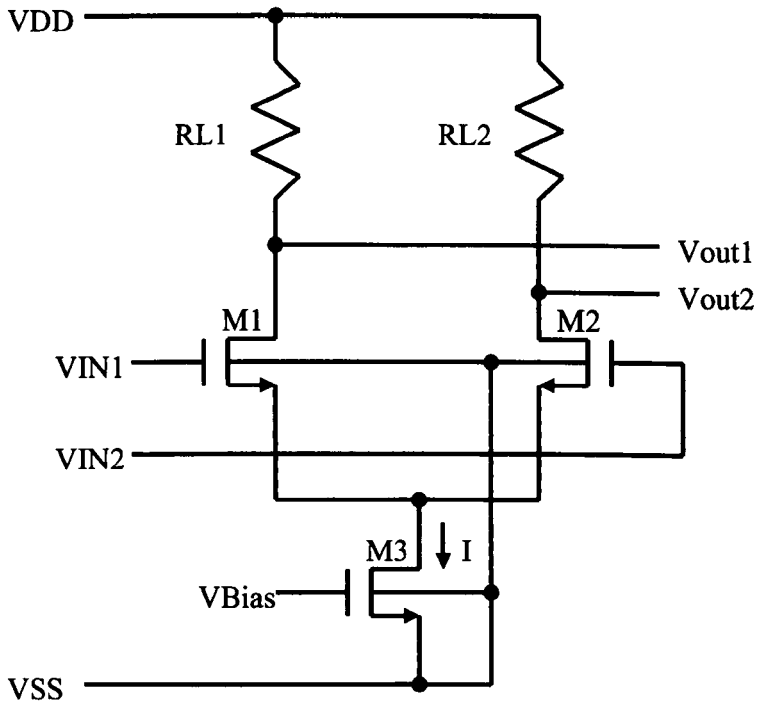


*Figure 3.8 – CML driver configuration*

The drain of M3 provides a high impedance node for the signal and due to the input being of a differential nature only one half of the long-tail pair will be active making the equivalent circuit a common source amplifier where:

$$Vout = -gmVin(RDS//RL) \tag{3.5}$$

$$Rout = \frac{Vout}{Iout} = RDS//RL \tag{3.6}$$

$$Rin = \infty \quad \& \quad Ai = \infty$$

To reduce the complexity of the schematic RL1 and RL2 represent termination with an ideal matched transmission line. The value of RL is fixed at 50Ω to provide impedance matching to the transmission line. This is one of the obvious drawbacks as this reduces the available voltage output swing.

The standard of CML, taken from Clause 47 of the IEEE 802.3 standard, states the differential output swing is $800mV_{P-P}$ and to relate to the next type of driver which is called the 'Low Voltage Positive Emitter Coupled Logic' (LVPECL) VDD will be set at 3.5V. The following equations define the parameters of I, M1, M2 of Figure 3.3.1.

Vout=VDD-0.8V = 3.5- 0.8 = 2.7V

$$AV = -gmRL' \quad \text{Where:} \quad (3.7)$$

AV = Votage Gain

RL' = RDS//RL

K = μnCox

substuting gm gives

$$= 2\sqrt{\frac{K}{2}\frac{W}{L}ID} \times RL' \quad (3.8)$$

rearranging for $\frac{W}{L}$ gives

$$AV = \sqrt{\frac{W}{L}} \times 2\sqrt{\frac{K}{2}ID} \times RL' \quad (3.9)$$

$$\frac{AV}{2\sqrt{\frac{K}{2}ID} \times RL'} = \sqrt{\frac{W}{L}} \quad (3.10)$$

$$\frac{W}{L} = \left[\frac{AV(RL + R_{DS})}{2\sqrt{\frac{K}{2}ID} \times RL \times R_{DS}}\right]^2 \quad (3.11)$$

$$= \left[\frac{0.9(50+75)}{2\times 50\times 75\times\sqrt{80\times 10^{-6}\times 15\times 10^{-3}}}\right]^2$$

$$= 187.5$$

$$\underline{\underline{W_{1\&2} = 187.5 \times L = 25\mu m}}$$

$$\underline{\underline{I = 15mA}}$$

The current, I, is set up using a simple current mirror. The schematic used in testing is show in Figure 3.9. To minimise power consumed by the current mirror the width of the current source transistor M4 has been scaled down by a factor of 27, this reduces the current flowing through M4 to 556μA from 15mA. The length of transistors M3 & M4 are increased to 0.5μm to improve the stability of the current mirror, in turn improving the common mode rejection ratio (CMRR) of the long tail pair.

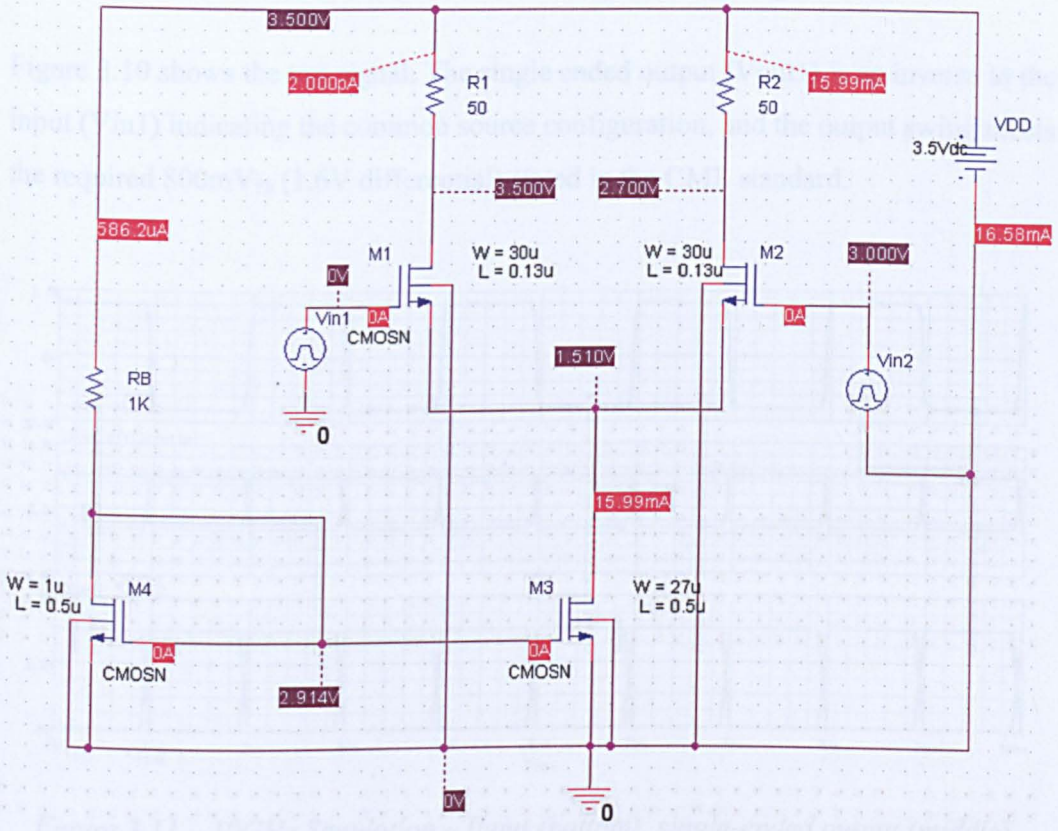


*Figure 3.9 – CML Simulator Schematicwith DC Annotation*

The first simulation will be a 1kHz test signal, shown in Figure 3.10. The purpose of this slow speed test is to ensure the circuit is operating at the required conditions before a high speed signal is applied.

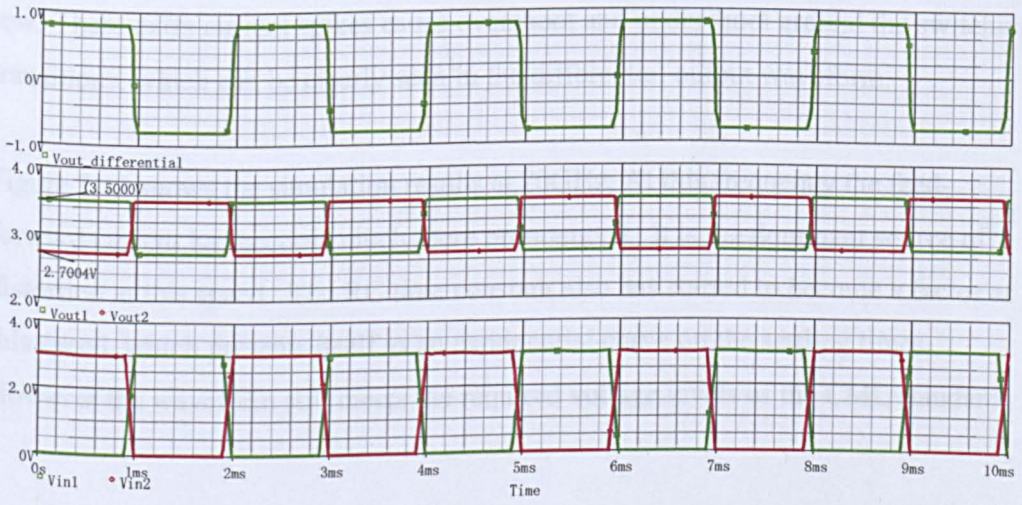


*Figure 3.10 - 1kHz Test Signal – Input (bottom), single-ended output (middle), differential output (top)*

Figure 3.10 shows the test signal. The single ended output (Vout1) is an inverse to the input (Vin1) indicating the common source configuration, and the output swing meets the required $800mV_{Pk}$ (1.6V differential) stated in the CML standard.

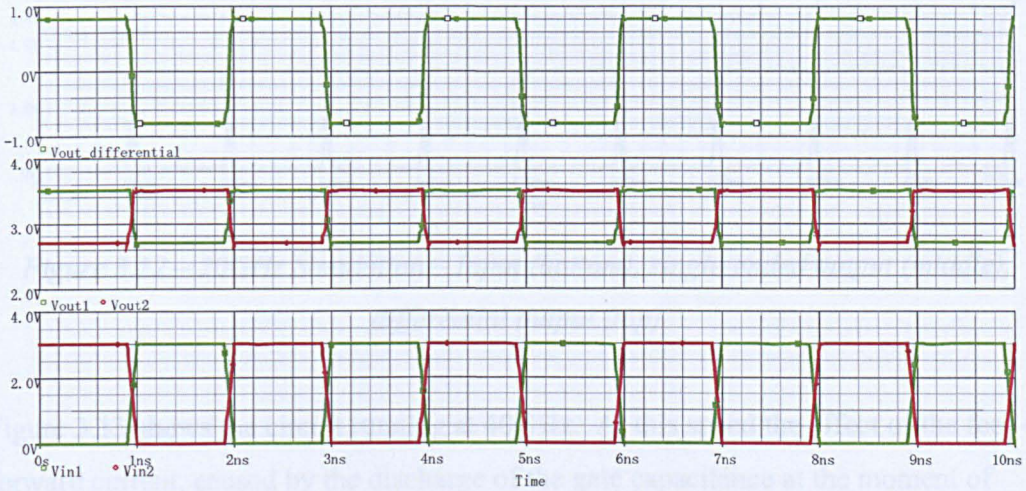


*Figure 3.11 – 10GHz Simulation – Input (bottom), single-ended output (middle), differential output (top)*

Figure 3.11 shows that CML will still work well at 10GHz because the output signal swing still meets the $800mV_{Pk}$ standard. There is a slight amount of feed-forward current which is produced by the parasitic capacitances, which prevents the transistor from discharging fast enough at the point where the input signal switches from high to low. These extra current spikes cause overshoot and undershoot around the switching transitions, which can be clearly seen in the differential output waveform.

Figure 3.12 shows the simulation results at 20GHz. At this frequency the feed-forward current has become much more pronounced. It is the dominant source of distortion at this speed. The RC time constant also has started to become a factor at this speed, which presents itself as an exponential curve on the settling times. However the waveform still meets the required voltage levels of the CML standard.

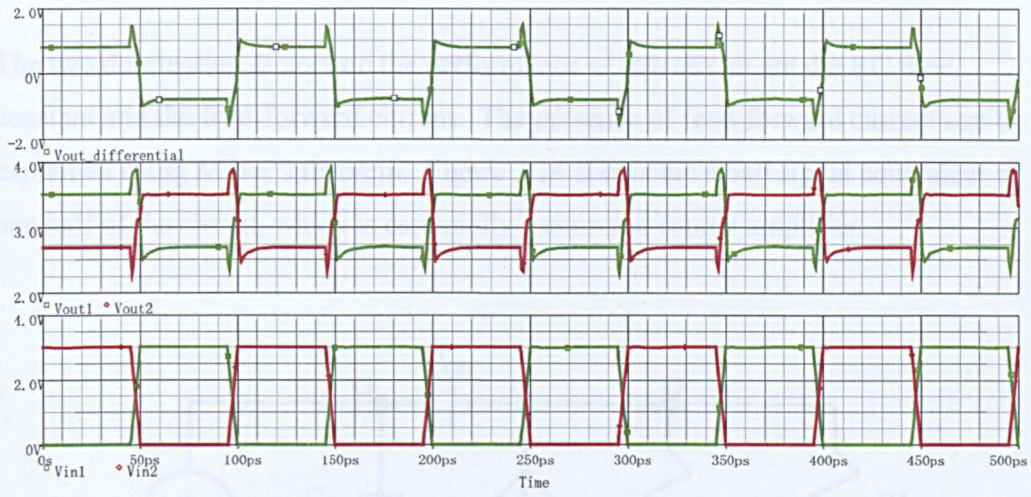


*Figure 3.12 – 20GHz Simulation – Input (bottom), single-ended output (middle), differential output (top)*

Figure 3.13 shows the circuit running at 40GHz. At this speed the effect of the feed-forward current, caused by the discharge of the gate capacitance at the moment of switching, coupled with the RC time constant has pushed the output voltages out of the standard mode of operation; this could cause the receiver to reject the signal. At some points the differential voltage reaches 2V which is over double the specified limit. Due to the feed-forward current distortion presented on the output voltage levels, the circuit no longer conforms to the defined standard and therefore is deemed not suitable for operation at 40GHz.

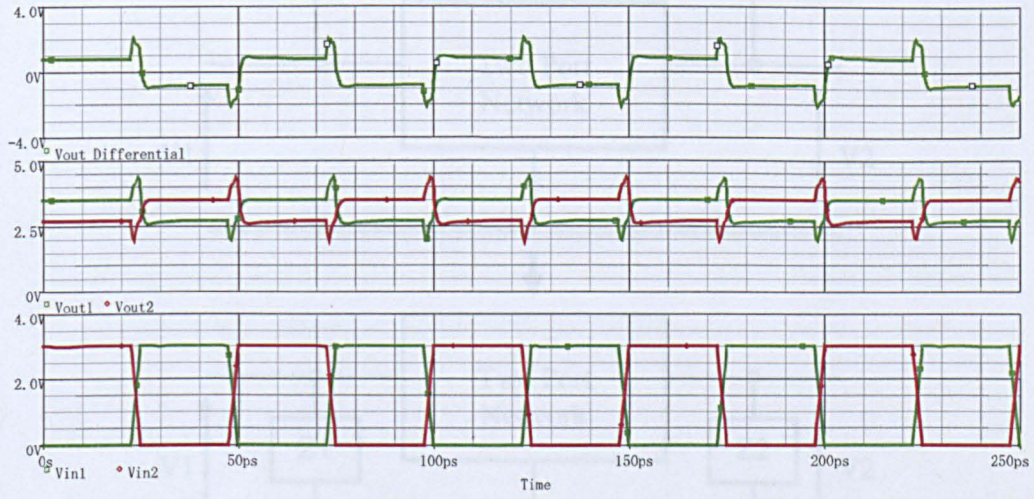


*Figure 3.13 – 40GHz Simulation – Input (bottom), single-ended output (middle), differential output (top)*

The two dominating factors on the performance of this circuit are the RC time constant and the feed-forward current. The presence of feed-forward current can be explained using Miller's theorem. Figure 3.14 shows the small signal equivalent of one half of the circuit, which is essentially a common source amplifier.

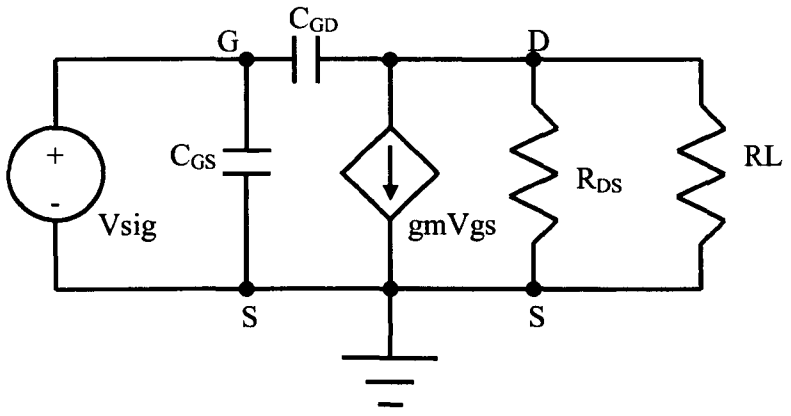


*Figure 3.14 – Small Signal Analysis [12]*

Miller's theorem states that impedance, Z, connected across the input and output of a linear two port network will have an equivalent circuit of separate input and output impedances, Z1 and Z2, [13]. This is better illustrated in Figure 3.15

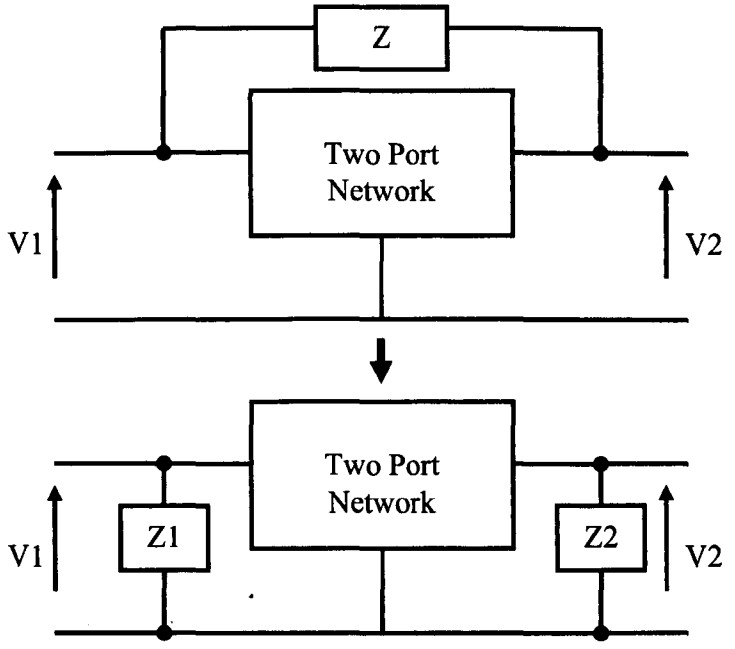


*Figure 3.15 – Miller's Theorem*

$$Z1 = \frac{Z}{1-A} \text{ and } Z2 = \frac{Z}{1-\frac{1}{A}} \text{ where A = Gain} \tag{3.12}$$

Looking back to Figure 3.14 it can be seen that capacitor $C_{GD}$ is connected between the Gate (input) and Drain (output), therefore Miller's theorem can be applied. Z1 and Z2 can be calculated using the following equations:

$$C_{GD} = CGDO(W_{eff})$$
$$= (3.98E-10)(30E-6)$$
$$= 0.012fF$$

Where:
CGDO = capacitance per unit
$W_{eff}$ = effective transistor width
(both taken from transistor model) (3.13)

$$C1 = C_{GD}(1 - gm(RL // R_{DS})) \tag{3.14}$$

$$= 0.012\times10^{-12}\left(1-\left(2\sqrt{\frac{K}{2}\frac{W}{L}I_D}\right)\left(\frac{50\times74}{50+74}\right)\right) = 0.012\times10^{-12}(1-(0.03437\times30))$$

$$= \underline{\underline{0.0004fF}}$$

and

$$C2 = C_{GD}\left(1-\frac{1}{gm(RL // R_{DS})}\right)$$

$$= 0.012\times10^{-12}\left(1-\frac{1}{\left(2\sqrt{\frac{K}{2}\frac{W}{L}I_D}\right)\left(\frac{50\times74}{50+74}\right)}\right) = 0.012\times10^{-12}\left(1+\frac{1}{(0.03437)(30)}\right)$$

$$= \underline{\underline{0.024fF}}$$

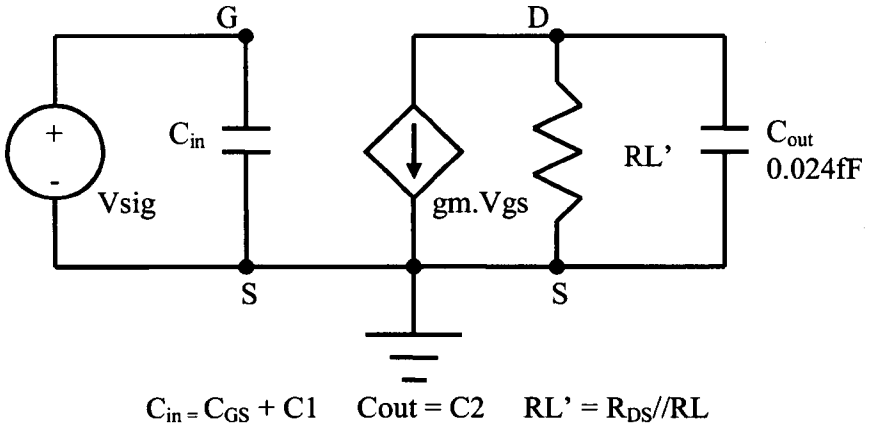


*Figure 3.16 – Small Signal Analysis with Miller's Theorem Applied*

Figure 3.16 now shows the appearance of a capacitor on the load which is the dominant source of the RC time constant and the feed-forward current. This model is just used as a graphical representation. Due to the very high frequency used in simulation a much larger, more complicated model is needed to simulate an equivalent circuit. Due to the complexity of the model another way to show the effect of $C_{GD}$ on the feed-forward current is to increase $C_{GD}$ by adding a capacitor from the Gate to the Drain. Figure 3.17 shows the circuit used to obtain the results by multiplying the capacitor $C_{GD}$ by the factor n and recording the amount of feedthrough current shown in Figure 3.18, which shows the graphical representation of the results.

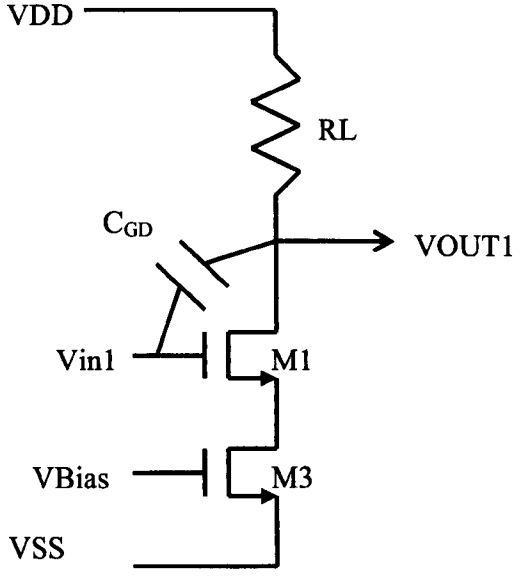


*Figure 3.17 – Feed-Forward Current Test Circuit*

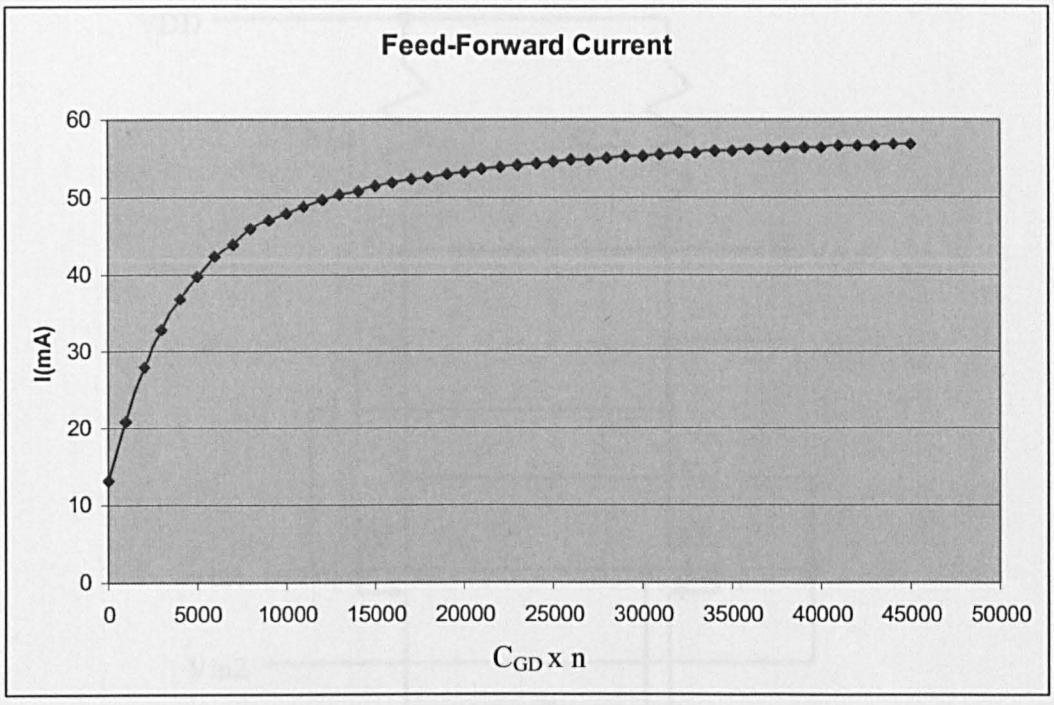


*Figure 3.18 – Graph of Feed-Forward Current vs. $C_{GD}$*

The results clearly show a correlation between $C_{GD}$ and the amount of feed-forward current.

A common technique employed in amplifier design is capacitance neutralisation [14]. The schematic of the 'neutralised' circuit is shown in Figure 3.19. The two capacitors, C1 and C2, counteract the Miller capacitance by providing equal but opposite currents to counteract the flow of current leaking through the gate of the transistor.

The design values for the circuit in Figure 3.19 are:

- VDD = 3.5V
- VSS = 0V (ground)
- RL1 = RL2 = 50Ω
- Vin1 = $3V_{p\text{-}p}$, 0° phase, square wave
- Vin2 = $3V_{p\text{-}p}$, 180° phase, square wave

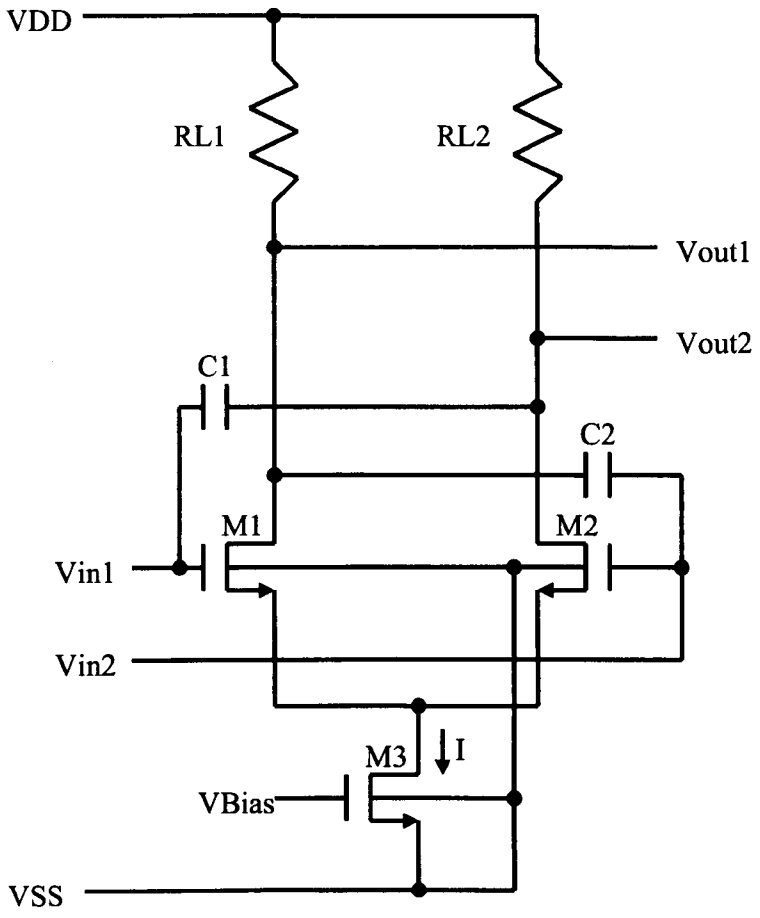


*Figure 3.19 – CML with Capacitive Neutralisation [15]*

This circuit was then converted to a 'Capture schematic', Figure 3.20, for simulation using the same design values as CML. A comparison of results can be found in Figure 3.21. Comparing CML with and without this neutralisation technique indicates a noticeable improvement in the feed-forward current when capacitance neutralisation is employed.

Capacitors C1 and C2 can be matched easier by using identical devices[15], where their Gate and Source will be connected to the input and the Drain will connect to the opposite output, as shown in Figure 3.20. This will not provide an exact match due to different biasing but will be very accurate.

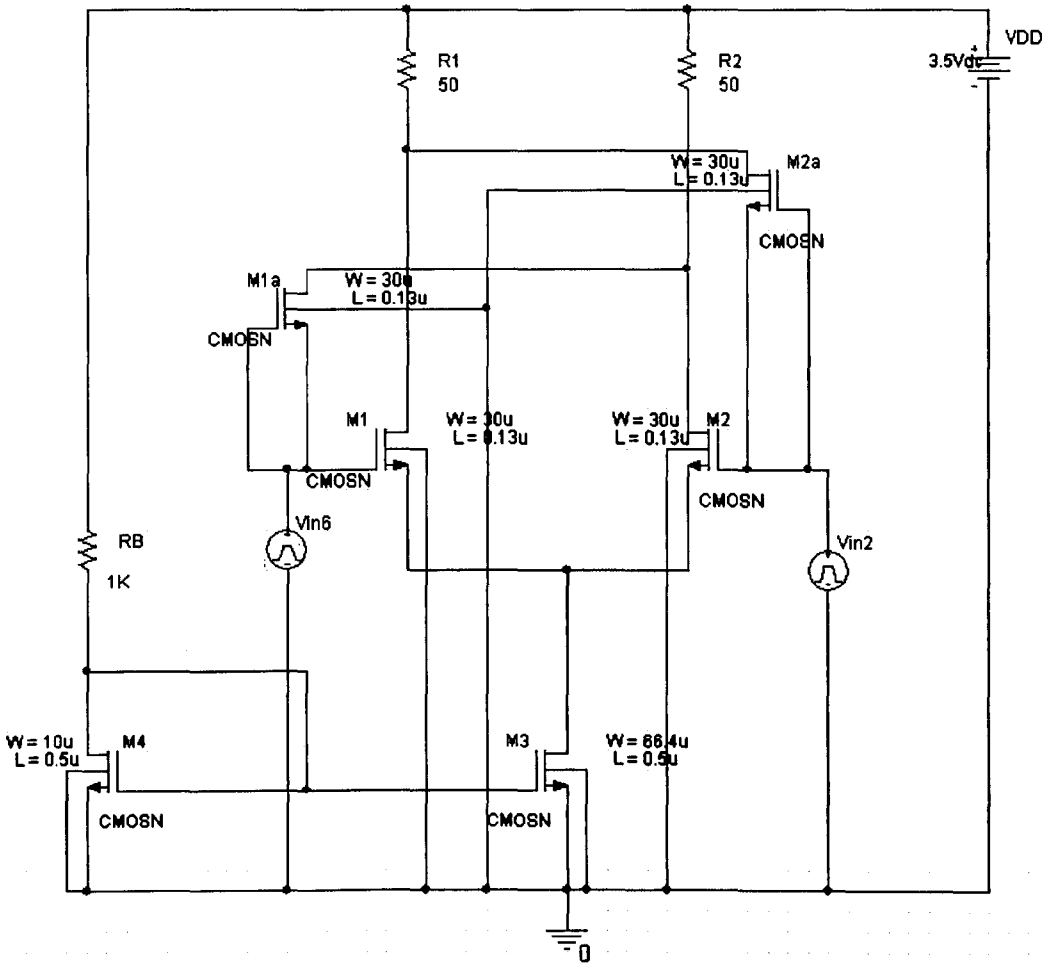


*Figure 3.20 – Neutralised CML Schematic*

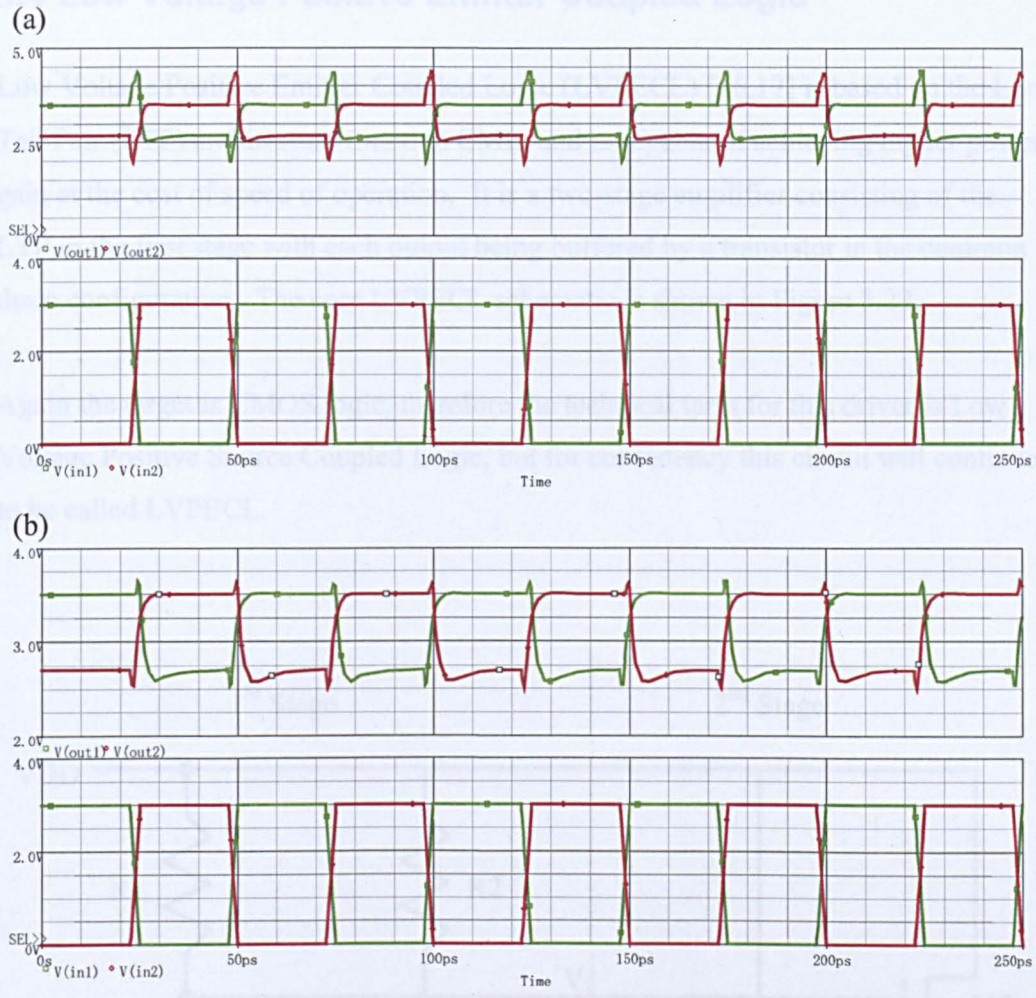


*Figure 3.21 – CML without Capacitive Neutralization (a), with Capacitive Neutralization (b)*

The chip area of the un-neutralised CML was 46 $um^2$ and power consumption was 64.0mW. By comparison the neutralised CML chip area increased to 61.6 $um^2$, and the power consumption remained unchanged. The neutralisation capacitors have dramatically reduced the signal spikes caused by feed-forward current, although not completely due to the slight biasing differences between the original transistor and neutralisation transistor causing a slight mismatch in capacitance. The drawback of adding the neutralisation capacitors adds to the load capacitance that the transistor needs to drive and therefore reducing the edge rate.

## 3.4 Low Voltage Positive Emitter Coupled Logic

Low Voltage Positive Emitter Coupled Logic (LVPECL) [16,17] is based on the Long Tail Pair (LTP) architecture found in CML, and is capable of achieving higher power gain at the cost of speed of operation. It is a two-stage amplifier consisting of the LTP in the first stage with each output being buffered by a transistor in the common drain configuration. The core LVPECL schematic is shown in Figure 3.22.

Again the target is CMOS logic, therefore the technical term for this driver is Low Voltage Positive Source Coupled Logic, but for consistency this circuit will continue to be called LVPECL.

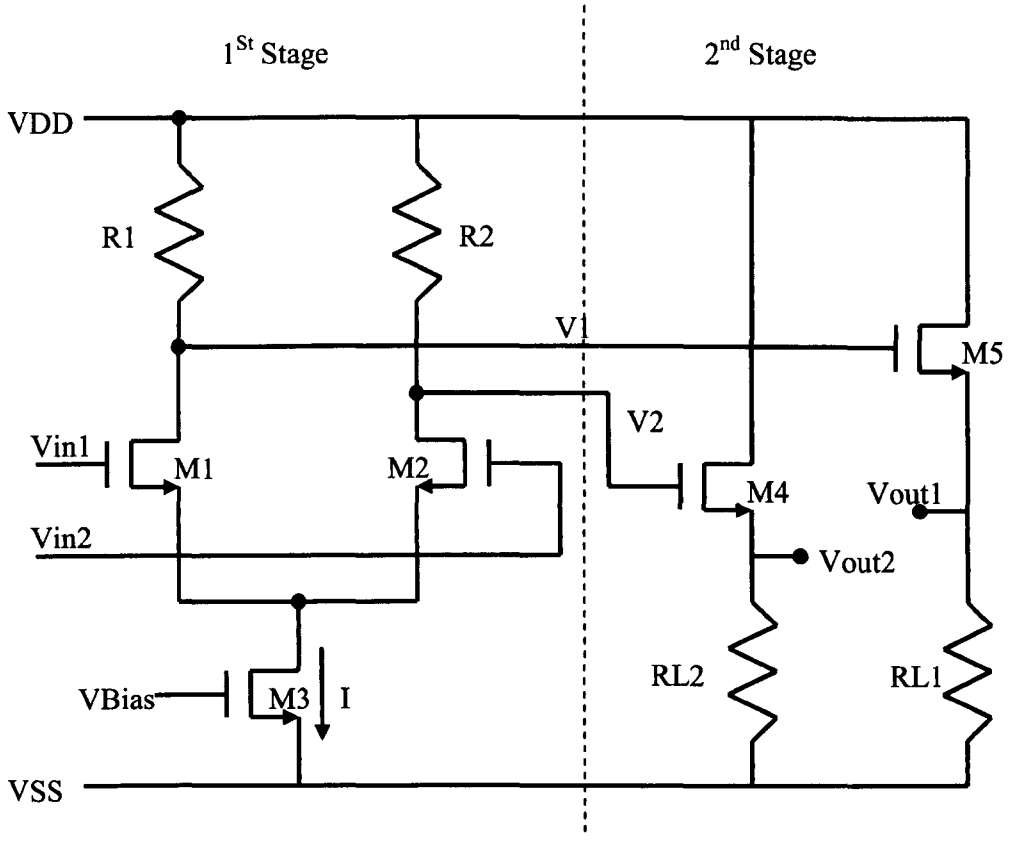


*Figure 3.22 – LVPECL Schematic*

The common drain amplifier, also known as the source follower, provides a high input impedance and low output impedance unity voltage gain, Av=1, with a large current gain. The first stage of the amplifier behaves exactly the same as in the CML driver. However this time the outputs are tailored to drive the second stage common drain amplifier rather than a transmission line directly as in the CML. As the common drain amplifier acts as a buffer, this means that resistors R1 and R2 can now be higher than 50Ω and they will not affect the output impedance of the circuit, therefore the first stage can now be designed more efficiently.

The second stage of the amplifier, the source follower, has an open-loop voltage gain given by

$$Avo = \frac{Ro}{Ro + \frac{1}{gm}} \tag{3.15}$$

where Avo is the open-circuit voltage gain, Ro is the unloaded output resistance and gm is the transconductance of the output stage transistors[12].

Usually Ro >> 1/gm and so the source follows the gate, hence the name source follower. However, due to the short length of the transistor used Ro is going to be a lot smaller than usual, perhaps 10s of Ohms instead of 100s of kOhms, hence the voltage gain will be significantly less than 1 so the full equation must be used to accurately model the source follower.

When the load is added the voltage gain becomes

$$Av = \frac{RL // Ro}{(RL // Ro) + \frac{1}{gm}} \tag{3.16}$$

where Av is the voltage gain

According to the standards, shown in Table 3.1 for LVPECL, $V_{OH}$ = 2.3V and $V_{OL}$ = 1.6V. The calculations below show the design parameters needed to achieve these standards.

$$\frac{Vout}{Vin} = \frac{RL // Ro}{(RL // Ro) + \frac{1}{gm}} \qquad \text{Let } RL//Ro = RL' \text{ and } gm = 2\sqrt{\frac{K}{2}\frac{W_5}{L}ID} \tag{3.17}$$

$$= \frac{RL'}{RL' + \frac{1}{2\sqrt{\frac{K}{2}\frac{W_5}{L}ID}}} \tag{3.18}$$

$$\frac{Av}{1} = \frac{RL'}{RL' + \frac{1}{\sqrt{\frac{W_5}{L}}} \bullet \frac{1}{\sqrt{2K \bullet ID}}} \tag{3.19}$$

Rearrange for RL'

$$RL' = Av \bullet RL' + Av \bullet \sqrt{\frac{L}{W_5}} \bullet \frac{1}{\sqrt{2K \bullet ID}} \tag{3.20}$$

Divide both sides by RL'+AV

$$RL'(1 - AV) = Av \bullet \sqrt{\frac{L}{W_5}} \bullet \frac{1}{\sqrt{2K \bullet ID}} \tag{3.21}$$

Rearrange to find $W_5$

$$\sqrt{\frac{L}{W_5}} = \frac{RL'(1 - Av)}{AV \bullet \frac{1}{\sqrt{2K \bullet ID}}} \tag{3.22}$$

$$\sqrt{\frac{L}{W_5}} = \frac{RL'(1 - Av)\left(\sqrt{2K \bullet ID}\right)}{Av} \tag{3.23}$$

$$\sqrt{\frac{W_5}{L}} = \frac{Av}{RL'(1-Av)\left(\sqrt{2K \bullet ID}\right)} \tag{3.23}$$

$$= \frac{Av(RL+Ro)}{(RL \times Ro)(1-Av)\left(\sqrt{2K \bullet ID}\right)} \tag{3.24}$$

Where:

$Av = 0.66$

$RL = 50$

$Ro = 26$

$K = 160 \times 10^{-6}$

$ID = 50 \times 10^{-3}$

$$\sqrt{\frac{L}{W_5}} = \frac{0.66(50+26)}{50 \times 26(1-0.66) \bullet \left(\sqrt{320 \times 10^{-6} \times 50 \times 10^{-3}}\right)} = 28.32$$

$$\frac{W_5}{L} = 805$$

$L = 0.13\mu m \therefore W_5 = W_6 = \underline{\underline{105\mu m}}$

Now the output voltages need to be considered to ensure that the LVPECL stand are met.

$$V_{OL} = Vin = \frac{Vout}{\left(\frac{RL//Ro}{(RL//Ro)+\frac{1}{gm}}\right)} = \frac{Vout}{\left(\frac{RL//Ro}{(Rl//Ro)+\frac{1}{\left[2\sqrt{\frac{K}{2}\frac{W_5}{L}I_D}\right]}}\right)} = V2 \tag{3.25}$$

$$V2 = \frac{1.6}{\left(\frac{17.1}{17.1+\frac{1}{2\sqrt{80E-6 \times 805 \times 50E-3}}}\right)}$$

$V2 = 2.42V$

Once the parameters for the second stage have been calculated the next stage is to design the first stage to provide V1=VDD and V2 = 2.42V

Using equation 3.11 from the previous CML circuit yields

$$\frac{W_1}{L} = \left[ \frac{Av(RL + R_{DS})}{2\sqrt{\frac{K}{2} ID \times RL \times R_{DS}}} \right]^2 \qquad (3.26)$$

$$= \left[ \frac{0.81(180+300)}{2\times 180\times 300\times \sqrt{80\times 10^{-6}\times 6\times 10^{-3}}} \right]^2$$

$$= 127$$

$$W_1 = W_2 = 4\mu m$$

Now all the parameters have been defined a simple current mirror circuit is added (consisting of RB, M4 and M5) to bias the LTP. The schematic for testing is shown in Figure 3.23.

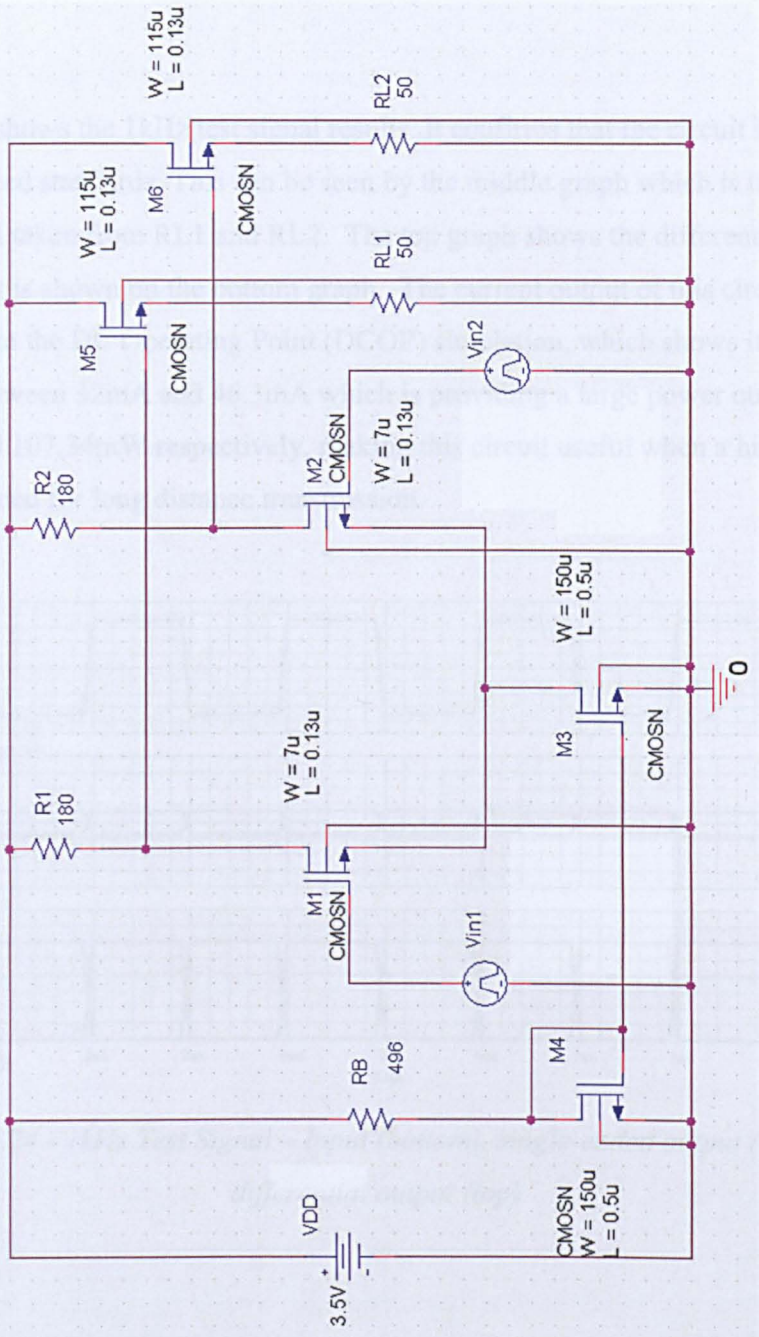


*Figure 3.23 – LVPECL Schematic with Annotated Biasing Conditions*

Figure 3.24 shows the 1kHz test signal results. It confirms that the circuit is working to the specified standards. This can be seen by the middle graph which is the single ended output taken from RL1 and RL2. The top graph shows the differential output and the input is shown on the bottom graph. The current output of this circuit can be obtained from the DC Operating Point (DCOP) simulation, which shows it is swinging between 32mA and 46.3mA which is providing a large power output, 51.5mW and 107.34mW respectively, making this circuit useful when a high power driver is needed for long distance transmission.

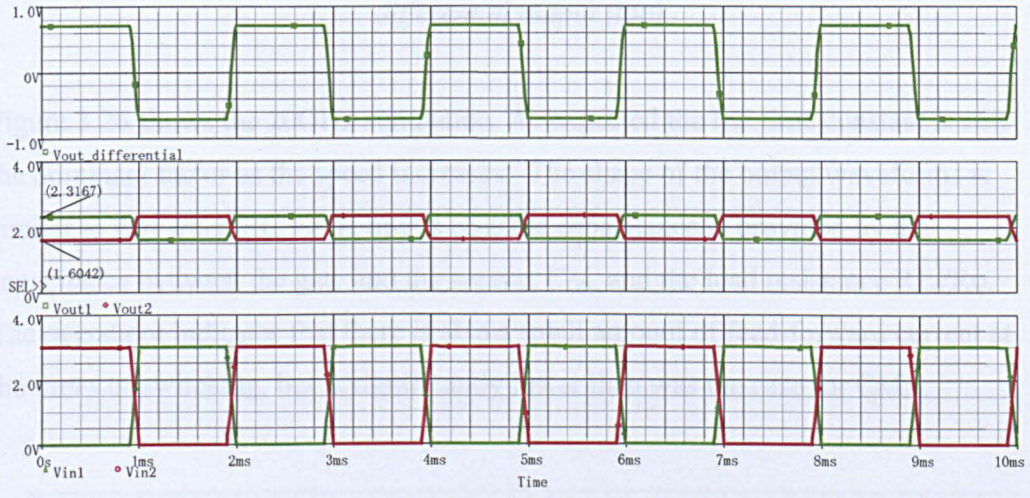


*Figure 3.24 - 1kHz Test Signal – Input (bottom), single-ended output (middle), differential output (top)*

Figure 3.25 shows the 10GHz simulation. The output waveforms are displaying a large exponential rise and fall time. This pattern is consistent with the effects of the RC time constant of the output stage when RC > T, where T is the period. This effect is the dominant source of distortion at this speed for this driver. From the single-ended output waveform it can be seen the driver is struggling to meet the required voltage levels defined by the standards.

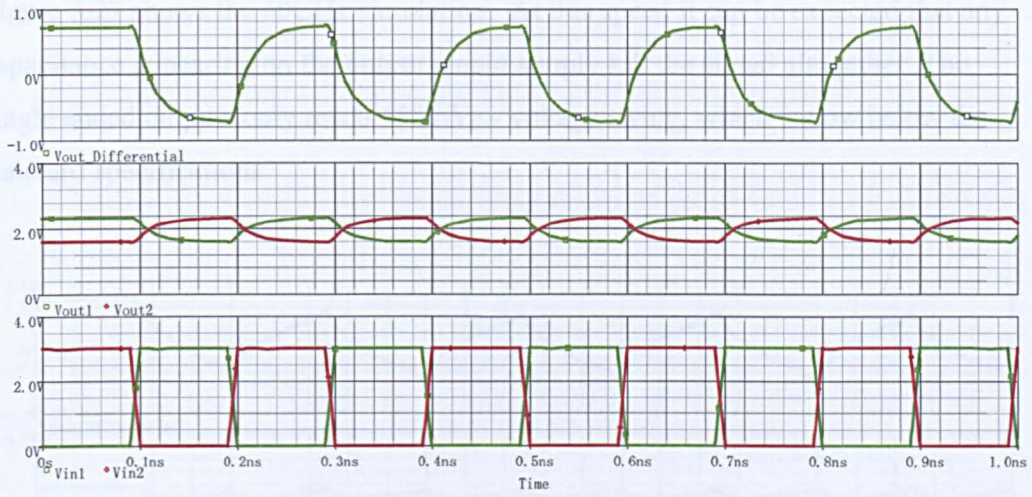


*Figure 3.25 – 10GHz Test Signal – Input (bottom), single-ended output (middle), differential output (top)*

Figure 3.26 shows the 20GHz simulation. As expected the RC time constant is still the dominant factor as the speed increases. The shape of the output waveforms is similar to that when RC >> T. In this case the capacitance is provided by the capacitance between the gate and the source, $C_{GS}$, and the load resistance RL//Ro. The overshoot indicates that there is also a small amount of feed-forward current at the times of switching, but is significantly lower than was the case for CML.

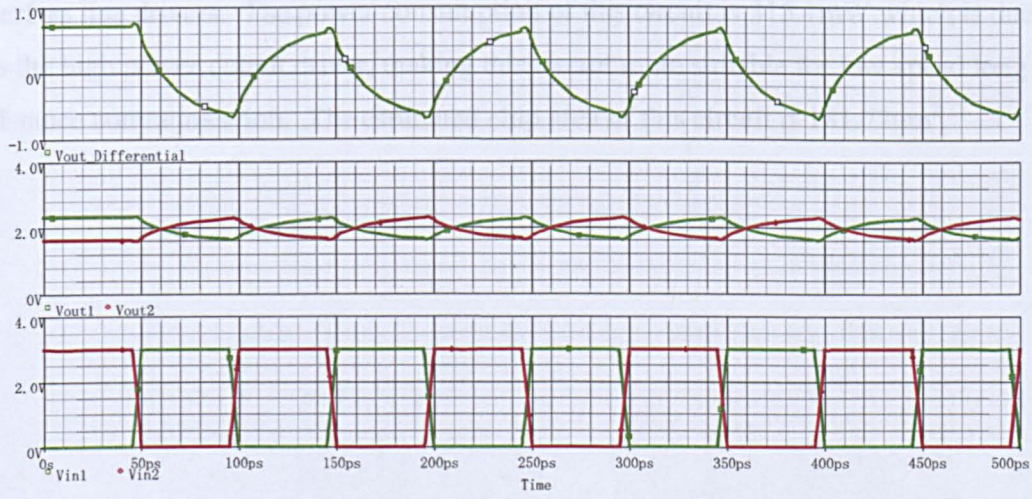


*Figure 3.26 – 20GHz Test Signal – Input (bottom), single-ended output (middle), differential output (top)*

Figure 3.27 shows the 40GHz simulation. At this speed it can be expected that any capacitance appearing on the output would simply kill the signal altogether. The single ended outputs only reach 450mV$_{P-P}$ voltage swing, which is now below the standard specifications.

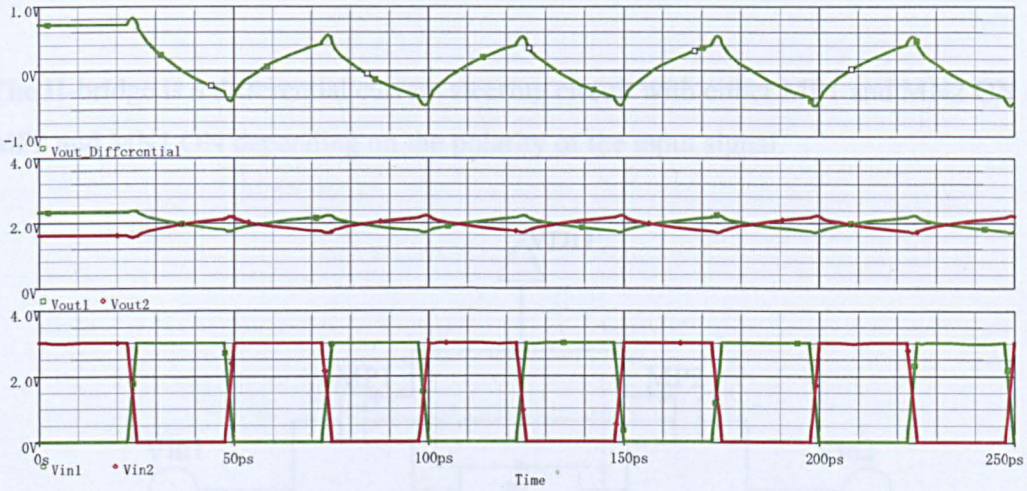


*Figure 3.27 – 40GHz Test Signal – Input (bottom), single-ended output (middle), differential output (top)*

From the simulations it can be seen that the dominating source of distortion is the RC time constant. In summary the circuit was not capable of the high speeds required by SerDes line drivers. The power consumption of this circuit is 315.1mW which is due to the high power output driver, making this circuit more suitable for low-speed long distance communication. The estimated chip area of this circuit is 181.72um$^2$.

## 3.5 H-Bridge

Although not commonly used in communication systems, the H-bridge is another possible architecture to consider for use as a SerDes line driver. The H-bridge is a four transistor current switching circuit, as shown in Figure 3.28. It uses two CMOS inverter circuits to change the polarity of current flowing through the load.

The H-bridge is a differential current steering circuit with either MP1 and MN2 ON or MP2 and MN1 ON depending on the polarity of the input signal.

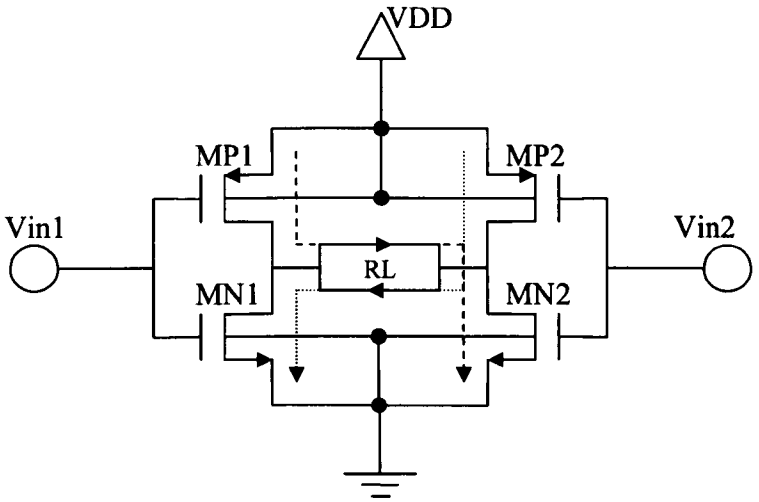


*Figure 3.28 – H-bridge schematic*

In case one where Vin 1 is high and Vin2 is low, MP2 and MN1 will be conducting allowing current to flow along the 'dotted' path, the other pair of transistors being OFF. Alternatively in case two Vin1 is low and Vin2 is high, MP1 and MN2 are now conducting allowing current to flow along the 'dashed' path, and again the other two transistors of the bridge are OFF.

The H-bridge is commonly used in motor drivers for applications such as robotics [18] where the load RL can be replaced with a motor which now can be driven digitally in both clockwise and anti-clockwise directions.

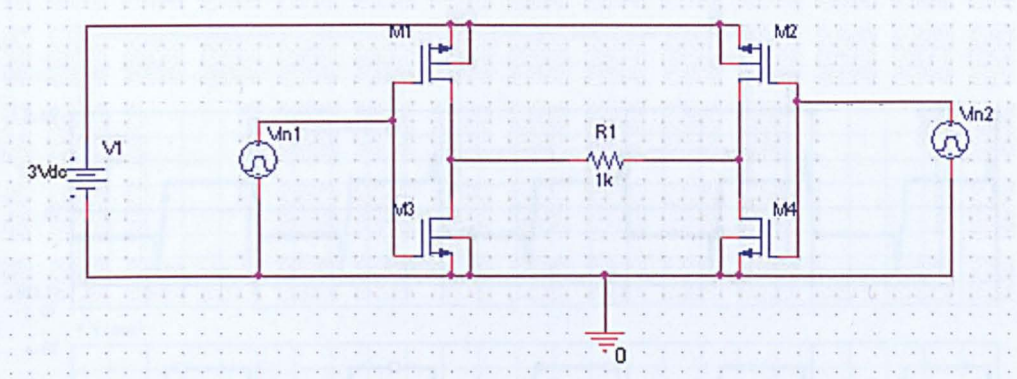


*Figure 3.29 – H-Bridge Capture schematic*

The H-Bridge schematic was entered into Capture, Figure 3.29, and the standard tests were performed with Vout taken across resistor R1:

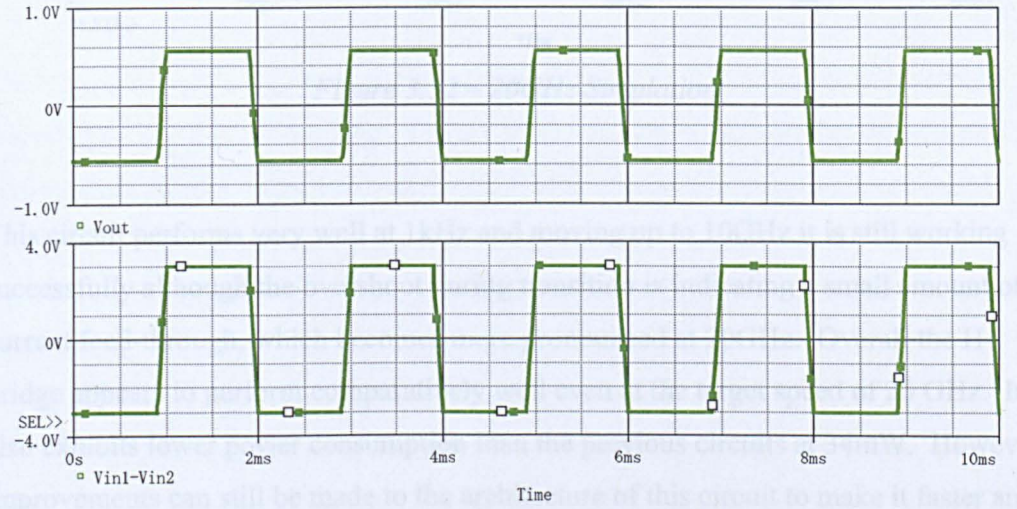


*Figure 3.30 – 1kHz Simulation*

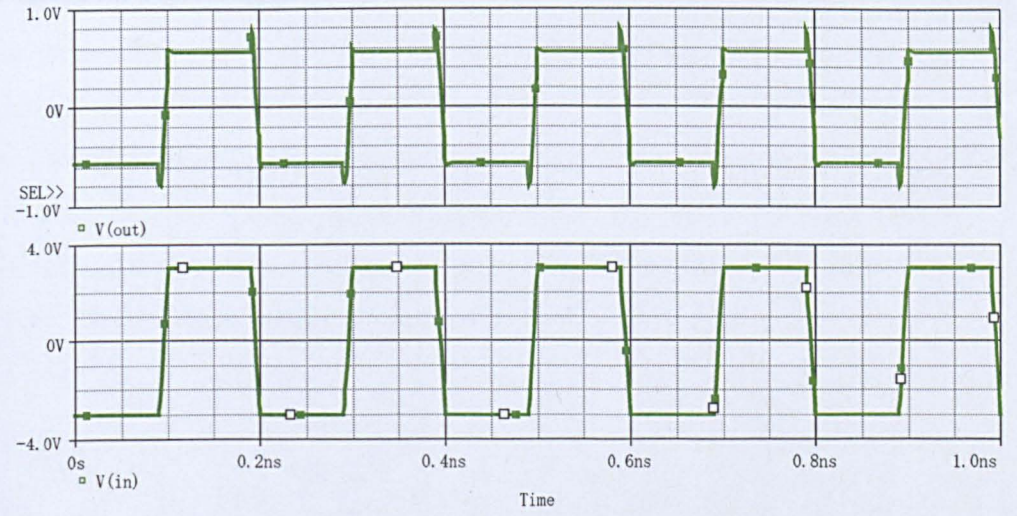


*Figure 3.31 – 10GHz Simulation*

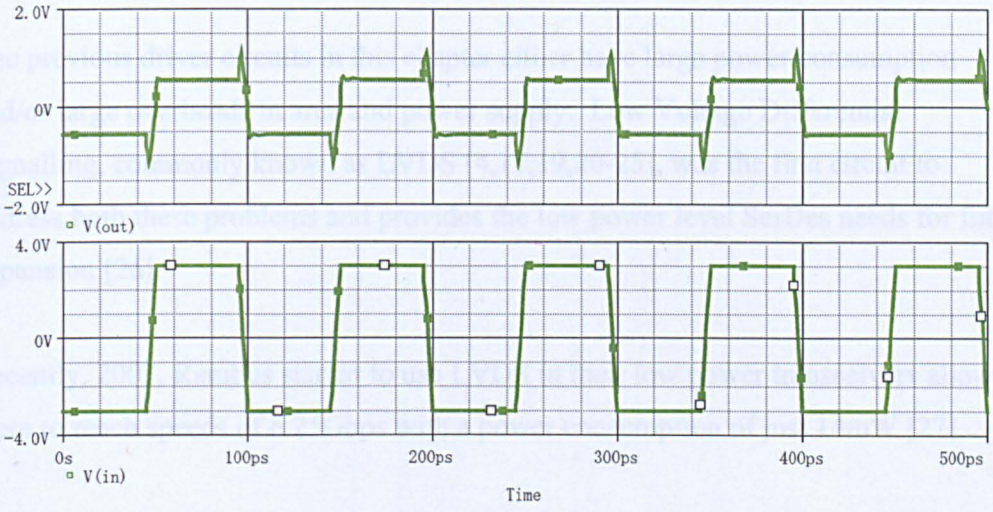


*Figure 3.32 – 20GHz Simulation*

This circuit performs very well at 1kHz and moving up to 10GHz it is still working successfully although the overshoot during transition is indicating a small amount of current feed-through, which becomes more pronounced at 20GHz. Overall the H-bridge appears to perform comparatively well even at the target speed of 20 GHz. It also exhibits lower power consumption than the previous circuits at 34mW. However improvements can still be made to the architecture of this circuit to make it faster and more efficient. These changes are shown in the next circuit, named Low Voltage Differential Signalling (LVDS).

## 3.6 Low Voltage Differential Signalling

The previous driver circuits in this chapter either have large power consumption and/or large overheads in area and power supply. Low Voltage Differential Signalling, commonly known as LVDS [4,17,19,20-25], was the first circuit to address both these problems and provides the low power level SerDes needs for future expansion [26].

Recently, 2007, Rambus started to use LVDS in their low power transceivers allowing them to reach speeds of 6.25Gbps with a power consumption of just 14mW [27].

The circuit in Figure 3.33 shows the basic circuit of LVDS. The circuit operates by receiving a digital input on either Vin1 or Vin2, like the H-Bridge, this input signal is used to steer current through RL with different polarities by using the four transistors, behaving as switches, as two pairs to provide two paths for the current to flow from constant current source I1 to VSS. A receiver is used to sense the polarity of current flow through RL and reconverts it back into the original data.

The LVDS is designed to be operated with a differential input signal. When Vin1 is high and Vin2 is low then M1 and M4 will be on, M2 and M3 will be off. In this case the current from the current source I1 will flow through transistor M1 to node A. As M2 is off the current has to flow up through RL in the direction of arrow A. Finally the current flows through M4 to VSS. Alternatively when Vin1 is low and Vin2 is high M1 and M4 will be off and M2 and M3 will be on. This time the current will flow from I1 through M3, through RL in the direction of arrow B and finally through M2 down to VSS. Finally, common-mode signals present on Vin1 and Vin2 will result in all 4 transistors being turned on routing current from VDD down to VSS bypassing RL which is not in the current path.

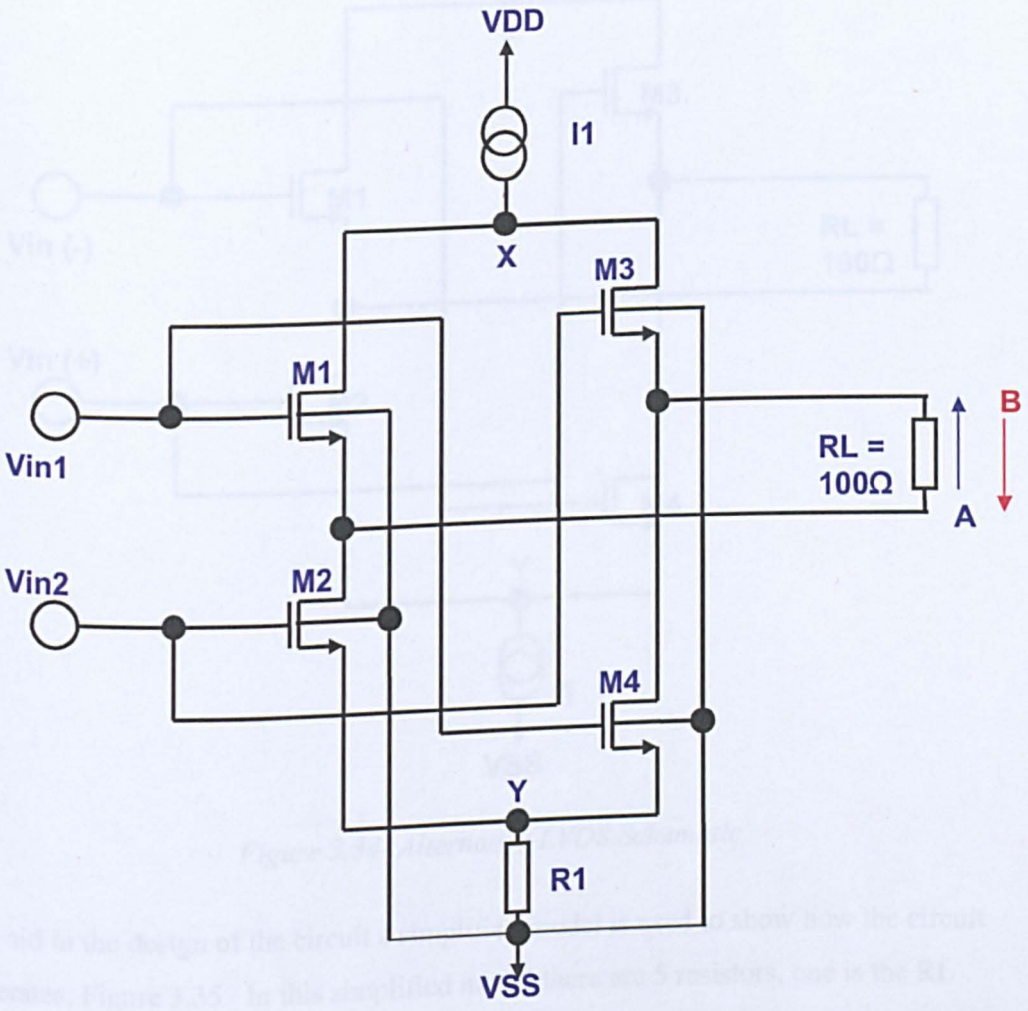


*Figure 3.33- Typical LVDS Schematic*

An alternative architecture for LVDS is shown in Figure 3.34. In this configuration the resistor R1 is replaced by a current sink which means that n-channel transistors can be used throughout reducing the total chip area. Also the drains of M1 and M3 can be connected directly to VDD. This also means that the resistor R1 is no longer needed as $V_{OH}$ is defined by $V_{DS1\&3}$ and $V_{OL}$ will be defined by the voltage drop across resistor RL.

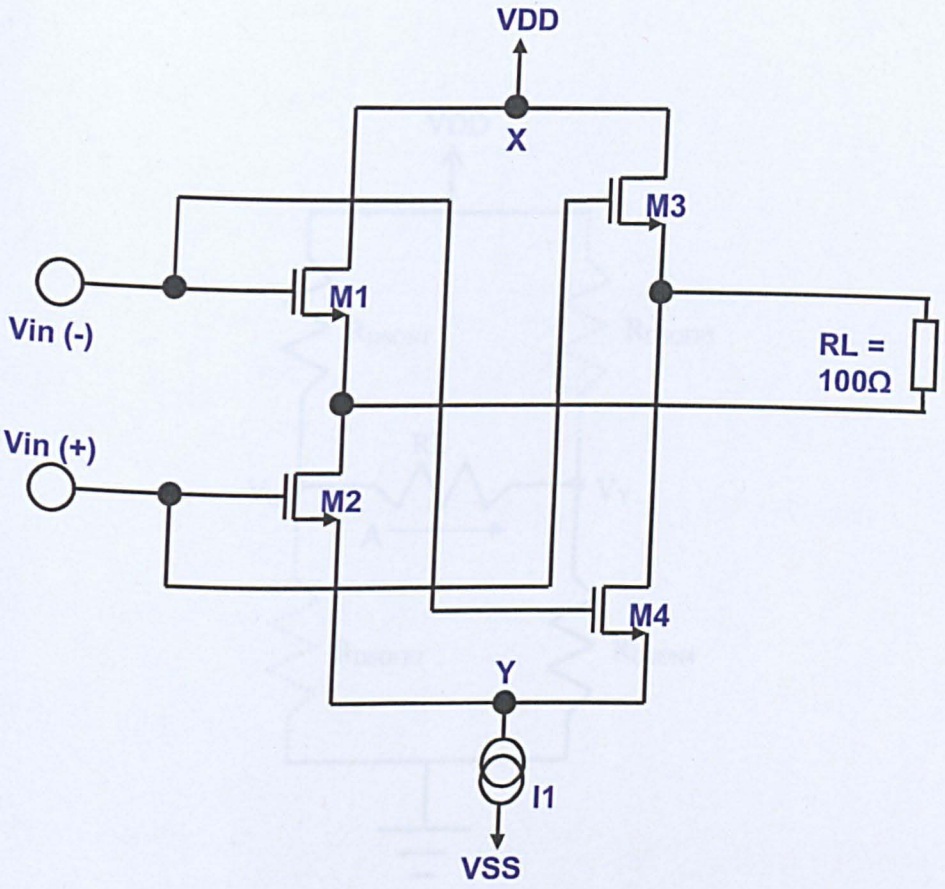


*Figure 3.34- Alternative LVDS Schematic*

To aid in the design of the circuit a simplified model is used to show how the circuit operates, Figure 3.35. In this simplified model there are 5 resistors, one is the RL resistor the other four represent the $R_{DS}$ of transistor M1 to M4, in H-configuration. In the operating condition A as stated above transistors M2 and M3 are OFF making. The voltage at $V_X$ will be defined by the voltage drop across $R_{DSON1}$ and $V_Y$ will be defined by the voltage drop across RL in a fashion similar to that of a two-stage potential divider.

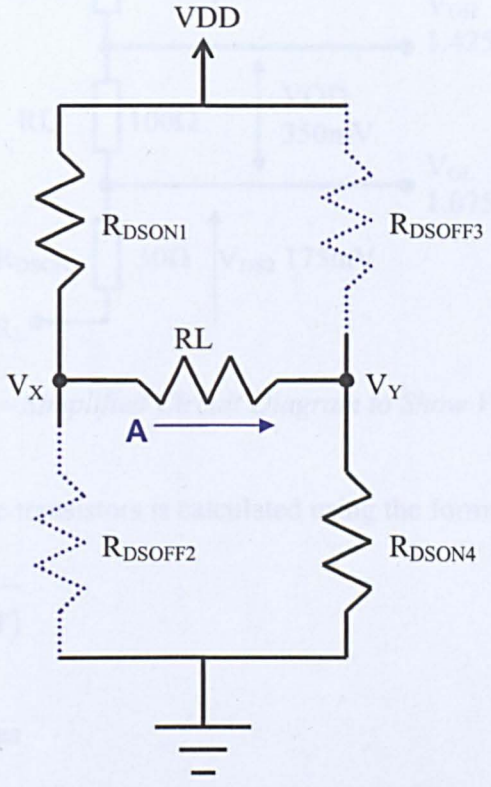


*Figure 3.35 – Simplified LVDS Model*

The resistor RL is a load resistor which terminates two 50Ω transmission lines, therefore the value needs to be 100Ω. LVDS needs an output voltage swing of $350mV_{P-P}$ therefore the current needed to provide that output swing is 3.5mA through RL.

The $R_{DSON}$ of each transistor needs to match the transmission line and therefore must be 50Ω furthermore the current needed to provide an output swing of 350mV across RL is 3.5mA. The $V_{DS}$ needed to achieve this will be 50x3.5mA = 175mV. To provide the correct output voltages, specified by the LVDS Standard, the driver circuit needs to be level shifted by using two supply voltages, $VR_H$ & $VR_L$, where $VR_H = V_{OH} + V_{DS1} = 1.6V$ and $VR_L = V_{OL} - V_{DS2} = 0.9V$. A graphical representation is shown in Figure 3.36.

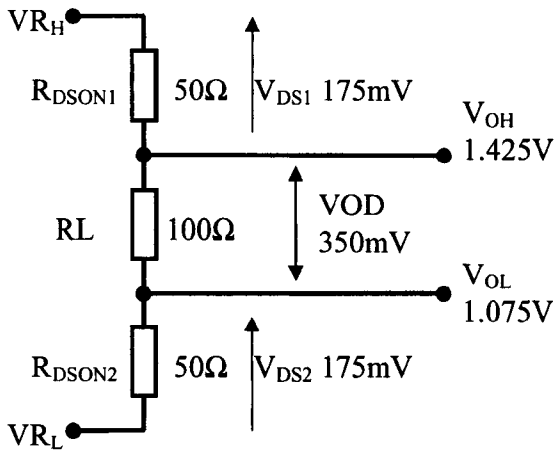


*Figure 3.36 – Simplified Circuit Diagram to Show Voltage Levels*

Finally the width of the transistors is calculated using the formula

$$R_{on} = \frac{1}{K\frac{W}{L}(VGS - VT)} \tag{3.27}$$

Re arranging for W gives

$$W = \frac{1}{K \bullet R_{on} \bullet (VGS - VT)} \bullet L \tag{3.28}$$

where VGS1 = Vin - $V_{OH}$ = 1.575V (3.29)

VGS2 = Vin - $V_{OL}$ = 1.925V (3.30)

VT = 0.45V

$W_{(1,2)}$ = 12μm

$W_{(3,4)}$ = 10μm

The final circuit used for simulation is shown in Figure 3.37

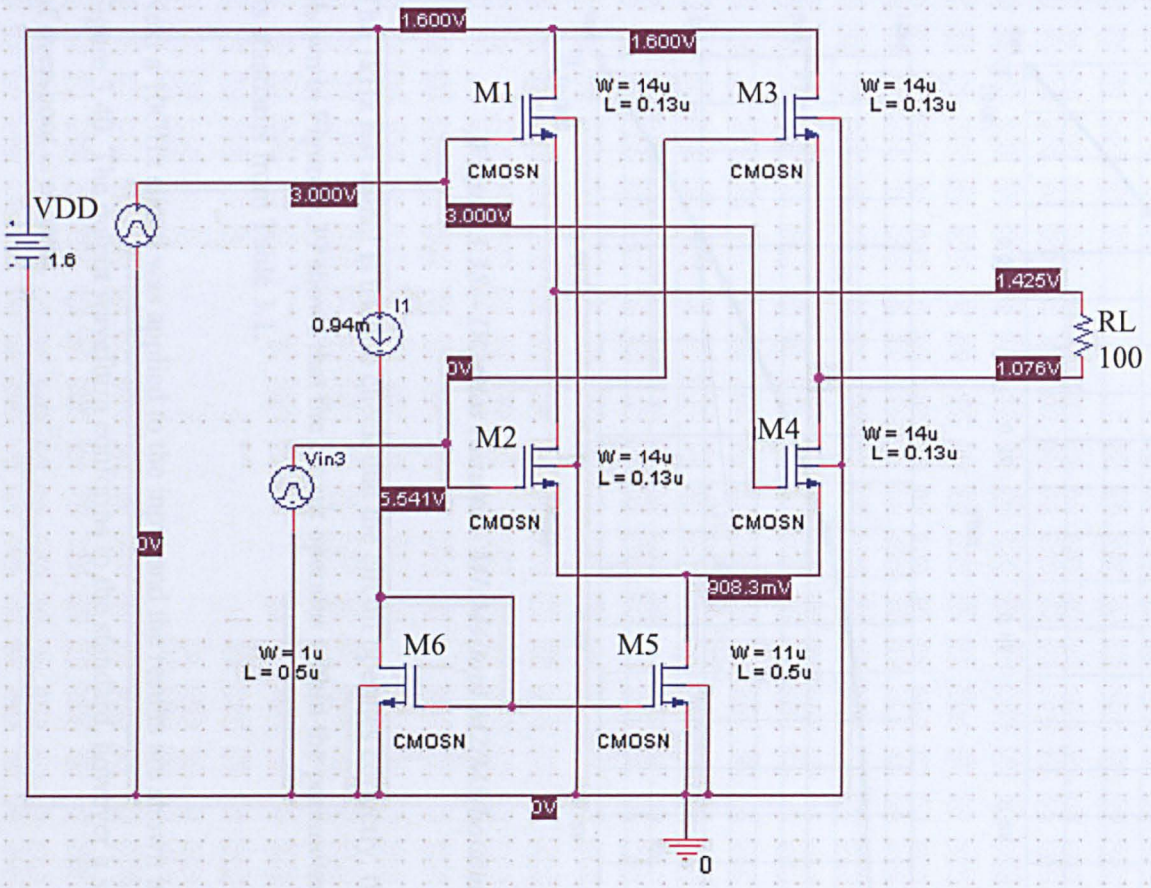


*Figure 3.37 – LVDS Schematic*

A DC bias check on the circuit is shown in Figure 3.38 confirming that the transistors are operating in the triode region.

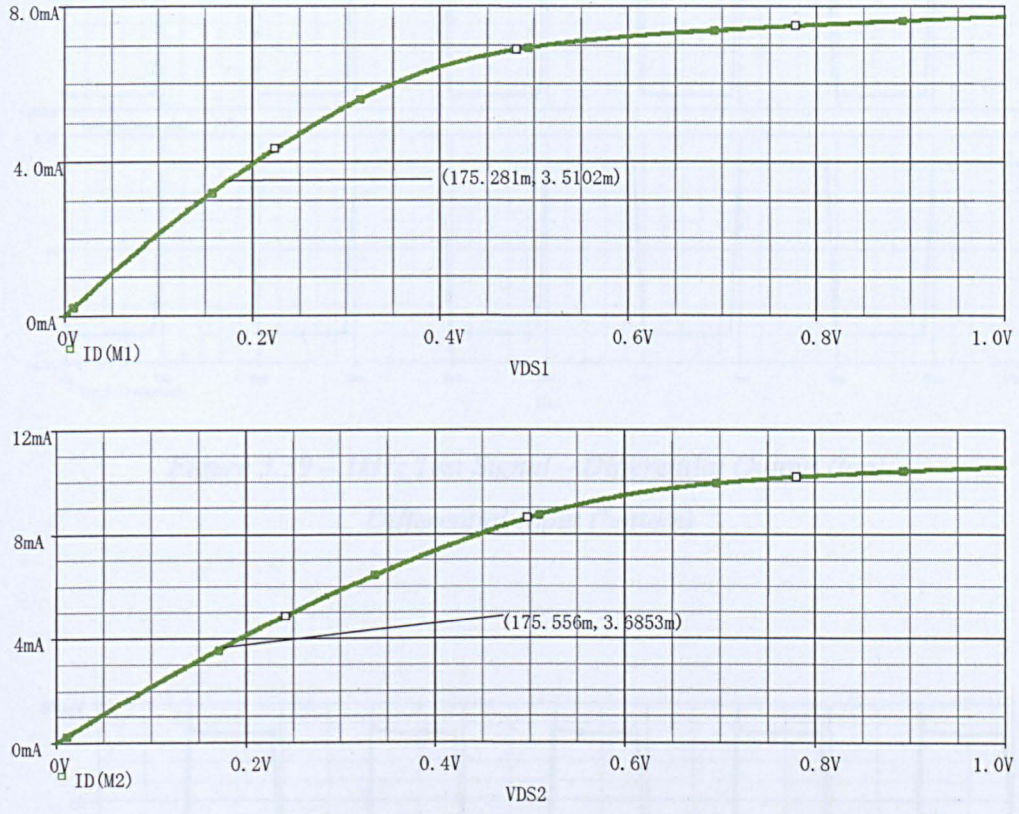


*Figure 3.38 – DC Bias Results – M1/M4(top) M2/M3(bottom)*

The 1kHz test signal is used to check that the circuit operates correctly, the results shown in Figure 3.39 shows that the circuit operates within the parameters defined by its standards from Table 3.1.

Next a 10GHz signal was applied to the input and the results are shown in Figure 3.40. The output waveform conforms to the standard, however a slight amount of overshoot is evident.

The 20GHz simulation, Figure 3.41, shows an increased amount of overshoot. The 40GHz simulation, Figure 3.42, shows similar attributes to the 20GHz signal but the operation is still within the LVDS Standards. Crossover distortion can also be clearly seen in Figure 3.6.10 due to the transistors not turning on or off at the same time.

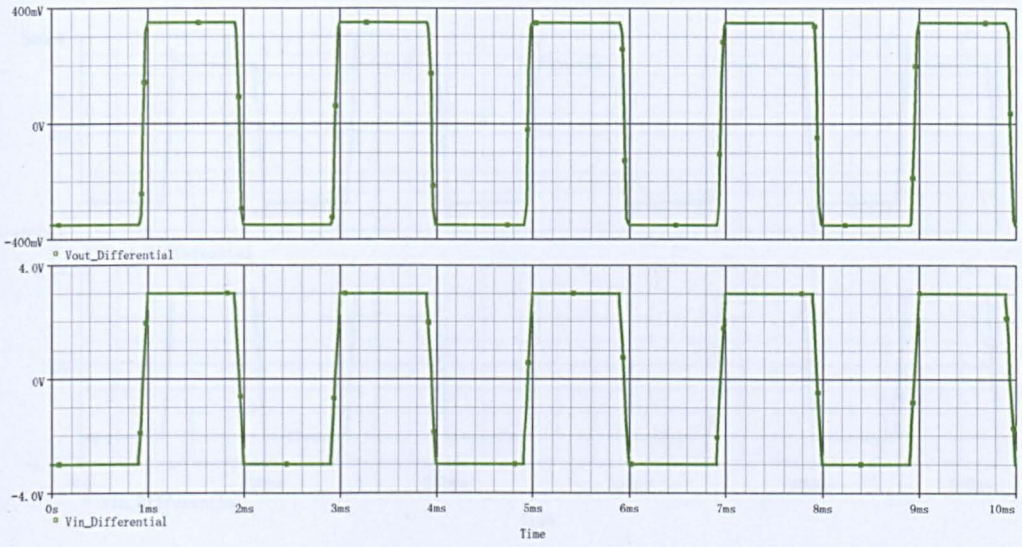


*Figure 3.39 – 1kHz Test Signal – Differential Output (top), Differential Input (bottom)*

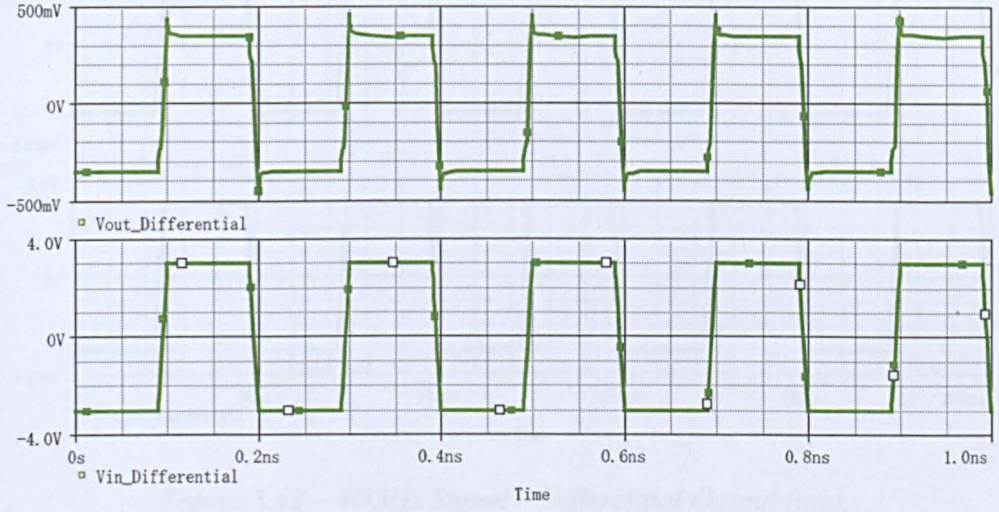


*Figure 3.40 – 10GHz Signal – Differential Output (top), Differential Input (bottom)*

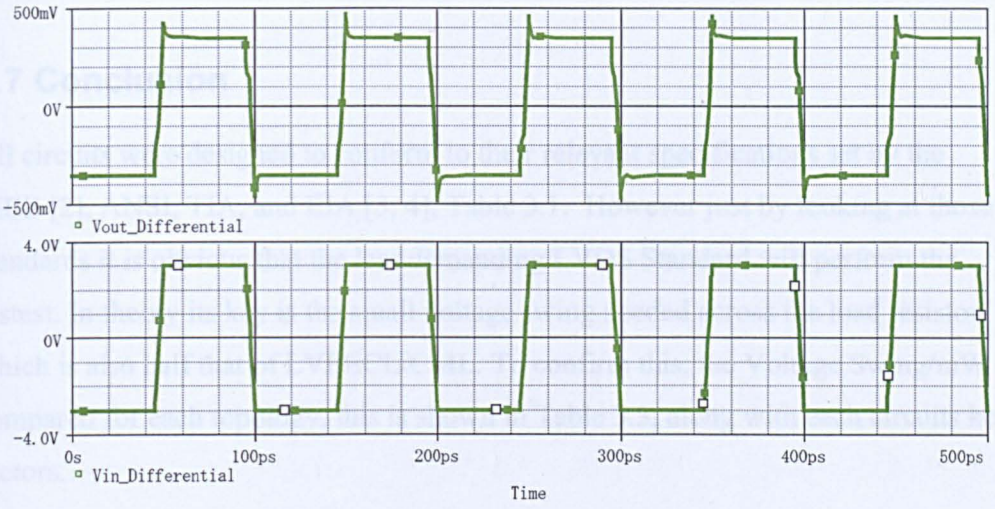


*Figure 3.41 – 20GHz Signal – Differential Output (top), Differential Input (bottom)*

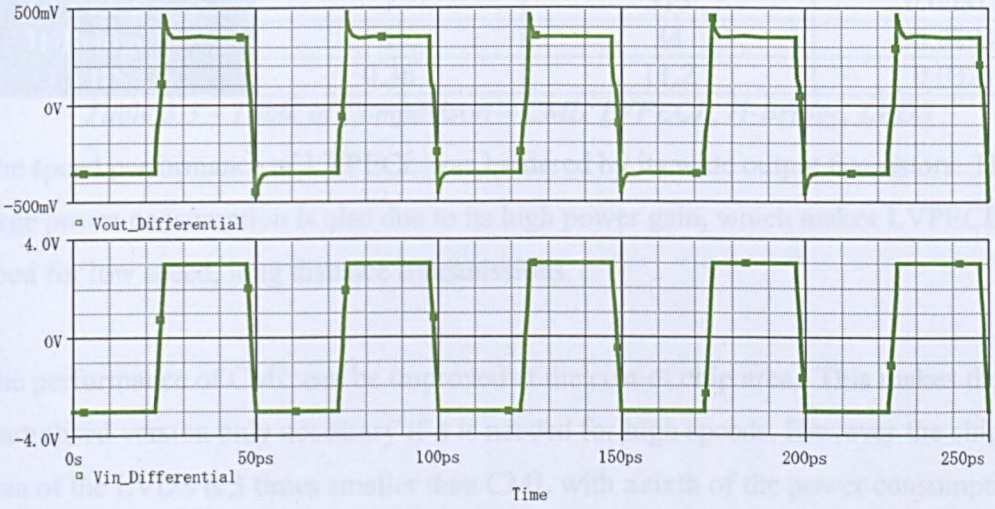


*Figure 3.42 – 40GHz Signal – Differential Output (top), Differential Input (bottom)*

The 40GHz simulation shows comparable performance with the neutralised version of CML with less chip area at 55µm, and lower power consumption at 7mW.

## 3.7 Conclusion

All circuits were designed to conform to their relevant specifications set by the IEEE [2], ANSI, TIA, and EIA [3, 4], Table 3.1. However just by looking at those standards it is obvious that the less demanding LVDS Standard will perform the fastest. In theory its key is the small voltage swing needed across the load resistor, which is also half that of LVPECL/CML. To confirm this, the Voltage Swing/mW is compared for each topology, this is shown in Table 3.3, along with each circuits key factors.

| | Output Voltage Swing (V) | Power Consumption (mW) | Voltage Swing per mW (V/mW) |
|---|---|---|---|
| **CML** | 1.5 | 64 | 0.0234 |
| **CML + Neutralisation** | 1.5 | 64 | 0.0234 |
| **LVPECL** | 1 | 315 | 0.00317 |
| **H-Bridge** | 1 | 34 | 0.0294 |
| **LVDS** | 0.36 | 11.2 | 0.0321 |

*Table 3.3 – Table of Comparison – CML, LVPECL, H-Bridge, LVDS*

The speed performance of LVPECL was hindered by its wide output transistors. The large power consumption is also due to its high power gain, which makes LVPECL good for low speed, long distance transmissions.

The performance of CML can be improved at the cost of chip area. This makes the neutralised version only necessary if it is needed for high speeds. However the chip area of the LVDS is 3 times smaller than CML with a sixth of the power consumption of CML.

In conclusion LVDS appears the prime contender for future line driver design where power and area limits are getting smaller. In Chapter 4 LVDS will make up the Core Driver of my novel work.

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# Chapter 4

# Composite LVDS (C-LVDS)

## 4.1 – Introduction

In Chapter 3, LVDS was identified as the fastest and most efficient line driver topology for 40Gigabit/s SerDes. In this chapter methods and techniques are examined to optimize its performance for 40Gbps data links. A novel line driver is presented called Composite Low-Voltage Differential Signalling, C-LVDS. The word composite is used as the output of the driver is the composite of each stage of the driver.

## 4.2 – Concept

As discussed in Chapter 2 one of the main problems that arises in high-speed data links is Inter-Symbol Interference (ISI), where the high frequency components are attenuated more than the low frequency components. To overcome this on the transmitter end a technique called pre-distortion is used. In this case a 'High Frequency Booster' (HFB) can be used to compensate for these channel effects. The idea is to have two or more drivers and turn on the extra driver/s only when the high frequency components are present. In theory the high frequency channel attenuation will be compensated. Figure 4.1 shows a graphical representation of a pre-distorted signal.

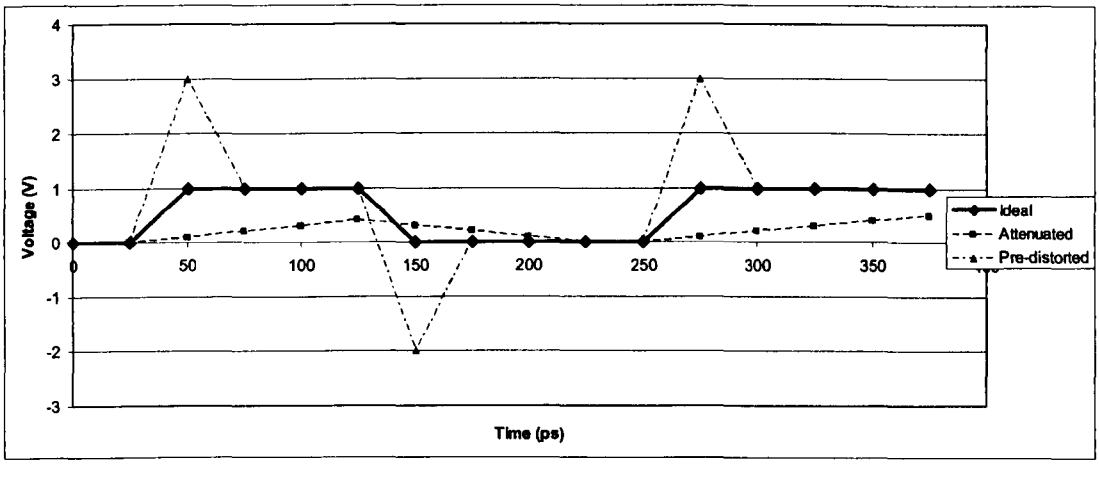


*Figure 4.1 – Representation of Pre-distortion*

The 'Ideal' line is the ideal/desirable situation. The 'Attenuated' line is a representation of the received signal of the ideal line after passing through a real channel. The 'Pre-distorted'

line represents how the signal needs to be distorted to compensate for the high frequency channel attenuation and hence return the signal close to the 'Ideal' line.
Another way of looking at Figure 4.1 from a time-domain perspective is that the driver needs to add signal boosting at the rise and falling edges to compensate for the resultant channel attenuation of the signal that will occur at these transitions. Ensuring that the signal reaches its voltage levels quickly will ensure that all bits will stay at the same voltage level, improve jitter, improve ISI and prevent DC drift.

## 4.3 - Design procedure

C-LVDS was designed to provide amplify high frequencies to distort the signal in a particular shape to compensate for losses during transmission through a transmission line. The full system is shown in Figure 4.21.

The C-LVDS line driver can be split into two main components, the 'Core' and the 'Interface'. The Core contains the 'DC Driver' as well as the 'High-Frequency Booster' all of which are setup in the LVDS configuration [1 - 9] and connected together in parallel, as shown in Figure 4.2.

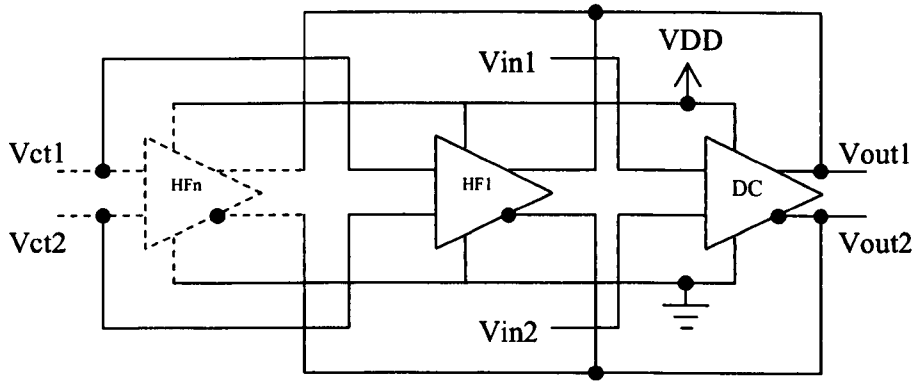


*Figure 4.2 – C-LVDS Core*

The Interface contains the control circuitry that turns on the High-Frequency Booster. There are several ways that the interface could be implemented, including both analogue

and digital techniques. However, due to the high speeds required by the interface a completely analogue control system will have more benefits than a digital control method.

Various analogue circuits were looked at including the One-Shot and various types of filters. The simplest circuit that worked well in C-LVDS was the single pole RC high pass filter (HPF), shown in Figure 4.3a. The high pass filter generates the control signal by allowing the high frequency components that are found at the rising edge of the pulse through, whilst attenuating the low frequency components. The result is a short pulse on the rising edge of each data pulse, shown in Figure 4.3b.

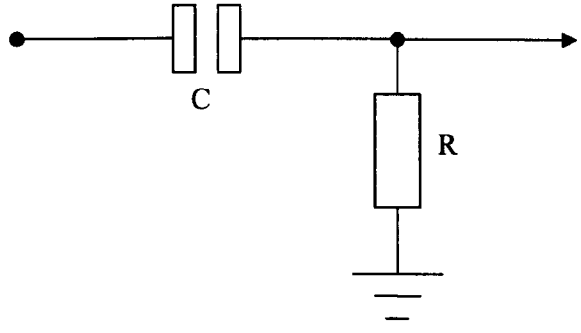


*Figure 4.3a – RC HPF Schematic*

The values of C and R vary slightly depending on which variation of C-LVDS is to be used, C-LVDS Type A is best optimised for voltage switching speed due to the filter connecting to Gates of MOSFETs all current will flow through the resistor R, therefore a high value of R will reduce power consumption. C-LVDS Type B is optimised for current transfer, in this case the filter is connected to the Drain of the MOSFETs therefore the filter needs to provide current through the transistor. This can be achieved by using a relatively large C value. These values become apparent in Sections 4.4 and 4.5 where the circuits are explained in more depth. In both cases care must be taken to keep the RC time constant low enough for high speed data, for 40Gbps the signal frequency is 20GHz thus the minimum RC time constant is 50ps.

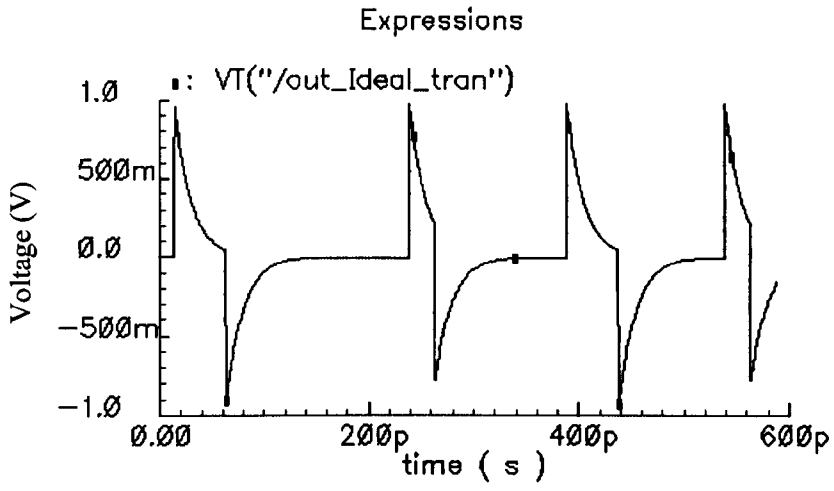


*Figure 4.3b – 20GHz HPF transient response*

The transient response in Figure 4.3b, which was generated using a Pseudo-Random Bit Sequence (PRBS) generator shows that a benefit to using a passive RC network is the high response time. Shortly after 200ps a 010 pattern is transmitted and the RC-network easily filters the 20GHz frequency and rapidly begins attenuating the rest of the pulse. This test showed that a simple single pole RC HPF will provide the right control signal for the high frequency boosters as the signal tracks the gain requirements of the high-frequency boosters. Furthermore the fall off of the gain can be controlled by the cut-off frequency of the filter.

## 4.4 – C-LVDS Type A

The most obvious arrangement for the filters is to use them to drive the gates of the MOSFETS. C-LVDS Type A consists of one DC-driver (DC) and one High-Frequency Booster (HFB). The DC-driver's gates are driven by the input data whilst the High-Frequency Booster is driven by the filtered data. A high level schematic of the 'Type A' architecture is shown in Figure 4.4.

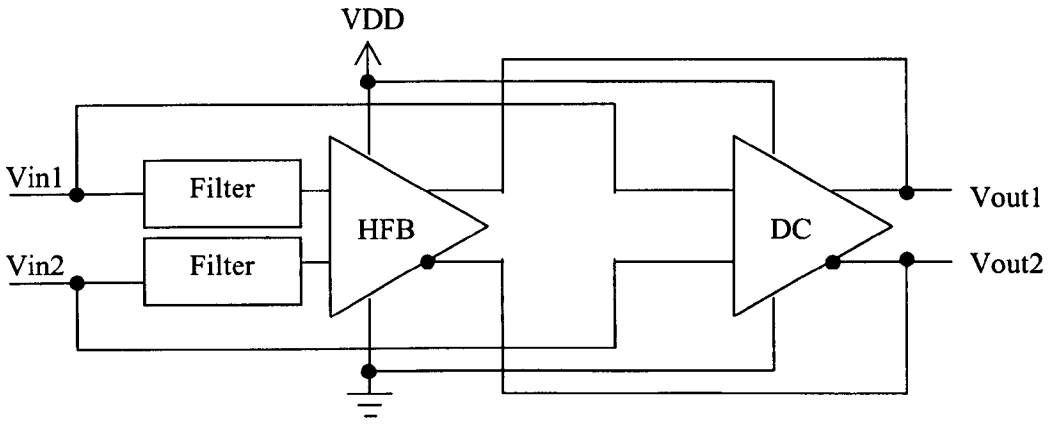


*Figure 4.4 – C-LVDS Type A – Block Diagram*

In order to see the performance of this architecture under ideal conditions a behavioural model was created in Matlab.

### 4.4.1 - Behavioural Model

The behavioural model for C-LVDS Type A, Figure 4.5, consists of two main devices (Interface and Core). There is also a differential signal generator, the channel and the receiver model. To simulate the differential effect of the circuit the model is mirrored and simulated at 180° phase from each other.

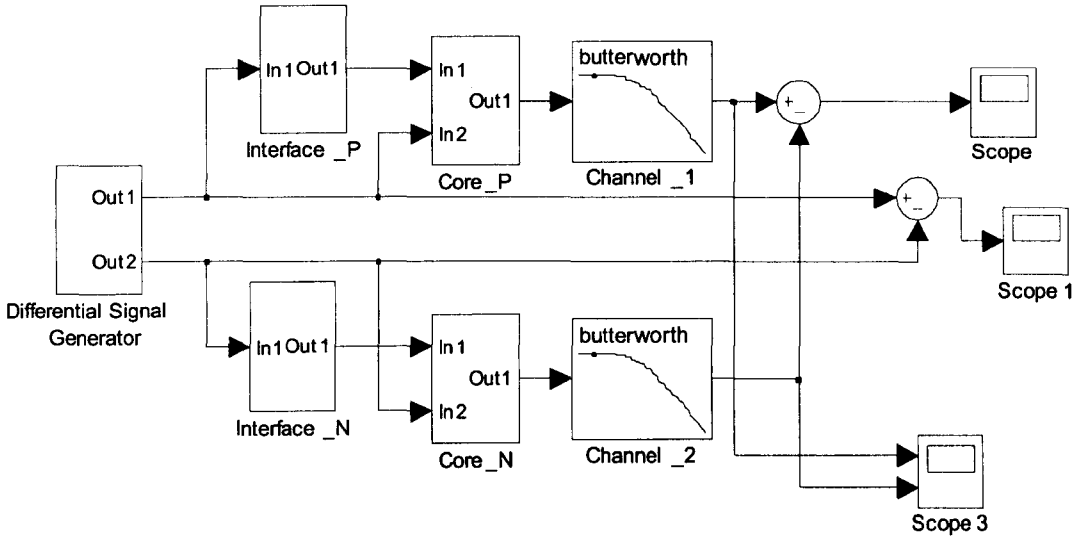


*Figure 4.5 – C-LVDS Type A behavioural model – top level*

The differential signal generator, Figure 4.6, generates a PRBS signal and inverts it to create two signals in 180° phase relationship.

The Bernoulli Binary Generator generates a pseudo random binary number. The switch is then used to invert the data by outputting a binary 0 when the generator produces a 1 and a 1 when the generator produces a 0. The inverted and non-inverted data streams are then output separately.

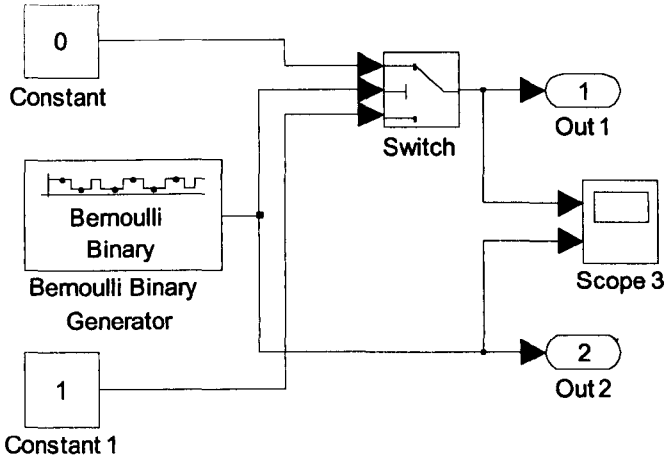


*Figure 4.6 – Differential Signal Generator – Matlab Model*

The interface, Figure 4.7, contains a HPF using the Butterworth model which filters the data stream to produce the wanted control signal, Figure 4.8.

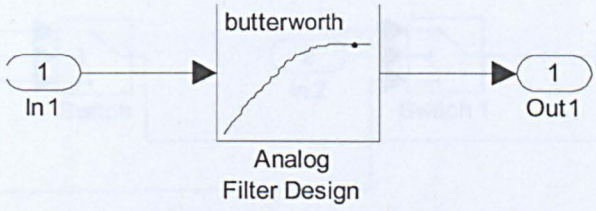


*Figure 4.7 – Interface Matlab model*

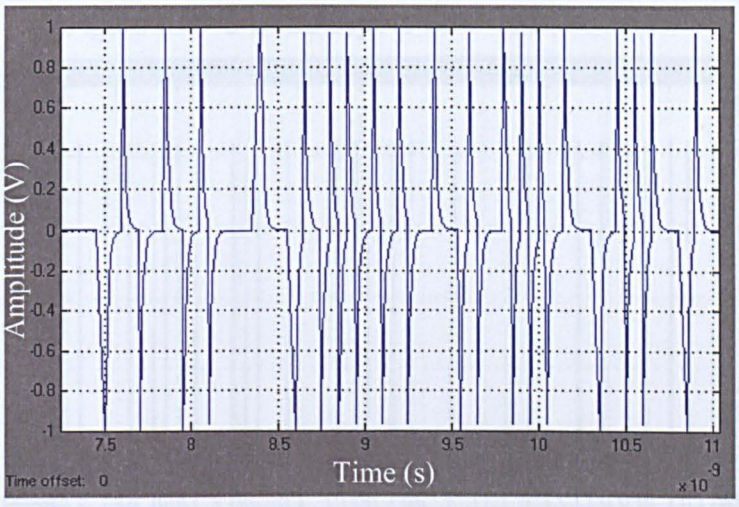


*Figure 4.8 – Interface Output*

The core, Figure 4.9, consists of two switches. The switches represent the switching action of the transistors within LVDS, one switch represents the High-Frequency Booster, and the other switch represents the DC-driver. Each switch is weighted to represent the amount of gain needed, for example the DC driver needs an output swing of 350mV hence is weighted at 0.35 where as the booster needs a very high gain to overcome the loss in the channel and therefore is weighted at 10 volts. The output of each switch is then summed together. This produces the pre-distorted signal, Figure 4.10, to be sent down the channel.

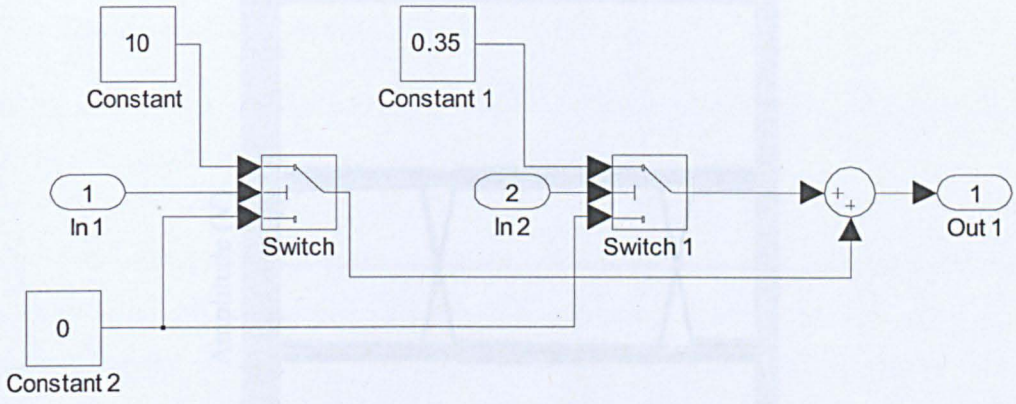


*Figure 4.9 – C-LVDS Type A Core – Matlab model*

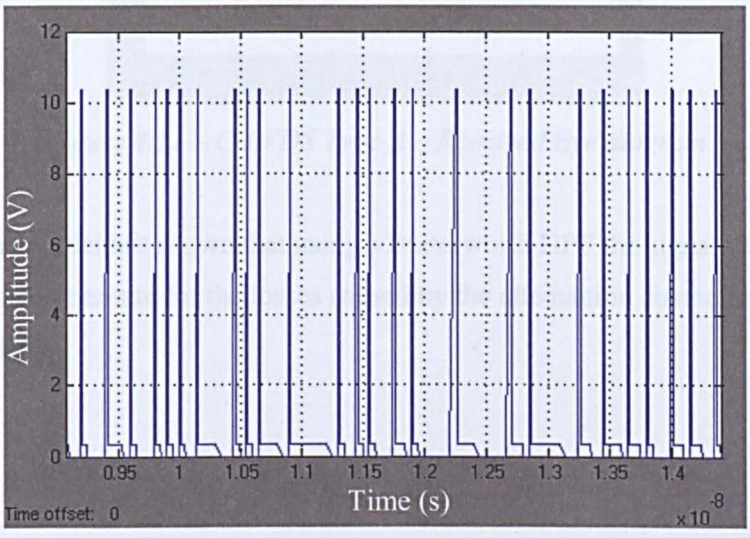


*Figure 4.10 – Single ended C-LVDS Core output*

The pre-distorted signal is now passed through the 'Channel' which is represented by a 2.65GHz Butterworth Low-Pass Filter (LPF) which has a loss of 15dB at 20GHz. The channel attenuation characteristics attenuates the transmitters output (the pre-distorted signal) and after subtracting the inverted received data stream from the non-inverted data stream the original data pattern is reproduced. Using an eye diagram module supplied by the communication block set within Matlab it can be seen that the received signal has a completely open eye, Figure 4.11.

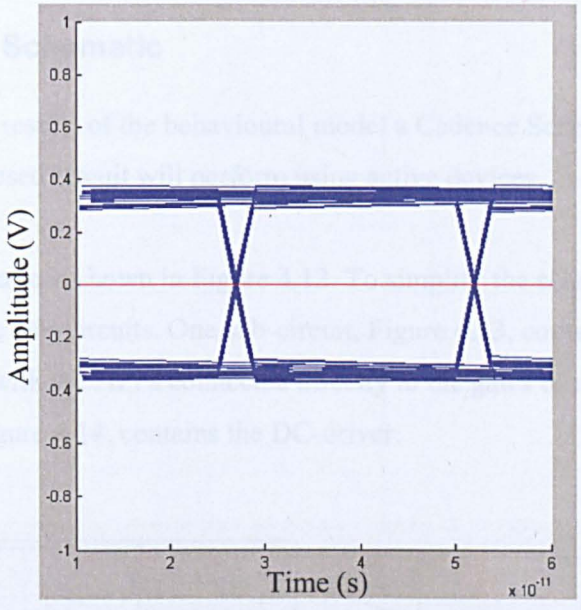


*Figure 4.11 – C-LVDS Type A – Received Eye diagram*

The behavioural model has shown that using a Butterworth HPF the signal can be pre-distorted to compensate for the losses caused by the attenuation characteristics of a known channel.

### 4.4.2 - Cadence Schematic

After the successful results of the behavioural model a Cadence Schematic can be created to see how the proposed circuit will perform using active devices.

The top level schematic is shown in Figure 4.12. To simplify the schematic the line driver was divided into two sub-circuits. One sub-circuit, Figure 4.13, contains the High-Frequency Booster with the HPFs connected directly to the gates of the transistors. The other sub-circuit, Figure 4.14, contains the DC-driver.

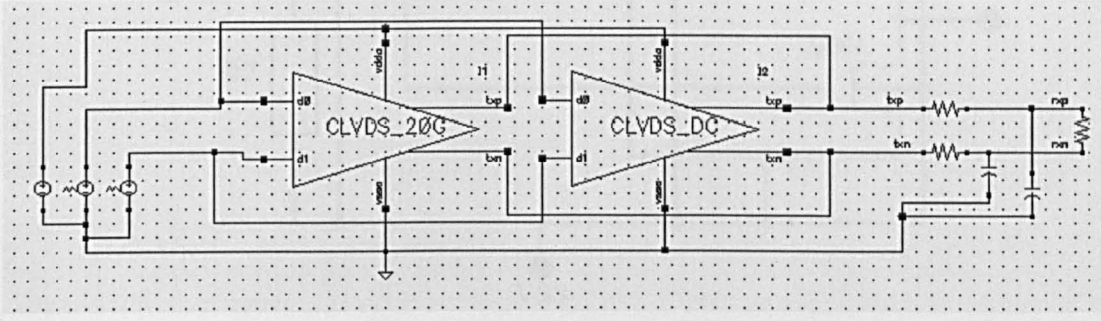


*Figure 4.12 – C-LVDS Type A - Top level – Cadence Schematic*

The outputs of the line driver are connected to a LPF which represent a 50Ω transmission line. A 100Ω load resistor is then connected between the differential outputs to complete the circuit, this will look like a 50Ω load for each half of the line when considered separately.

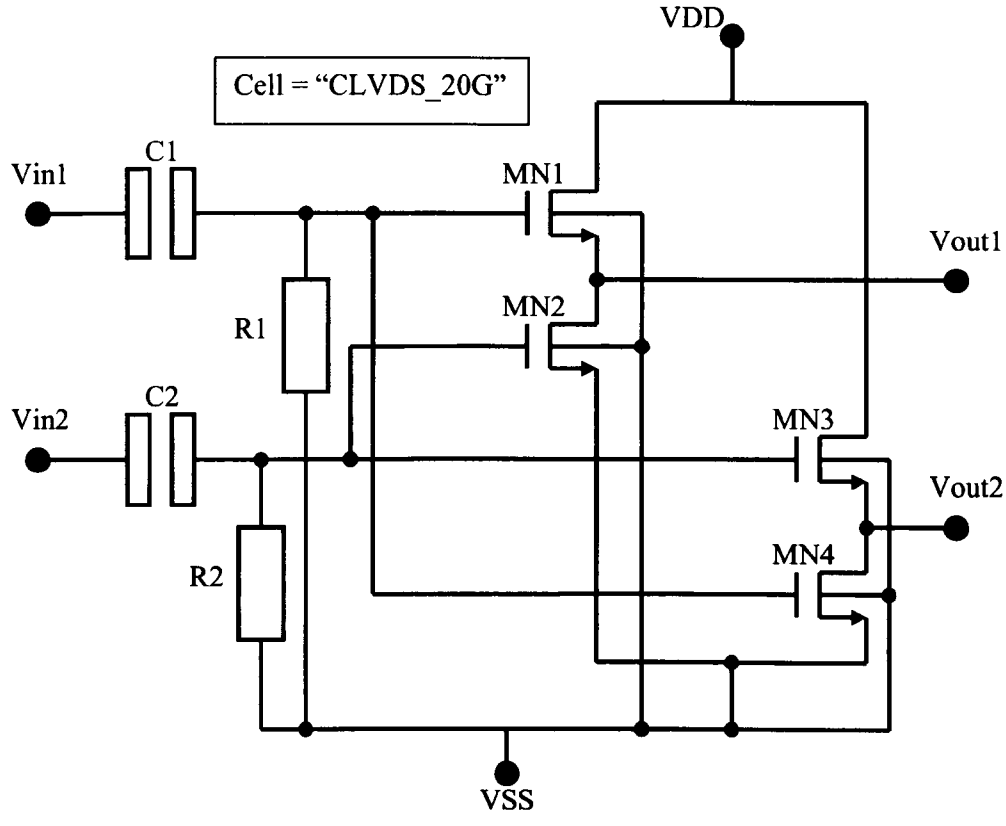


*Figure 4.13 – C-LVDS Type A - High-Frequency Booster – Cadence Schematic*

Figure 4.13 shows the circuit of the High Frequency Booster (HFB). It contains an LVDS style driver however the data input is filtered using a single pole HPF with a cut-off frequency of 11GHz. The output of the filters generates the control signal which turns the driver off shortly after the rising edge of the data. Lowering the cut-off frequency will allow the driver to stay on longer, this can be used to shape the output characteristics of the driver to counter the characteristics of the channel.

All the transistors are operating in the triode region and are very wide to improve the switching speed, w = 200μm, l = 0.065μm. The size of the transistors can be reduced on a smaller geometry where the switching speed of the transistors will be improved.

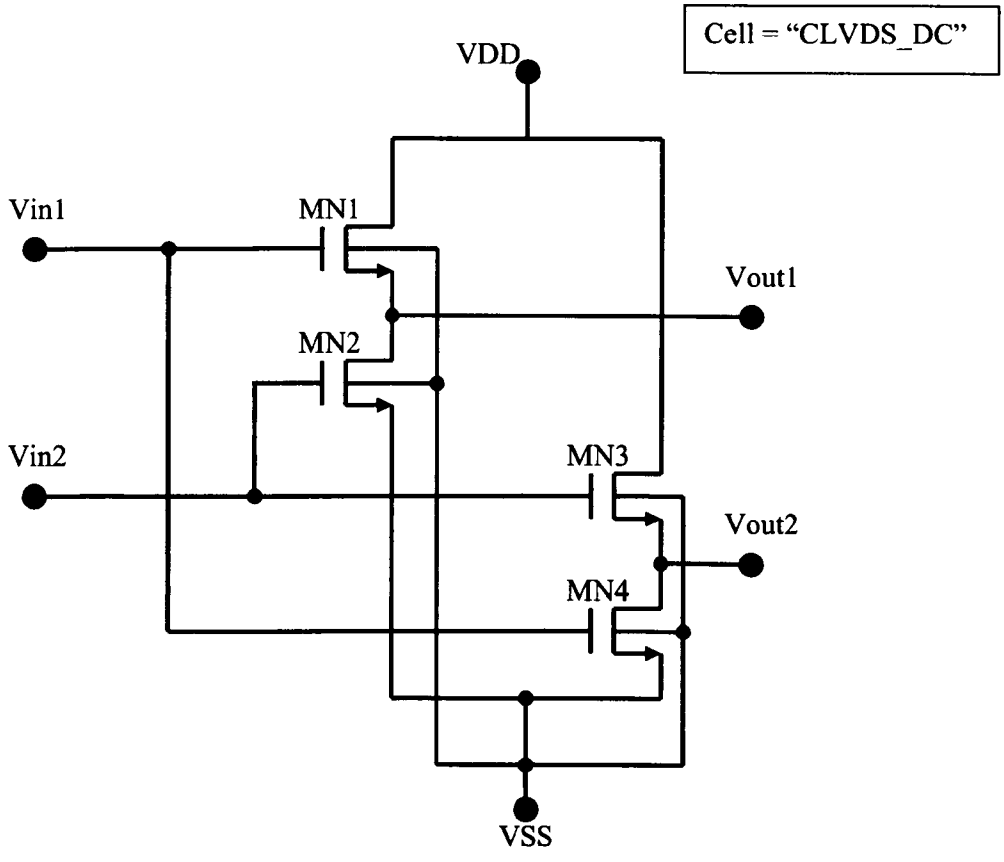


*Figure 4.14 – C-LVDS Type A – DC-Driver*

Figure 4.14 shows the schematic for the DC Driver. It is also a LVDS style driver circuit. Again all transistors are operating in the triode region and are wide enough to enable high speed switching, w = 200μm, l = 0.065μm.

It is the function of the DC-Driver to provide a constant supply of 3.5mA through the receivers termination resistor. This will provide a 350mV swing across a 100Ω termination resistor.

### 4.4.3 - Simulation Results

Eye diagrams were produced in Cadence. For comparison one simulation was performed with the High-Frequency Booster turned on, Figures 4.15 (a) and (b), and one simulation with the booster turned off, Figures 4.15 (c) and (d).

Figures 4.15 (a) and (c) show the output of the transmitter (labelled 'txp' and 'txn' on Figure 4.12) and Figures 4.15 (b) and (d) show the received signal (labelled 'rxp' and 'rxn' on Figure 4.12). It can be seen that the booster is causing a slight improvement however the filters are unable to drive the large transistors making the gain insufficient to effectively pre-distort the signal as intended. By comparing Figures 4.15 (b) and (d) (labelled 'rxp' on Figure 4.12) it can be seen that there is a slight improvement of the eye-diagram opening however it can not provide enough gain to overcome the attenuation characteristic of the channel.

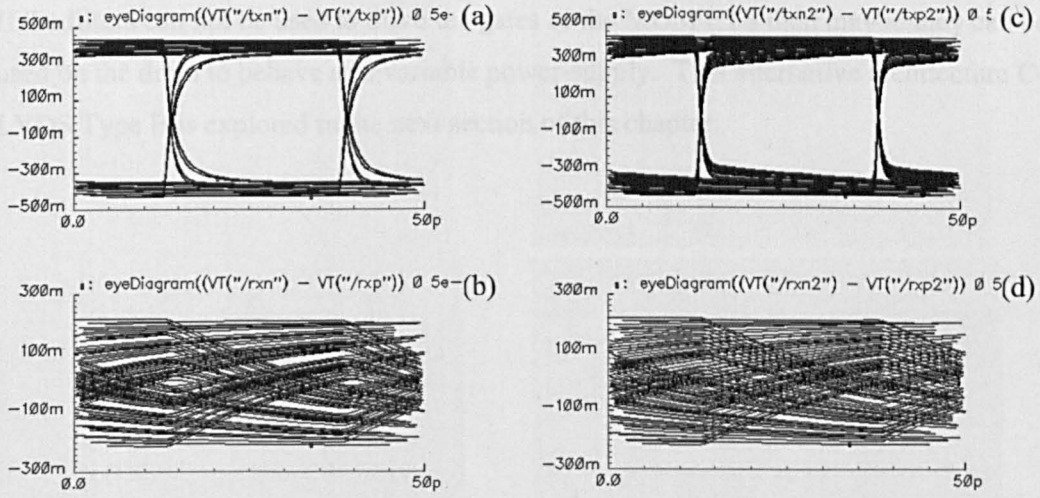


*Figure 4.15 – C-LVDS Type A Results (a)Transmitted Eye (HFB Enabled), (b)Received Eye (HFB Enabled), (c)Transmitted Eye (HFB Disabled), (d)Received Eye (HFB Disabled)*

### 4.4.4 – C-LVDS Type A Summary

Although the behavioural model verified the theory of using passive HPFs to perform pre-emphasis on the transmitter, the architecture failed due to the filter not being able to drive the transistors. This due to a combination of the transistors having a large W/L ratio and to provide the right amount of gain at the right time they need to be able to switch on and off approximately 10 times faster than the data rate, roughly 200GHz. The input capacitance of the transistors is also affecting the HPF by adding another pole. The only way to overcome this would be to reduce the source resistance which makes R1 and R2 smaller but harder to drive as more current would be needed in the pre-driver.

The slight improvement in eye-opening is likely to be due to the variable width of the MOSFET due to the circuits being in parallel. Alternative architectures warrant exploration due to the performance shown by the behavioural model.

If the filters can not be used to drive the gates of the MOSFETS then maybe they can be used on the drain to behave as a variable power-supply. This alternative architecture C-LVDS Type B is explored in the next section of this chapter.

## 4.5 – C-LVDS Type B

C-LVDS Type B is the second novel architecture of C-LVDS which I designed to overcome the problems of its Type A counterpart. This section describes the key areas of the design that make it suitable as a pre-distortion line driver. Type A 'failed' in simulation due to the RC filter network being unable to drive the "wide", or large W/L ratio, transistors of the High-Frequency Booster. As mentioned in section 4.4.4, a solution to this problem would be to drive all the gates from the data and use the filters to change the $V_{DS}$ of the MOSFETs [10], effectively reducing the power-supply to the High-Frequency Booster thus turning it off during low frequency signals making suitable for equalisation.

### 4.5.1 - Behavioural Model

The test bench of the behavioural model for Type B is the same as Type A, the only blocks being modified are (i) the 'Interface' and (ii) the 'Core'.

The Core, shown schematically in Figure 4.16, was modified to allow the gates to be driven by the data, In1, and the filters determine the power supply via In2 and In3. The constant connected to port 1 of switch 9 determines the voltage swing of the output, which will be $350mV_{P-P}$. As the RC filters can only provide a finite amount of current two High-Frequency Boosters need to be implemented.

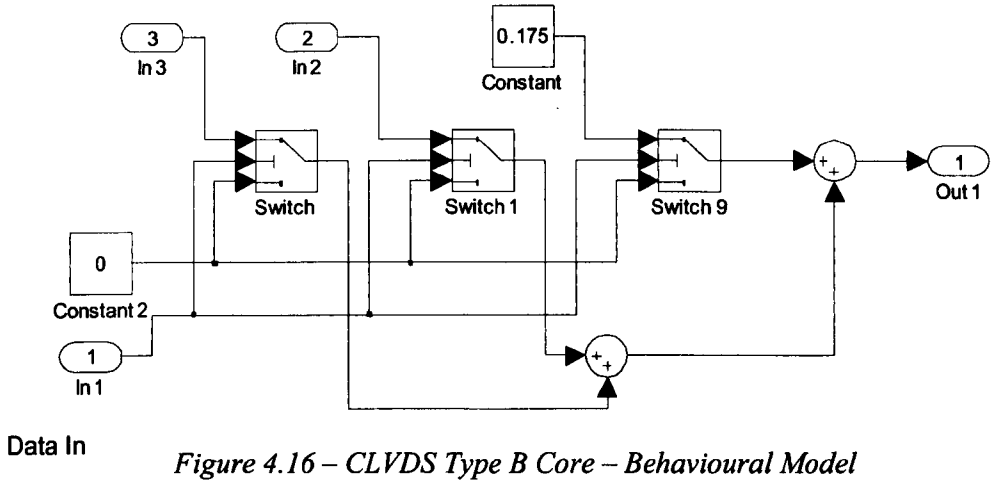


*Figure 4.16 – CLVDS Type B Core – Behavioural Model*

In the interface, shown schematically in Figure 4.17, an extra filter was added for the corresponding High-Frequency Booster in the Core.

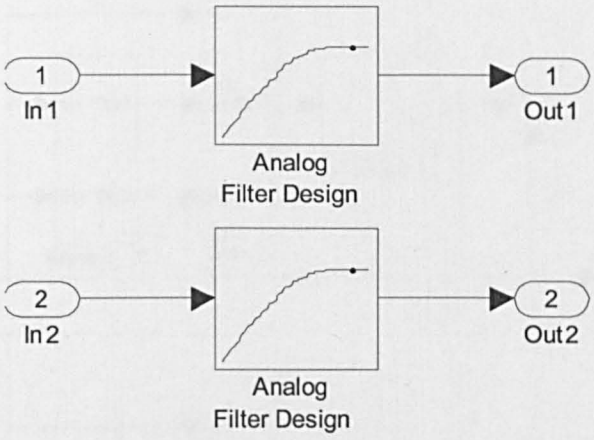


*Figure 4.17 – C-LVDS Type B Interface – Behavioural Model*

The output of the driver is shown in Figure 4.18. From this output it can be noted that the voltage gain requirement for channel correction is substantially lower, at 13, than that of Type A, at 31.5. A possible reason for this is that the load is now distributed between two High-Frequency Boosters.

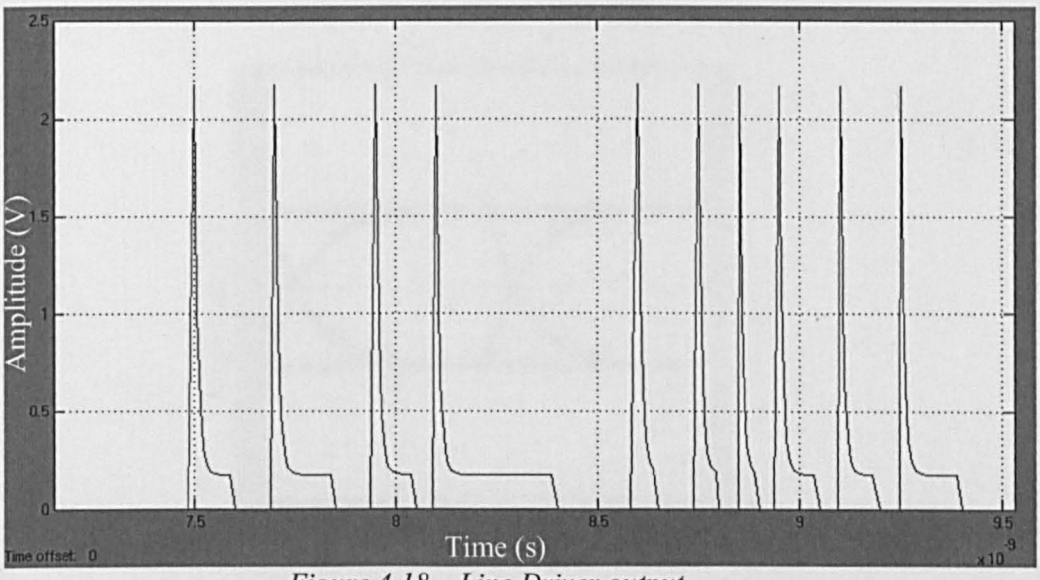


*Figure 4.18 – Line Driver output*

The top level behavioural model is shown in Figure 4.19, with the received eye diagram in Figure 4.20.

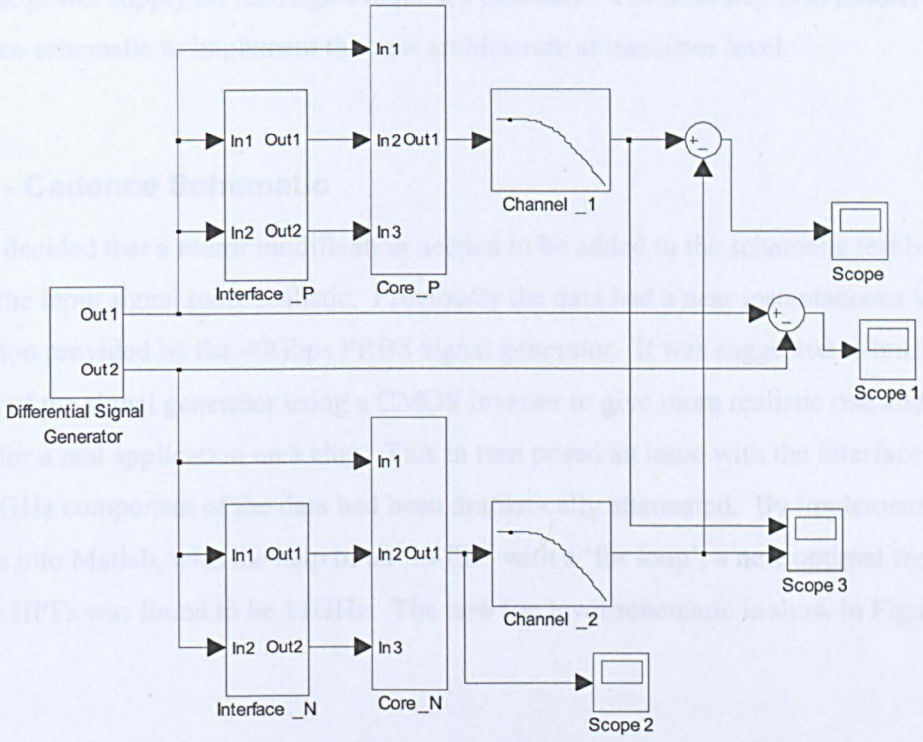


*Figure 4.19 – C-LVDS Type B top level – Behavioural Model*

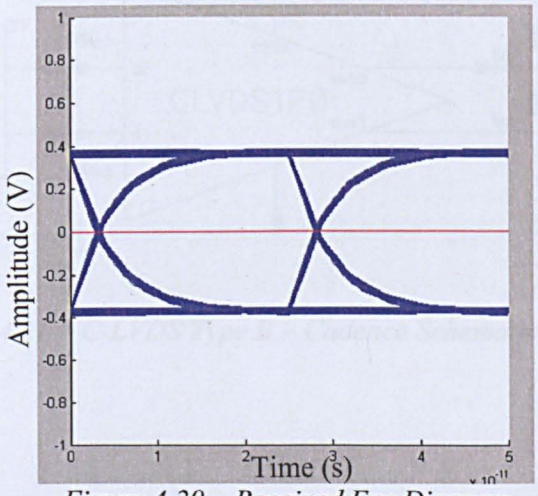


*Figure 4.20 – Received Eye Diagram*

Again the behavioural model supports the theory that filters can effectively be used as a variable power supply on the High-Frequency Boosters. The next step is to modify the Cadence schematic to implement the new architecture at transistor level.

### 4.5.2 - Cadence Schematic

It was decided that a minor modification needed to be added to the schematic test bench to make the input signal more realistic. Previously the data had a near instantaneous voltage transition provided by the 40Gbps PRBS signal generator. It was suggested to buffer the output of the signal generator using a CMOS inverter to give more realistic rise and fall times for a real application on a chip. This in turn posed an issue with the interface as now the 20GHz component of the data had been dramatically attenuated. By implementing this change into Matlab, with the help of an 'm-file' with a 'for loop', a new optimal frequency for the HPFs was found to be 11GHz. The new top level schematic is show in Figure 4.21.

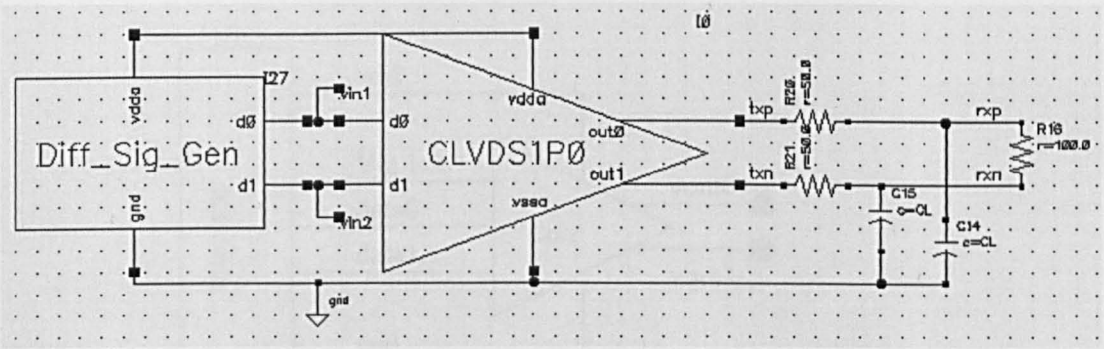


*Figure 4.21 – C-LVDS Type B – Cadence Schematic – Top level*

The 'Diff_Sig_Gen' block, shown in Figure 4.22, contains the PRBS signal generators connected to two branches, one containing a transmission gate and inverter and the second containing two inverters. These two branches provide differential PRBS Data. This block contains all the inputs that the line driver needs to operate including the DC power supply (vdd).

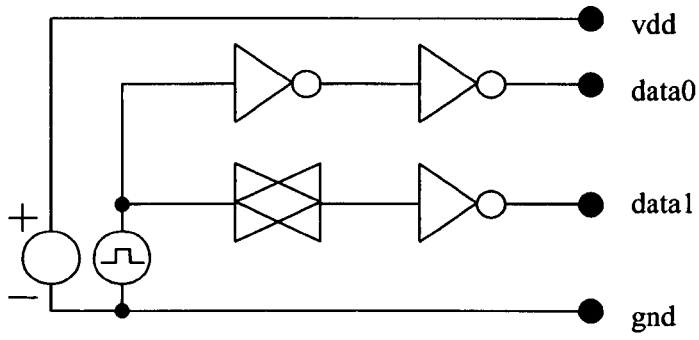


*Figure 4.22 – C-LVDS Type B – Diff_Sig_Gen*

The block 'CLVDS1P0' in the top level, Figure 4.23, contains the interface, Figure 4.24, and the core, Figure 4.25.

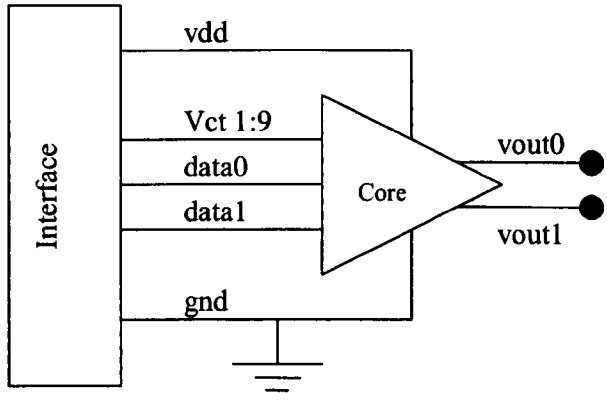


*Figure 4.23 – C-LVDS Type B – CLVDS1P0*

The interface, Figure 4.24, contains the RC filter array and the core, Figure 4.25, contains the High-Frequency Boosters as well as the DC Driver. As was found in Matlab, each filter in the Interface can only provide a small amount of current to be 'injected' into the High-Frequency Booster. However the Matlab models work with voltages not current. LVDS is a current switching circuit and the output of the filter produces less current than was represented by the model, therefore more filters and boosters are needed than the initial Matlab simulation predicted.

By simulating the circuit, and adding an extra HFB on each run while monitoring the receiver's eye-diagram, the optimum number of HFBs was found to be nine. It should be noted that this number can change depending on receiver accuracy, bit error rate requirements and power consumption.. The nine HFBs are needed to provide the right amount of current gain to correctly pre-distort the signal. As before, in Type A, each driver needs two filters, one for the positive data cycle and one for the negative data cycle, therefore an array of eighteen filters are needed. Where R = 11Ω and C = 700fF

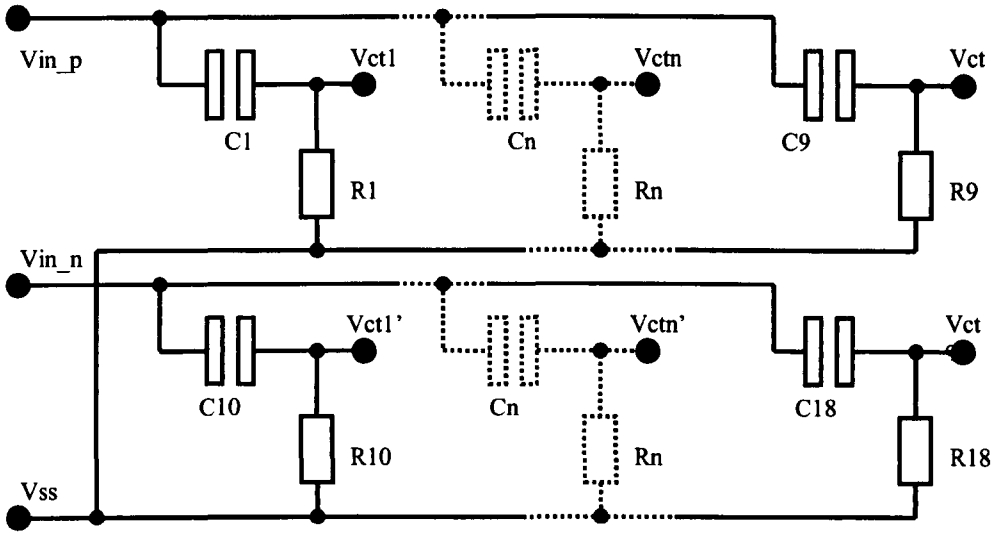


*Figure 4.24 – C-LVDS Type B - Interface*

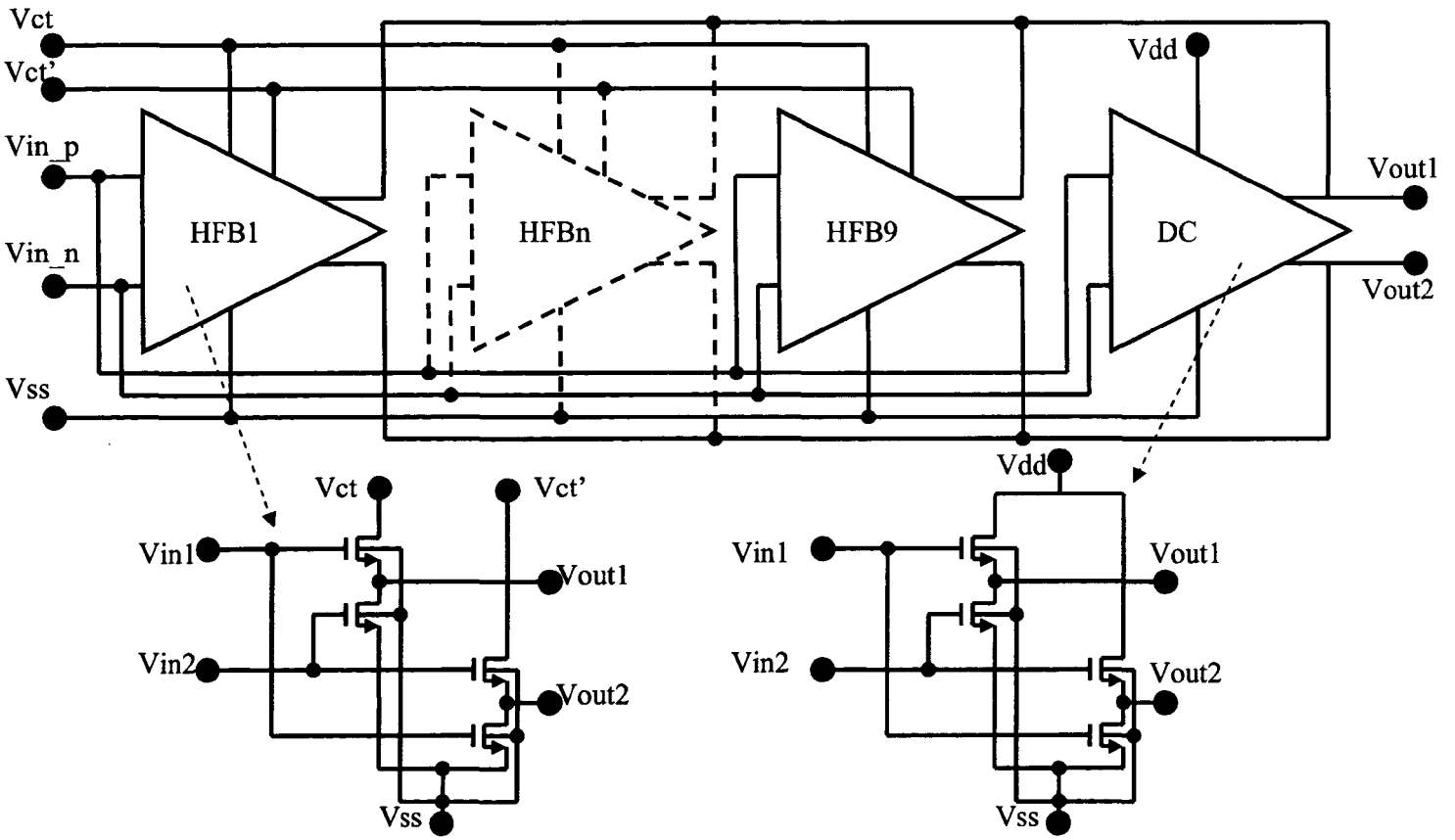


*Figure 4.25 – C-LVDS Type B - Core*

### 4.5.3 - Simulation Results

The voltages across the outputs of the transmitter (Vout2 –Vout1) and the termination resistor (RL) were measured and an eye diagram was produced using Cadence.
The transmitter eye diagram, Figure 4.26, shows the data signal have been correctly pre-distorted. The amount of pre-distortion needed is close to the Matlab model results verifying that both the Matlab and Cadence circuits agree. There is a small glitch on the transition which is introduced by the buffer used in the differential signal generator which occurs when both n and p channel transistors are on, this could be rectified by delaying the differential data to make it non-overlapping.

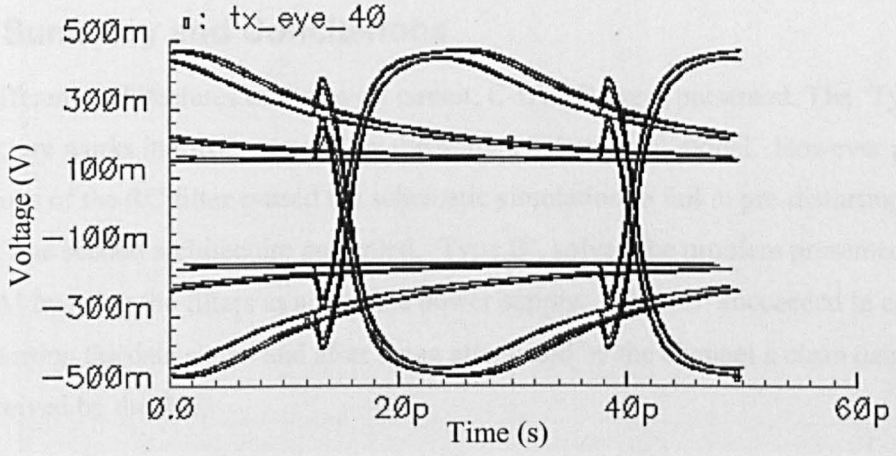


*Figure 4.26 – C-LVDS Type B – Transmitter output*

Now that the driver is operating correctly the pre-distorted data signal is attenuated by the channel and the Rx eye diagram, Figure 4.27, has a balanced output waveform making the eye wide open. The eye height is 126mVp-p with an amplitude dispersion of 30mV, and the eye width is 22.5ps with 2.5ps Jitter.

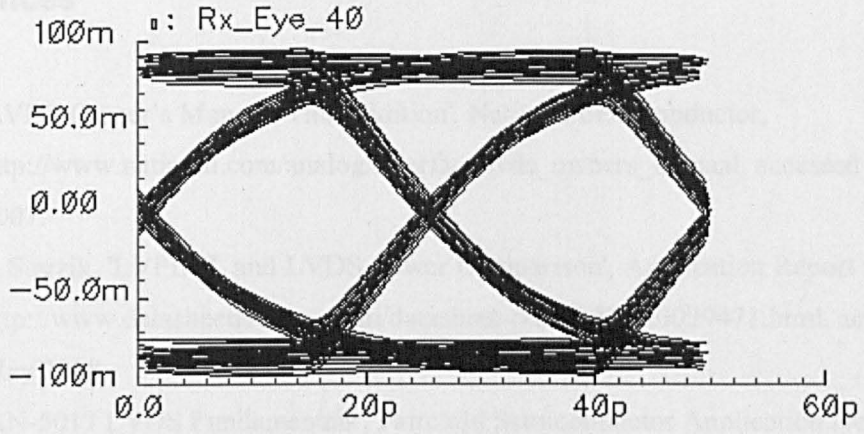


*Figure 4.27 – C-LVDS Type B – Received Signal*

## 4.6 – Summary and Conclusions

Two different architectures of the novel circuit, C-LVDS, were presented. The 'Type A' architecture works in theory, proved by the Matlab behavioural model. However practical limitations of the RC filter caused the schematic simulation to fail in pre-distorting the data signal. The second architecture presented, 'Type B', solved the problem presented by 'Type A' by using the filters as a variable power supply. 'Type B' succeeded in correctly pre-distorting the data signal and after being attenuated by the channel a clean data pattern was received by the Rx.

Because of these results C-LVDS Type B will be used as the schematic to take to layout where an RC extracted simulation can be performed to see how the circuit will perform at transistor level with more realistic parasitics. This will be presented in Chapter 5.

In both Type A and Type B multiple filters at different frequencies could be used to provide a more complex pre-distorted signal. However in this example a single pole approximation of a channel was used and therefore the best method to compensate is to use identical single pole HPFs with the same cut-off frequency.

## References


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[2] C. Sterzik, 'LVPECL and LVDS Power Comparison', Application Report SLLA103, http://www.datasheetarchive.com/datasheet-pdf/02/DSA0029471.html, accessed May 2008.

[3] 'AN-5017 LVDS Fundamentals', Fairchild Semiconductor Application Note, www.fairchildsemi.com/an/AN/AN-5017.pdf, accessed February 2009.

[4] J.R. Estrada, 'LVDS Driver for Backplane Applications', U.S. Patent 6 111 431, 29 August 2000.

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[8] 'LVDS Fundamentals', Fairchil Semiconductor Application Note, AN-5017, www.fairchildsemi.com/an/AN/AN-5017.pdf, accessed February 2008.

[9] A. Boni, et al, 'LVDS I/O Interface for Gb/s-per-pin Operation in 0.35-um CMOS', IEEE Journal of Solid State Circuits, Vol. 36, No. 4, 2001.

[10] P.R.Gray, P.J.Hurst, Et al., 'Analysis and Design of Analog Integrated Circuits', Fourth Edition, 2004.

# Chapter 5

# Layout and Post-Layout Simulation

## 5.1 - Introduction

The layout of a circuit is an important stage when producing an Integrated Circuit (IC). The layout consists of multiple layers, each separately defined by using a separate colour and/or pattern. When the layout is complete each layer is separated and used directly as masks for the etching process used for the particular technology.

When designing a circuit in schematic view devices generally have few parasitics, depending on the detail of the model of the device. There are also no parasitics modelling traces that interconnect all the devices. Once the design has been converted to a layout almost all the parasitics are present, again this depends on the detail of the layout model or P-Cell. The extra parasitics added by laying out the design can seriously degrade the performance of the circuit, especially in high frequency designs, therefore great care is needed when laying out a circuit. For this reason the layout is usually created by highly experienced layout engineers.

With specific reference to the line-drivers presented earlier in this thesis, this Chapter will contain the following:

- Photolithography and transistor formation
- A detailed description of all the devices used in my design
- The layout design with a breakdown of each component
- Post-layout simulations.

## 5.2 – Photolithography[1]

The process used to produce Integrated Circuits (ICs) is called photolithography, which means printing by light. As the name suggests a combination of light and photo-resist is used to pattern the surface of a silicon wafer so that dopants (impurities) or metal can be implanted in or on the silicon wafer. The basic process flow for photolithography is as follows:

1) Device Insulation Layer Formation – A silicon oxide film is created around the active regions in which the devices are to be formed and is etched using the 'Oxide Mask'. This process develops the oxide layer that insulates the Gates of MOSFETS.

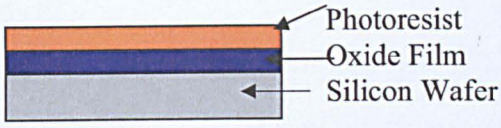
2) Transistor Formation – At this stage a poly silicon layer is deposited and etched using the polysilicon mask which completes the Gates of the device. Another mask is used to implant impurities to create the n-type diffusion layers of the Drain and Source.

3) Metallisation – Finally metal layers are placed and etched, again using masks and photolithography, to produce the connections between devices. Each metal layer is insulated using a metal oxide film.

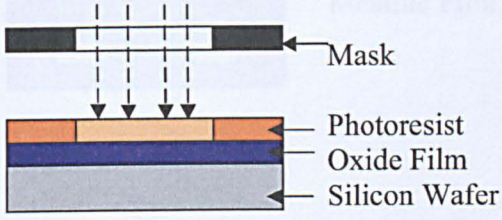
Throughout the photolithography process 'Masks' are used to block the light in certain areas of the photo resist layer to provide protected areas used in the etching processes. The masks are glass panels with metal strips to block the light, the pattern placed on the glass panels are created by a layout engineer.

To provide a more detailed example I will now describe the steps that are used to produce a single transistor.

[1] The following section is a compilation of data from the following sources [1-3]

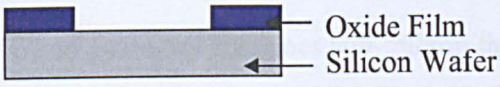



Once a silicon wafer has been prepared an oxide film is placed on the surface using thermal oxidation. Next a layer of photoresist resin is used to coat the oxide.



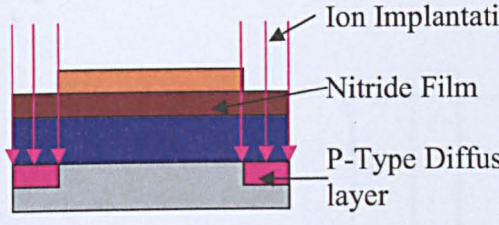

Light will be used to change the chemical makeup of the resin.
A mask is used to block the light to prevent the light from causing a chemical change in certain areas.

In this case 'negative resist' is used and the area chemically changed can be washed away in a developing agent leaving a 'resist pattern' on the oxide film.



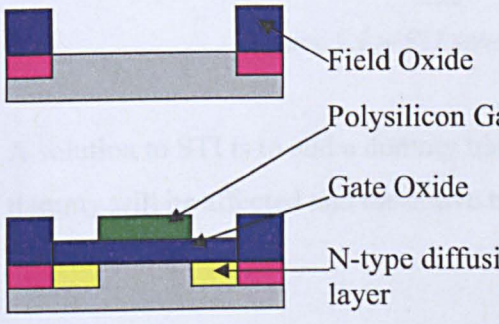

Etching is used to remove the oxide film exposed by the resist pattern and finally the photoresist is removed and the wafer is cleaned.

These steps are repeated several times, each time the oxide film is replaced with the necessary layer material to form the device.

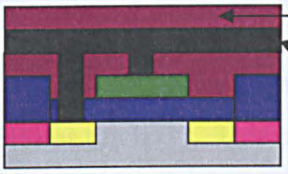



A field oxide film is formed around the active region of the device and Ion implantation is used to create a P-Type diffusion layer. A nitride film can be used to protect the oxide from impurities.

The device insulation is completed by removing the nitride film and etching the oxide.




The device is now formed on the active region by growing a thin oxide layer, gate oxide, and a polysilicon layer, which is etched to form the gate.
The N-type diffusion layer is created using ion implantation.




The device is insulated using a thick and flat insulation film (oxide film) and contacts are drilled through the insulation film where necessary.

Contact holes are filled with metal and a metallic film can then be placed over the insulation film, which is then etched to create the desired interconnect pattern. This process is repeated several times depending on how many layers the process/design needs.

Finally an extra insulation oxide film is used to insulate the top layer.

When geometry size goes sub-micron there become several technology issues that can affect the performance of the device including gate leakage, Shallow Trench Isolation (STI) and electromigration [3].

STI is a side effect of using wavelengths of light many times greater than the size of geometry. The effect can have a significant affect on device mismatching, especially in multi-finger devices where the outside drain/source is distorted by stress, shown in Figure 5.1.

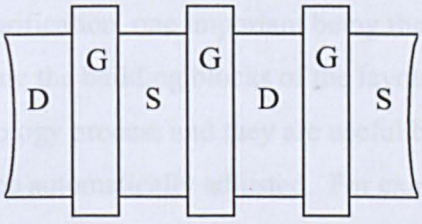



*Figure 5.1 – STI stress on a multi-finger MOSFET*

A solution to STI is to add a dummy transistor on either side, this means only the dummy will be affected and the active transistor is now uniform.

Diffusion Proximity is a side effect of ion implantation which can significantly modify the $V_T$ of the device. It occurs due to the scattering of ions from, for example, an N-well to a P-well during ion implantation.

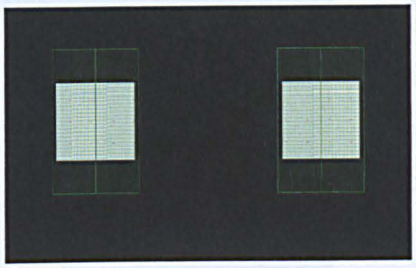
In deep submicron technologies the gate oxide thickness has been reduced down to 10 atoms thick [3]. This makes leakage a big problem in small geometry processes as the gate, in theory, should accept no current (or very little). This leakage can dramatically impact on the power efficiency of the chip and the gain of the individual transistors. Usually technologies allow for variable gate oxide thickness and the thickness of the oxide can be increased at the cost of speed.

Electromigration is the effect where metal ions from the interconnect are attracted towards the positive anode, the effect can be likened to the flow of sediment in a river. Electromigration has historically been a problem in the power bus, however with smaller geometry processes the metal is thinner and more susceptible to electromigration during normal operation. The result of prolonged exposure to electromigration can cause voids in the interconnect creating an open circuit or a large build up at positive anodes creating a short circuit to another node.

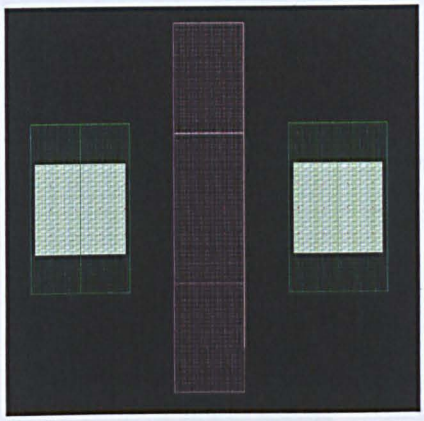
As mentioned in the introduction of this chapter the layout design engineer designs the patterns to be used on the masks that create the circuit. Cadence uses various tools to help with the design and verification, one important being the ability to create 'P-Cells' (paramatised cells) which are the building blocks of the layout. There should be P-Cells for all devices in the technology process and they are useful because parameters can be entered and the mask will be automatically adjusted. For example when creating the mask of a resistor the resistance is $R = \frac{\rho}{Depth} \bullet \frac{Length}{Width}$ where $\rho$ = resistivity of the material, with a P-Cell all you need to do is enter the desired Ohmic value and either the length or the width (as $\frac{\rho}{Depth}$ is typically constant for an individual device) and the P-Cell will then calculate the remaining parameter(s) and will automatically adjust the mask accordingly.

Three P-Cells are needed for the design of C-LVDS:

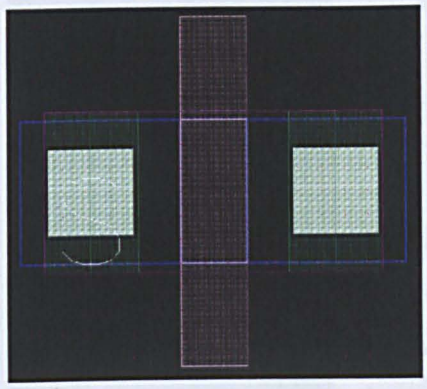
1. NMOS Transistor:



The white squares are metal-silicon contacts which connect to the drain and source of the transistor to the metal routing layer. The green squares represent the 'metal 1' layer, this layer is the closest to the silicon it is also the thinnest, in depth, and so has very little current handling abilities compared with the higher layers of metal that are usually used as routing.

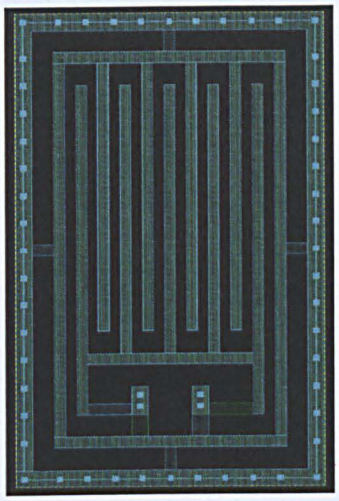


The purple strip represents polysilicon used for the gate. The gate is connected in a similar manner as the drain/source contacts which can be added manually or via options in the P-Cell.

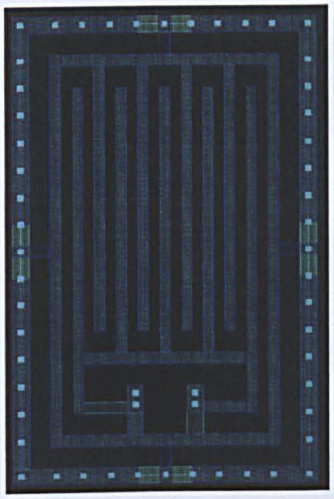


The blue lines enclose the active area of the transistor. The basic transistor mask seems simple as the transistor actually resides in the silicon, however the mask gets more complicated as the number of gates or 'fingers' increase.

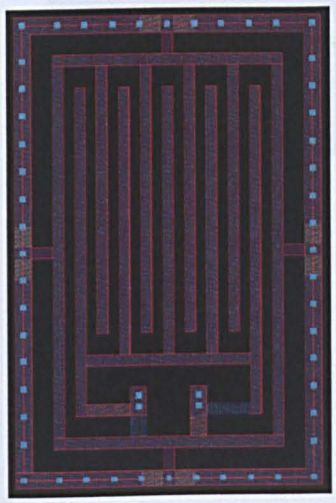
2. Metal 1-5 Capacitor:



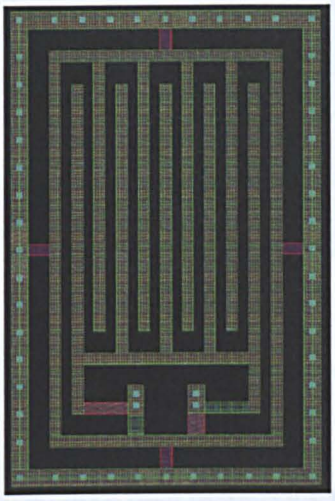
The Metal 1-5 Capacitor was chosen for its low leakage (effectively zero) at the cost of increased size and the routing problems that occur when using five out of the seven layers available for routing. The P-Cell maximizes the capacitance by using interleaved fingers and alternating the polarity of the fingers in the layers above and below.



Metal 3 contains the access for the positive connection by leaving a gap in the outside ring.

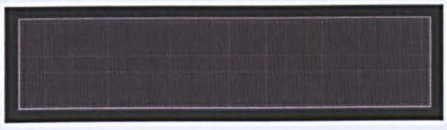


Similarly metal 4 provides access to the negative connection of the capacitor. It should also be noted that the whole ring technically is the negative connection as layers 1-5 of the ring are connected using 'vias'.



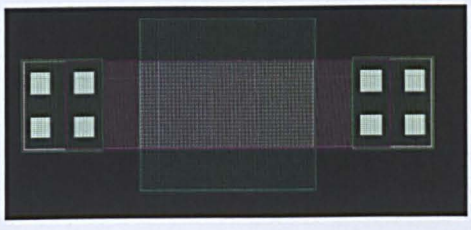
Metal 5 completes the Capacitor P-Cell

3. ZTC N-Well Resistor:

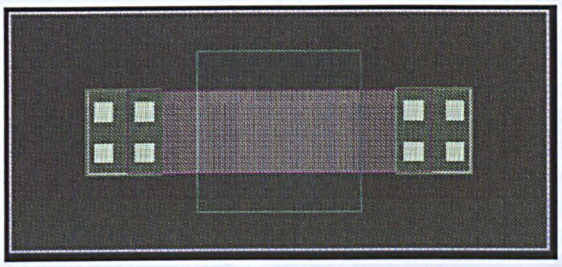


The basis of the resistor is a strip of polysilicon as it is roughly 500-1000 time more resistive than metal.

Metal-poly contacts are used to connect to the metal layers.



A special layer called SIBLK (Silicide Block) is used to block a particular dopant implant into the poly. The implant will reduce the resistance of the poly improving the performances of gates on transistors but making the poly useless for resistors. The implant is placed all over the polysilicon areas, thus preventing any mask misalignment errors, and therefore needs to be blocked where resistors are needed.



Another special layer called ZTCR which combines N and P dopant in a mixture where the Temperature Coefficient of the Silicon becomes zero.

## 5.3 - Layout Floor Plan & Mask Design

### 5.3.1 – Floor Plan

The floor plan defines the boundaries that the circuit must lay within and from there I can then plan where each subsection will fit. The area is defined by the package, in this case it is a 'Flip Chip' package and therefore uses 'bumps' to get the signals in/out of the chip, and in between the two bumps is where all the high speed transistors need to be placed. Figure 5.2 shows the floor plan for C-LVDS.

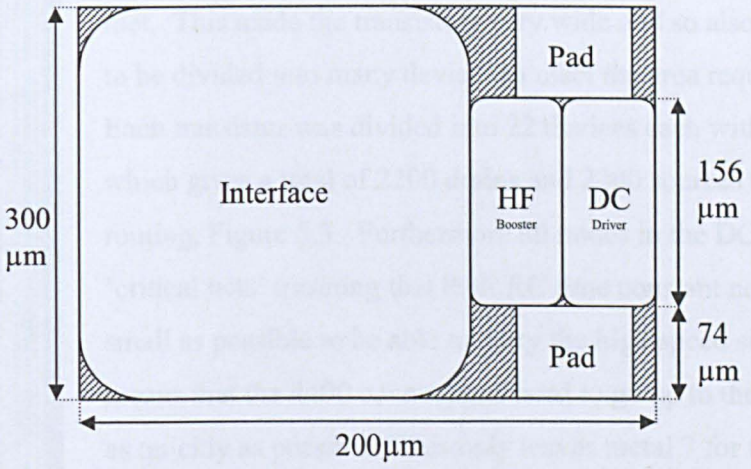
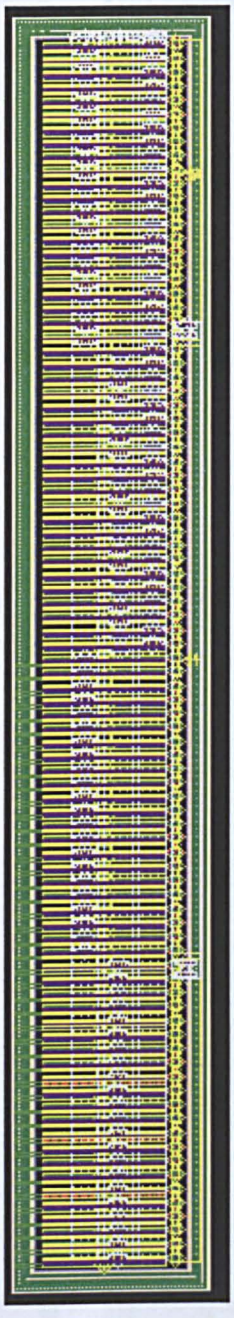



*Figure 5.2 – Floor Plan*

### 5.3.2 – Mask Design: DC Driver



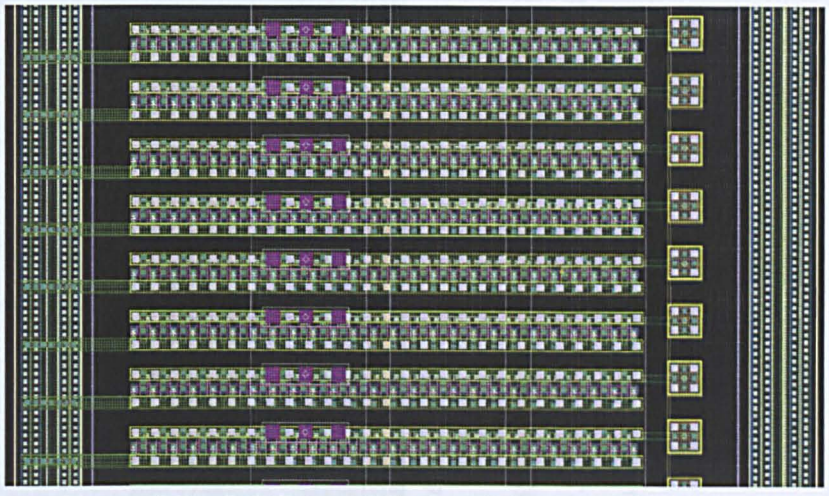


*Figure 5.3 – DC Driver full view (left), magnified (above)*

The four switching transistors that make up the DC Driver needed to have many fingers to ensure current handling requirements are met. This made the transistors very wide and so also they needed to be divided into many devices to meet the area requirements. Each transistor was divided into 22 devices each with 50 fingers which gives a total of 2200 drains and 2200 sources that need routing, Figure 5.3. Furthermore all nodes in the DC Driver are 'critical nets' meaning that their RC time constant needs to be as small as possible to be able to carry the high speed signal. This means that the 4400 connections need to go up to the metal 6 layer as quickly as possible. This only leaves metal 7 for the vertical routing.

### 5.3.3 – Mask Design: HF Booster

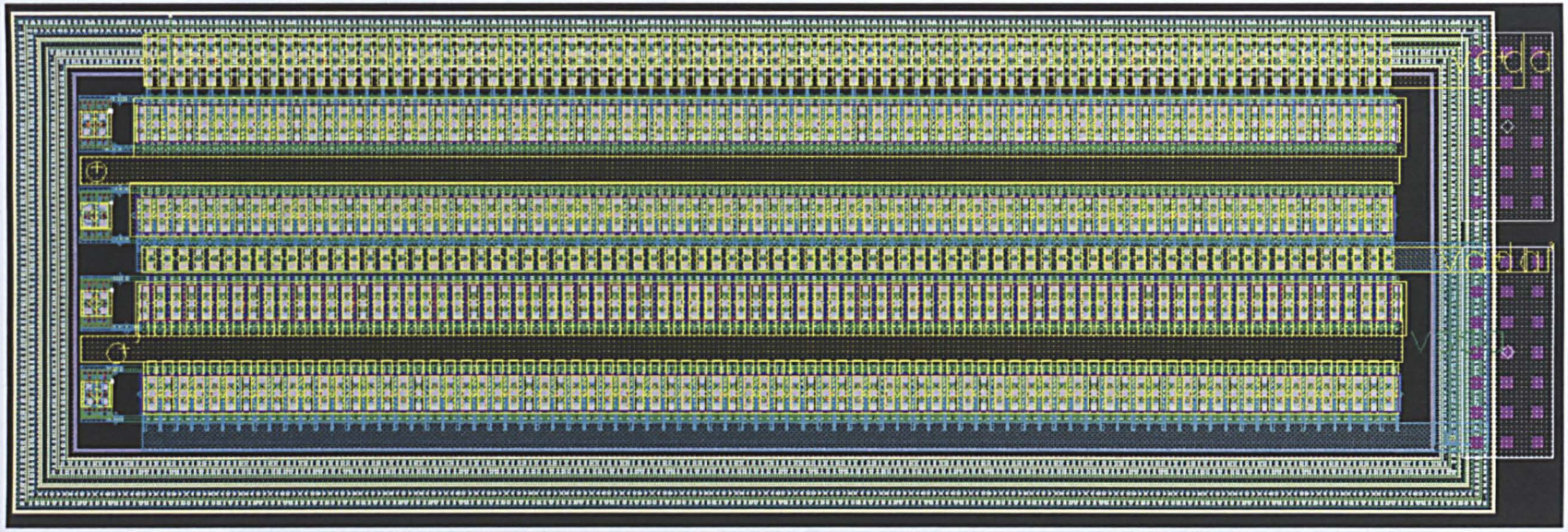
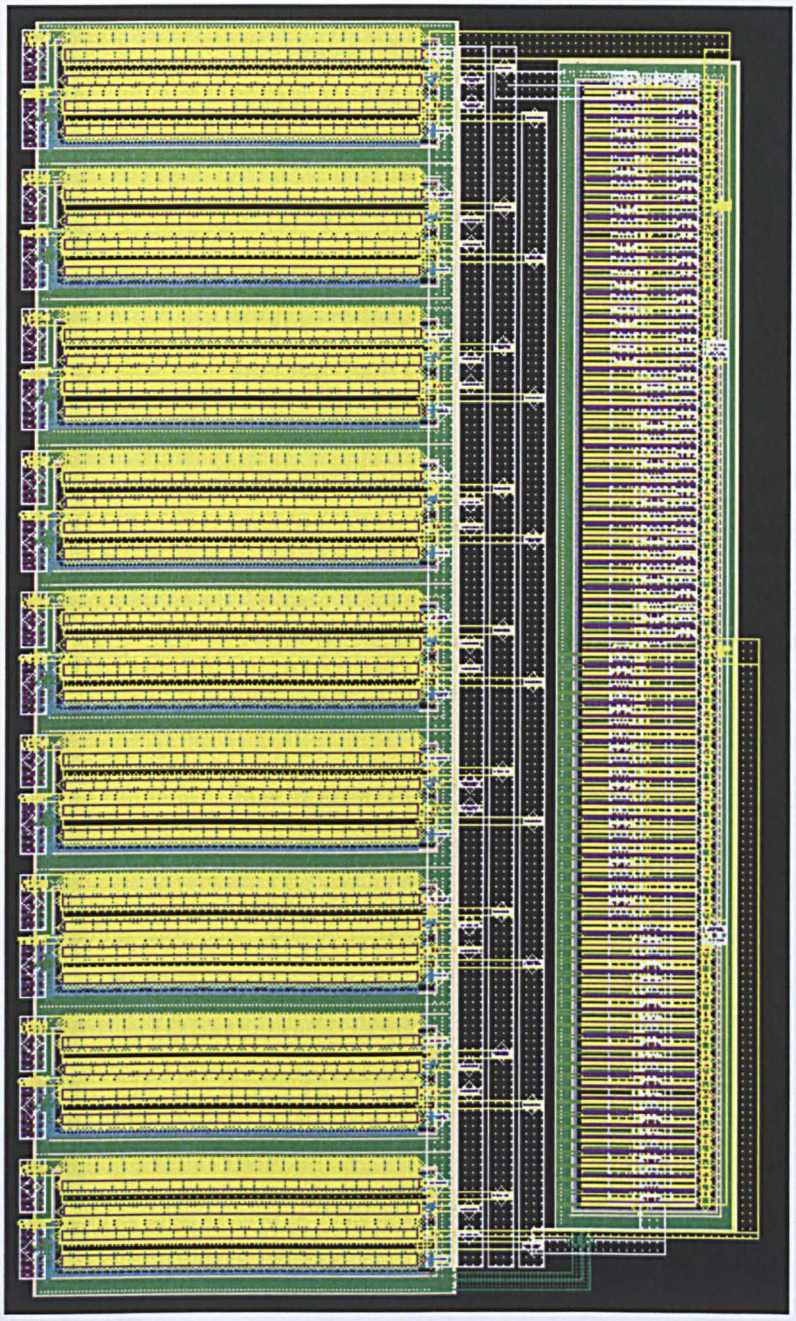


*Figure 5.4 – High-Frequency Booster*

The HF Boosters each handle less current than the DC Driver and therefore fewer fingers are needed. Each transistor is made up of one device with 160 fingers creating 320 drains and 320 sources in total. The HF Booster, Figure 5.4 shares a lot of the critical nets of the DC Driver so again the connections go straight to metal 6 where possible again leaving metal 7 for vertical routing.

### 5.3.4 – Driver Core



The DC Driver and the nine HF Boosters are connected together using more metal 6 and metal 7 for routing, Figure 5.5, leaving the data inputs on the right and the Vct inputs on the left. The differential outputs are placed centrally to connect directly to the bumps above and below the core.

*Figure 5.5 – CLVDS Core*

### 5.3.5 – Mask Design: 10GHz Filter

Figure 5.6
10GHz HPF

The drawbacks of using the metal 1-5 capacitor become apparent in the layout view, to achieve the required capacitance makes the area of the capacitor twice the amount allotted for the interface, at the moment this is unavoidable as the other smaller capacitors suffer heavily from leakage. The ZTC Resistor is placed at the top of the filter to reduce the distance that the Vct output signal needs to travel keeping the RC time constant of the net to a minimum.

The capacitor in the middle of Figure 5.6 is using the minimum possible width to ensure that the interface meets the height requirements. A workaround for the extended length of the capacitor would be for the driver to span two lanes of the SerDes chip with each lane running at 20Gpbs.

The input to the filter is connected to the bottom of the filter giving room for a low-output impedance pre-driver.

### 5.3.6 – Mask Design: Interface

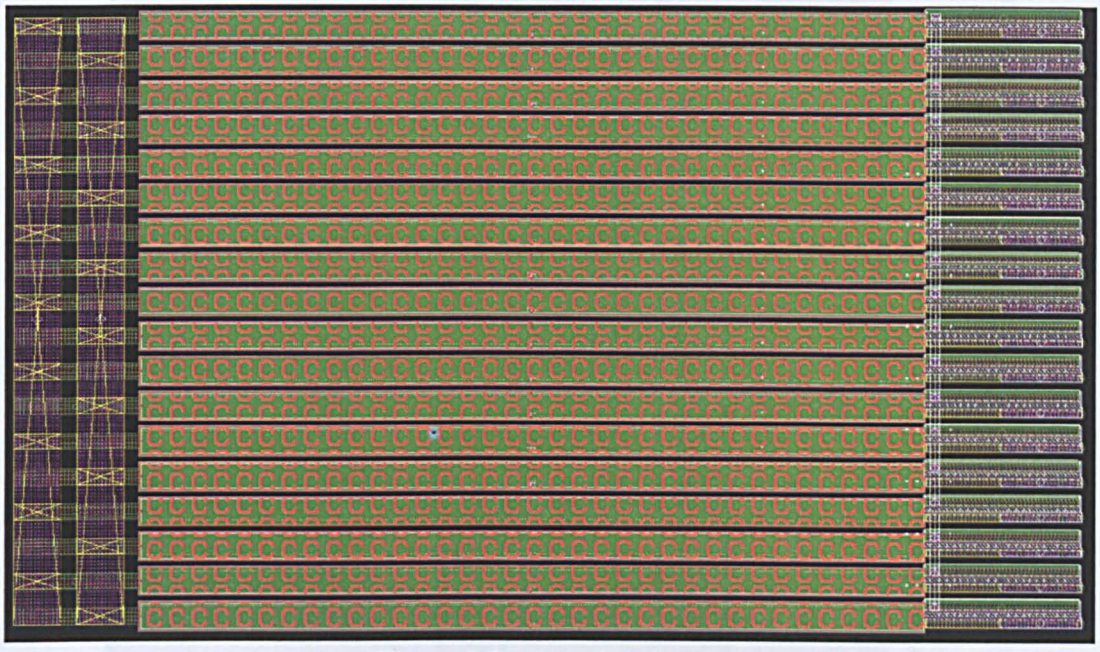


*Figure 5.7 – Interface layout*

The 10GHz HPF is copied to create the interface by making an array of 18 filters, Figure 5.7. The inputs are connected using metal 6 and metal 7 in parallel to keep the input impedance as low as possible.

### 5.3.7 – Mask Design: Top Level

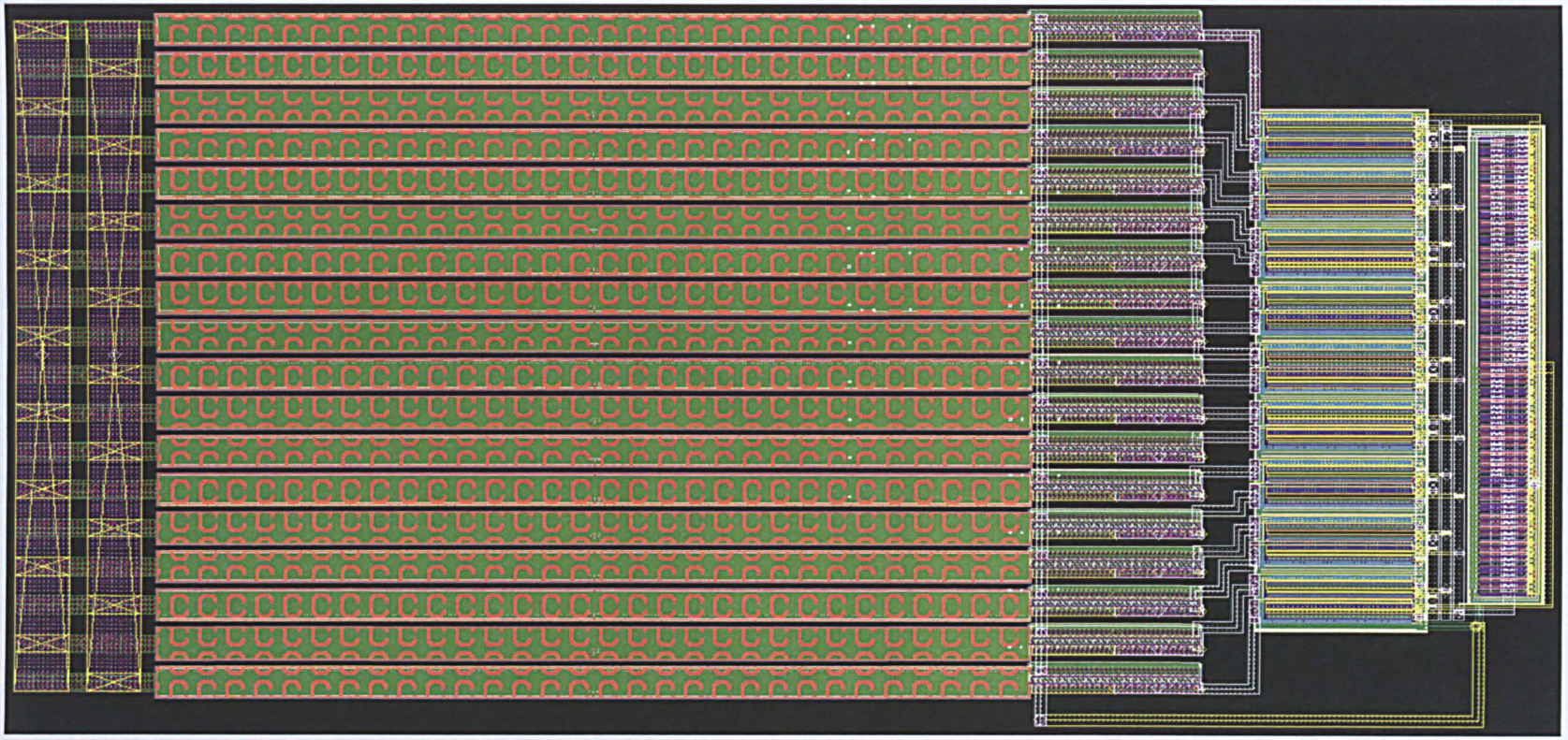


*Figure 5.8 – Top Level layout*

The design is completed by connecting the interface to the core using more metal 6 and metal 7 in parallel to reduce the RC time constant of the Vct net, Figure 5.8. The yellow connection at the bottom right will eventually be replaced by the power grid.

## 5.4 - Post Layout Simulation

### 5.4.1 – Ideal Simulation

The 'Ideal' simulation run is used for comparison. Although it is not a post-layout simulation as such, the ideal components used previously (i.e. resistors and capacitors) have been replaced with more complex 'real' models selected from the 65nm technology library.

Figure 5.9 Shows the results of this simulation in an Eye-diagram format.

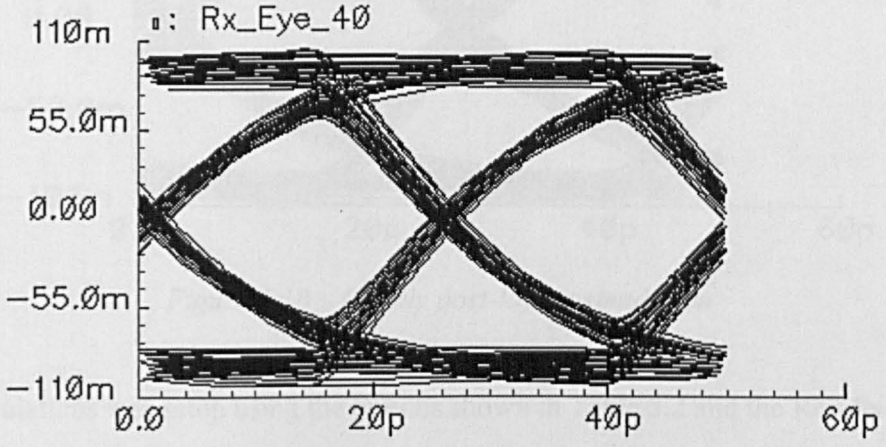



*Figure 5.9 – Ideal post-layout simulation for the CLVDS*

| Eye Height | 125.8mV |
|---|---|
| Eye Width | 22ps |
| Jitter | 3ps |

Table 5.1 – Ideal Post-Layout Simulation Results

### 5.4.2 – Capacitance Only Simulation

The capacitor only simulation is a relatively quick simulation used to gauge the performance of the driver in the early stage of development. The eye diagram in Figure 5.10 shows a slight eye closure, which would be expected, however the results are satisfactory for further testing.

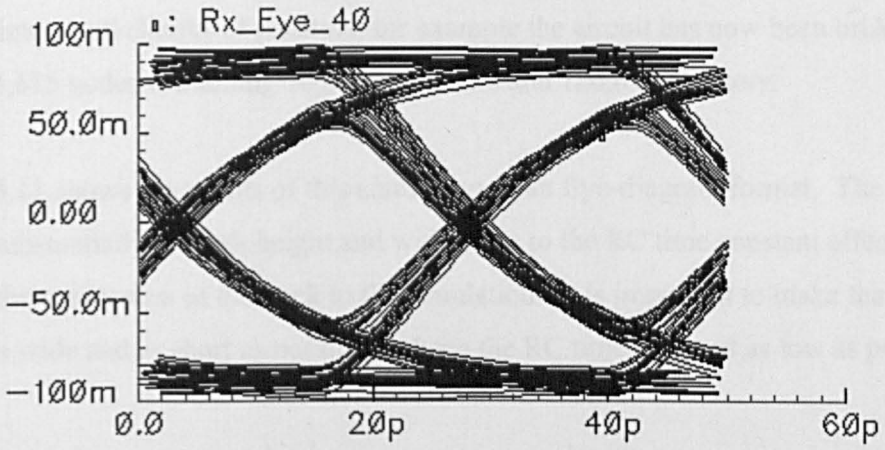



*Figure 5.10 – C Only post-layout simulation*

The Simulations was setup using the options shown in Table 5.2 and the Results are in Table 5.3.

| Capacitance | Maximum |
|---|---|
| Track Resistance | None |
| Temperature | 125°C |

Table 5.2 – C Only Simulation Options

| Eye Height | 106.7mV(pk-pk) |
|---|---|
| Eye Width | 21.4ps |
| Jitter | 3.6ps |

Table 5.3 – C Only Simulation Results

### 5.4.3 – Resistance and Capacitance (Best Case)

The first RC simulation sets the environment for a best case scenario, this scenario assumes that the IC manufacturing process produces perfect contacts and no defects. This simulation includes perfect via contacts and lowest track resistance.

Adding resistors into the simulation substantially increases the time needed to simulate the circuit, approximately four hours for my circuit. This occurs because all the nets are broken into small chunks of resistors, for example the circuit has now been broken up into 114,615 nodes containing 70,819 capacitors and 120,619 resistors.

Figure 5.11 shows the results of this simulation in an Eye-diagram format. The eye has closed substantially, in both height and width, due to the RC time constant effect of adding the resistances of the track to the simulation. It is important to make the critical nets was wide and as short as possible to keep the RC time constant as low as possible.

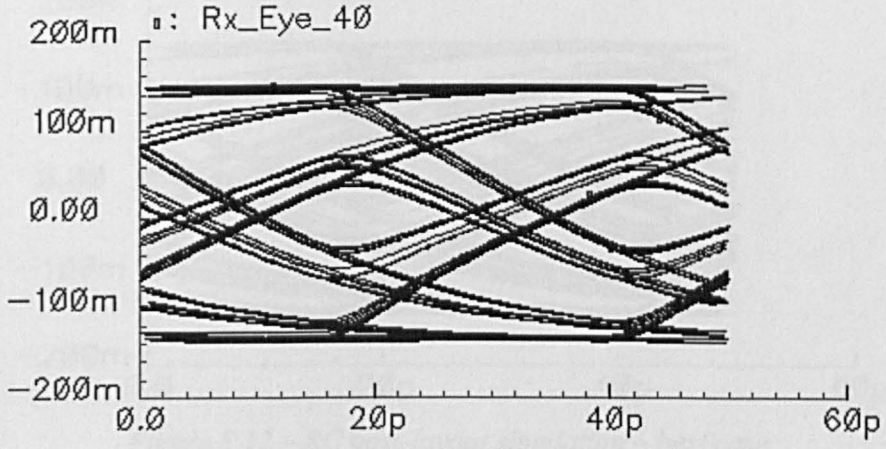



*Figure 5.11 – RC post-layout simulation – best case*

| Capacitance | Nominal |
|---|---|
| Resistance | Minimum |
| Via Resistance | Minimum |
| Temperature | 25°C |

*Table 5.4 – RC Simulation Options (Best Case)*

| | |
|---|---|
| Eye Height | 70mV |
| Eye Width | 16.1ps |
| Jitter | 8.9ps |

*Table 5.5 – RC Simulation Results (Best Case)*

### 5.4.4 – Resistance and Capacitance (Worst Case)

This RC simulation covers the worst case scenario, where the IC manufacturing causes poor contacts and lots of defects producing high via (contact) resistance, high track resistance and large parasitic capacitances.

Figure 5.12 shows the results of this simulation in an Eye-diagram format. As expected by increasing the resistance of the nets the RC time constant has increased closing the eye even further. However the eye is still open and the receiver will still easily be able to define bit edges.

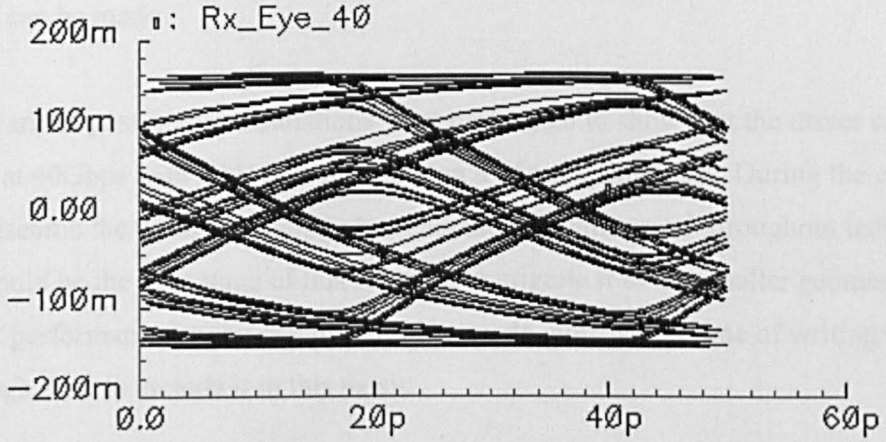



*Figure 5.12 – RC post-layout simulation – best case*

| | |
|---|---|
| Capacitance | Maximum |
| Resistance | Maximum |
| Via Resistance | Maximum |
| Temperature | 125°C |

*Table 5.6 – RC Simulation Options (Worst Case)*

| Eye Height | 40mV |
|---|---|
| Eye Width | 12.1ps |
| Jitter | 12.9ps |
| Power Consumption | 4.54mW/Gb/s |

*Table 5.7 – RC Simulation Results (Worst Case)*

## 5.5 – Summary

This chapter describes the steps in the fabrication process photolithography with details on how transistors are fabricated. Some of the problems of deep sub-micron technology, during both manufacturing and use under normal conditions, were explored and ways to overcome these issues were highlighted.

Also described in this Chapter is each section of layout for C-LVDS, in which the hierarchy used in the design was closely followed. Further design tweaks maybe needed as there are a few more tests, i.e. current handling, that are carried out before a test chip can be made.

Finally various post-layout simulations were performed to show that the driver can perform at 40Gbps with a 1V power supply on a 65nm technology. During the course of this research the 45nm technology has become the widespread throughout industry and it would be the next stage of this research to migrate it to the smaller geometry to see what performance improvements could be made, however at time of writing there is not enough time to include it in this thesis.

A drawback that has come to light during this stage is the need to have a very low output impedance pre-driver stage. This will cost a lot more power than currently stated. One method to avoid this was using two separate pre-drivers, one to drive the core and the other to drive the interface. This would reduce the cost slightly as now the low output impedance pre-driver only needs to drive the interface. Another method could be to design a buffer between the pre-driver and interface where only the buffer would need to show low output impedance.

## 5.6 – References

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# Chapter 6

# Conclusions, Future Work and Applications

This chapter is a reflection of the work undertaken and reported in this thesis, with summary of each part of the research programme. The chapter ends with a discussion and tentative review of applications and future development work for the novel C-LVDS that has been the principal outcome of this research programme.

## 6.1 – Conclusions

In Chapter 1 the primary driving factor behind SerDes was introduced, namely data skew which is prominent on high speed parallel data busses. SerDes is a 'one-stop' solution (i) to improve the speed of systems by converting the parallel data into a serial data stream so that it can be transmitted at very high data rates, in excess of 10Gbps, and (ii) to eliminate any data skew. Another SerDes device can then be used to reverse the serial data stream back into a parallel format which can then be easily read by the destination device.

Chapter 1 also introduces the highly demanding specifications that need to be met by the new line driver design. Under most circumstances a designer either needs to design a line driver capable of operating at high speeds or to operate at low voltage levels, each being demanding tasks on their own. Designing a line driver to operate at both high data rates and low voltage supplies simultaneously creates lots of problems including head room issues which make it impracticable to stack more than two transistors, even with the low threshold voltage of the 65nm CMOS process. On top of this great care is needed to make the design as power efficient as possible as power consumption is a key factor where every milliwatt counts.

Chapter 2 is a review chapter of existing SerDes designs. This includes the principle architecture of SerDes and some of its common applications, including chip-to-chip communication within supercomputers and data routers, followed by some of the challenges faced by SerDes designers today and how the line driver plays its role in overcoming the challenges of increasingly higher bit-rates.

Different equalisation techniques have been presented showing the power consumption benefits of performing equalisation on the transmitter, called pre-distortion, rather than on the receiver, where Decision Feedback Equalisation (DFE) is commonly used for high data rate links [1]. This saving in power would be crucial to the success of the higher speed line driver as a 40Gbps line driver would inherently consume more power than existing lower speed line driver topologies. Therefore some of the power savings from the receiver could be spent on the transmitter should it be able to perform this task efficiently within the analogue domain.

Once the parameters for the new line driver design had been finalised in Chapter 2, an extensive search for existing line driver topologies was carried out. This is the focus of the critical review in Chapter 3. The search revealed four common types of line driver, CML, LVPECL, H-Bridge and LVDS. Standards were found for LVPECL and LVDS however CML and the H-Bridge are more of an interface and therefore the electrical standard are taken from the requirements of Clause 47 of the IEEE 802.3 standard which defines the physical layer of the XAUI interface.

Texas Instruments' 65nm CMOS transistor technology allows a maximum $V_{GS}$ of around 1.5V before oxide breakdown occurs and as the LVPECL and the LVDS standards require a higher voltage level a more suitable higher voltage transistor needed to be found. The IBM 130nm T68A model was freely available from the internet, its thicker oxide allows for higher voltage without reducing its switching speed so much that it becomes unfeasible to operate at 40Gbps. Various tests were performed to identify key parameters that are used in the main design equations such as $V_T$, $\mu_x C_{ox}$ and $\lambda$.

CML, possibly the more common line driver due to its Long-Tail Pair (LTP) nature, was the first to be designed and tested. The test bench for the simulations were decided to be as perfect as possible, this way the only difference in perceived performance would be due to the individual circuit topology, including differences in parasitics. In most cases the biggest limiting factor for performance is the transmission line itself. If parasitics were to be added to the test bench, to model a transmission line for example,

this would be the limiting factor in most of the tested circuits possibly masking the full potential of a circuit. A transient analysis was performed at various speeds and the output of the line driver was monitored to ensure it was still performing within the parameters defined by the relevant standard. In the case of CML it performed well up to 40GHz, twice the target speed was chosen due to the lack of parasitics, however there was a significant amount of feed-forward current present in the output. Through analysis this was shown to be caused by the Miller effect and therefore could be compensated using capacitive neutralisation between the input and output of each driving transistor, which is relatively easily implemented with a LTP topology.

This lead to a second CML topology to be tested with neutralisation capacitors, implemented with CMOS transistors. In this case the neutralisation capacitors dramatically reduced the signal spikes caused by feed-forward current, although not completely, due to the slight biasing differences between the original transistor and neutralisation transistor causing a minor mismatch in capacitance. The drawback of this neutralisation technique was that it reduced the edge rate of the line driver. However this did not degrade the overall performance significantly.

The next circuit to be designed and tested was LVPECL, which is usually used as a low-speed long distance transmitter, and this is exactly what the simulations results confirmed. Its high power consumption and low effective speed make it an unsuitable candidate for a low-power high-speed SerDes application.

The H-Bridge is essentially two CMOS Inverters with the outputs connected via a load resistor, this makes the design and analysis relatively straightforward. It is the closest design to LVDS and operates in a very similar fashion by alternating the flow of current through a load resistor. However, the large output swing it generates makes it unable to match the speeds and efficiency of LVDS. The PMOS transistors in this circuit are inherently larger and have a greater $V_T$ than an all NMOS circuit like LVDS, allowing LVDS to potentially operate at a lower power supply level than the H-Bridge.

The final circuit that was designed and tested was LVDS. This circuit matched CML in its speed capabilities. However, LVDS exceeded the efficiency of CML when comparing the voltage swing per mW of power. This made it a good candidate for the next phase of the research reported in Chapter 4, which is focused solely on the LVDS topology and looked at various methods to combine the line driver with properties of controlled pre-distortion.

Chapter 4 opens with the concepts and development behind the novel line driver named Composite LVDS (C-LVDS) with particular focus on pre-distortion and how it can prevent ISI, followed by the design procedure that was used to design the unique topology named C-LVDS.

The design procedure is split into two distinct sections (i) the 'Core' which contains all the active devices for both the 'DC driver' and the 'High-frequency booster' (ii) the 'Interface' which contains the passive circuitry that provides the control signals.

There are also two types of C-LVDS presented in this thesis (i) 'Type A', which has the Interface controlling the Gates of the transistors within the High-frequency booster (ii) 'Type B' where the interface is connected to the Drains of the transistors within the High-frequency boosters, acting as a variable power supply. Both types were tested using Matlabs Simulink to produce an ideal behavioural model, and then Cadence using Texas Instruments' 65nm CMOS technology.

The behavioural model for both types showed that the circuits should work. Furthermore, by comparing the eye-diagrams for both types showed that Type A would perform the best as it showed a much higher edge rate than Type B. However in the Cadence simulation Type B outperformed Type A. The degradation of the performance of Type A is most likely due to the added input capacitance, provided by the HPF, on the Gates of the transistors in the High-frequency booster making them unable to switch fast enough, which was not modelled by the ideal switches used in the behavioural model.

The eye-diagram produced in Cadence for Type B was comparable to the performance shown in the behavioural model eye-diagram produced in Matlab, making Type B the suitable candidate to develop further and take to layout.

In Chapter 5 the Type B C-LVDS was taken to layout and re-simulated using RC extracted parasitics to verify the performance of the final practical design. This work highlights the importance of producing a layout design from a schematic and how great care is needed to maintain a satisfactory level of performance once the layout design has been completed.

The photolithographic process for deep sub-micron integrated circuits in high speed CMOS technology is described in great detail. The manufacturing process is directly related to the layout design where the layered patterns created by the layout designer are used as the mask patterns in photolithography, making layout the last stage in the design process.

A benefit of producing a layout design for the novel line driver presented in this thesis is to take advantage of the post-layout simulations that can only be performed once a layout design has been created. The post-layout simulation is the most realistic simulation that can be performed before a test chip is produced. It is at this stage that a lot of final testing takes place to ensure that the device has the best chance of working. For example current handling tests are performed to ensure that a trace will not burn out from excessive current load. Layout extraction tools are also used to add the extra parasitics presented by the interconnect traces which can then be added to the original schematic for a more detailed simulation.

It took three months and several designs to produce the layout design presented in this thesis. The schematic was broken down into small sections, each section was then converted into a layout design using a Layout versus Schematic (LvS) tool and then simulated using extracted RC values to ensure that the section would not excessively degrade performance. It was often the case that when individual sections were connected in a higher level of hierarchy a "bottle neck" would form, therefore great care

was taken to only add one section in between extracted simulations so that the "bottle neck" could easily be identified. The removal of one bottle neck would often reveal a secondary bottle neck making the design process very long and drawn out. However the solution to a problem in one section could usually be implemented across all sections, thereby improving the performance of the whole design.

At time of writing, the core is complete and is ready to be implemented on silicon. It conforms to the area parameters set out by the package used in the 65nm SerDes test chip and care was also taken to ensure that current handling limits were met.

However the interface still needs a fair amount of work before it can be implemented in silicon. It is almost twice the size of the allotted area for it in the floor plan, mainly due to the metal 1-5 capacitors that were chosen for their low leakage properties. Other capacitors were tested but all suffered a 2dB loss in voltage amplitude making the filter output too small to be effective. Furthermore the increased distance that the control signal has to travel, due to the large capacitors, combined with the high frequency that the control signal operates at causes an additional attenuation when connected in the top-level layout design causing a 50% loss in eye height. Therefore further research and development is needed on the interface before the new C-LVDS could be implemented fully onto a test chip.

In conclusion, this thesis presents a novel asynchronous line driver that operates at 40Gbps, performs pre-distortion and works off less than a 1V power supply. The material presented within the first three Chapters provides a thorough background review of both SerDes and the role a line driver plays in SerDes. Chapters 4 and 5 follow the design and development of the novel C-LVDS line driver including two architectures, namely 'Type A' and 'Type B'. A layout design of 'Type B' is presented in Chapter 5, and a parasitic extraction was performed on the layout which was then used in post-layout simulations verifying the final design. The post-layout simulations show that the concepts behind C-LVDS worked extremely well. The design would benefit from more research and development to enhance the 'Interface' component of C-LVDS to optimise performance.

## 6.2 – Future work

The production of a test chip is the driving factor for future work. At the time of writing there are several factors preventing immediate submission for silicon fabrication:

i) The novel line driver is asynchronous and needs a 40Gbps data stream to enable the control signal to the 'Core' of the line driver. The design team at TI believe this will require substantial work to produce this data rate using their existing test chip technology. A possible solution would be to scale back the line driver to a lower frequency, 10Gbps for example. However, it would not accurately represent operation at 40Gbps in terms of power consumption and performance.

ii) The post-layout simulation indicates that the 65nm technology may not be suitable for operation at 40Gbps. Migration to a 45nm technology should provide a noticeable increase in performance.

iii) A suitable low-power low-output impedance pre-driver, which is needed to drive the filter array within the 'Interface' is not readily available.

iv) Both this chapter and Chapter 5 indicate that more research and development is needed on the 'Interface', which creates the control signals for the 'Core', in the following areas:
   a) Reduction of sensitivity to the output impedance of a pre-driver.
   b) HPF design including a method for finding the optimum R and C values for use in C-LVDS.
   c) The ability to change the frequency of the HPFs will be a useful function and can be easily implemented using an array of capacitors in parallel with transistors operating as switches.

## 6.3 – Applications

Although C-LVDS was originally designed for SerDes applications, due to its asynchronous nature, it can also be implemented as a TransImpedance Amplifier (TIA).

A transimpedance amplifier, also know as a current-to-voltage converter [2], is commonly used to amplify the output of a photodiode in an optical communications link, Figure 6.1.

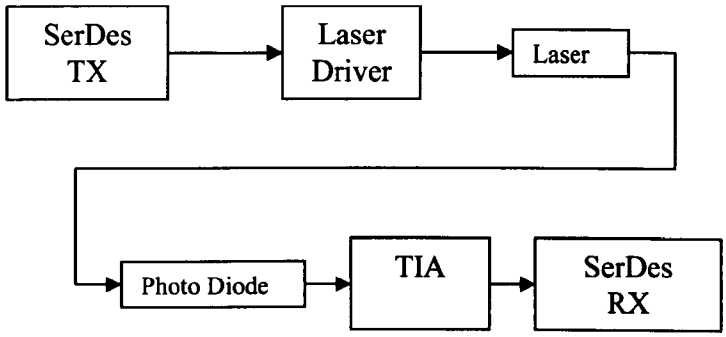


*Figure 6.1 – Simplified Optical Link Block Diagram*

Optical data links generally work at high data rates and is an application of SerDes to get the data in and out of these optical links.

With some modifications the C-LVDS design could be implemented as a TIA as there is no clock available at the output of the photodiode, thus an asynchronous amplifier is required.

This will benefit the overall system as the use of a strong line driver, such as C-LVDS, can mean that the SerDes device no longer needs to be housed in the receiver module and can be moved back to the receiver line card.

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# APPENDIX 1 AND 2

# MATERIAL EXCLUDED FROM DIGITISED THESIS

# PLEASE REFER TO THE ORIGINAL TEXT TO SEE THIS MATERIAL